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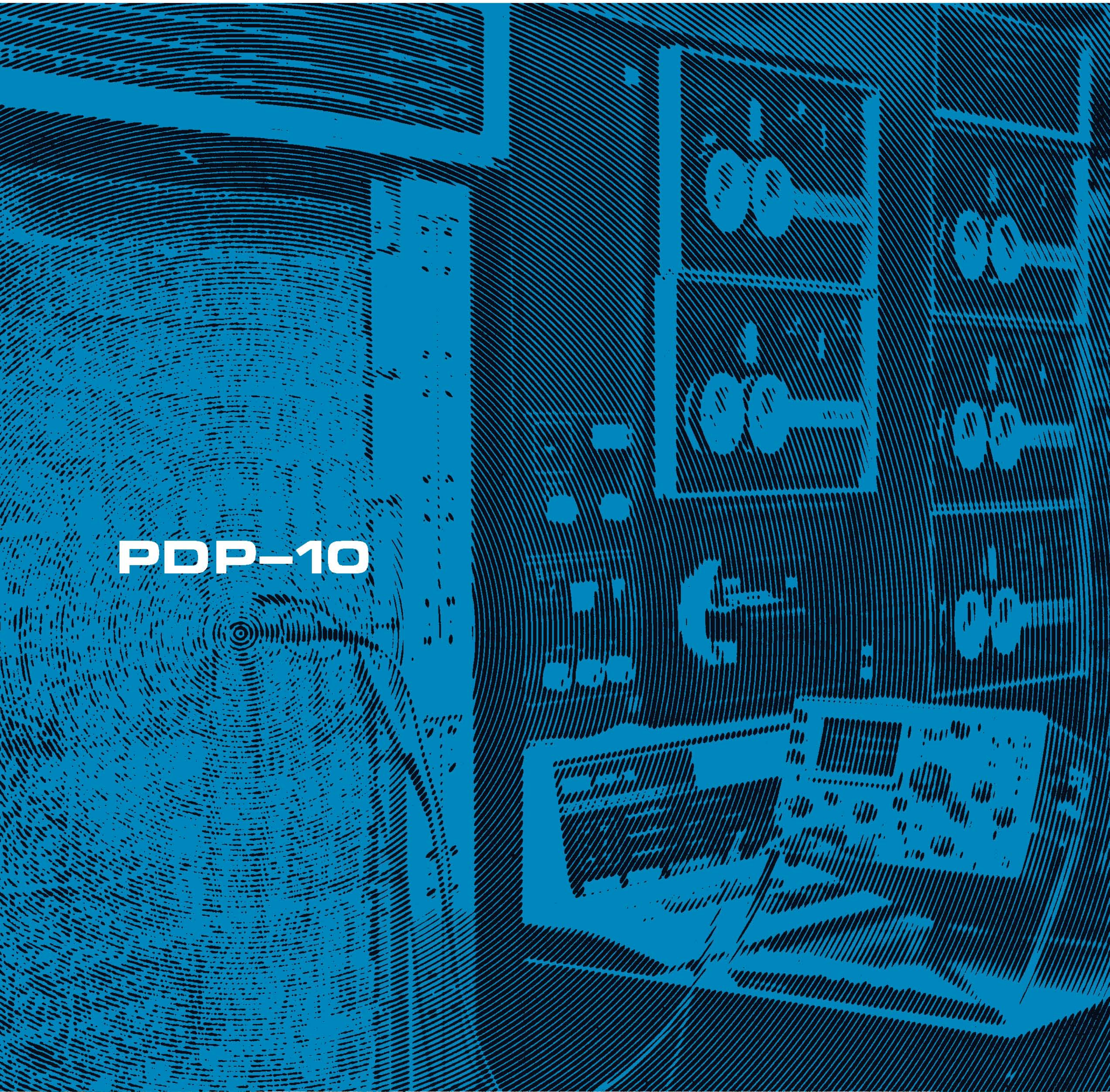
BA10 HARD COPY CONTROL



DEC-10-I2AA-D

BA10
HARD COPY CONTROL
MAINTENANCE MANUAL

July 1968

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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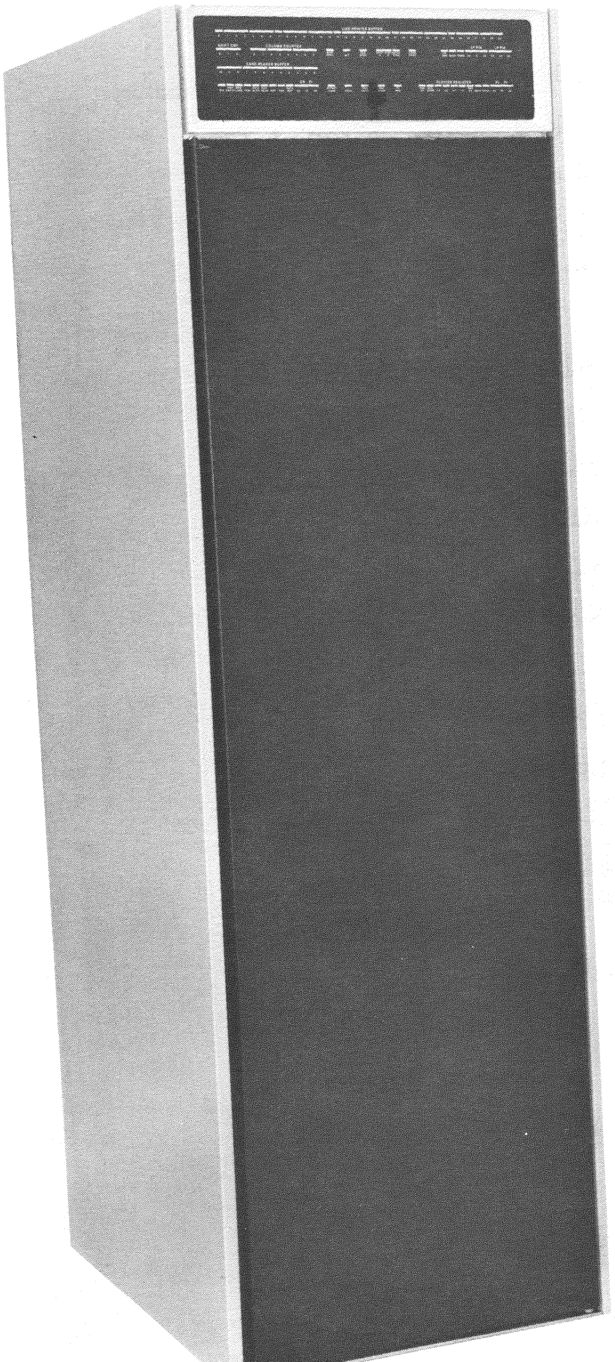


BA10 Hard Copy Control Unit

CHAPTER 1
INTRODUCTION

The BA10 Hard Copy Control manufactured by Digital Equipment Corporation Maynard, Mass. is an optional unit in the PDP-10 system and contains the control logic for the CR10 Card Reader, LP10 Line Printer, and the XY10 Plotter. This manual, when used in conjunction with the documents referenced, provides the information that is necessary to install, operate and maintain the BA10 unit.

The level of discussion in this manual assumes that the reader is familiar with DEC logic, signals, and notation, the KA10 Processor and its operations and the operation of the peripheral devices controlled by the BA10.

Engineering drawings referenced in this manual are located in the PDP-10 Peripheral Engineering Drawing Set, Volume IV (BA10-DA10).

1.1 CONTROL DESCRIPTIONS

A general description of the CR10 Card Reader Control, the LP10 Line Printer Control and the XY10 Plotter Control is contained in the following paragraphs.

1.1.1 CR10 Card Reader Control

The Type CR10 Card Reader Control interfaces the KA10 Processor with one Soroban Compact Card Reader, Model ERD and allows the information on standard 80-column punched cards to be transferred to the processor through the input/output bus at a rate of up to 1000 cards per minute. The following description of the card reader system refers to Figure 1-1.

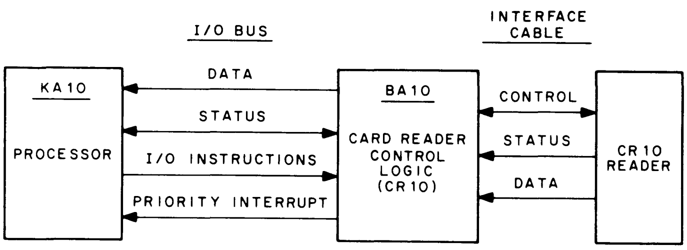


Figure 1-1 CR10 Card Reader System Configuration

Status information is routed from the card reader to the card reader control logic via the card reader interface cable. In the card reader control logic, a series of status gates are conditioned according to the contents of the status register and the status information is fetched by the central processor after a program interrupt request. From the status information the central processor determines system status and performs the required I/O instruction.

After loading the card reader hopper, the operator starts card reader operations at the card reader. Control signals from the card reader condition the card reader control logic to send a program interrupt request to the central processor via the I/O bus, and status signals condition the status gates in the card reader control logic. The program in the central processor performs a CONI instruction addressing the card reader to fetch the status information. The status information indicates that the card reader is in the ready to read condition. At this time, the central processor performs a CONO instruction addressing the card reader to pick a card from the card reader hopper and clear the program interrupt.

The first card column is read photoelectrically by the card reader, the data is strobed into temporary storage in the card reader buffer register contained in the control logic, and a program interrupt request is sent to the central processor. To service the program interrupt request, the central processor again performs a CONI instruction to fetch the status information which indicates the presence of data in the card reader buffer register. At this time, the central processor performs a DATAI instruction addressing the card reader to fetch the data from the card reader buffer register and clear the program interrupt.

The read data and data transfer procedures are repeated for each card column until the 80 card columns are read. Shortly after the last card column is read, an end of card status signal is routed to the central processor when the status information is fetched. The central processor picks the next card under program control and performs the data transfer procedures as explained above. Under normal operating conditions, the punched cards are read on demand until the hopper is empty or a malfunction is detected.

If the card reader detects a malfunction, or if the card reader hopper becomes empty, or the stacker becomes full, the status information indicates these conditions to the central processor and the card reader operation is halted when the end of the card is reached. The normal read operation is not resumed until the fault is corrected, the card reader CLEAR switch is depressed, and the card reader START switch is depressed.

1.1.2 LP10 Line Printer Control

The Type LP10 Line Printer Control interfaces the KA10 Processor to either a LP10A or LP10B Line Printer. The LP10A allows printing of up to 300 lines per minute and the LP10B allows printing of up to 600 lines per minute. Both are Anelex printers which use 64-character fonts and print 132-column lines. Figure 1-2 depicts a typical system configuration for the LP10 Line Printer Control.

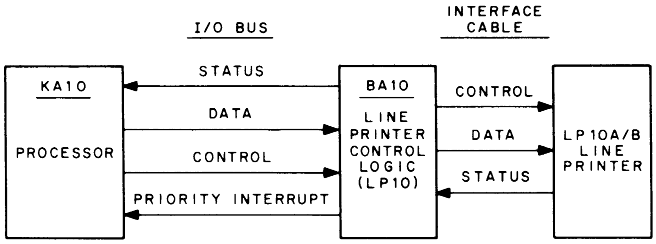


Figure 1-2 LP10 Line Printer System Configuration

Under program control, the LP10 line printer control logic accepts data from, or transmits status indications to, the central processor. Each data word may include characters to be printed, control characters causing printing and/or spacing, or illegal characters (codes not identified by the line printer). Printable characters and format control signals are sent to the line printer at a rate determined by the printer. Illegal character codes are ignored. Five characters at a time are transferred from the processor, and are unpacked and transmitted to the printer without further program intervention. The line printer informs the program that it requires the program's attention by means of the PDP-10 priority interrupt system. Status indications are done (ready for data), busy (line printer busy performing some function), and printer error (line printer is off line, interface cable disconnected, printer out of paper, etc.).

1.1.3 XY10 Plotter Control

The Type XY10 Plotter Control is used to interface the KA10 Processor to a CalComp Digital Incremental Plotter, Model 502, 518, 563 or 565, or to a similar incremental X-Y plotter which uses the same type of data and control information. The associated plotter allows data information to be graphically displayed on paper.

Figure 1-3 shows a typical system configuration for the XY10 Plotter Control.

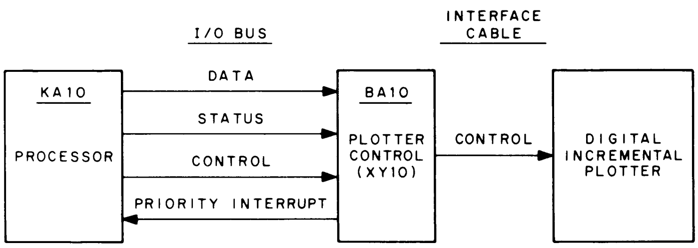


Figure 1-3 XY10 Plotter Control System Configuration

All plotter operations except the setting of coordinates at which the plotting operation begins are controlled by the plotter control logic and the central processor. The program in the processor performs a CONI instruction, addressing the plotter, to fetch status information from the status register. This information is transferred to the processor via the I/O bus and indicates whether the plotter is ready to accept data from the processor. When the status information indicates that the plotter is ready to accept data, the processor performs a CONO instruction to assign a priority interrupt channel. A DATAO instruction is performed to specify one or more of the following functions: raise or lower the plotter pen; move the pen carriage to the left or right; move the paper drum up or down. These functions are accomplished by setting associated flip-flops in the plotter control logic.

1.2 PHYSICAL CHARACTERISTICS DESCRIPTIONS

Descriptions of the BA10 Unit and associated devices are contained in the following paragraphs. For more detailed information on the card reader, line printer, and plotters refer to the device manuals listed in Section 1.4.

1.2.1 BA10 Unit

The BA10 Unit, a standard DEC CAB-9B cabinet, consists of the assemblies shown in Figure 1-4. Access doors, mounted on both front and rear of the unit, are held closed by magnetic latches.

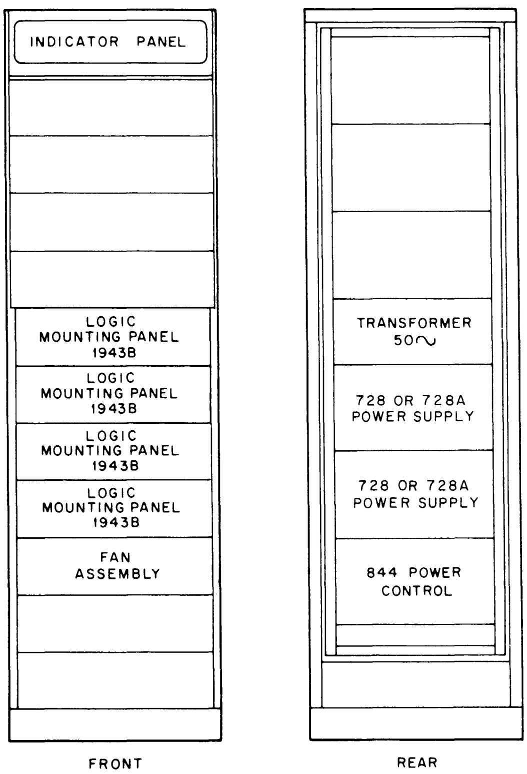


Figure 1-4 Type BA10 Unit Assembly Locations

The Type 844 Power Control and Type 728 Power Supplies are mounted inside the rear door on on a plenum door that is latched at the top by a spring-loaded pin. Module mounting panels are mounted behind the front door with the wiring side facing outward.

A fan at the bottom of the cabinet draws cooling air into the cabinet through a dust filter. This air is passed over the modules by a blower assembly mounted below the module mounting panel, and is exhausted through an opening at the top of the cabinet.

1.2.2 CR10 Card Reader

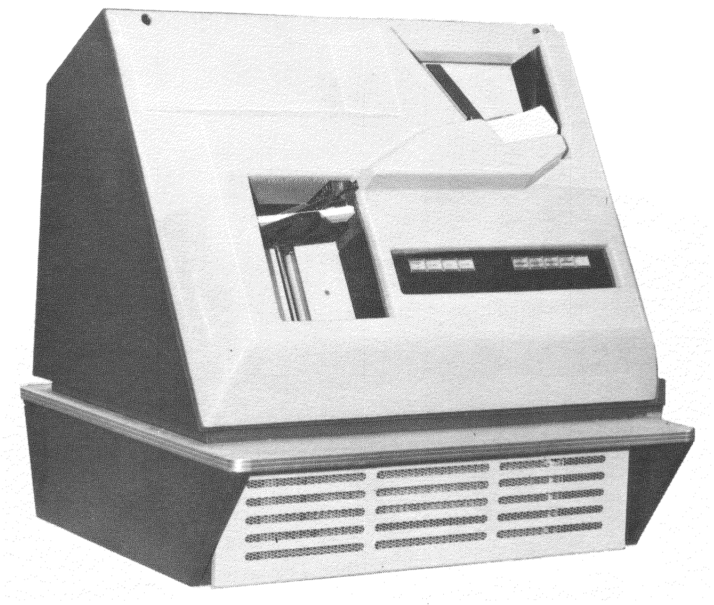


Figure 1-5 CR10 Card Reader

The CR10 Card Reader consists of a Model ERD Compact Card Reader manufactured by Soroban Engineering, Inc., Melbourne, Florida, card reader control logic mounted in the BA10, and the necessary interface cabling. The Soroban Model ERD Compact Card Reader, shown in Figure 1-5, is a high-performance desk top unit that end feeds standard 80-column punch cards on demand at a rate of approximately 1000 cards per minute (60 Hz power) or 830 cards per minute (50 Hz power). It includes a card handling deck with a supply hopper, photoelectric read station and stacker hopper. The connector modules of the card reader control cable are screwed into CD19 and CD20 of the BA10 and the power cable for the card reader is wired into the power control of the BA10.

There are two configurations of the card reader system available; the Type CR10A is a 60 Hz configuration and the Type CR10B is a 50 Hz configuration. With the exception of timing and power wiring, both configurations are similar. However, the operating times of the CR10B are slower throughout when compared to the operating times of the CR10A. The differences in the power wiring of the two configurations are shown on drawing D-IC-BA10-0-AC.

1.2.3 LP10A/LP10B Line Printers

The LP10A Line Printer System comprises a Model 4000 Line Printer shown in Figure 1-6 and manufactured by Anelex Corporation, Boston, Massachusetts, line printer control logic mounted in the BA10 cabinet, and the necessary interface cabling. The LP10B System consists of the same units except that the Anelex Corporation's Model 5000 Line Printer, shown in Figure 1-7, replaces the Model 4000.

Figure 1-6 LP10A Line Printer

Figure 1-7 LP10B Line Printer

The Anelex line printers print 132-column lines and are equipped with from 64- to 128-character fonts. LP10A printers print up to 300 lines per minute, while LP10B printers print up to 600 lines per minute. Both series printers are housed in free standing, console-type cabinets. Controls and indicators used during normal operations and for certain test functions are located on control panels on the front of and inside the cabinets.

1.2.4 XY10 Incremental Plotter

The XY10 Plotter System consists of a digital incremental plotter, plotter control logic mounted in the BA10 unit, and the necessary interface cabling. The most common plotters used with the XY10 are Models 563, 565, 502, or 518, manufactured by CalComp*, however, other plotters using similar control information may be used. These electromechanical plotter mechanisms are high precision units. Speed and paper size vary with the model used. Interfacing between the plotter and the plotter control logic is accomplished through an 8-line cable with a Cannon Connector Type SK-19-21C at one end and a DEC Type W028 Cable Connector at the other.

Typical plotter mechanism power requirements are: 105 to 125V, 50 or 60 cycles single phase (1.5A at 115V). Primary power is applied through a line cord supplied with the plotter.

*For additional information on the CalComp plotters specified, refer to the manuals listed in Section 1.4.

1.3 EQUIPMENT SPECIFICATIONS

Table 1-1 lists the general specifications for the BA10 and referenced peripheral devices and Table 1-2 lists the environmental requirements.

Table 1-1
Equipment Specifications

Component	Voltage (ac)	Current (A) Nominal @ 115V	Power Dissipation (W)	Heat Dissipation (Btu/Hr)	Dimensions (in.)	Service Clearance (in.)	Weight (lb)	Signal Cable Length (ft)
BA10 Cabinet	See note	20	600	2046	Height 69 Width 19-3/4 Depth 27	Front 36 Rear 36		N/A
Card Reader			1500	5100	Height 35 Width 35 Depth 32	Front 36 Rear 36	250	25
LP10A	See note	14	1500	5100	Height 50-3/4 Width 42-5/8 Depth 29	Front 36 Rear 48	1100	25
LP10B	See note	20	2500	6750	Height 55 Width 56 Depth 30	Sides 36 Rear 36	1600	25

NOTES

PDP-10 systems normally operate from 3-phase (WYE connected), 115V ± 10%, 60 Hz ± 2 Hz, or 230V ± 10%, 50 Hz ± 2 Hz phase to neutral. Individual devices have separate power cords using 3-wire 30A (single phase) Hubbell Twistlock Connectors. An earth/ground connection must be supplied through the power cord in addition to the ground bus requirements.

NOTES (Cont)

Equipment for use within North America will have the following power cord cap (male plug) supplied on the end of 25 ft line cord.

3-wire Hubbel #3331 (mates with Hubbell #3330)

Equipment for use outside of North America will have a pressure-type terminal strip suitable for 8 to 18 gauge wire enclosed inside of the equipment's power control.

Table 1-2
Environmental Requirements

Component	Operating Temperature (min-max F)	Storage Temperature (min-max F)	Humidity (relative min-max)
LP10A	60 to 95	0 to 125	40% to 80%
LP10B	60 to 95	0 to 125	40% to 80%

1.4 REFERENCE MATERIAL

The following documents contain material supplementing the information in this manual. These documents may be obtained from the nearest DEC office or from

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts

Title	Description
Digital Logic Handbook (C-105)	Specifications and descriptions of each FLIP CHIP module, plus simplified explanation of the selection and use of these modules in numerous applications
PDP-10 Maintenance Manual Volume I DEC-10-HMAA-D Volume II DEC-10-HMBA-D Volume III DEC-10-HMCA-D	Complete information on the internal operation of PDP-10 logic, memory, basic input/output, and processor options
PDP-10 System Reference Guide DEC-10-HGAA-D	Programming and operating information for the computer, including brief instruction on the Type CR10 Card Reader, LP10 Line Printer and XY10 Plotter

Title	Description
Instruction Manual for the Anelex Series 4000 Printer System	Complete operating instructions, principles of operation, and maintenance information for the Anelex Series 4000 Line Printer
Instruction Manual for the Anelex Series 5000 Printer System	Complete operating instructions, principles of operation, and maintenance information for the Anelex Series 5000 Line Printer.
PDP-10 Installation Manual	General information on system components necessary for planning layout and installation
Instruction Manual for the CalComp Digital Incremental Plotter, Models 563, 565, 502, or 518	Complete operating instructions, principles of operation, and maintenence instructions for the CalComp Digital Incremental Plotter used.
Technical Manual for the Soroban Compact Card Reader Model ERD	Complete operating instructions, principles of operation and maintenance instructions for the Soroban Engineering, Inc. Card Reader Model ERD

CHAPTER 2
OPERATING AND INSTALLATION INFORMATION

This chapter provides maintenance personnel with installation and operating information for the BA10 Hard Copy Control Unit and the three options. Tabular listings of the controls and indicators, with a brief explanation of their functions, are included. Installation information necessary to set up the BA10 and the three options includes; I/O bus connections, device cables, and jumper placement of the device selection cards. Operating notes discuss the BA10 power application and operation of the three options as well as device selection and I/O instructions. Programming notes provide the user with general programming information, the CR10 card codes and LP10 line printer codes.

2.1 BA10 CONTROLS AND INDICATORS

2.1.1 Power Control Panel

The Type 844 Power Control panel, Figure 2-1, controls the application of power to the BA10 and logic power to the three options. From the power control panel, input power is turned on, the BA10 power supplies are controlled, and either the local or remote power mode is selected. A tabular listing of the controls and indicators on the power control panel is given in Table 2-1.

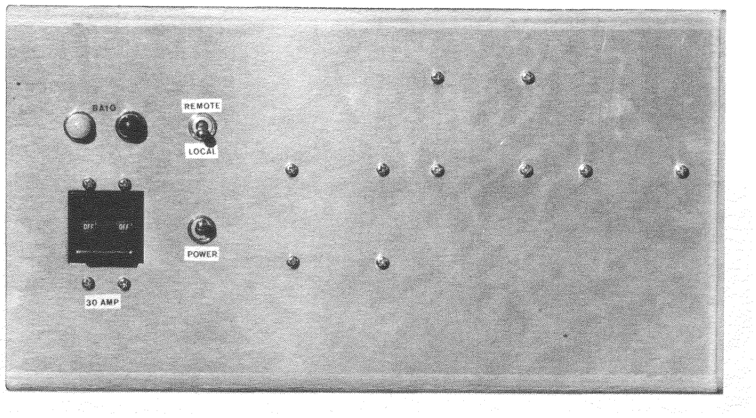


Figure 2-1 Type 844 Power Control Panel

Table 2-1
Type 844 Power Control Panel,
Controls and Indicators

Number	Nomenclature	Item	Function
1		Indicator - White	Indicates when 115 Vac or 230 Vac line power is applied.
2		Indicator - Red	Indicates when the 115 Vac line power is polarized wrong or when 230 Vac power is applied.
3	30A	Circuit Breaker	Controls line power to the convenience outlets and the BA10 option and protects input line.
4	REMOTE/ LOCAL	Toggle Switch	Selects the local mode or the remote mode.
5	POWER	Toggle Switch	Controls line power to the BA10 power supplies, line power to the card reader, and logic power to the control logic of the options.

2.1.2 BA10 Indicator Panel

The BA10 indicator panel, mounted on the top front of the BA10 unit, contains indicator lights to display the contents and status of the registers and flip-flops of the LP10, CR10, and XY10 controls. Figure 2-2 shows the indicator panel; the indicators and functions are listed on Table 2-2, 2-3 and 2-4.

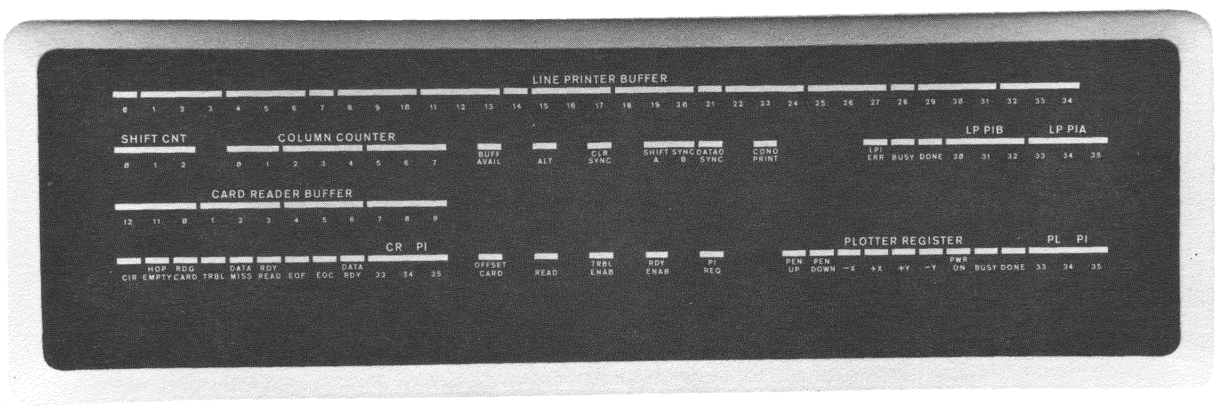


Figure 2-2 BA10 Cabinet Indicator Panel

Table 2-2
Card Reader Indicators

Nomenclature	Item	Function
CARD READER BUFFER 0 through 12	12 Indicators	Indicates the contents of the card reader buffer.
CIR (CARD IN READER)	Indicator	Lights to indicate when a card is passing through the read station.
HOP EMPTY	Indicator	Lights to indicate when the card reader hopper is empty.
RDG CARD	Indicator	Lights when the CRST READING CARD flip-flop is set.
TRBL	Indicator	Lights when a trouble signal is being received from the card reader.
DATA MISS	Indicator	Lights when the CRST DATA MISSED flip-flop has been set.
RDY READ	Indicator	Lights when a ready signal is being received from the card reader.
EOF	Indicator	Lights when the CRST END OF FILE flip-flop is set.
EOC	Indicator	Lights when the CRST END OF CARD flip-flop is set.
DATA RDY	Indicator	Lights when the CRST DATA READY flip-flop is set.
CR PI 33 34 35	3 Indicators	Indicates the program interrupt channel (CRST PI 33-35)
OFFSET CARD	Indicator	Lights when an offset command is generated.
READ	Indicator	Lights when the CRCN READ flip-flop is set.
TRBL ENAB	Indicator	Lights when the CRCN READER TRBL ENAB flip-flop is set.
RDY ENAB	Indicator	Lights when the CRCN READY ENAB flip-flop is set.
PI REQ	Indicator	Lights when a program interrupt is being requested on the assigned PI channel.

Table 2-3
Line Printer Control Logic Indicators

Nomenclature	Function
LINE PRINTER BUFFER 0-34	Displays the contents of the line printer buffer. Marked in five 7-bit groups.
SHIFT CNT 0-2	Displays the count in the shift counter that keeps track of the number of times the buffer register contents are shifted following a DATAO.
COLUMN COUNTER 0-7	Displays the contents of the column counter that counts the number of printable characters sent to the printer following a print command.
BUFF AVAIL	Lights when the line printer is in a condition to accept data.
ALT	Lights when the ALT flip-flop is set, indicating that the control logic has decoded a delete character. (Applicable to full 96- and 128-character printers only.)
CLR SYNC	Lights during the printer's BUFFER CLEAR operation.
SHIFT SYNC A	Lights when the LPCN SHIFT SYNC A flip-flop is set. Setting the flip-flop inhibits the initiation of a character transfer before the previous character is shifted out of the buffer register or during a line printer storage register overflow condition.
SHIFT SYNC B	Lights when the LPCN SHIFT SYNC B flip-flop is set. This flip-flop operates in conjunction with the LPCN SHIFT A flip-flop.
DATAO SYNC	Lights when the LPCN DATAO SYNC flip-flop is set. The flip-flop is set 2.2 μs after a DATAO SET pulse and remains set until the next DATAO CLEAR.
CONO PRINT	Lights when the CONO PRINT flip-flop is set. The flip-flop is set during print operations initiated by line printer storage overflow conditions.
LPI ERR	Lights to indicate various line printer error conditions such as printer off-line, out of paper, interface cable disconnected, etc.
BUSY	Lights when the LPST BUSY flip-flop is set. This flip-flop is set by CONO and DATAO commands and remains set until the line printer and/or control logic operations relating to those commands are completed.

Table 2-3 (Cont)
Line Printer Control Logic Indicators

Nomenclature	Function
DONE	Lights when LPST DONE flip-flop is set. The flip-flop is set at the end of a BUFFER CLEAR operation, and after all five characters sent by a DATAO have been processed. It is cleared by a CONO or DATAO command.
LP PIB 30-32	Display the contents of the LPST PIB 30-32 flip-flops that designate the channel over which line printer error interrupts are sent to the processor.
LP PIA 33-35	Display the contents of the LPST PIA 33-35 flip-flops that designate the channel over which done data interrupts are sent to the processor.

Table 2-4
Plotter Indicators

Nomenclature	Item	Function
PEN UP	Indicator	Lights when the PLCN RAISE PEN flip-flop is in the 1 state.
PEN DOWN	Indicator	Lights when the PLCN LOWER PEN flip-flop is in the 1 state.
-X	Indicator	Lights when the PLCN -X flip-flop is in the 1 state.
+X	Indicator	Lights when the PLCN +X flip-flop is in the 1 state.
+Y	Indicator	Lights when the PLCN +Y flip-flop is in the 1 state.
-Y	Indicator	Lights when the PLCN -Y flip-flop is in the 1 state.
PWR ON	Indicator	Lights when power is applied to the plotter mechanism. (Not present on all models.)
BUSY	Indicator	Lights when the PLST PLOT BUSY flip-flop is in the 1 state.
DONE	Indicator	Lights when the PLST PLOT DONE flip-flop is in the 1 state.
PL PI 33, 34, 35	3 Indicators	Indicates the program interrupt channel (PLST PI 33-35).

2.2 CR10 CONTROLS AND INDICATORS

Figure 2-3 shows control panel of the card reader and Table 2-5 is a tabular listing of the controls and indicators.

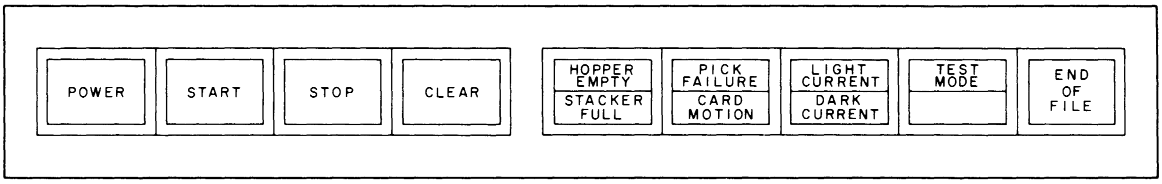


Figure 2-3 Card Reader Controls and Indicators

Table 2-5
Card Reader Controls and Indicators

Nomenclature	Item	Function
CARD MOTION	Indicator	Red when a card does not complete pass through the read station in less than 50 ms or if the trailing edge of the card is approximately 1/3 column or more out of synchronization with the timing signals. Indicates a jam or card movement error has caused trouble signal. WARNING If jam occurs, depress POWER switch to place the card reader in the power-off condition. Keep clear of belts and pulleys unless power is off. Depressing the CLEAR switch will start the drive motor if power is on; this could cause injury to personnel.
LIGHT CURRENT	Indicator	Red if read station phototransistor fails to see light after a card is picked and before the leading edge reaches the read station. Indicates defective light source or foreign material has caused a trouble signal. Remains red until trouble has been corrected and CLEAR switch is depressed.

Table 2-5 (Cont)
Card Reader Controls and Indicators

Nomenclature	Item	Function
DARK CURRENT	Indicator	Red if read station phototransistors are not darkened by the leading edge of card before column 1 is sensed. Indicates that a malfunction in the read station or a torn or perforated leading edge has caused trouble signal. Remains red until trouble has been repaired and the CLEAR switch depressed.
TEST MODE	Indicator	Red when the card reader TEST/NORMAL switch is in the TEST position.
END OF FILE	Momentary Push Switch	Causes an end-of-file signal to be generated.
TEST/NORMAL (not shown in Figure 2-1)	Toggle Switch	Located on logic circuit assembly. In TEST position, a continuous select and read command is simulated to permit self-sequencing of reader
	Circuit Breaker (not shown in Figure 2-1)	Located on the rear of the card reader. Controls the application of primary power and protects card reader from overload.
POWER	Alternate Push Switch	Applies operating power to the card reader dc-power supply and drive motor. Enables operation of other card reader controls and indicators. Causes a card reader power-on reset pulse to be generated to set initial conditions in the card reader logic circuits.
	Indicator	Green when power is on. Dark when power is off.
START	Momentary Push Switch	Places the card reader logic in the START condition (if not prevented by a trouble condition). In the TEST mode, causes picking and reading to begin at maximum throttled rate.
	Indicator	Green when card reader is in START condition. White when card reader is in STOP condition.
STOP	Momentary Push Switch	Places the card reader logic in the STOP (off-line) condition. Stops picking and reading.
	Indicator	Yellow when card reader is in STOP condition. White when card reader is in START condition.

Table 2-5 (Cont)
Card Reader Controls and Indicators

Nomenclature	Item	Function
CLEAR	Momentary Push Switch	Resets the card reader logic and starts drive motor if trouble condition that caused the stop has been corrected.
	Indicator	Red when card reader logic has detected a trouble condition. White when there is no trouble.
HOPPER EMPTY	Indicator	Red when there are no cards in the card reader hopper. Remains red until additional cards are placed in hopper and CLEAR switch is depressed.
STACKER FULL	Indicator	Red when card reader stacker contains approximately 1000 cards. Remains red until cards are removed from hopper and CLEAR switch is depressed.
PICK FAILURE	Indicator	Red when a card does not reach the card reader read station within 18 ms* after the picker is energized. Remains red until trouble is corrected and CLEAR switch is depressed.

*CR10A operating times are used throughout this manual; CR10B operating times are slower.

2.3 LP10 CONTROLS AND INDICATORS

Since more than one line printer system may be used with the LP10 control logic, refer to the appropriate line printer instruction manual for a description of the controls and indicators. Line printer indicators on the BA10 are shown in Figure 2-2 and a brief functional description of each is contained in Table 2-3.

2.4 XY10 CONTROLS AND INDICATORS

Because several models of plotters can be used with the XY10 control logic, reference should be made to the instruction manual for the plotter used in regard to the location of indicators and controls. Plotter indicators on the BA10 are shown in Figure 2-2 and a brief functional description of each is contained in Table 2-4.

2.5 OPERATING NOTES

2.5.1 BA10 Power Application

Application of power to the BA10 is controlled at the central processor's console power switch when the following switches on the BA10 power control are placed in the following positions and the system's REMOTE TURN ON BUS is connected to the BA10 power control.

a. The LOCAL/REMOTE switch in the REMOTE position

b. The POWER switch in the up position

c. The circuit breaker in the up position

These are the normal switch positions.

To control the application of power at the power control panel of the BA10 unit during maintenance operation, the LOCAL/REMOTE switch is placed in the LOCAL position and the circuit breaker is left in the up position. Then, the POWER switch may be used to control the application of power, as desired.

2.5.2 CR10 Operation

The operational control of the card reader system is exercised by the central processor under program control after power has been applied and the card reader start-up procedure has been performed. Power application is controlled at the central processor's console power switch during normal operation; but, it is also possible to control power application at the BA10 power control during maintenance operation. The card reader is placed in the START condition by performing the card reader start-up procedure.

The card reader is interfaced to the card reader control logic contained in the BA10. The card reader control logic is interfaced to the central processor I/O bus. Device selection lines of the I/O bus are used to select the card reader and the I/O instructions are used to control the card reader operation.

2.5.2.1 Card Reader Start Procedure - To place the card reader in the START condition, the following card reader switches are placed in the indicated positions in the following sequence after power has been applied.

a. The TEST/NORMAL switch in the NORMAL position.

b. The circuit breaker in the up (ON) position.

c. Depress the POWER switch.

d. Load the cards into the card reader hopper.

e. Depress the CLEAR switch.

f. Depress the START switch.

2.5.2.2 Card Reader Shutdown - To shut down the card reader, perform one of the following:

a. Depress the card reader STOP switch.

b. Allow the hopper empty condition to occur.

To remove the primary ac power from the card reader, place the card reader circuit breaker in the down (OFF) position (usually not necessary except for maintenance).

2.5.3 LP10 Operation

Operational control of the line printer system is exercised by the central processor under program control after power has been applied and the line printer start-up procedure has been performed.

2.5.3.1 Line Printer Operation - The line printer houses its own dc supplies and is powered from any ac source that meets system specifications. Pressing the ON switch on the line printer control panel initiates the sequencing on of the printer's power supplies. When the sequence is completed, the ON switch illuminates. With ON illuminated, pressing the START switch places the line printer on-line, unless some printer alarm is true. The on-line condition enables the interface between the line printer and the control logic.

When pressed, the line printer STOP switch places the printer off-line with the power supplies still active. If the line printer is placed off-line with the printer storage register still containing characters, the MANUAL PRINT switch lights. The characters will be printed out if the MANUAL PRINT switch is pressed.

The line printer OFF switch initiates the sequence for deactivating the power supplies. Also, the LP control provides the printer with the TURN OFF level which, during normal operation is at -3V. If the REMOTE/LOCAL switch on the line printer maintenance panel is in the REMOTE position, the LP10 can turn off the printer by grounding the TURN OFF level. This condition occurs only when the BA10 power is turned off. When this happens, the line printer power supplies are deactivated in the same manner as when the OFF switch is pressed. As long as the TURN OFF level is at ground and the printer's REMOTE/LOCAL switch is in the REMOTE position, the printer cannot be turned on. When the level returns to -3V, the ON switch can be used to reactivate the printer.

2.5.4 XY10 Operation

The plotter is completely under the control of the central processor after application of power to the plotter and the BA10.

Power to the BA10 is controlled by the central processor's console switch during normal operation. It is also possible to control power application at the BA10 power control during maintenance operation. The plotter mechanism obtains its primary ac power through its own line cord which can be connected to any suitable 115V receptacle.

The plotter is connected to the plotter control logic contained in the BA10. The plotter logic is connected to the central processor's I/O bus. Device selection lines of I/O bus select the plotter and the I/O instruction controls plotter operation.

2.5.4.1 Plotter Start Procedure - To initialize the plotters, the following procedure should be followed.

a. The circuit breaker on the BA10 should be in the ON position.

b. The plotter POWER ON/OFF switch should be in the ON position.

c. The user should prepare the chart paper and designate the coordinates where the plot is to begin as described in the plotter manual.

2.5.5 Device Selection

An I/O device is selected by bits 3-9 of the I/O instruction from the processor. Seven complementary pairs of signals representing IOS3 through IOS9 of the I/O bus are routed to the device selection cards in the BA10 cabinet. Jumpers are inserted at the device selection cards, to provide a binary configuration corresponding to the number designated for a particular device. When this number appears on the I/O bus, the device is selected.

The following configurations correspond to each device listed.

CR10	Card Reader	001	101	0	(150_8)
LP10	Line Printer	001	010	1	(124_8)
XY10	Plotter	001	100	0	(140_8)

2.5.6 I/O Instructions

A brief summary of the I/O instructions for the three options is contained in this section. For a more detailed discussion of the I/O instructions refer to the Programming Notes, Section 2.6.

2.5.6.1 CR10 I/O Instructions - The card reader is designed to respond to three of the four standard I/O instructions. In the following section, the I/O instructions are identified and a brief summary of their functions is provided. Refer to Section 2.6, Programming Notes, for a general reference to card reader programming.

Instruction	Function
CONO (Conditions Out)	A transfer of conditions from the central processor to the card reader control logic; may perform one or more of the following. a. Clear the card reader control logic b. Load the PI channel number into the PI register. c. Pick a card from the card reader's hopper. d. Generate an offset command e. Enable the reader trouble and/or ready-to-read program interrupts.
CONI (Conditions In)	Transfers card reader and card reader control logic status information into the central processor.
DATAI (Data In)	Transfers data from the card reader control logic buffer register into the central processor.

2.5.6.2 LP10 I/O Instructions - The line printer is designed to respond to three of the four standard PDP-10 I/O instructions as described below.

Instruction	Function
CONO (Conditions Out)	Controls the line printer by performing functions such as: a. Setting or clearing the BUSY flag, b. Setting or clearing the DONE flag, c. Assigning channels for done and printer-error interrupts, d. Clearing the LPT buffer.
CONI (Conditions In)	Transfers line printer status information to the processor.
DATAO (Data Out)	Sets the BUSY flag, clears the DONE flag, and loads five 7-bit characters into the control logic's buffer register.

2.5.6.3 XY10 I/O Instructions - The plotter responds to three of the four standard I/O instructions as described below. Section 2.7, Programming Notes, explains these instructions in greater detail.

Instruction	Function
CONO (Conditions Out)	A transfer of conditions from the central processor to the plotter control logic; may perform one or more of the following. a. Load the PI channel number into the PI register b. Clear or set the BUSY or DONE flip-flops
CONI (Conditions In)	Reads the plotter status register
DATAO (Data Out)	Transfers data from the central processor into the plotter control data buffer.

2.6 PROGRAMMING NOTES

This section contains programming notes for the three options to provide maintenance personnel with a general description of system programming.

2.6.1 CR10 Programming Notes*

The CR10 Card Reader reads 80-column cards on a column-by-column basis. The card reader supplies data in the column binary mode; thus, the programmer can supply any translation desired (e.g., from card codes to ASCII). The card reader supplies data to the processor, one column at a time, using the 12 least-significant bits of the data word (bits 24 through 35).

2.6.1.1 DATAI - The layout of the data word read into the central processor during a DATAI is shown in Figure 2-4 and the card codes are shown in Table 2-6.

ROW	12	11	0	1	2	3	4	5	6	7	8	9	DATAI
BIT	24	25	26	27	28	29	30	31	32	33	34	35	

Figure 2-4 DATAI Data Word

* Programming notes are effective as of January 4, 1968.

Table 2-6
Card Codes

Rows Punched	026 Data Processing	026 FORTRAN	029	DEC 026	DEC 029	Octal Representation
(None)	(space)	(space)	(space)	(space)	(space)	0000
12	&	+	&	+	&	4000
11	-	-	-	-	-	2000
0	0	0	0	0	0	1000
1	1	1	1	1	1	0400
2	2	2	2	2	2	0200
3	3	3	3	3	3	0100
4	4	4	4	4	4	0040
5	5	5	5	5	5	0020
6	6	6	6	6	6	0010
7	7	7	7	7	7	0004
8	8	8	8	8	8	0002
9	9	9	9	9	9	0001
12-0	N/A	N/A	N/A	?	N/A	5000
12-1	A	A	A	A	A	4400
12-2	B	B	B	B	B	4200
12-3	C	C	C	C	C	4100
12-4	D	D	D	D	D	4040
12-5	E	E	E	E	E	4020
12-6	F	F	F	F	F	4010
12-7	G	G	G	G	G	4004
12-8	H	H	H	H	H	4002
12-9	I	I	I	I	I	4001
11-0	N/A	N/A	N/A	:	N/A	3000
11-1	J	J	J	J	J	2400
11-2	K	K	K	K	K	2200
11-3	L	L	L	L	L	2700
11-4	M	M	M	M	M	2040
11-5	N	N	N	N	N	2020
11-6	O	O	O	O	O	2010
11-7	P	P	P	P	P	2004

Table 2-6 (Cont)
Card Codes

Rows Punched	026 Data Processing	026 FORTRAN	029	DEC 026	DEC 029	Octal Representation
11-8	Q	Q	Q	Q	Q	2002
11-9	R	R	R	R	R	2001
0-1	/	/	/	/	/	1400
0-2	S	S	S	S	S	1200
0-3	T	T	T	T	T	1100
0-4	U	U	U	U	U	1040
0-5	V	V	V	V	V	1020
0-6	W	W	W	W	W	1010
0-7	X	X	X	X	X	1004
0-8	Y	Y	Y	Y	Y	1002
0-9	Z	Z	Z	Z	Z	1001
8-2	N/A	N/A	:	←	:	0202
8-3	#	=	#	=	#	0102
8-4	@	-	@	@	@	0042
8-5	N/A	N/A	'	↑	'	0022
8-6	N/A	N/A	=	'	=	0012
8-7	N/A	N/A	"	\	"	0006
12-8-2	N/A	N/A	¢	N/A	[	4202
12-8-3	.	.	.	.	.	4102
12-8-4	⌑	)	<	)	<	4042
12-8-5	N/A	N/A	(	]	(	4022
12-8-6	N/A	N/A	+	<	+	4012
12-8-7	N/A	N/A	|	!	↑	4006
11-8-2	N/A	N/A	!	N/A	!	2202
11-8-3	$	$	$	$	$	2102
11-8-4	*	*	*	*	*	2042
11-8-5	N/A	N/A	)	[	)	2022
11-8-6	N/A	N/A	;	>	;	2012
11-8-7	N/A	N/A	¬	&	\	2006
0-8-2	N/A	N/A	"0-8-2"	;	]	1202
0-8-3	,	,	,	,	,	1102

Table 2-6 (Cont)
Card Codes

Rows Punched	026 Data Processing	026 FORTRAN	029	Data 026	Data 029	Octal Representation
0-8-4	%	(	%	(	%	1042
0-8-5	N/A	N/A	—	"	←	1022
0-8-6	N/A	N/A	>	#	>	1012
0-8-7	N/A	N/A	?	%	?	1006
12-11-0-1	N/A	N/A	N/A	End of File	End of File	7400
12-0-2-4-6-8	N/A	N/A	N/A	Mode Switch	Mode Switch	5252
7-9	N/A	N/A	N/A	Binary	Binary	XX05

NOTE

12-0 is converted to 12-8-2 internally in DEC 026
11-0 is converted to 11-8-2 internally in DEC 026

2.6.1.2 CONO - The layout of the conditions word transferred to the card reader control logic during a CONO is shown in Figure 2-5.

CLEAR READER	OFFSET CARD		READ CARD	READER TRBL ENAB	CLEAR DATA MISSED	READY ENAB	CLEAR END OF FILE	CLEAR END OF CARD	CLEAR DATA READY	PI CHANNEL			CONO
23	24	25	26	27	28	29	30	31	32	33	34	35	

Figure 2-5 CONO Conditions Word

The CONO bits have the following significance:

a. Bit 23 = 1, clears the card reader control logic flip-flops. That is, the PI channel number is set to 0, the data missed, end of file, end of card, and data ready flags are set to 0. The reader trouble and ready to read signals are disabled from causing a program interrupt. The same actions are also caused by turning on the card reader control and by the IOB RESET signal.

b. Bit 24 = 1, causes the card presently being read to be offset from the rest of the stacked cards. This command is only effective when the card is in the reader (CONI bit 24 = 1).

c. Bit 26 = 1, causes a card to be read. To maintain maximum speed, the read command must be given before the ready to read flag appears. However, applying the read command a few hundred microseconds after the ready to read flag will not slow the card reader significantly.

d. Bit 27 = 1, sets the CR CN READER TRBL ENAB flip-flop; bit 27 = 0, clears the CRCN READER TRBL flip-flop (jam transferred).

e. Bit 28 = 1, clears the data missed flag.

f. Bit 29 = 1, sets the CRCN READY ENAB flip-flop; bit 29 = 0, clears the CRCN READY ENAB flip-flop (jam transferred).

g. Bit 30 = 1, clears the end-of-file flag.

h. Bit 31 = 1, clears the end-of-card flag.

i. Bit 32 = 1, clears the data ready flag.

j. Bits 33 through 35 load the PI channel.

2.6.1.3 <u>CONI</u> - The layout of the status word read into the central processor during a CONI is shown in Figure 2-6.

READER TROUBLE ENABLE	READER READY ENABLE	PICK ERROR	PHOTO CELL ERROR	CARD MOTION ERROR	READER STOP	CARD IN READER	HOPPER EMPTY OR STACKER FULL	READING CARD BUSY	READER TROUBLE PI	DATA MISSED PI	READY TO READ (PI)	END OF FILE (PI)	END OF CARD (PI)	DATA READY (PI)	PI CHANNEL		
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

Figure 2-6 CONI Status Word

The CONI bits have the following significance.

a. Bit 18 = 1, indicates that the CRCN READER TRBL ENAB flip-flop is set. When this flip-flop is set, the READER TROUBLE PI is enabled.

b. Bit 19 = 1, indicates that the CRCN READY ENAB flip-flop is set. When this flip-flop is set, the READY TO READ PI is enabled.

c. Bit 20 = 1, indicates that the card reader did not pick a card when the IRC signal was routed to the card reader (card reader PICK FAILURE indicator).

d. Bit 21 = 1, indicates that the card reader failed the light/dark current test before the card was read. Indicates a defective light source, foreign material in the read station, or a defective card.

e. Bit 22 = 1, indicates that a card has slipped or jammed while moving through the card reader (CARD MOTION indicator).

f. Bit 23 = 1, indicates that the card reader power is on, but the card reader is off-line due to an error condition or the stop mode (STOP switch depressed).

g. Bit 24 = 1, indicates the card is actually in the card reader; when bit 24 = 1, the offset signal can be given. This signal is true (1) from approximately 1.8 ms before the first data ready program interrupt until approximately 1.8 ms after the last (eightieth) data ready program interrupt.

h. Bit 25 = 1, indicates that the card reader hopper is empty or that its stacker is full.

i. Bit 26 = 1, indicates that the card reader is busy reading a card. This signal goes true (1) upon initiation of a Read Card command and goes false (0) when the card in reader signal becomes false.

j. Bit 27 = 1, indicates that the card reader has detected internal trouble, or the card reader has been placed off-line by depressing the STOP switch. This signal is caused by one of the following conditions.

(1) Hopper empty; stacker full: pick failure - failure to start reading a card on command

(2) Read failure - failure to distinguish presence and absence of holes in the card

(3) Card motion error - the card is slipping or jammed in the reader; or card reader off-line. Any of these conditions require operator intervention. The card reader has illuminated indicators to allow the operator to determine exactly what the trouble is.

k. Bit 28 = 1, indicates that the central processor did not read a column of data in time to prevent its being destroyed by the next column of data. Except for column 80, the data must be read in the central processor with a DATAI within approximately 350 μs after the data ready program interrupt.

l. Bit 29 = 1, indicates that the card reader is ready to read a card and will accept a read card command. This ready to read signal is true when the trouble signal is false, hopper empty or stacker full signal is false, and card in reader signal is false.

m. Bit 30 = 1, indicates that the END OF FILE switch on the card reader has been depressed. This switch is ignored unless the reader trouble is true (i.e., a red indicator is illuminated) or the card reader is off-line. To reset this flag, a CONO is performed with bit 30 = 1.

n. Bit 31 = 1, indicates that the end of the card has been reached. This flag is set when the card in reader signal goes false (bit 24 = 0) and is cleared by a CONO with bit 31 = 1.

o. Bit 32 = 1, indicates that a column of data is ready to be read into the central processor. This flag is cleared when the column of data is read by a DATAI or by doing a CONO with bit 32 = 1. If the data is not read before the next data is available, the old data is available, the old data is destroyed and the data missed flag is set.

p. Bits 33 through 35 indicate the current setting of the PI channel register.

2.6.2 LP10 Programming Notes

2.6.2.1 Line Printer Character Codes - The PDP-10 sends 7-bit ASCII (modified) characters (see Table 2-7) to the printer. For 64- and 96-character printers, codes 000-037_8 and 177_8 are control characters, and codes 040_8-176_8 are printable characters. Only ten of the control codes are decoded to cause line printer functions. These functions are the same as those performed on a teleprinter (except that a carriage return is performed before all paper feed functions). Except when a 128- character printer is employed, the other control codes are ignored. The ten control characters that are decoded and simulated are as follows.

a. Horizontal Tab (ASCII 011_8) - A horizontal tab of eight columns is simulated by feeding the necessary spaces to the line printer. The character following the horizontal tab character is printed in the column corresponding to the tab stop (i.e., column 9, 17, 25, etc.). At least one space always exists between the characters before and after the horizontal tab.

b. Carriage Return (ASCII 015_8) - A teleprinter-style carriage return is simulated, i.e., the contents of the line printer memory are printed, but paper spacing is inhibited. The next print cycle overprints the line printed by the carriage return, unless a paper-spacing character appear before the next printable character. A printing character after a carriage return prints in column 1.

c. Line Feed (ASCII 012_8) - Simulates a teleprinter-style carriage return followed by a teleprinter style line feed. The line printer memory is printed, then the paper is spaced until a hole is seen in channel 8 of the vertical format tape, ordinarily one vertical space. The next character is printed in column 1. Vertical spacing is discussed in greater detail in the following subparagraph.

d. Vertical Tab (ASCII 013_8) - Simulates a teleprinter-style carriage return followed by a vertical tab. The line printer memory is printed and the paper is spaced until a hole is seen in channel 7 of the vertical format tape, ordinarily 20 vertical spaces. The next character is printed in column 1.

e. Form Feed (ASCII 014_8) - Simulates a teleprinter-style carriage return and form feed. The line printer memory is printed and the paper is spaced until a hole is seen in channel 1 of the vertical format tape, ordinarily at the top of the page. The next character is printed in column 1.

f. DC_0 through DC_4 (ASCII 020_8 through 024_8) - These device control functions simulate a teleprinter-style carriage return followed by vertical paper motion. The line printer memory is printed and the paper is spaced until a hole is seen in the channel of the vertical format tape corresponding to the command given (channel 2 through channel 6). The next character is printed in column 1.

The printable characters employed by a line printer system depend on the number of characters contained on the printer drum. Printable characters 040_8 through 137_8 are used for 64 - character printers, and 040_8 through 176_8 for 96-character printers. If a lower case character (140_8 through 176_8) is sent to a 64-character printer, the corresponding upper case character (100_8 through 136_8) is printed.

On 128-character printers, printing characters are hidden under control codes HT (011_8), CR (015_8), LF (012_8), VT (013_8), NULL (000_8), FF (014_8), DC_0 through DC_4 (020_8 to 024_8), and delete (177_8). The hidden characters are printed by prefixing each character with the delete character. Thus, DELETE LF loads the printer buffer with the character hidden under LF.

On certain special "full 96-character" printers a character is hidden underneath the delete character. This character is printed by sending the string "delete delete" to the printer. The first delete indicates that a hidden character follows, and the second delete is put into the printer memory to be printed.

Table 2-7
PDP-10 ASCII (Modified USASCII X3)

Parity Bit	7-Bit Octal "ASCII"	Name(s)	Comments
0	000	NULL IDLE	Sometimes known as tape feed, control @, control shift P.
1	001	SOM SOH	Control A, start of message, start of heading.
1	002	EOA STX	Control B, end of address, start of text.
0	003	EOM ETX	Control C, end of message, end of text.
1	004	EOT	Control D, end of transmission, disconnects data sets
0	005	WRU ENQ	Control E, who are you, enquiry, triggers identification in TTY equipped with feature.
0	006	RU ACK	Control F, are you, acknowledge.
1	007	BELL BEL	Control G, rings bell in TTY.
1	010	FE0 BS	Control H, backspace, format effector, backspaces some TTYs
0	011	HTAB HT	Control I, horizontal tab, performs horizontal tab function
0	012	LINE FEED LF	Control J, line feed, advances paper to next line (without returning to beginning of line)
1	013	VTAB VT	Control K, vertical tab, performs vertical tab function
0	014	FORM FF	Control L, form feed, skips to top of next page
1	015	RETURN CR	Control M, carriage return, returns to beginning of present line
1	016	SO Black	Control N, shift out, change ribbon color to black
0	017	SI Red	Control O, shift in, change ribbon color to red
1	020	DLE DC0	Control P, device control 0, data link escape
0	021	DC_1 X-ON	Control Q, device control 1, transmitter on
0	022	DC_2 AUX-ON	Control R, device control 2, tape punch on, auxiliary on
1	023	DC_3 X-OFF	Control S, device control 3, transmitters off
0	024	DC_4 TAPE AUX-OFF	Control T, device control 4, tape punch off, auxiliary off
1	025	ERR NAK	Control U, error, negative acknowledge
1	026	SYNC SYN	Control V, synchronous idle
0	027	LEM ETB	Control W, logical end of medium, end of transmission block

Table 2-7 (Cont)
PDP-10 ASCII (Modified USASCII X3)

Parity Bit	7-Bit Octal "ASCII"	Name(s)	Comments
0	030	S_0 CAN	Control X, separator 0, cancel
1	031	S_1 EM	Control Y, separator 1, end of medium
1	032	S_2 SUB	Control Z, separator 2, substitute
0	033	S_3 ESC	Control shift K, separator 3, escape (ALTMODE)
1	034	S_4 FS	Control shift L, separator 4, file separator
0	035	S_5 GS	Control shift M, separator 5, group separator
0	036	S_6 RS	Control shift N, separator 6, record separator
1	037	S_7 US	Control shift O, separator 7, unit separator
1	040	(space)	
0	041	! shift 1	
0	042	" shift 2	
1	043	# shift 3	
0	044	$ shift 4	
1	045	% shift 5	
1	046	& shift 6	
0	047	´ shift 7 (accent acute)	
0	050	(shift 8	
1	051	) shift 9	
1	052	* shift :	
0	053	+ shift ;	
1	054	,	
0	055	-	
0	056	.	
1	057	/	
0	060	Ø	
1	061	1	
1	062	2	
0	063	3	
1	064	4	
0	065	5	
0	066	6	

Table 2-7 (Cont)
PDP-10 ASCII (Modified USASCII X3)

Parity Bit	7-Bit Octal "ASCII"	Name(s)	Comments
1	067	7	
1	070	8	
0	071	9	
0	072	:	
1	073	;	
0	074	< shift ,	
1	075	= shift -	
1	076	> shift .	
0	077	? shift /	
1	100	@	
0	101	A	
0	102	B	
1	103	C	
0	104	D	
1	105	E	
1	106	F	
0	107	G	
0	110	H	
0	111	I	
1	112	J	
0	113	K	
1	114	L	
0	115	M	
0	116	N	
1	117	O	
0	120	P	
1	121	Q	
1	122	R	
0	123	S	
1	124	T	
0	125	U	

Table 2-7 (Cont)
PDP-10 ASCII (Modified USASCII X3)

Parity Bit	7-Bit Octal "ASCII"	Name(s)	Comments
0	126	V	
1	127	W	
1	130	X	
0	131	Y	
0	132	Z	
1	133	[	
0	134	\	
1	135	]	
1	136	↑	
0	137	←	
0	140	`	
1	141	a	
1	142	b	
0	143	c	
1	144	d	
0	145	e	
0	146	f	
1	147	g	
1	150	h	
0	151	i	
0	152	j	
1	153	k	
0	154	l	
1	155	m	
1	156	n	
0	157	o	
1	160	p	
0	161	q	
0	162	r	
1	163	s	
0	164	t	

Table 2-7 (Cont)
PDP-10 ASCII (Modified USASCII X3)

Parity Bit	7-Bit Octal "ASCII"	Name(s)	Comments
1	165	u	
1	166	v	
0	167	w	
0	170	x	
1	171	y	
1	172	z	
0	173	{	
1	174	¬ (NOT)	
0	175	}	
0	176	|	
1	177	(Rubout) (Delete)	

2.6.2.2 Vertical Format Tape - Eight of the characters sent to the line printer direct the printer to space the paper vertically. When executing one of these characters, the printer determines the amount of spacing required by examining an 8-column vertical-format tape, each column of which corresponds to one of the vertical control characters. The printer spaces the paper vertically until it encounters a hole in the tape column specified by the character being executed. Any vertical format tape may be used, but a tape in format as shown in Figure 2-8, is supplied as a general-purpose tape for 11-in. high fan-fold paper.

Table 2-8
Vertical Spacing Characters

Control Character (ASCII)	Tape Column	Number of vertical spaces between holes
Line Feed (012_8)	8	1
Vertical Tab (013_8)	7	20
Form Feed (014_8)	1	*Top of page
DC_0 (020_8)	2	30
DC_1 (021_8)	3	2

*This channel is used by the TOP-OF-FORM button.

Table 2-8 (Cont)
Vertical Spacing Characters

Control Character (ASCII)	Tape Column	Number of vertical spaces between holes
DC_2 (022_8)	4	3
DC_3 (023_8)	5	1 punched every space
DC_4 (024_8)	6	10

Six blank lines are left on the control tape before the top-of-page position except in the DC_3 case. In the vertical format control column corresponding to DC_3, holes are punched to allow printing across the fold for ease of photoreproduction. Usual operation allows 60 printing lines per page, with 66 printing lines in the case of DC_3 spacing.

2.6.3 XY10 Programming Notes

This section contains a brief description of the CONO, CONI, and DATAO commands that are used by the plotter.

2.6.3.1 DATAO - The configuration of the data word that is sent to the plotter control logic from the PDP-10 central processor during a DATAO is shown in Figure 2-7.

PEN RAISE (UP)	PEN LOWER (DOWN)	-X (DRUM UP)	+X (DRUM DOWN)	+Y (CARRIAGE LEFT)	-Y (CARRIAGE RIGHT)
30	31	32	33	34	35

Figure 2-7 DATAO Data Word

The DATAO bits have the following significance.

a. Bit 30 = 1, the pen is raised from the paper

b. Bit 31 = 1, the pen is lowered to the paper

c. Bit 32 = 1, the pen is moved in the -X direction

d. Bit 33 = 1, the pen is moved in the +X direction

e. Bit 34 = 1, the paper drum is moved in the +Y direction

f. Bit 35 = 1, the paper drum is moved in the -Y direction

In addition, the DATAO instruction clears the PLST PLOT DONE flip-flop and sets the PLST PLOT BUSY flip-flop. After the plotter has finished with the previous movement, the PLST PLOT BUSY flip-flop is cleared and the PLST PLOT DONE flip-flop is set, causing a PI request.

2.6.3.2 CONO - The configuration of the control word that is transferred to the plotter control during a CONO is shown in Figure 2-8.

	BUSY	DONE	PI CHANNEL		
30	31	32	33	34	35

Figure 2-8 CONO Conditions Word

The CONO bits have the following significance.

a. Bit 31 = 1, sets the PLST PLOT BUSY flip-flop

b. Bit 32 = 1, sets the PLST PLOT DONE flip-flop, thereby clearing the PLST PLOT BUSY flip-flop

c. Bits 33-35 load the PI channel

2.6.3.3 CONI - The configuration of the status register that is read by a CONI is shown in Figure 2-9.

POWER ON*	BUSY	DONE PI	PI CHANNEL		
30	31	32	33	34	35

* OPTIONAL WITH PARTICULAR PLOTTER

Figure 2-9 CONI Status Word

The CONI bits have the following significance.

a. Bit 30 = 1, indicates power is applied to the plotter*

b. Bit 31 = 1, indicates that the plotter is presently performing a command

c. Bit 32 = 1, indicates the plotter has finished the last command and will accept another. The DONE flag causes a PI request. It is cleared by either a CONO or DATAO instruction.

d. Bit 33-35 contain the present setting of the PI channel register.

2.7 INSTALLATION

This section contains general information on card reader, line printer and plotter installation. Interface cabling information is provided as an aid to installation and installation planning. Option adjustments that are required during installation are described.

2.7.1 Device Selection Cards

Device selection of the three options is obtained by decoding information on the device selection lines. The following paragraphs describe how each device is selected.

The device numbers from the central processor are routed to all devices connected to the I/O bus via the 14 device-selection lines (7 pairs) of the I/O bus. The device selection lines connect to the device number selection cards located in slots of the BA10 as follows.

CR10 Card Reader	H10 and H11
LP10 Line Printer	J11 and J12
XY10 Plotter	J8 and J9

Jumpers located on the selection cards can be arranged so that the device control logic will respond to any device number. If a special device number has not been specified by the customer, the jumpers on the device selection cards are connected so the device will respond to the standard device numbers (Section 2.5.5). To prevent the device control logic from responding to more than one device number, one jumper from each pair must always be connected. If a device option is not utilized, the device decoder is disabled by connecting a jumper between E and C on the appropriate card as follows.

CR10 Card Reader	H11
LP10 Line Printer	J12
XY10 Plotter	J9

Figures 2-10, 2-11, and 2-12 are provided to aid maintenance personnel in understanding the device number selection cards. A schematic representation of the device number selection cards, drawing D-BS-BA10-0-IOCA, shows jumper placement for the standard device number. The location

*Optional with particular plotter.

of the jumper associated with each octal digit is shown in a pictorial representation. If a different device number is to be used, the tables in Figures 2-10 through 2-12 may be used to determine the location of the jumpers.

STANDARD DEVICE NUMBER 150_8

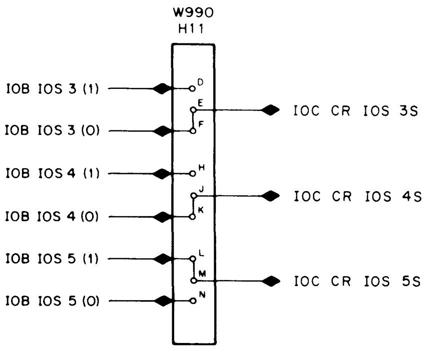
FIRST OCTAL DIGIT			SECOND OCTAL DIGIT			THIRD OCTAL DIGIT
BIT 3 0	BIT 4 0	BIT 5 1	BIT 6 1	BIT 7 0	BIT 8 1	BIT 9 0

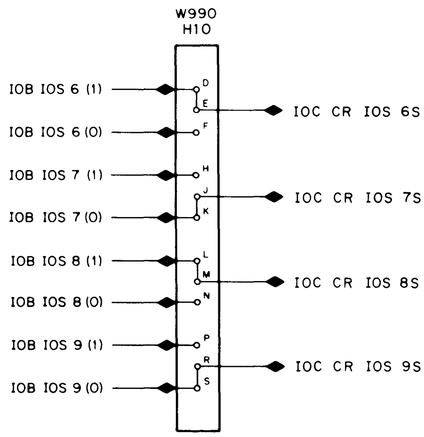
H11 JUMPERS

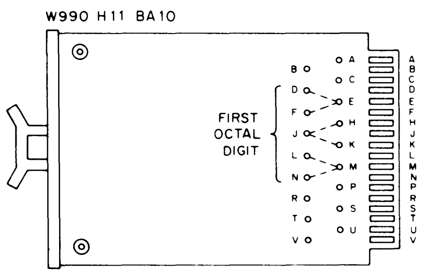
BIT 3 — E TO F
BIT 4 — J TO K
BIT 5 — M TO L

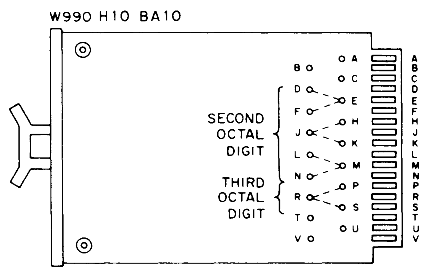
H10 JUMPERS

BIT 6 — E TO D
BIT 7 — J TO K
BIT 8 — M TO L
BIT 9 — R TO S









	BIT NO.	H11 JUMPERS FROM	H11 JUMPERS TO
FIRST OCTAL DIGIT	BIT 3=1	E	D
	BIT 3=0		F
	BIT 4=1	J	H
	BIT 4=0		K
	BIT 5=1	M	L
	BIT 5=0		N

	BIT NO.	H10 JUMPERS FROM	H10 JUMPERS TO
SECOND OCTAL DIGIT	BIT 6=1	E	D
	BIT 6=0		F
	BIT 7=1	J	H
	BIT 7=0		K
	BIT 8=1	M	L
	BIT 8=0		N
THIRD OCTAL DIGIT	BIT 9=1	R	P
	BIT 9=0		S

Figure 2-10 Card Reader Device Number Selection Cards

STANDARD DEVICE NUMBER 124_8

FIRST OCTAL DIGIT			SECOND OCTAL DIGIT			THIRD OCTAL DIGIT
BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	BIT 9
0	0	1	0	1	0	1

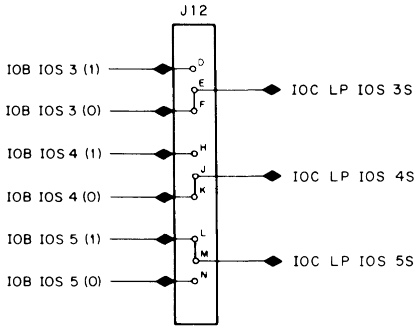
J12 JUMPERS

BIT 3 – E TO F
BIT 4 – J TO K
BIT 5 – M TO L

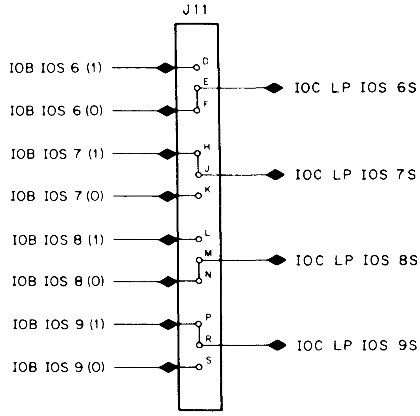
J11 JUMPERS

BIT 6 – E TO F
BIT 7 – J TO H
BIT 8 – M TO N
BIT 9 – R TO P

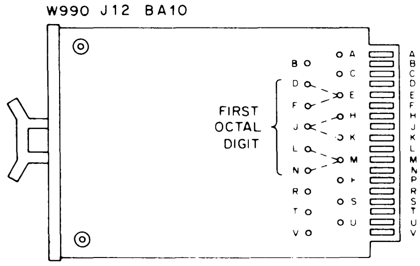
W990
J12



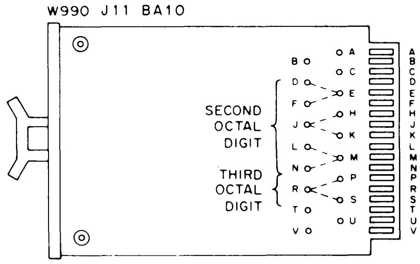
W990
J11



W990 J12 BA10



W990 J11 BA10



	BIT NO.	J12 JUMPERS FROM	J12 JUMPERS TO
FIRST OCTAL DIGIT	BIT 3=1	E	D
	BIT 3=0		F
	BIT 4=1	J	H
	BIT 4=0		K
	BIT 5=1	M	L
	BIT 5=0		N

	BIT NO.	J11 JUMPERS FROM	J11 JUMPERS TO
SECOND OCTAL DIGIT	BIT 6=1	E	D
	BIT 6=0		F
	BIT 7=1	J	H
	BIT 7=0		K
	BIT 8=1	M	L
	BIT 8=0		N
THIRD OCTAL DIGIT	BIT 9=1	R	P
	BIT 9=0		S

Figure 2-11 Line Printer Device Number Selection Cards

STANDARD DEVICE NUMBER 140_8

FIRST OCTAL DIGIT			SECOND OCTAL DIGIT			THIRD OCTAL DIGIT
BIT 3 0	BIT 4 0	BIT 5 1	BIT 6 1	BIT 7 0	BIT 8 0	BIT 9 0

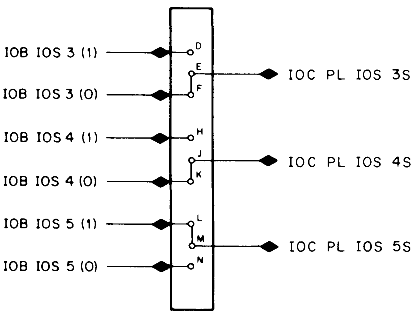
J9 JUMPERS

BIT 3 – E TO F
BIT 4 – J TO K
BIT 5 – M TO L

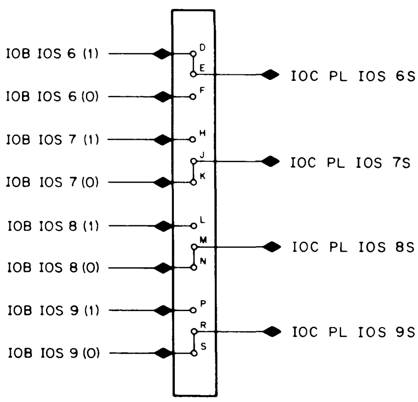
J8 JUMPERS

BIT 6 – E TO D
BIT 7 – J TO K
BIT 8 – M TO N
BIT 9 – R TO S

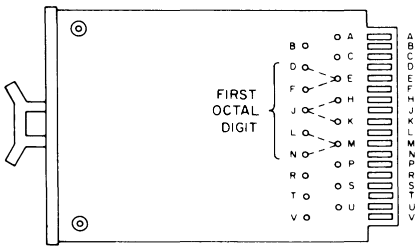
W990
J9



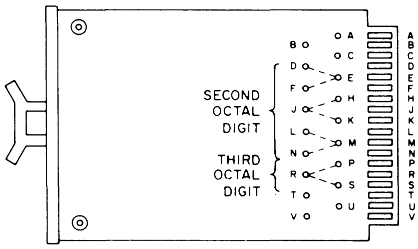
W990
J8



W990 J9 BA10



W990 J8 BA10



	BIT NO.	J9 JUMPERS FROM	J9 JUMPERS TO
FIRST OCTAL DIGIT	BIT 3=1	E	D
	BIT 3=0		F
	BIT 4=1	J	H
	BIT 4=0		K
	BIT 5=1	M	L
	BIT 5=0		N

	BIT NO.	J8 JUMPERS FROM	J8 JUMPERS TO
SECOND OCTAL DIGIT	BIT 6=1	E	D
	BIT 6=0		F
	BIT 7=1	J	H
	BIT 7=0		K
	BIT 8=1	M	L
	BIT 8=0		N
THIRD OCTAL DIGIT	BIT 9=1	R	P
	BIT 9=0		S

Figure 2-12 Plotter Device Number Selection Cards

2.7.2 BA10 I/O Bus Connections

The BA10, which contains the card reader, line printer and plotter control logic, is connected to the central processor via the I/O bus. In the PDP-10 system, the I/O bus cables are routed from the central processor and are looped through each of the options that operate from the I/O bus. These cables end in connector modules that plug into the logic racks. The margin cable and remote turn-on cable are also routed to the logic racks to complete the margin and remote turn-on circuits.

Since the floor plan for each PDP-10 system may vary, the routing of the I/O bus cables may also vary. Therefore, the I/O bus cables for each option may be custom manufactured to meet a specific system requirement. To determine I/O bus routing for the BA10, refer to the floor plan for the system. Guidelines for installation of the I/O bus cables are contained in the PDP-10 Installation Manual.

2.7.3 CR10 Device Cables

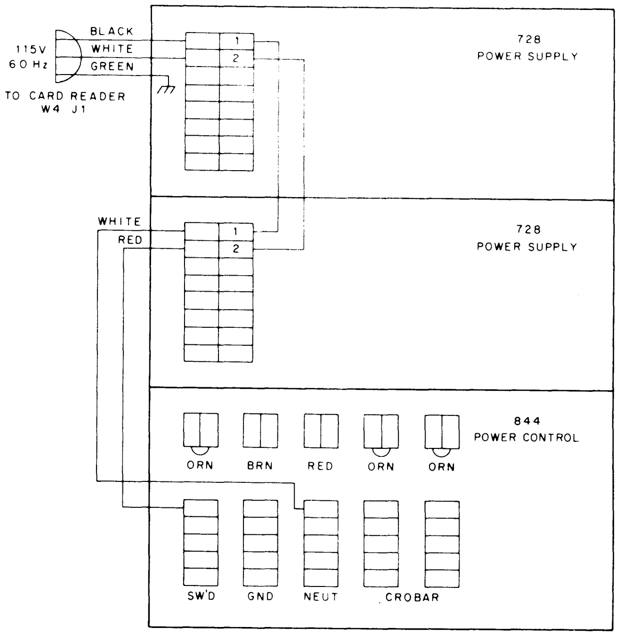
The card reader and the BA10 logic rack are connected together via the card reader device cables. In the card reader device cables, logic and control signals are routed over the device cable and power is routed over a power cable.

One end of the device cable has a 60-pin connector that mates with W2J1 of the card reader. From the 60-pin connector, there is a 36-pair cable terminated with two W852 connector modules joined by mechanical hardware. The connection is completed by screwing the connector assembly into card slots CD19 and CD20 of the BA10 logic. Refer to drawing D-CL-CR10-0-CRCL for pin connections, signal names and signal conditions.

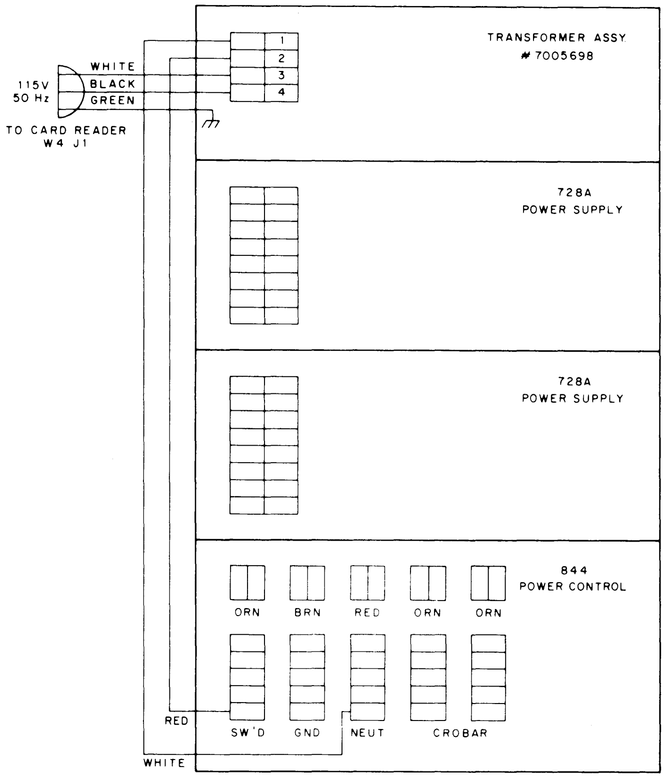
The power cable is connected between W4J1 of the card reader and the BA10. The card reader end of the power cable has a female twist-lock connector, and the BA10 end of the cable is connected to a terminal board inside the cabinet. See Figure 2-13 and drawing D-IC-BA10-0-AC for power wiring details.

2.7.4 LP10 Device Cables

The line printer connects to the control logic in the BA10 cabinet through a single interface cable. One end of the cable has a 50-pin connector that mates with a line printer socket. The other end connects to two double-height W851 connector modules that plug into card slots CD17 and CD18 of the BA10 logic racks. Refer to drawing D-CL-LP10-0-LPCL for pin connections, signal names, and signal types.



115V 60 Hz ac Wiring



230V 50Hz ac Wiring

Figure 2-13 Card Reader Power Wiring

2.7.5 XY10 Device Cables

The plotter and the BA10 logic rack are connected together via the device cable. All control signals for the plotter are sent over this cable. One end of the device cable has a Cannon Connector, Type SK-19-21C. The other end terminates in a DEC Type W028 Connector module which fits into the card slot at F32 on the BA10 or at J31 on the TD10.

In addition to carrying control signals, the cable also serves to complete the logic circuit ground and carry an optional PLCN POWER OFF signal.

The Type 884 Power Control in the BA10 is not used by the plotter. Primary power to the device is applied external to the BA10.

CHAPTER 3

CR10 THEORY OF OPERATION

This chapter contains a theoretical discussion of CR10 Card Reader operation. The discussion is arranged in this order: functional description of the card reader system using a simplified block diagram; identification and functional description of the card reader and I/O bus interface lines; operational description of the card reader control logic using block schematics. The theory of operation for the card reader is contained in the technical manual supplied with the Soroban Compact Card Reader, Model ERD and is not duplicated in this chapter.

3.1 BLOCK DIAGRAM ANALYSIS

The Type CR10 Card Reader provides the control logic and interface necessary to read data from standard 80-column punched cards and transfer the data into the PDP-10 central processor. A series of cycles are performed to complete these card reader operations. These cycles are controlled by a series of I/O instructions performed by the central processor under program control. Program interrupt requests are generated to indicate changes in status, and the status register is read to identify the changes. Refer to Figure 3-1 during the following functional description.

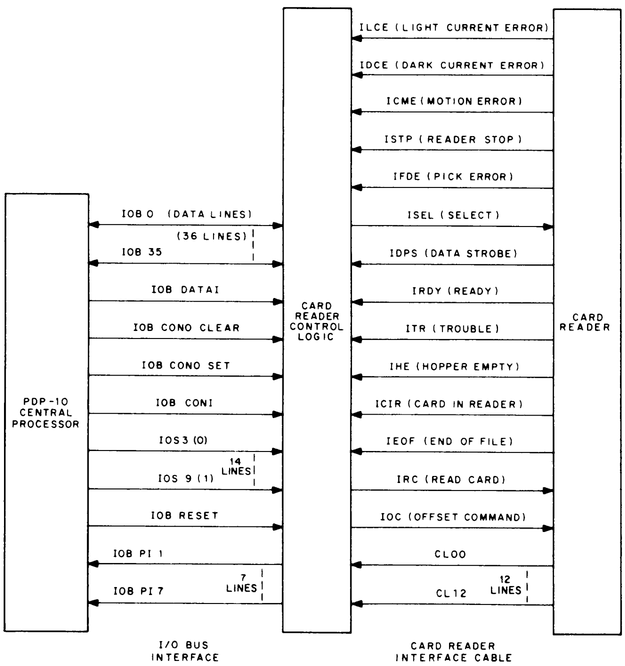


Figure 3-1 Simplified Block Diagram of the CR10 Card Reader

When a ready signal (IRDY signal is true) from the card reader is detected, the card reader control logic generates a program interrupt request that is routed to the central processor via the assigned PI line of the I/O bus. The central processor performs a CONI instruction to service the program interrupt and detects the ready-to read condition.

Next, the central processor performs a CONO instruction which causes the card reader control logic to generate the read command (IRC). The read command causes the card reader to pick a punched card from the card reader hopper and deliver the punched card, end first, to the first pair of synchronized pinch-roller metering capstans. After reaching the capstans, the punched card is transported toward the read station. Before the first card column reaches the read station, the card reader performs a light current and dark current test to insure normal read station operation.

The next cycle to be performed is the read data cycle. In the read data cycle, the data punched in the first card column is read photoelectrically, is placed on the data lines of the card reader interface cable, and is allowed to settle. Then, the data strobe (IDPS) signal is generated by the card reader and is sent to the card reader control logic. In the card reader control logic, the data strobe signal generates a load buffer signal that gates the data into a buffer register where it is temporarily stored. The load buffer signal also sets a data ready flip-flop causing a program interrupt request to be sent to the central processor over the assigned program interrupt line.

To service the program interrupt request, the central processor again performs a CONI instruction to transfer the contents of the status register into the central processor via the data lines of the I/O bus. Bit 32 of the status register indicates the presence of data in the card reader control logic buffer register.

With data present in the buffer register, the next cycle to be performed is the data transfer cycle. To complete the data transfer cycle, the central processor performs a DATAI instruction to fetch the data via the data lines of the I/O bus.

During these cycles, the card reader continues to move the punched card through the read stations. The central processor has approximately 350 μs to complete the transfer data cycle without missing the data. At the end of this time, the data in the next card column is placed on the data lines of the card reader interface cable and is strobed into the buffer register. The read data and data transfer cycles are performed as explained above to transfer the next column of data. This action is repeated until the 80 card columns have been read. Then, the punched card is transported out of the read station and into the card reader stacker.

Approximately 1.8 ms after the last card column has left the read station, the card-in-reader (ICIR) signal from the card reader goes false and performs the following functions: Clears the reading card flip-flop , and sets the end-of-card flip-flop causing a program interrupt request. The central processor performs a CONI instruction to service the program interrupt request and read the contents of the status register. The status information informs the central processor that the end of card has been reached. A CONO instruction is performed to clear the end-of-card flip-flop clearing the program interrupt request.

The central processor now performs a CONO instruction to set the read flip-flops conditioning the control logic for the next pick cycle. Approximately 8 ms after the punched card leaves the read station, the ready (IRDY) signal from the card reader goes true and generates a ready signal (assuming there is no trouble and that more cards are in the hopper). The ready signal enables a read card signal that is used to generate a read command (IRC). When the read command is sent to the card reader, the next card is picked from the card reader hopper.

The punch card is transported to the read station and the read data and data transfer cycles are repeated for each card column. This action is repeated until the card reader is turned off, until all cards in the hopper have been read, or until a fault is detected.

Additional status information may be generated in the card reader control logic and routed to the central processor during a CONI instruction to inform of a change in status. These status changes can indicate the following: missed data, indicates the transfer data cycle was not completed before the next card column was read; card reader trouble, indicates a hopper empty, stacker full, feed error, light/dark current error, card motion error, or card reader off-line; empty hopper, indicates an empty card reader hopper, or a full stacker; and end of file, indicates the operator has depressed the card reader EOF switch to signify that the last card of a file has been read. Refer to Section 3.1.1 for a complete discussion of the card reader cables.

3.1.1 CR10 Card Reader Cables

Refer to Figure 3-1 for the following descriptions of the CR10 Card Reader Interface lines. Tables 3-1 and 3-2 contain a brief functional description of the interface lines.

Table 3-1
I/O Bus Interface Cable
(Partial Listing)

Signal Line	Function
IOB0 through IOB35	Transfers data and status information into the central processor and control signal into the card reader control logic. In the CR10, only IOB18 through IOB35 are used.
IOB DATAI	Gates data into the central processor and clears the data ready flag.

Table 3-1
I/O Bus Interface Cable (Cont)
(Partial Listing)

Signal Line	Function
IOB CONO CLEAR	Clears the card reader control logic and sets read, trouble enable and/or ready enable flip-flops.
IOB CONO SET	Occurs 1 μs after IOB CONO CLEAR. Gates the assigned PI channel number into the PI register, to clear the card reader control logic, and/or to generate an offset command.
IOB CONI	Gates the card reader status into the central processor.
IOS3(0) through IOS9(1)	Identifies the device number to the card reader control logic.
IOB RESET	Clears the card reader control logic.
IOB PI1 through IOB PI7	Transfers the program interrupt signal to the central processor. Only one line is assigned to the card reader at one time.

Table 3-2
Card Reader Interface Cable

Signal Line	Function
IFDE	Indicates that the card reader failed to pick a card.
IDPS	Generates a load buffer pulse after the data has settled on the data lines. Causes a program interrupt.
ISEL	Selects the card reader (always true).
IRDY	Indicates when the card reader is ready to accept a read command. Can cause a program interrupt.
ITR	Indicates when a card reader trouble has been detected. Can cause a program interrupt.
IHE or IOSF	Indicates when the card reader hopper is empty or when the stacker is full.
ICIR	Indicates when a card is present in the read station.
IEOF	Represents pressing of the EOF switch.
IRC	Starts the pick cycle (read command).
IOC	Causes a card in the stacker to be offset for identification.
ILCE or IDCE	Indicates a light or dark current error.
ICME	Indicates that a card has jammed or slipped (card motion error).

Table 3-2
Card Reader Interface Cable (Cont)

Signal Line	Function
ISTP	Indicates the card reader power is on but that the card reader is off-line (stop).
CL00 through CL12	Transfers the 12 bits of data from the card reader to the buffer register in the card reader control logic. Signals remain until the next column reaches the read station (approximately 350 μs). The order of bits from MSD to LSD are as follows: CL12, CL11, CL00 through CL09.

3.2 CARD READER CONTROL LOGIC OPERATION

In the following discussions, the operation of the card reader logic has been divided into a series of cycles. Even though the actual operating sequence is a function of the program, these cycles have been selected to describe circuit operation during a normal operating sequence. In block schematic references in the following discussions, the location of the circuits under discussion are noted by a zone number and the drawing title abbreviation portion of the block schematic number (i.e., C5-CRST indicates the circuit under discussion is located in zone C5 of block schematic D-BS-CR10-CRST).

3.2.1 Power Turn-on and Initialization Cycle

When input power is applied to the Type 844 Power Control in the BA10 logic cabinet, power is applied to the card reader control logic and card reader. Within the power control, the opening of a normally closed (NC) contact is delayed for 4s. The output line from the NC contact is connected to a clamped load (A5-IOCB) and the IOC POWER UP signal remains in the true condition during the 4s delay. With the IOC POWER UP signal in the true condition, the IOC POWER UP one-shot (A4-IOCA) remains in the 1 state during the 4s forcing the PI register (C3, C4-CRST) to the 0 state. The output signal from the one-shot is ORed and inverted to generate the IOC CLEAR signal. With the IOC CLEAR signal in the true condition, the IOC CR CLEAR signal is generated by the level amplifier feature of an R613 Pulse Amplifier (C6-IOCB). The IOC CR CLEAR signal clears the card reader buffer register (CRBR) and the following flip-flops; CRST READING CARD, CRST DATA MISSED, CRST END OF FILE, CRST END OF CARD, CRST DATA READY, CRCN READ, CRCN READER TRBL ENAB, CRCN READY ENAB. At the same time, the IOC CR CLEAR signal is routed to a pulse amplifier (B6-IOCB) to generate the IOC CR CONO CLEAR signal that clears the PI register (C3,C4-CRST).

The card reader control logic is now clear and ready to be conditioned by the program. The central processor performs a CONO instruction addressing the card reader control. To complete a CONO instruction, the central processor sends the CONO CLEAR pulse first and then sends the CONO SET pulse 1 μs later.

When the card reader control logic is addressed, the card reader device number is routed over the IOS3(0) through IOS9(1) lines (C6-IOCA) of the I/O bus and is applied to the card reader selection cards (D3-IOCA). The card reader selection cards are jumpered to select a device number (150_8) as shown on drawing IOCA. From the selection cards, the output lines are ANDed (D1-IOCA) and the resultant signal, IOC CR SELECT, is used to enable the CR CONO CLEAR gate (B5-IOCB), the CR CONO CLEAR A gate (B3-IOCB) and other gates not discussed at this time.

During the CONO CLEAR portion of the CONO instruction, the central processor can condition the card reader control logic to perform one or more of the following functions by placing the required information on I/O bus lines IOB26 through IOB33 (drawing IOB). IOB26 = 1 causes picking of a card from the card reader hopper; IOB27 = 1 enables the READER TROUBLE PI signal (C2-CRCN) or IOB27 = 0 disables the signal; IOB28 = 1 clears the DATA MISSED flip-flop (C7-CRST); IOB29 = 1 enables the RDY TO READ PI signal (C1-CRCN) or IOB29 = 0 disables the signal; IOB30 = 1 clears the END OF FILE flip-flop (C6-CRST); IOB31 = 1 clears the END OF CARD flip-flop (C6-CRST); IOB32 = 1 clears the DATA READY flip-flop (C5-CRST).

The central processor sends the IOB CONO CLEAR pulse (C8-IOCA) to the card reader control logic. The IOB CONO CLEAR pulse is inverted and the resultant signal, IOC CONO CLEAR, is sent to the enabled CONO clear gates to generate the IOC CR CONO CLEAR signal (C5-IOCB) and the IOC CR CONO CLEAR A signal (C2-IOCB). The IOC CR CONO CLEAR signal is used to clear the PI register. (This function is not required the first time because the PI register was cleared during power turn-on, but is used to change the card reader PI channel assignment during normal operation.) At this time, the IOC CR CONO CLEAR A signal is used to perform one or both of the following functions: the CRCN READER TRBL ENAB flip-flop (C3-CRCN) is set if the IOB27 signal is a 1; and/or the CRCN READY ENAB flip-flop (C2-CRCN) is set if the IOB29 signal is a 1. Other functions that can be performed during the CONO CLEAR portion of the CONO instruction are not discussed at this time because the card reader is being conditioned for normal operation under program control. These additional functions will be discussed as they are encountered.

The next operation to be performed is the CONO SET portion of the CONO instruction. The central processor sends the IOB CONO SET pulse (C8-IOCA) to the card reader control logic. After inversion, the resultant signal, IOC CONO SET, is sent to the CONO SET gate (B6-IOCB). Since the IOC CR SELECT signal is still true, the CONO SET gate is enabled and the IOC CR CONO SET signal is generated. The IOC CR CONO SET signal gates the PI channel assignment number into the PI register (C3, C4-CRST). When the CONO SET pulse occurs, the following functions may be performed. The card reader control logic is cleared if IOB23 = 1; a card offset command is generated if IOB24 = 1; the PI register is set to the PI channel assignment number contained in IOB33 through IOB35. The offset or reset functions would not be utilized at the first CONO, but the IOC CR CONO SET pulse is used to perform these functions. At this time, the card reader control logic is conditioned to receive a ready signal from the card reader.

3.2.2 Program Interrupt Cycle

After the card reader control logic has been conditioned for normal operation, conditions remain the same until a ready signal is received from the card reader. To generate the ready signal, the card reader must be in the ready condition (power on, stop flip-flop cleared, card not presently in the reader, no reader troubles, etc.), the card reader START switch must have been depressed, and TEST/NORMAL switch must be in the NORMAL position. Under these conditions, the IRDY signal (C8-CRCN) from the card reader is true and is applied to a positive level converter and the resultant signal is inverted to generate the CRCN READY signal. The CRCN READY signal is ANDed (B3-CRCN) with the CRCN READ CARD signal generating the CRCN READY TO READ signal. The CRCN READY TO READ signal is ANDed (C2-CRCN) with the 1 side of the CRCN READY ENAB flip-flop that was set during the CONO instruction. The CRCN RDY TO READ PI signal, resulting from the ANDing, is sent to the PI OR gate (B8-CRST) and is used to generate the CRST PI REQUEST signal. From the output of the PI OR gate, the CRST PI REQUEST signal enables the PI decoder (B7-CRST) and the PI channel assignment number is decoded. The assigned PI line is grounded sending a program interrupt request to the central processor.

At the same time, the CRCN READY TO READ signal conditions its associated status gate (D5-CRST). The PI channel assignment number is also routed to its associated status gates (D1, D2-CRST).

The central processor performs a CONI instruction to service the program interrupt request. The card reader device number contained in the CONI instruction is decoded to generate the IOC CR SELECT signal (D1-IOCA). The IOB CONI signal (C8-IOCA) is routed from the central processor and is inverted to generate the IOC CONI signal. The IOC CR SELECT, the IOC POWER UP and the IOC CONI signals are ANDed (C4-IOCB) to generate the IOC CR CONI signal.

With IOC CR CONI signal (D8-CRST) true, the information in the status register is gated into the I/O bus and into the central processor. During this transfer, the following status information is received by the central processor: IOB29 = 1 to indicate a ready signal has been received from the card reader, IOB33 through IOB35 are used to indicate the assigned PI channel number.

All program interrupt cycles are performed in a similar fashion. In the following discussions, the program interrupt cycle will not be discussed in detail, but as different status bits are used they will be explained. For a discussion of all status bits, refer to the Programming Notes contained in Section 2.6.1.

3.2.3 Pick Cycle

During the pick cycle, a punched card is picked from the card reader hopper and transported to the read station. When the status information indicates to the central processor that a ready signal has been received, the central processor performs a CONO instruction. During the CONO instruction, a 1 is transferred via IOB26 and the set gate of the CRCN READ flip-flop (C4-CRCN) is conditioned by IOB26B. The central processor routes the IOB CONO CLEAR pulse and the card reader device number to the card reader control logic which then generates the IOC CR CONO CLEAR A signal which functions as explained in the POWER turn-on discussion.

With the set gate of the CRCN READ flip-flop enabled, the IOC CR CONO CLEAR A signal sets the CRCN READ flip-flop. The 1 side of the CRCN READ flip-flop is ANDed (C4-CRCN) with the CRCN READY signal and the resultant signal starts a 25-μs pulse one-shot (D3-CRCN). From the one-shot, the output signal is inverted to generate the CRCN READ CARD signal. The CRCN READ CARD signal is routed to a positive output converter (C5-CRCN) and the IRC (read command) signal is generated and routed to the card reader. In the card reader, the IRC signal causes a card to be picked from the hopper and transported to the read station. When the CRCN READ CARD signal goes true, the CRCN RDY TO READ signal goes false and the program interrupt request is removed.

The CRCN READ CARD signal also sets the CRST READING CARD flip-flop (C8-CRST); the 1 side of this flip-flop conditions the reading card status gate (D6-CRST). Although this information is not transferred to the central processor until the next CONI instruction, the CRST READING CARD flip-flop remains in the set condition as long as the punched card remains in the read station. After the 25 μs delay, the delay one-shot (D4-CRCN) returns to the normal condition. At this time, the CRCN READ CARD signal goes false and remains in the false condition until the next pick cycle. When the CRCN READ CARD signal goes false, the CRCN READ flip-flop is cleared. The CRCN READ flip-flop remains clear until the central processor performs a CONO instruction with a 1 in IOB26. This is usually performed after the end of card cycle.

3.2.4 Read Data Cycle

During this cycle, the following functions are repeated for each column: the data contained on the punched card is read photoelectrically; the data is stored temporarily in the card reader control logic buffer register; a program interrupt request is generated and sent to the central processor; and the central processor performs a CONI instruction to transfer the status information.

Once the punched card has been picked, the first pair of synchronized metering capstans grip the card and drive it through the read station. A toothed timing gear is driven in synchronism with the metering capstans and, as the gear teeth rotate past a reluctance pickup, a series of timing pulses is generated for each card column. The metering capstans continue to move the card through the read station even if a trouble is located and deposit the card in the card reader stacker. During the reading, the 80 card columns are read and a read data cycle and data transfer cycle is performed for each card column before the next card column is read.

The card reader read station, located between the two pairs of metering capstans, consists of a beginning-of-card phototransistor and light source, 12 data phototransistors and 12 light sources spaced to match the locations of the 12 card data rows, and an end-of-card phototransistor and light source. The signals from the phototransistors, when referenced to the timing signals from the reluctance timing pickup, enable the card reader logic circuits to form a series of signals corresponding to the image of the holes punched in the card.

The card reader performs a light-current error check before the card reaches the beginning-of-card phototransistor and a dark-current error check after the card reaches the beginning-of-card phototransistor but before the first card column reaches the 12 data phototransistors. In this way, the normal functioning of the 12 data phototransistors in the light and dark current conditions is insured before data sensing begins.

The card reader generates the card-in-reader (ICIR) signal approximately 1.8 ms before the first column reaches the read station and the signal is true until approximately 1.8 ms after the last column.

The ICIR signal is applied to a positive level converter (B2-CRCN) and the resulting signal is inverted to generate the CRCN CARD IN READER signal. The CRCN CARD IN READER signal conditions the card-in-reader status gate (D8-CRST) as long as the signal remains in the true condition. A typical interface line circuit used in the transfer of signals from the card reader to the control logic is shown in Figure 3-2.

When the first card column passes between the phototransistors and their respective light sources, any hole punched in the card admits light and activates the associated phototransistor. The resultant signals from the phototransistors are gated onto the card reader interface cable data lines by a series of control signals generated in the card reader. Each data line is connected to an associated positive level converter (CRBF) in the card reader control logic. The output signal from each positive level converter is connected to an inverter and, from the inverters the resultant signals are routed to their associated card reader buffer register input gate (CRBF).

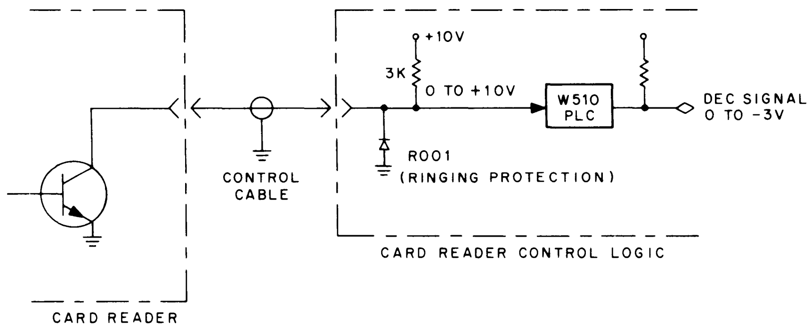


Figure 3-2 Card Reader Interface Line Circuit

Approximately 28 μs after the data has been placed on the card reader interface data lines, the card reader generates the data strobe (IDPS) signal. The IDPS signal is applied to a positive level converter (D7-CRCN) and the resultant signal is used to generate the CRCN LOAD BUFFER pulse. When the CRCN LOAD BUFFER pulse is generated, the card reader buffer input gates are strobed and the data is jammed into the buffer register. At the same time, the CRCN LOAD BUFFER pulse sets the CRST DATA READY flip-flop (C5-CRST).

The data output gates connected to the buffer register are conditioned according to the stored data. The 1 side of the CRST DATA READY flip-flop is used to condition the data ready status gate (D3-CRST) and enable the PI OR gate (B8-CRST). The PI decoder is enabled by the output signal from the PI OR gate and the program interrupt request is sent to the central processor via the I/O bus.

After the program interrupt request has been sent to the central processor, the central processor has approximately 350 μs to perform a CONI instruction to discover that the data is ready, and a DATAI instruction to fetch the data stored in the buffer register. Though the performance of these instructions requires only a few microseconds, there exists a possibility that the central processor could be engaged in higher priority transfers and that the next column of data might be jammed into the buffer register before the central processor had fetched the previous data. Since loss of data is possible but not part of the normal operation, normal operation will be discussed now and the loss of data possibility will be discussed at the end of this section.

The central processor services the program interrupt caused by the CRST DATA READY flip-flop by performing a CONI instruction, as explained in the discussion of the program interrupt cycle. During the CONI instruction, the IOC CR CONI signal (D8-CRST) is used to enable the status gates (CRST) and the following information is transferred to the central processor via the I/O bus: IOB24 = 1 to indicate that a card is in the reader; IOB26 = 1 to indicate that a card is being read; IOB32 = 1 to indicate that the presence of data in the buffer (this is the significant bit of information); and the PI channel assignment number is contained in IOB33 through IOB35.

The read data cycle is now completed and the card reader control logic is conditioned for the data transfer cycle. After the data transfer cycle is performed, the read data cycle is repeated for the next column of data. Each read data cycle is performed in an identical fashion until the end of the card is reached, a card reader trouble is located, the end of a file is reached, or a column of data is missed. The first three of these conditions are discussed under separate section headings, but the fourth condition is explained in this section.

When the central processor fails to fetch a column of data before the next column of data is jammed into the buffer register, the data missed status gate is conditioned and a program interrupt request is sent to the central processor via the I/O bus. To perform these functions, the CRST DATA READY(1) signal is used to condition the set gate of the CRST DATA MISSED flip-flop (C7-CRST) and the CRST DATA READY(1) signal remains true until the data in the buffer register is transferred into the central processor. If the CRCN LOAD BUFFER pulse for the next read data cycle occurs before data transfer cycle is completed, the CRCN LOAD BUFFER pulse strobes the set gate of the CRST DATA MISSED flip-flop. Since the CRST DATA READY(1) signal is still true, this sets the flip-flop. The 1 side of the CRST DATA MISSED flip-flop conditions the data missed status gate (D5-CRST) and enables the PI OR gate. After inversion, the resultant signal from the PI OR gate enables the PI decoder. The program interrupt request from the PI decoder is sent to the central processor via the I/O bus. To service the data missed program interrupt, the central processor performs a CONI instruction to fetch the status information. When a data missed program interrupt has occurred, the status information contains a 1 in IOB28 to indicate the loss of data. Under these circumstances, the central processor must perform a CONO instruction with a 1 in IOB28 to clear the CRST DATA MISSED flip-flop and remove the program interrupt. It also takes appropriate action to indicate that erroneous data has been read.

3.2.5 Data Transfer Cycle

In this section, the circuit operation of the card reader control logic during a data transfer is discussed. To review conditions up to this point, one column of data has been read from a punched card and temporarily stored in a buffer register. A program interrupt request has been routed to the central processor and the central processor has performed a CONI instruction to fetch the status information which indicates the presence of data in the buffer to the central processor. Now, the central processor performs a DATAI instruction to fetch the data stored in the buffer register.

The central processor sends the IOB DATAI signal (C8-IOCA) and the card reader device number (C6-IOCA) to the card reader control logic. The device number is decoded (D1-IOCA) and the resultant signal, IOC CR SELECT, is used along with the IOC POWER UP signal to condition the DATAI AND gate (D4-IOCB). After the IOB DATAI signal is inverted, IOC DATAI, the resultant signal, is routed to the enabled DATAI AND gate to generate the IOC CR DATAI signal. The

IOC CR DATAI signal is routed to the data output gates of the buffer register (CRBR) and is used to gate the data onto I/O bus lines IOB24 through IOB35 and into the central processor. The trailing edge of the IOC CR DATAI signal is used to clear the CRST DATA READY flip-flops (C5-CRST). When the CRST DATA READY(1) signal goes false, the program interrupt is cleared and the card reader control logic is ready for the next read data cycle.

The data transfer cycle is performed in an identical fashion for each card column until the 80 columns have been read. When the end of a card is reached, the end-of-card cycle begins.

3.2.6 End-of-Card Cycle

When the end of a card is reached, the ICIR signal from the card reader goes to the false condition. This happens approximately 1.8 ms after the last card column of data is read. When the ICIR signal goes false, the CRCN CARD IN READER signal (B5-CRCN) goes false and disables the card-in-reader status gate. When the CRCN CARD IN READER signal goes true, the CRST END OF CARD flip-flop (C6-CRST) is set and the CRST READING CARD flip-flop (C8-CRST) is cleared.

When the 1 side of the END OF CARD flip-flop enables the PI OR gate (B8-CRST), the CRST PI REQUEST signal is true and the PI decoder is enabled. With the PI decoder enabled, the PI channel assignment number stored in the PI register is decoded and a program interrupt request is sent to the central processor via the assigned PI line.

The central processor services the program interrupt request by performing a CONI instruction as explained in the priority interrupt cycle. When the IOC CR CONI signal is generated, the following status information is routed to the central processor: IOB24 = 0 to indicate a card is not present in the reader; IOB26 = 0 to indicate a card is not being read; IOB31 = 1 to indicate the end of a card has been reached. The central processor performs a CONO instruction with a 1 in IOB31 to clear the END OF CARD flip-flop. When the END OF CARD flip-flop is cleared, the program interrupt request is removed.

If there are additional cards to be read and no trouble is indicated, the central processor may perform a CONO instruction with a 1 in IOB26 to set the CRCN READ flip-flop. Approximately 8 ms after the last card column, the IRDY signal from the card reader goes to the true condition (assuming the presence of cards and no trouble) and causes the CRCN READY signal (C7-CRCN) to be generated. The CRCN READY signal is ANDed with the 1 side of the CRCN READ flip-flop to enable the CRCN READ CARD signal. The CRCN READ CARD signal, a 25 μs signal, is used to generate the IRC signal that initiates the next pick cycle.

If the CRCN READ flip-flop has not been set before the CRCN READY signal is generated, the CRCN READ CARD signal is not enabled by the CRCN READY signal. To indicate the presence of the ready (IRDY) signal under these conditions, the CRCN READY signal is ANDed with the CRCN READ CARD signal, which is false at this time. The CRCN READY TO READ signal is generated and

ANDed (C3-CRCN) with the 1 side of the CRCN READY ENAB flip-flop. With the ready enable flip-flop set, the CRCN RDY TO READ PI signal is generated. The PI decoder is enabled and a program interrupt request is sent to the central processor. The central processor services the program interrupt request by performing a CONI instruction to fetch the status information. During the transfer, IOB29 = 1 to indicate the card reader is in the ready condition.

To start the next pick cycle under these conditions, the central processor must perform a CONO instruction with IOB26 = 1 to set the CRCN READ flip-flop. The 1 side of the CRCN READ flip-flop is ANDed with the CRCN READY signal enabling the CRCN READ CARD signal. When the CRCN READ CARD signal goes true, the read command (IRC) is generated and sent to the card reader to start the next pick cycle. At the same time, the CRCN RDY TO READ PI signal goes false removing the ready-to-read program interrupt request.

3.2.7 Fault Location Cycle

The card reader contains logic circuits that constantly monitor the card reader for malfunctions during normal read operations. If a malfunction is detected, a trouble signal is routed to the card reader control logic, a card reader indicator that identifies the malfunction is illuminated, and the card reader drive motor is stopped after the read station is cleared.

When a trouble is detected, the ITR signal is routed to a positive level converter (B6-CRCN) and the resultant signal is inverted to generate the CRCN READER TROUBLE signal. The CRCN READER TROUBLE signal is used to condition the reader trouble status gate (D6-CRST) and is ANDed (C5-CRCN) with the 1 side of CRCN TRBL ENAB flip-flop to generate the CRCN READER TROUBLE PI signal. The CRCN READER TROUBLE PI signal conditions the PI OR gate and the resultant signal after inversion enables the PI decoder. When the PI decoder is enabled, the PI channel assignment number is decoded and a program interrupt request is routed to the central processor via the assigned PI line.

The central processor services the program interrupt request by performing a CONI instruction as explained in the program interrupt cycle. When the IOC CR CONI signal is generated during the CONI instruction, the status gates, IOB18 through IOB35, are enabled and the status information is sent to the central processor. Refer to Section 2.6.1 Programming Notes, for a discussion of these status bits. Under these conditions, the important status gate is the reader trouble status gate (IOB27) that is a 1 to indicate the presence of a card reader trouble. The ITR signal remains in the true condition and the program interrupt remains on the I/O bus until the trouble is corrected, the card reader CLEAR switch is depressed, and the card reader START switch is depressed.

3.2.8 End-of-File Cycle

The card reader control logic provides the program with an end-of-file indication. The end-of-file circuit remains disabled until the last card of a file has been picked and has generated the trouble (ITR) signal and the operator has depressed the card reader EOF switch generating the end-of-file (IEOF) signal. The ITR signal is used to generate the CRCN READER TROUBLE signal. Then, the CRCN READER TROUBLE and IEOF signals are inverted and ANDed (C5-CRCN) to generate the CRCN EOF signal.

The CRCN EOF signal sets the CRST END OF FILE flip-flop (C6-CRST) and the 1 side of the flip-flop enables the PI OR gate. With the PI OR gate enabled, a program interrupt request is generated and sent to the central processor. The central processor performs a CONI instruction to service the program interrupt request and fetch the status information. At this time, IOB24 = 0 indicating a card is not present in the read station, IOB25 = 1 indicating the hopper is empty, IOB26 = 0 indicating a card is not being read, IOB27 = 1 indicating a reader trouble has been detected, IOB30 = 1 indicating the end of a file has been reached (the significant bit of information), and IOB31 = 1 indicating the end of a card has been reached. To remove the EOF program interrupt request, the central processor performs a CONO instruction with a 1 in IOB30 clearing the CRST END OF FILE flip-flop.

3.2.9 Hopper Empty/Stacker Full Cycle

During normal operation, the operator may allow the hopper to become empty or the stacker full. When this occurs, the ITR signal and IHE or IOSF signals are generated by the card reader and are routed to the card reader control logic. The ITR signal causes the CRCN READER TROUBLE signal (C7-CRCN) to be generated and the IHE or IOSF signal causes the CRCN HOPPER EMPTY signal (B7-CRCN) to be generated. The CRCN HOPPER EMPTY signal conditions the hopper empty status gate (D7-CRST) and the CRCN READER TROUBLE signal conditions the reader trouble status gate (D6-CRST). At the same time, the CRCN READER TROUBLE signal is ANDed (C3-CRCN) with the 1 side of the CRCN READER TRBL ENAB flip-flop. The resultant signal, CRCN READER TROUBLE PI, enables the PI OR gate and causes a program interrupt request to be sent to the central processor.

The central processor services the program interrupt request as explained in the program interrupt cycle. During the CONI instruction, the following status information is routed to the central processor: IOB25 = 1 to indicate the hopper is empty; IOB27 = 1 to indicate the presence of a card reader trouble; and the PI channel assignment number is contained in IOB33 through IOB35.

At this time, the card reader drive motor is stopped and the card reader HOPPER EMPTY indicator or the STACKER FULL indicator is illuminated. To restart the card reader, the operator loads the hopper or clears the stacker and depresses the card reader CLEAR switch and the START switch.

3.2.10 Card Offset Cycle

The card offset cycle provides the operator with a visual indication of a program selected card by offsetting the card in the card reader stacker under program control. To perform this function, the central processor performs a CONO instruction with a 1 in IOB24 while the CRCN CARD IN READER signal is true. IOB24B is used to condition an input gate to a 25 μs one-shot (B3-CRCN). When the IOC CR CONO SET pulse occurs the one-shot is triggered. The output signal from the one-shot is inverted to generate the CRCN OFF SET CARD signal. Then, the CRCN OFF SET CARD signal is applied to a positive level converter (B3-CRCN) to generate the card offset (IOC) signal that is sent to the card reader via the card reader interface cable.

In the card reader, the IOC signal is used to generate two control signals that energize the offset solenoid located at the stacker capstan. When the solenoid is energized, the card in the capstan is offset and deposited on the deck in the stacker with a long edge protruding about 1/4 inch.

After approximately 28 ms, both of the offset control signals have returned to the false condition and the offset solenoid is de-energized. The next card may be picked and the read data and data transfer cycles may be started before the offset cycle is completed.

3.2.11 Clear Cycle

The card reader control logic circuits can be cleared in two different ways by the signals from the central processor. The first method involves the central processor placing a 1 on IOB23 while a CONO instruction is being performed. After input buffering, the resultant signal, IOB23B, is applied to the input gate of a 1 μs one-shot (B5-IOCB). When the IOC CR CONO SET pulse occurs, the one-shot is triggered. The trailing edge of the output signal from the one-shot, IOC CR CONO RESET DLY, occurs 1 μs after the CONO SET pulse and generates the IOC CR CLEAR signal (D6-IOCB). The IOC CR CLEAR signal generates the IOC CR CONO CLEAR signal (C6-IOCB). With the IOC CR CLEAR and IOC CR CONO CLEAR signals true, all the card reader control logic flip-flops, buffer and PI register are cleared.

Using the second method, the central processor generates the IOB RESET signal in one of several ways and routes the IOB RESET signal to the card reader control logic. This method occurs at power-on and power-off times. After inversion, the resultant signal, IOC RESET, enables an OR gate (A4-IOCA) to generate the IOC CLEAR signal. The IOC CLEAR signal conditions the reset circuits in the same fashion as explained in the power turn-on cycle.

CHAPTER 4
LP10 THEORY OF OPERATION

This chapter contains the theory of operation for the LP10 Line Printer Control. The general functional description is followed by an analysis of specific operations discussed at the logic diagram level. Theory of operation for the printer itself is contained in the appropriate Anelex Corporation manual.

4.1 BLOCK DIAGRAM ANALYSIS

The precise manner in which the processor controls a line printer system is a function of the program in use. A description of a typical system in operation follows (see Figure 4-1).

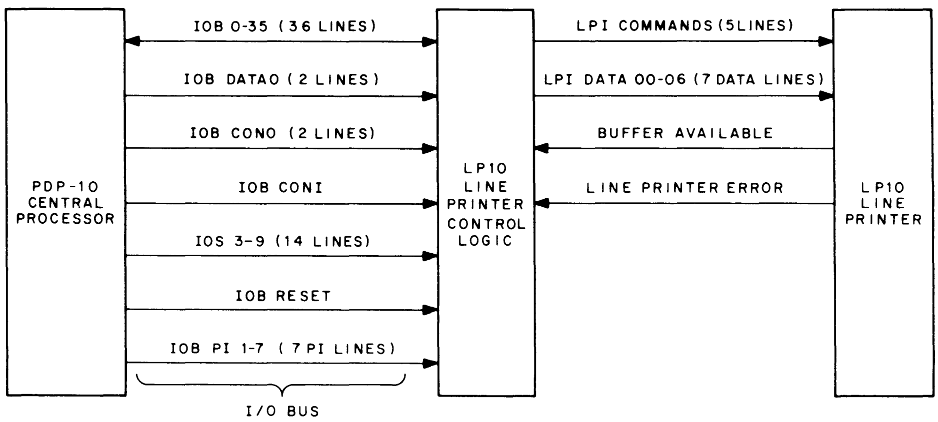


Figure 4-1 LP10 Line Printer System

A CONO instruction addressing the line printer loads "conditions out" data into the control logic status register. In response to the CONO, the control logic conditions the line printer system to receive data words from the processor. When these conditions have been established, the control logic sends the processor a done interrupt.

In response to the interrupt, the processor interrogates line printer status with a CONI instruction. If the processor determines that the system is ready, a DATAO instruction loads five 7-bit characters into the control logic buffer register. The control logic then examines the characters, one at a time, and processes each one according to its code.

If a character decodes as a printable character, the control logic transfers it to the line printer memory for storage. If a character decodes a control character, the control logic generates a control pulse that forces the appropriate response from the printer. Except for the horizontal tab character, all control characters cause the printer to print out the contents of its memory and then space the paper vertically according to the specific character code. Like a printable character, the horizontal tab character causes data to be stored in the line printer memory. In this case, the data comprises a series of space characters, each of which causes the printer to skip one horizontal space when encountered during a memory printout.

As each character is processed, it is shifted out of the buffer register and the next character is readied for processing. A character cannot be processed until the line printer has completed its response to the preceding character and enables the BUFFER AVAILABLE signal. When all five characters have been processed, the control logic raises the done flag, and the processor initiates the transfer of five more 7-bit characters.

4.2 LINE PRINTER CONTROL LOGIC OPERATION

The following analysis is written with reference to the DEC prints contained in Volume IV, PDP-10 Peripheral Device Engineering Drawing Set, DEC-10-I6DA. Reference to these prints in text is made by using the drawing title abbreviations of the DEC print number. For example LPCN identifies line printer control print D-BS-LP10-0-LPCN.

4.2.1 CONO/CONI Operations

To perform a CONO, the central processor places conditions and line printer device code on the I/O bus, and sends the IOB CONO CLEAR and IOB CONO SET pulses. The CONO pulses, in conjunction with the device number, are converted to IOC LP CONO CLEAR and IOC LP CONO SET, respectively, by the R613 Pulse Amplifiers shown on DEC print IOCC. IOC LP CONO CLEAR clears the status register comprising the LPST ERROR ENAB, BUSY, DONE, PIB30-32, and PIA33-35 flip-flops (LPST); IOC LP CONO SET loads the conditions into the status register. The contents of the register's PIA and PIB flip-flops define the channels over which interrupts are sent to the processor at the completion of certain data transfers and as an indication of line printer errors.

With a 1 on I/O bus line IOB25, IOC LP CONO SET also forces B165 inverter HJ at D04 (LPCN) to generate the LPCN SHT CNT INITIALIZE pulse. This pulse jams the shift counter (flip-flop LPBF SHT CNT0-2, LPBF) to four. At the same time, LPCN SHT CNT INITIALIZE clears the control register (LPCN) comprising flip-flops LPCN ALT, CLR SYNC, SHIFT SYNC A, SHIFT SYNC B, DATAO SYNC, and CONO PRINT. One microsecond after LPCN SHT CNT INITIALIZE, R613 Pulse

Amplifier MN at D11 generates the LPCN CLEAR pulse. LPCN CLEAR sets the LPST BUSY flip-flop and clears the LPST DONE flip-flop in the status register. In addition, it sets the control register LPCN CLR SYNC flip-flop and clears the column counter comprising flip-flops LPCC0-6 (LPCC).

In approximate coincidence with LPCN CLEAR, R613 Pulse Amplifier FH at D11 (LPCN) generates the LPCN CLR PRINTER BUF pulse. This pulse is delayed and is sent to the line printer as the LPI CLEAR BUFFER PLS signal (LPI) that clears the line printer memory.

When the line printer has cleared its memory, it sends the BUFFER AVAILABLE level that is converted to LPI BUFFER AVAILABLE by S107 gate SR at B09. The combination of LPI BUFFER AVAILABLE and LPCN CLR SYNC (1) causes R602 Pulse Amplifier PRUV at B06 (LPCN) to generate LPCN DONE, clearing the control register LPCN CLR SYNC flip-flop. LPCN DONE also clears the status register LPST BUSY flip-flop (LPST) and sets the LPST DONE flip-flop. If an interrupt channel was assigned, setting the DONE flip-flops sends an interrupt to the processor (decoder B152 at H25), signaling the completion of the CONO operation. If not, the processor samples the status of the done flag by performing a CONI instruction addressing the line printer. This brings up an IOC LP CONI level (B134 gate DEFH at H02, IOCC). IOC LP CONI gates the contents of the line printer status register (LPST) onto the I/O bus via the B163 gates at F18 and F19. With these conditions established, the control logic waits for further input from the processor.

4.2.2 Character Handling

Following the initializing operation, a DATAO instruction places five 7-bit characters on the I/O bus and sends the IOB DATAO CLEAR and IOB DATAO SET pulses. The logic shown on print IOCC converts the device code and DATAO pulses to the IOC LP DATAO CLEAR and SET pulses. IOC LP DATAO CLEAR clears the control register LPCN DATAO SYNC flip-flops, sets the status register LPST BUSY flip-flop, and clears the status register LPST DONE flip-flop. In addition, IOC LP DATAO CLEAR is converted to the LPBF DATAO CLR A and B pulses that clear the shift counter and buffer register.

IOC LP DATAO SET is converted to the LPBF DATAO A and B pulses. These pulses load the 7-bit characters on the I/O bus into the buffer register and set the control register LPCN SHIFT SYNC A and B flip-flops (LPCN). Also, the IOC LP DATAO SET pulse is delayed 2.2 μs and converted to the IOC LP DATAO SET DELAY signal (IOCC) that sets the LPCN DATAO SYNC flip-flop (LPCN). With the LPCN DATAO SYNC and LPCN SHIFT SYNC A and B flip-flops set, and the LPI BUFFER AVAILABLE level at -3 Vdc, R613 Pulse Amplifier TU at C06 generates the LPCN GO pulse. Control logic operation from this point is dictated by the 7-bit character in flip-flops LPBF0-6 of the buffer register. This character is decoded by the logic shown on print LPDA.

The decoding function is detailed in a subsequent paragraph. In essence the decoder defines the character as one of four character types: printing character, vertical control character, horizontal control character, or illegal character.

4.2.2.1 Printing Character - If the 7-bits in buffer flip-flops LPBF0-6 are decoded as a printing character, the LPCN GO pulse is converted to the LPCN DATA STROBE pulse (S107 gate ML at C06, LPCN). LPCN DATA STROBE is delayed 2.5 μs and becomes the LPI DATA STROBE pulse (LPI) which transfers the contents of the first six buffer register flip-flops into the line printer. The data is sent to the printer by the B163 gates shown on print LPI. These gates are conditioned by the LPDA NORMAL CODE which was enabled by the decoder for a printable character situation. During the transfer, the line printer disables the BUFFER AVAILABLE level, preventing the generation of further LPCN GO pulses.

The LPCN DATA STROBE pulse also initiates the stepping of the column counter (LPCC0-7, LPCC) that keeps track of the number of characters sent to the line printer memory. For this purpose, LPCN DATA STROBE is converted to the LPCN CC ADD ONE pulse by the R613 Pulse Amplifier FH at C08 (LPCN).

The same LPCN GO pulse that initiates the data strobe operation clears the LPCN SHIFT SYNC A and B flip-flops. In addition, it is delayed 4 μs and becomes the LPCN CYCLE pulse (B165 gate DE at D04). Upon receiving LPCN CYCLE, R613 Pulse Amplifier TU at C08 generates the LPCN SHIFT pulse. The pulse amplifier input is conditioned to pass the LPCN CYCLE pulse because the original DATAO pulse stepped the shift counter to a zero count.

The LPCN SHIFT pulse is converted to the LPBF SHIFT A and B pulses (LPBF1). These pulses step the shift counter to 001, and shift the contents of the buffer register (LPBF2). The shift is such that the contents of LPBF0-6 are lost; the contents of LPBF7-13 move into LPBF0-6; the contents of LPBF14-20 move into LPBF7-13, and so forth. Note that although the contents of LPBF28-34 shift into LPBF21-27, no new data is shifted into LPBF28-34. Consequently, the contents of these flip-flops remain unchanged.

In addition to initiating the shift operation, the LPCN SHIFT pulse sets the control register LPCN SHIFT SYNC B flip-flop (LPCN). After a 1 μs delay, LPCN SHIFT becomes LPCN SHIFT DLY (R302 delay TUV at C07) and sets the LPCN SHIFT SYNC A flip-flop. With the setting of the SHIFT A and B flip-flops, the R613 Pulse Amplifier TU at C06 is conditioned to generate another LPCN GO pulse when the line printer again enables the BUFFER AVAILABLE level. Assuming that the buffer register has been filled with printable characters, the next LPCN GO pulse initiates the same operations as the first LPCN GO pulse. Essentially, this means that the character in buffer flip-flops LPBF0-6 is strobed into the line printer, the column and shift counters are incremented, and the contents of the buffer register are shifted. This same cycle occurs twice more, transferring four of the five printable characters into the line printer, and stepping the shift counter to four (100).

When the fifth LPCN GO pulse is generated, it causes the fifth character to be strobed into the line printer. It also produces another LPCN CYCLE pulse (B165 gate DEF at D04, LPCN). But, the count of four in the shift counter prevents the generation of another LPCN SHIFT pulse (R613 Pulse Amplifier RSTU at C08). Instead, it forces R602 Pulse Amplifier STUV at B06 to generate an LPCN DONE pulse. LPCN DONE clears the LPST BUSY flip-flop (LPST0) and sets the LPST DONE flip-flop.

Setting the LPST DONE flip-flop causes decoder B152 at H25 to send the processor an interrupt request. The processor can sample the status of the LPST DONE flip-flop by a CONI instruction specifying the line printer device number. This brings up an IOC LP CONI level (B134 gate DEFH at H02, IOCC). IOC LP CONI gates the contents of the line printer status register (LPST) onto the I/O bus via the B163 gates at F18 and F19.

4.2.2.2 Vertical Control Characters - Up to and including the generation of LPCN GO, vertical control characters cause essentially the same control logic operations as printable characters. A major difference is that in the decoder they produce the LPDA SPACE ONLY or LPDA PRINT AND SPACE command.

When an LPDA SPACE ONLY command is decoded, the LPCN GO pulse causes R613 Pulse Amplifier RSTU at D12 (LPCN) to generate the LPCN SPACE COMMAND. This signal is converted to the LPI SPACE COMMAND level by R302 delay SUV at D13 (LPI) and B684 driver NMR at D15. Upon receiving the LPI SPACE COMMAND level, the printer spaces the paper vertically according to the three least-significant bits of the control character. These bits are sent to the line printer via the output gates shown on DEC print LPI. Depending on the type of vertical character, these bits are gated to the printer as a result of a LPDA NORMAL CODE level (codes 020_8-024_8) or as a function of B133 gate TUV at B08 and B135 gates KLMN and RSTU at C14 (codes 012_8-014_8). The significance of the various character codes are discussed in detail in the subsequent paragraph, Decoder.

Operations initiated by a print and space character are nearly identical to those produced by a space only character. The major difference is that the R613 Pulse Amplifier DEFH at D12 (LPCN) converts the LPCN GO pulse to the LPCN PRINT AND SPACE signal. This signal in turn, is converted to the LPCN CLR CC pulse (R613 Pulse Amplifier KLMNP) that clears the column counter. LPCN PRINT AND SPACE also becomes the LPI PRINT AND SPACE B signal that is sent to the line printer (R302 delay EFJLM, B684 driver CDFKL, LPI). In response to LPI PRINT AND SPACE B, the line printer prints out all of the characters in its memory. When the printout is complete, the printer spaces the paper vertically, using the three least-significant bits of the character in the same manner as during a space only operation.

For both the space only and print-and-space operations, shifting of the contents of the buffer register is accomplished as in a printing character transfer. The BUFFER AVAILABLE level from the printer is again employed to indicate the printer's readiness to handle additional characters.

4.2.2.3 Horizontal Control Character - The horizontal tab operation is similar to the printable character operation in that LPI DATA STROBE B is generated and strobes a 7-bit character into the printer. In this case, the 7-bit code is the space character.

Whenever the horizontal tab operation is encountered, the space character is repeatedly sent to the printer until the column counter (LPCC) reaches a multiple of 8_{10}. To determine the status of the column counter, expanded gate S111 KLN at C12 and R002 HJK at C11 examine the contents of the three least-significant counter flip-flops (LPCC5-7). Included at the input to the gating structure is the LPDA DO H TAB level that the decoder provides during the horizontal tab operation. When LPCC5-7 contain all 1s the LPCC TAB STOP level from gate R107 HF at C09 is true. Otherwise, the LPCC TAB STOP level is false.

The false conditon of LPCC TAB STOP is ANDed with LPDA DO H TAB by B134 gate JKL at B07 (LPDA). During a horizontal tab cycle, then, this gate generates the LPDA TAB CYCLE level as long as the three least-significant character flip-flops do not contain all 1s. When the LPDA TAB CYCLE level is true, it inhibits the input to R302 delay TUV at C05 (LPCN), thereby preventing the LPCN GO pulse from initiating the LPCN CYCLE pulse (B165 gate DE at D04) and the ensuing shift cycle. As for a printable character operation, however, LPCN GO does produce the LPCN DATA STROBE pulse (S107 gate LM at C09) that eventually strobes bits LPI DATA00-06 (LPI) into the printer.

Because the decoder does not generate LPDA NORMAL during a horizontal tab operation, the gates that drive LPI DATA00 and LPI DATA02-06 are not enabled. On the other hand, the LPDA DO H TAB level enables B165 gate DE at C15 driving LPI DATA01. As a result, code 040_8, the space character code, is sent to the printer. (When the printer encounters a space character during a printing print cycle operation it inhibits the corresponding hammer.) When the printer has accepted the space character it re-enables the BUFFER AVAILABLE level.

In the absence of a shift cycle, the shift counter is not stepped and the buffer register data is not shifted. Therefore, the horizontal tab code remains in the final stage (LPBF0-6) of the buffer register. Each time the printer re-enables BUFFER AVAILABLE after reading in a horizontal space character, the cycle is repeated.

With the generation of each data strobe command, the horizontal space character is read into the printer and the character counter is stepped. This procedure is repeated until the generation of the data strobe command that causes the three least-significant flip-flops of the character counter to reach a count of seven. When the printer responds to this transfer with the BUFFER AVAILABLE signal, another character stobe cycle occurs. The count of seven in character counter flip-flops LPCC5-7 forces the LPCC TAB STOP level true (R107 gate HF at C9, LPCC). With the LPCC TAB STOP level true, the LPDA TAB CYCLE level goes false (B134 gate JKL at B07, LPDA). This enables the input to R302 delay SUV at C05 (LPCN), thus permitting a shift cycle. This time, as the horizontal space character is transferred to the printer, the three least-significant character counter bits are stepped to 000 and the content of the buffer register is shifted. The next cycle processes the character following the horizontal tab character.

4.2.2.4 Illegal Character - When the character contained in line printer flip-flops LPBF0-6 does not decode as a printing, vertical-control, or horizontal character, it is treated as an illegal character. In this case, the LPCN GO pulse does not initiate any of the control pulses that normally trigger line printer action, instead it initiates an LPCN CYCLE pulse and the ensuing shift cycle. As a result, the character is simply shifted out of the buffer register and lost, and the line printer is not affected.

4.2.2.5 Printing-Character Overflow - Transferring 132 consecutive printing characters to the printer fills the printer's memory to capacity. If the 133rd character initiates a printing operation, the memory is emptied and the printer is readied to receive more printing characters. If the 133rd character is another printing character, however, the control logic must force a printing operation. The operation is such that the 133rd printing character is not lost, but rather becomes the first character sent to the printer following the memory printout.

The control cycle that transfers the 132nd consecutive printing character to the printer steps the column counter to 133_{10}. From this count the decoder, shown in the lower left of the LPCC print, generates the LPCC LINE OVER ERROR level. Because the 133rd character is a printing character, the control logic initiates another data strobe cycle. As for every cycle of this type, LPCN GO is converted to the LPCN DATA STROBE pulse (LPCN). This pulse, in turn, produces the 2.2 μs LPI DATA STROBE level that initiates the strobing of the character into the line printer. However, the line printer does not accept the character, because its memory is full.

With the column counter count (133_{10}) enabling the LPCC LINE OVER ERROR level, the trailing edge of LPI DATA STROBE performs three operations. First, it sets the LPCN CONO PRINT flip-flop (LPCN), inhibiting the generation of an LPCN CYCLE pulse and the resultant LPCN SHIFT pulse. (As a result, the shift counter is not incremented, nor is the content of the buffer register shifted.) Second, LPI DATA STROBE clears the LPCN SHIFT SYNC A and B flip-flops, inhibiting the initiation of further transfers. (This is a precaution to insure that these flip-flops are cleared in the event that the character being decoded is the horizontal tab character.) Third, LPI DATA STROBE triggers the R302 delay EFJLM at E03 (LPCN). At the end of the 4-μs delay the logic generates the LPCN CONO PRINT PLS and LPCN CONO PRINT DLY pulses.

The LPCN CONO PRINT PLS pulse sets the LPCN SHIFT SYNC B flip-flop in preparation for another character transfer. It also generates the LPCN PRINT AND SPACE pulse that causes the printer to print out the contents of its memory and space the paper according to the code on output lines LPI DATA00-06 (LPI). Because the LPCN CONO PRINT flip-flop is set, LPI DATA04 and 05 are 1s.

As usual, the LPCN PRINT AND SPACE pulse also produces the LPCN CLEAR CC pulse (R613 pulse amplifier MNP at C08, LPCN) which clears the column counter in preparation for subsequent character transfers.

Approximately 4 μs after the LPCN PRINT AND SPACE pulse, the LPCN OVERFL DATA DLY level goes positive (R302 delay SUV at E03). The positive transition clears the LPCN CONO PRINT flip-flop and sets the LPCN SHIFT SYNC A flip-flop. When the printer completes the printout and sends a BUFFER AVAILABLE level, the control logic begins another transfer cycle. Since the final register flip-flops still contain the printing character that initiated the printout, that character is now transferred to the printer.

4.2.3 Decoder

The decoder's (LPDA) prime function is to determine whether the contents of buffer register flip-flops LPBF0-6 define a printable character, a control character, or an illegal character. Having made this distinction, it conditions the remainder of the control logic accordingly.

4.2.3.1 Printer Types - Table 2-7 in Chapter 2 of this manual shows the ASCII code as modified for use in the PDP-10 system. Codes 011_8 through 015_8 and 020_8 through 024_8 always define control characters. However, the printable character codes used vary with the line printer type. Sixty-four character printers are equipped with the printable characters defined by codes 040_8 through 137_8. Ninety-six character printers are equipped with printable characters defined by codes 040_8 through 177_8. One-hundred twenty-eight character printers are equipped with printable characters defined by the codes 000 through 177_8. In the latter case, certain control circuits are used to recognize the printable characters that use the same codes as the ten control characters. These same circuits are used to print a character for the null code (000) and the delete code (177_8).

Jumper wires on the W990 module at A03 adapt the control logic for use with the various printers. No jumpers are required for 64-character printers. For 96-character machines that do not print a symbol for the delete code (177_8), a jumper is inserted between terminals C and D of the module, enabling the LPDA 96 CHAR level (S107 gate NP at A04). Essentially, printers of this type are

95-character printers. For full 96-character machines, that is, printers that do print a symbol for the delete code, terminal C is jumpered to D, and terminal H is jumpered to J. The latter jumper enables the LPDA FULL 96 CHAR (S107 gate RS at A4). For 128-character printers jumpers are inserted between C and D, H and J, and E and F. The latter jumper enables the LPDA 128 CHAR (S107 gate TU at A04). These levels are used throughout the control logic to enable functions relevant to the different printer types.

4.2.3.2 LPDA PRINTING CHARACTER - The LPDA PRINTING CHAR level is generated by the S107 gate JK at A04. This signal eventually enables the LPI DATA STROBE B level that sends printable characters to the line printer. In its most obvious application, then, it is brought up by the codes (040_8 - 176_8) for printable characters (S111 gates DEH, KLN, and RSU at A06). It is also enabled by the DO H TAB level (S107 gate HF at A04) to send a series of space characters to the line printer during a horizontal tab operation.

Two other groups of gates also enable LPDA PRINTING CHAR. The first group (S111 gate RSU at A11 and R002 gate LN at A13) is concerned with printing a character for the delete code on full 96-character line printers. This operation requires that the central processor send two delete codes. The first delete code sets the LPCN ALT flip-flop (LPCN); the second is transferred to the line printer as a printable character.

The second group (S111 gates DEH KLN, and RSU at A05, LPDA is used with 128-character printers. It enables the use of control character codes and the codes for null (000) and delete (111) to define printable characters. Most critical to this operation is the use of the LPDA CONTROL level (S107 gate LM at A04). This level is enabled when a control character, delete, or null is decoded. S111 gate DEH at A05 uses this signal in conjunction with the set LPCN ALT flip-flop to force an LPD PRINTING CHAR level for delete, null, and the control characters. Again, setting the LPCN ALT flip-flop is accomplished by preceding the code to be printed as a character with a delete code. S111 gate KLN at A05 uses the false condition of the LPDA CONTROL to force an LPDA PRINTING CHAR level for all other codes including 010_8, 016_8, and 017_8.

4.2.3.3 LPDA PRINT AND SPACE - The LPDA PRINT AND SPACE level is generated by S107 gate HF at B09 whenever a print operation is required. S111 gate KLN at B01 forces the signal when LPCC = 0 is false and LPDA FORM ADVANCE is true. The false condition of LPCC = 0 is enabled as long as a printable character has been sent to the printer since the last LPDA PRINT AND SPACE. B134 gate JKL at A01 generates the LPDA FORM ADVANCE level for all vertical control codes except LPDA CAR RET, providing the LPCN ALT flip-flop is not set. (If this flip-flop were set, it would initiate a conversion from a control to a printable character function for a 128-character printer. See Section 4.2.3.2.)

The LPDA PRINT AND SPACE COMMAND is converted to the LPI PRINT AND SPACE B signal (LPI) that directs the printer to print the contents of its memory. When the printout is complete, the printer spaces the paper vertically, according to the configuration of bits LPI DATA04-06. These bits are enabled by B133 gate TUV at B08 and B135 gates KLMN and RSTU at C14. In turn, these gates are conditioned as a function of the decoded vertical character.

The LPDA PRINT AND SPACE level is also enabled for a carriage return operation. When the LPDA CAR RET character is decoded (S151 decoder at A10, LPDA) and the LPCN ALT flip-flop is not set, S107 gate KJ at B09 (LPI) generates the LPI INHIBIT SPACE B level, this level is sent to the printer to inhibit a spacing operation. At the same time, LPI INHIBIT SPACE B causes S107 gate HF at B09 (LPDA) to generate the LPDA PRINT AND SPACE level. This level is also sent to the printer as LPI PRINT AND SPACE B. In response to LPI INHIBIT SPACE B and LPI PRINT AND SPACE B the printer prints a line but does not space the paper vertically. Consequently, the next print command can cause an overprint.

4.2.3.4 LPDA SPACE ONLY - The LPDA FORM ADVANCE level (B134 gate JKL at A01) is ANDed with the LPCC = 0 level to generate LPDA SPACE ONLY (S111 gate RSY at B01). Consequently, LPDA SPACE ONLY is produced by any vertical control code except LPDA CAR RET, provided the LPCN ALT flip-flop is not set and no printable characters have been sent to the printer.

As during a print and space operation, paper spacing is accomplished as a function of the decoded vertical character. This character is made available to the printer via V133 gate TUV at B08 (LPI), and B135 gates KLMN and RSTU at C14.

4.2.3.5 LPDA CASE SHIFT - When a lower-case character is decoded (codes 140_8 - 176_8) and the printer is equipped with only 64 characters, S111 gate RSU at A07 (LPDA) generates the LPDA CASE SHIFT signal. This signal prevents the enabling of the LPI DATA 01 line to the printer (B135 gate DEFH at C14, LPI). Consequently, the printer "sees" a code between 100_8 and 136_8, and prints the upper-case equivalent of the lower-case character.

4.2.3.6 LPDA NORMAL CODE - The LPDA NORMAL CODE level gates the contents of buffer register flip-flops LPDB00-06 to the printer via the output gates shown on DEC print LPI. It is generated by ANDing the outputs from two gates. The output from the first gate (B133 gate NPR at B08, LPDA) is true when a printing character or vertical control character codes 012_8 - 014_8 are decoded. The second gate (B134 gate TUV at B07) prevents the output from the first gate from enabling the LPDA NORMAL CODE during a CONO PRINT or horizontal tab operation. These restrictions are imposed since both CONO PRINT and horizontal tab require specific codes to be sent to the line printer.

If the false condition of the LPDA DO H TAB level were not included at the input to the second gate, LPDA NORMAL CODE would be enabled during a horizontal tab operation because that operation enables the LPDA PRINTING CHAR level. As a result the line printer would "see" the entire horizontal tab character rather than "seeing" a 1 only on bit LPI DATA01 (LPI). The LPCN CONO PRINT (0) level is included in the gating structure (LPDA) for essentially the same reason. In this case, of course, the printer is forced to "see" 1s on bits LPI DATA04 and 05 (LPI).

CHAPTER 5

XY10 THEORY OF OPERATION

This chapter contains the theory of operation for the Type XY10 Plotter. The information is given in this order: functional description of the plotter system using a simplified block diagram, Figure 5-1; identification and functional description of the plotter and I/O bus interface lines; explanation of the operation of the plotter control.

The theory of operation for the model of plotter mechanism used is contained in the supplied instruction manual for the specific plotter and is not duplicated in this document.

5.1 BLOCK DIAGRAM ANALYSIS

The Type XY10 Plotter provides the control logic and interface necessary for implementation of a plotter to a PDP-10. A series of functions controlled by I/O instructions initialize the plotter control logic, and generate priority interrupt requests to indicate a change in status, and initiate a plotting operation. Refer to Figure 5-1 for the following functional description.

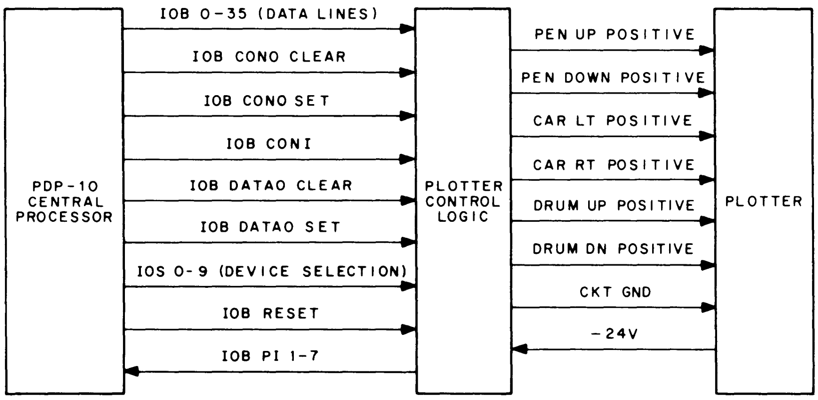


Figure 5-1 Simplified Block Diagram of the XY10 Plotter System

When power is first applied to the Type 884 Power Control of the BA10 cabinet, and the POWER ON/OFF switch on the plotter is in the ON position, the BUSY and DONE flags and the PI register in the plotter control logic are cleared. These operations occur whether or not the XY10 is selected.

If the plotter has been selected, a CONO instruction is performed prior to a plotting operation. This instruction clears the BUSY and DONE flags and the PI register. The device selection number (140_8) and the PI channel assignment number are sent to the control logic during a CONO instruction.

A DATAO instruction is sent to the plotter control logic and actuates the plotter. Following this, a CONI reads the status gates of the control logic to determine whether or not the plotter is ready to accept another command.

Tables 5-1 and 5-2 contain a functional description of the XY10 interface lines.

Table 5-1
I/O Bus Interface Cable

Signal Line	Function
IOB 0 through IOB 35	Used to transfer data and status information into the central processor and control signal into the plotter control logic. In the XY10, only IOB30 through IOB35 are used.
IOB CONO CLEAR	Used to clear the BUSY and DONE flags and the PI register.
IOB CONO SET	Occurs 1 μs after IOB CONO CLEAR. Used to gate the PI channel number into the PI register and clear the DONE and/or BUSY flags.
IOB CONI	Used to gate plotter status into the central processor.
IOB DATAO CLEAR	Clears the DONE flag, sets the BUSY flag and triggers internal delays.
IOB DATAO SET	Occurs 1 μs after IOB DATAO CLEAR. Gates data into the plotter control register.
IOS 3(1) through IOS 9(0)	Used to identify the device number to the plotter control logic.
IOB RESET	Used to clear the plotter control logic.
IOB PI1 through PI7	Used to transfer the program interrupt signal to the central processor. Only one line is assigned to the plotter at a time.
DATAO CLEAR	Clears the DONE flag, sets the BUSY flag, and triggers internal delays.
DATAO SET	Permits data to be loaded into the plotter function control flip-flop register.

Table 5-2
Plotter Interface Cable

Signal Line	Function
PEN UP POSITIVE	Raises the plotter pen
PEN DOWN POSITIVE	Lowers the plotter pen
CAR LT POSITIVE	Moves the pen carriage one increment to the left

Table 5-2
Plotter Interface Cable

Signal Line	Function
CAR RT POSITIVE	Moves the pen carriage one increment to the right
DRUM UP POSITIVE	Causes the paper drum to move up one increment
DRUM DN POSITIVE	Causes the paper drum to move down one increment

5.1.1 Plotter Logic Operation

The operation of the plotter control logic is discussed in this order: the initialization of the control logic that occurs after the application of power; the operation of the control logic during the CONO, DATAO, and CONI instructions. In the discussion of the DATAO instruction, the major operations performed as a result of the DATAO instruction are described separately as there are differences between some of the operations. Where the generation of the control signals is similar, the operations are discussed as a group. Next, the different ways to clear the XY plotter control logic are discussed. Last, the differences between the XY plotter control logic when housed in the DECtape logic rack are described.

In these discussions, the circuits as shown on the block schematics are referenced in the text the first time the circuit is discussed. To simplify the references, only the zone number where the circuit is located and the drawing number abbreviation of the block schematic number are provided (e.g., a PLST PLOT BUSY flip-flop (B4-PLST) reference indicates that the PLST PLOT BUSY flip-flop is located in zone B4 of drawing number D-BS-XY10-0-PLST).

5.1.2 Power Turn-On

When input power is applied to the Type 844 Power Control in the BA10 cabinet, power is applied to the plotter control logic. A normally closed (NC) contact in the power control is delayed from opening for 4s, and the IOC POWER ON integrating one-shot delay in the plotter control logic (B3-IOCA) goes to the 1 state.

With IOC POWER ON in the 1 state, it generates an IOC CLEAR signal. IOC CLEAR is applied to a pulse amplifier (D4-IOCD) to generate IOC PL CONO CLEAR which clears the PLST PLOT DONE flip-flop (B5-PLST), the PLST PLOT BUSY flip-flop (B4-PLST), and the 3-bit PI (priority interrupt) register (D3 through D5-PLST). The plotter control logic is now ready to be conditioned for normal operation.

After the 4s delay, the (NC) contact in the power control opens and the IOC POWER UP signal goes true. This causes the IOC POWER ON one-shot to return to the 0 state, where it remains as long as the input power is in the on condition.

5.1.3 CONO Instruction

The CONO instruction is performed to establish initial conditions in the plotter control logic.

To perform a CONO instruction, the central processor generates an IOB CONO CLEAR signal and the plotter device selection number (140_8). These signals are routed to the plotter control logic via the I/O bus. The device selection number is decoded by the plotter device decoder (C4-IOCA) to generate IOC PLOT SELECT, while IOB CONO CLEAR is inverted to generate IOC CONO CLEAR (C7-IOCA).

The IOC PLOT SELECT signal conditions four DCD gates (A5 through D5-IOCD). When IOC CONO CLEAR occurs, IOC PL CONO CLEAR is generated and clears the PLST PLOT DONE flip-flops (B5-PLST), the PLST BUSY flip-flop (B4-PLST), and the 3-bit PI register (A3 through A5-PLST). The central processor generates an IOB CONO SET signal and routes it to the plotter control logic 1 μs later. The central processor places the PI channel assignment number on IOB 33 through IOB 35 of the I/O bus. A 1 may be placed on IOB 32 to set the PLST PLOT DONE flip-flop, clear the PLST PLOT DONE flip-flop, and cause a program interrupt when the CONO instruction is executed, or on IOB 31 to set the PLST BUSY flip-flop. After input buffering (drawing IOB), the resultant signals are routed to their respective gates on drawing PLST.

The IOB CONO SET signal is inverted (C6-IOCA) and the resultant signal, IOC CONO SET, is routed to a DCD gate (C5-IOCD). Since the IOC PLOT SELECT signal is true, the gate is enabled and IOC PL CONO SET is generated. This pulse loads the PI channel assignment into the PI register, sets the PLST PLOT DONE flip-flop and clears the PLST BUSY flip-flop if IOB 32 is a 1 and/or sets the PLST PLOT BUSY flip-flop if IOB 31 is a 1. To read the plotter status register, the central processor may perform a CONI instruction.

5.1.4 CONI Instruction

The CONI instruction is performed after a program interrupt to read the plotter status register. To perform the CONI instruction, the central processor generates an IOB CONI signal and the plotter device selection number and routes these signals to the plotter control logic via the I/O bus. The plotter device selection number is decoded to generate IOC PLOT SELECT while IOB CONI is inverted to generate IOC CONI.

IOC CONI and IOC PLOT SELECT are ANDed (D3-IOCD) to generate IOC PL CONI which enables the plotter control logic status gates (B7 through D7-PLST). The following status information is gated onto the I/O bus and into the central processor; if the plotter power is turned on, IOB 30 = 1; if the PLST PLOT BUSY flip-flop is set, IOB 31 = 1; if the PLST PLOT DONE flip-flop is set, IOB 32 = 1; and the PI channel assignment number is read by IOB 33 through IOB 35.

The central processor determines the state of the plotter system from the status information. When the plotter power is on and the PLST PLOT BUSY flip-flop is cleared and the PLST PLOT DONE flip-flop is set, the plotter is ready for data.

5.1.5 DATAO Instruction

During the DATAO instruction, the central processor sends signals to the plotter control logic via the I/O bus. These signals cause various control signals to be generated in the plotter control logic. Output signals from the plotter control logic initiate plotter operations. These output signals are compatible with the various CalComp plotters.

Due to the differences in plotter timing requirements, the raise pen and lower pen operations are discussed separately. The other plotter operations are performed in a similar fashion and are explained as a group.

5.1.6 Operation of DATAO

To send data to the plotter, the central processor generates an IOB DATAO CLEAR signal and the plotter device selection number (140_8). These signals are placed on their respective I/O bus lines. IOB 30 contains a 1. The device selection number is decoded (B4-IOCA) to generate IOC PLOT SELECT and IOB DATAO CLEAR is inverted to generate IOC DATAO CLEAR.

IOC PLOT SELECT is used to condition a DCD gate (B5-IOCD) which is enabled by IOC DATAO CLEAR. The resultant signal from the DCD gate is routed to a pulse amplifier and an inverter to generate IOC PL DATAO CLEAR. At this time, the following operations are performed: the PLST PLOT DONE flip-flop (B5-PLST) is cleared; the PLST PLOT BUSY flip-flop (B4-PLST) is set; a 2.5 ms one-shot delay (A5-PLCN) is triggered.

5.1.6.1 Move Pen or Drum - The four motions which cause the paper drum to be moved up or down and the pen carriage left or right are similar in nature. The operation to take place is determined by which IOB line of IOB 32 through IOB 35 contains a 1. In the following discussion it will be assumed that the pen carriage is to be moved an increment to the left.

The plotter logic operations up to and including the generation of IOC PL DATAO SET are explained above in Section 5.1.

IOB 32 (1) is buffered (B7-IOB) to produce IOB 32B (1), thereby conditioning the DCD gate associated with the PLCN -X flip-flop (C6-PLCN). When the IOC PL DATAO SET pulse is generated, the PLCN -X flip-flop is set. The 1 side of the flip-flop is routed to a negative level amplifier. The output of the amplifier, CAR LT POSITIVE (car left positive), is routed to the plotter via the plotter interface cable and is used to move the plotter's pen carriage an increment to the left.

The output of the 2.5-ms delay, PLCN REG CLEAR, clears the PLCN -X flip-flop and triggers a second 2.5-ms delay. The trailing edge of this second delay, PLCN MOVE DONE, pulses the DCD gate conditioned by PLST RAISE DONE (B5-PLST) to set the PLST PLOT DONE flip-flop. The 1 side of PLST PLOT DONE is inverted and serves to clear the PLST PLOT BUSY flip-flop as before, the same flip-flop enables the PI decoder. With the PI decoder enabled, the PI channel assignment number stored in the PI register is decoded and a program interrupt is routed to the central processor via the assigned PI line. At this time, the plotter is ready to receive the next control signal.

One microsecond after the generation of IOB DATAO CLEAR, the central processor generates an IOB DATAO SET pulse which is inverted to produce IOC DATAO SET. This pulse enables a DCD gate (A5-IOCD) that was conditioned by IOC PLOT SELECT to output an IOC PL DATAO SET pulse. Data held on IOB 30 through IOB 35 are loaded into the DATA flip-flops when this pulse occurs.

5.1.6.2 Raise Pen - When the IOC PL DATAO SET pulse is generated and IOB 30 (1) is true, the PLCN RAISE PEN flip-flop is set. The 1 side of the flip-flop is applied to a negative level amplifier (NLA) and a DCD gate (B2-PLST) associated with a 7.5-ms delay (B2-PLST). The output signal from the NLA, PEN UP POSITIVE, is applied to the plotter mechanism via the plotter interface cable and is used to raise the plotter pen.

At the completion of the 2.5-ms delay mentioned in Section 5.1.6.1, the PLCN REG CLEAR pulse (B5-PLCN) is generated and is used to trigger the 7.5-ms delay and clear the PLCN RAISE PEN flip-flop. When the 7.5-ms delay is completed, PLST RAISE DONE is generated and is used to collector trigger the PLST PLOT DONE flip-flop (C5-PLST). With the flip-flop in the 1 state, the PI decoder (C2-PLST) is enabled. With the PI decoder enabled, the PI channel assignment number, stored in the PI register, is decoded and a program interrupt request is sent to the central processor via the assigned PI line.

The 1 side of the PLST PLOT DONE flip-flop clears the PLST PLOT BUSY flip-flop. The plotter control and mechanism are now ready for the next instruction.

5.1.6.3 Lower Pen - With this instruction, the conditioning levels described above hold true with the exception that IOB 31 = 1. After input buffering (B7-IOB) the resultant signal, IOB 31B, conditions the set gate of the PLCN LOWER PEN flip-flop (C7-PLCN). When the IOC PL DATAO SET signal is generated, the set gate of the PLCN LOWER PEN flip-flop is enabled and the flip-flop is set. The 1 side of the flip-flop is routed to a negative level amplifier. The output of the negative level amplifier, PEN DOWN POSITIVE, is routed to the plotter via the plotter interface and is used to lower the plotter's pen.

After a 2.5-ms delay, the PLCN REG CLEAR signal (B5-PLCN) is generated and is used to trigger the 30-ms delay and clear the PLCN LOWER PEN flip-flop.

When the 30-ms delay is completed, a second 30-ms delay is triggered. The completion of this delay produces PLCN PEN DONE which is used to set the PLST PLOT DONE flip-flop and which, in turn, clears the PLST PLOT BUSY flip-flop. The plotter has had 62.5 ms total to lower the pen.

As before, with the condition PLST PLOT DONE (1), the PI decoder is enabled and the PI assignment number, stored in the PI register, is decoded and a program interrupt is routed to the central processor via the assigned PI line. At this time the plotter is ready to receive the next control signal.

5.1.7 Logic Clear

Besides clearing the plotter logic through an IOB CONO CLEAR instruction and the power turn-on procedure, this function can be accomplished by way of an IOB RESET pulse sent from the PDP-10 to the plotter control via the I/O bus.

The incoming pulse is inverted (B6-IOCA) to produce IOC RESET. This signal, in turn, is doubly inverted to generate IOC CLEAR (B4-IOCA). IOC CLEAR is applied to the pulse amplifier (D4-IOCD) from which it emerges as a 100-ns IOC PL CONO CLEAR pulse. This pulse is used to clear the plotter control logic as explained in Section 5.1.2, Power Turn-On.

5.1.8 DECtape Logic

The plotter can also utilize the TD10 logic rack for control. The circuitry involved is shown on the drawings labeled CONT.

The main difference between the BA10 and TD10 is slightly different signal designations. Specific differences are explained in the paragraphs which follow. Module locations will obviously be different.

The main difference deals with the CROBAR pulse. PL CONO CLR, in the TD10, serves the same purpose as IOC CONO CLEAR in the BA10; namely, to clear the 3-bit PI register and the PL DONE and PL BUSY flip-flops, which are shown across the top of CONT, sheet 1. A DCD gate conditioned by CROBAR, which is analogous to IOC POWER UP in the BA10, is strobed by T CLOCK. These signals arrive from the TD10 logic. All other TD10 logic functions are similar to those in the BA10.

CHAPTER 6
MAINTENANCE

Maintenance of the BA10 and the three options consists of preventive maintenance procedures that are performed periodically, troubleshooting procedures that are performed in the event of equipment malfunction, and corrective maintenance procedures that are performed to repair equipment malfunctions. The procedures presented here assume that maintenance personnel are familiar with the theory of operation of the equipment contained in this manual, the PDP-10 input/output programming described in the PDP-10 Systems Reference Guide (DEC-10-HGAA-D), the programming notes contained in the manufacturer's technical manuals written for the various equipment.

6.1 EQUIPMENT REQUIRED

The equipment in this system does not require special test equipment for maintenance. Standard test equipment, hand tools, cleaners, test cables and probes are considered a part of every well-equipped maintenance activity and are not listed here.

6.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to the initial operation of the BA10 and the three options and periodically during their operating life to ensure that they are in satisfactory operating condition. Faithful performance of these tasks forestalls possible future failure by correcting minor damage and discovering progressive deterioration at an early stage. A log book used to record data found during the performance of each preventive maintenance task will indicate the rate of circuit deterioration and provide information which will enable maintenance personnel to determine when components should be replaced to prevent failure of the equipment. All preventive maintenance tasks, except for checking the card reader oil supply when appropriate, should be performed as a function of conditions at the installation site taking into consideration average usage and the down-time limitations of equipment. Perform the mechanical checks at least once each month or as often as required to maintain efficient functioning of the cooling equipment. All other tasks should be performed on a regular schedule, at an interval determined by the average usage, and the reliability requirements of the system. For a typical application, a schedule of every four months or 1,000 equipment operating hours, whichever occurs first, is suggested.

6.2.1 Mechanical Checks

The following steps should be performed during a mechanical check; and the indicated corrective action should be performed if a substandard condition is located.

a. Clean the exterior and the interior of each equipment cabinet by using a vacuum cleaner or clean cloths moistened in nonflammable nonconductive solvent. Be sure the solvent is not harmful to paint.

b. Clean dirt from the blower assemblies while using care not to damage cable assemblies or modules.

c. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas.

d. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring.

e. Inspect each row of modules to assure that each module is securely seated in its connector.

f. Verify that the proper I/O bus cables and all other interconnecting cables are firmly seated in their respective connectors.

g. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors giving these signs of malfunction.

h. Clean the lint and dust that has collected on the exposed surfaces of the card reader, card hopper, output stacker, and other areas. On the plotter, clean the pen rods with alcohol.

6.2.2 Power Supply Check

Check the output voltage and ripple content of the supplies and assure that they are within tolerances. Use a multimeter to check the output voltage without disconnecting the load and use an oscilloscope to measure the peak to peak ripple content on the dc output.

6.2.2.1 DEC 728 Power Supply - Check the two output voltages from this supply at the logic end. These voltages are not adjustable, so if the output voltage or ripple content is not within the tolerance specified, the supply is considered defective and troubleshooting procedures should be performed.

Check the +10V output between the red (+) and black (-) wires to assure that it is between +9.5 to +11.0V with less than 800 mV rms ripple. Check the -15V output between the blue (-) and black (+) wires to assure that it is between -14.5 and -16.0V with less than 100 mV rms ripple. Note that the black wires are common with the power supply chassis.

6.2.3 Margin Checks

Margin checks are performed to aggravate borderline conditions within the logic circuits, thereby revealing solid observable faults. In this way, marginal conditions can be corrected to fore-stall equipment downtime. Margin checks can also be used as a troubleshooting aid for locating marginal or intermittent components. Checks may be performed by varying the logic voltages manually at the margin control panel of the central processor while performing a diagnostic procedure under program control.

6.2.4 Card Reader Oil Supply Check

When an oil-lubricated vacuum pump is used, oil vapor is fed to the vacuum pump mounted on the drive motor by a carburation system in the head of the oil supply system. Oil is stored in the larger reserve container on the top and the oil is automatically fed into the smaller, lower glass container to maintain the oil level at approximately 3/4 oz. Check the oil level in both the larger and smaller container and empty any oil which accumulates in the collector can at the outlet of the pump.

If the oil level in the reserve container is low, the reserve container is removed and refilled with one of the lubricants listed below. A valve rod permits the reserve container to be removed and replaced without spilling the oil. To fill the reserve container, pull it up and out of the adjusting sleeve and invert. Add oil to the reserve container slowly while depressing the valve stem. Replace the reserve container by inserting it quickly against the stop. To adjust the oil level in the bottom container loosen lock nut and move adjusting sleeve until the desired oil level is reached.

The recommended lubricant is Pneumatic Lubricating Oil, SAE #10, Gast Mfg. Corp., P/N AD 220. Acceptable substitutes are American S1 #10, Citgo C-310, Gulf Gulflube HD-10, Humble Encolube HDX-10, Mobile Delva 1110, Shell Rotalla #10, Sinclair Super TBT #10, Sun Sunvis 610, or Texaco URSA S-1 #10.

6.2.5 XY10 One-Shot Adjustments

Table 6-1 lists the increment times for the four plotter models that can be used with the XY10 Plotter Control logic. The "time per step" column lists the time required for the paper to move one increment from an initial coordinate for given step size.

The PLCN REG CLEAR and PLCN MOVE DONE one-shot delays (B4-PLCN) are adjusted to these times for the plotter mechanism used. The adjustments are performed in conjunction with the diagnostic program. The program yields a typeout of the delay setting. It is merely necessary to adjust the delays until the desired delay is obtained.

Table 6-1
Increment Times

CalComp Model	Step Size	Steps/second	time per step
502	all	300	3.3 ms
518	.005 in.	200	5.0 ms
	.002 in.	450	2.2 ms
	.1 mm	200	5.0 ms
	.05 mm	400	2.5 ms
563	.010 in.	200	5.0 ms
	.005 in.	300	3.3 ms
	.1 mm	300	3.3 ms
565	all	300	3.3 ms
602	all	450/900	2.2 ms/1.1 ms
618	.005/.0025 in.	200/400	5.0 ms/2.5 ms
	.002/.001 in.	450/900	2.2 ms/1.1 ms
	.1/.05 mm	200/400	5.0 ms/2.5 ms
	.05/.025 mm	450/900	2.2 ms/1.1 ms
663	.010/.005 in.	350/700	2.9 ms/1.4 ms
	.005/.0025 in.	450/900	2.2 ms/1.1 ms
	.0025/.00125 in.	450/900	2.2 ms/1.1 ms
665	all	450/900	2.2 ms/1.1 ms

6.3 CORRECTIVE MAINTENANCE

In this section, corrective maintenance procedures for the BA10 control logic are detailed. Corrective maintenance procedures for the three options are contained in separate technical manuals and are not repeated in this section.

The BA10 control logic is constructed of highly reliable transistorized modules and standard circuits. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment downtime due to failure. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the system. Maintenance personnel should become thoroughly familiar with the theory of operation described in this manual, theory of operation of the optional equipment contained in their technical manuals, specific circuit modules described in DIGITAL Logic Handbook, the engineering drawings listed in this manual, and the location of mechanical and electrical components described in Chapter 1.

Diagnosis and remedial action for a malfunction are performed in the following phases.

a. Preliminary investigation to gather all information and to determine the mechanical and electrical security of the optional equipment and control logic.

b. System troubleshooting to isolate the malfunction to a module through the use of diagnostic program; if the malfunction is not located during the diagnostic program, signal tracing, and/or aggravation techniques may be used.

c. Module troubleshooting to locate defective components within a module.

d. Repairs to correct the cause of the malfunction.

e. Validation test to assure that the malfunction has been corrected.

f. Log entry to record pertinent data.

6.3.1 Preliminary Investigation

It is virtually impossible to outline any specific procedure for locating malfunctions within the card reader, line printer, and plotter control logic. Before beginning troubleshooting procedures, explore every possible source of information; ascertain all possible information concerning any unusual function of the system prior to the malfunction and all possible program information such as the routine in progress, the condition of the indicators, etc; search the maintenance log to determine if this type of malfunction has occurred before or if there is any cyclic history of this type of malfunction, and determine how this condition was previously corrected. When the entire control logic fails, perform a visual inspection to determine the mechanical and electrical integrity of all power sources, cables, connectors, etc. Assure that the power supplies are operational by performing the power supply checks as described under Preventive Maintenance.

6.3.2 System Troubleshooting

Do not attempt to troubleshoot the BA10 control logic without first gathering all information possible concerning the malfunction, as outlined under Preliminary Investigation.

Commence troubleshooting by repeating the operation during which the malfunction was initially observed, using the same conditions. Thoroughly check the operating conditions for proper control settings and note the operation of all indicators before and at the time of malfunction. Careful checks should be performed to assure that the system is actually at fault before continuing the corrective maintenance procedures. Loose or faulty cable connections can often give indications very similar to those caused by internal malfunctions. Faulty ground connections between pieces of equipment are a source of trouble. The optional equipment and the control logic must be properly grounded to prevent high voltage transients.

If the malfunction has been determined to lie within the control logic, but cannot be localized to a specific logic function, perform the diagnostic program procedure. When the malfunction has been isolated to a specific logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the malfunction is intermittent, a form of aggravation test should be employed to locate the malfunction.

The equipment flow charts supplied in Volume IV of the Peripheral Device Engineering Drawing Set are very useful in system troubleshooting. These charts illustrate the events that occur during normal operation and the sequence of the events. When an event does not occur at the proper moment, all possible conditions leading up to its schedule occurrence can be located on the flow chart and can be checked for normal operation. All such information can be related to individual logic elements on the block schematics by cross references on the flow diagram.

6.3.2.1 <u>CR10 Diagnostic Program</u> - The most efficient means of troubleshooting the card reader system makes use of the diagnostic program described in MAINDEC-10-D2EB-D. This routine provides a complete test of the card reader and control logic under operational conditions. In the diagnostic, tests are included to check essentially every circuit in the control logic, both with and without card motion. During the diagnostic program, a special deck of cards that contains known data is read by the card reader and the data is transferred into the central processor where it is checked under program control. A malfunction during this test will provide an indication of the possible fault.

6.3.2.2 <u>LP10 Diagnostic Program</u> - The MAINDEC-10-D2DA-D diagnostic program provides the most efficient means of troubleshooting the line printer system. This program provides a complete test of the line printer and control logic under dynamic conditions. Ideally, indications that occur in the event of a failure isolate the trouble to a functional component of a single module. Sometimes, however, the indications isolate the malfunction to a relatively large circuit cluster, portions of which are contained on a number of modules. In the latter case, the technician should employ certain troubleshooting techniques while the failing diagnostic routine is repeated continuously. These techniques are outlined in Chapter 8 of the PDP-10 Maintenance Manual.

6.3.2.3 <u>XY10 Diagnostic Program</u> - The most efficient means of troubleshooting the plotter system makes use of the diagnostic program described in MAINDEC-10-D2FA-D. Many plotters can be used in a plotter system. These vary as to speed of operation; therefore, various delays are incorporated into the plotter control logic to compensate for the differences. When running the diagnostic program, the user must specify the plotter model used by setting the console data switches. The program then proceeds to check certain gates and delays in the control logic. In addition, a regular pattern, in which any irregularities can easily be detected, is plotted.

6.3.2.4 Signal Tracing - If a malfunction has been isolated to a specific logic element, program the central processor to repeat instructions such that all functions of that logic element are utilized. If the central processor cannot be used for the required test, control flip-flops or register flip-flops can be cleared or set manually by momentarily placing a ground to the appropriate flip-flop output terminal. Under these conditions, use the oscilloscope to trace signal flow through the suspected logic element. The oscilloscope sweep may be synchronized with card reader control signals by connecting the trigger input of the oscilloscope to the appropriate module terminal. Trace output signals from the connector to its final destination. The signal-tracing method can be used to determine with certainty the quality of pulse amplitude, duration, rise time, and the correct timing sequence of the signal. If an intermittent malfunction occurs, signal tracing should be combined with an appropriate form of aggravation test.

6.3.2.5 Intermittent Malfunctions - Intermittent malfunctions caused by poor wiring connections can often be revealed by tapping the modules while running a repetitive routine, such as the diagnostic program. Wiping the handle of a screwdriver across the back of a suspect row of modules is another useful technique. By repeatedly starting the program and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector, the module connector for wear, misalignment, and malfunction, and the module for a poor connection.

6.3.3 Module Troubleshooting

The procedure followed for troubleshooting and correcting the cause of a malfunction within modules and power supplies depends upon the downtime limitations. Where downtime must be kept at a minimum, it is suggested that a replacement parts program be adapted to maintain at least one spare module or power supply which can be inserted into the cabinet when system troubleshooting procedures have traced the fault to a particular component. A list of modules and power supplies can be compiled from the engineering drawings listed in this manual.

CAUTION

The primary ac power is present in the BA10 power control even though the logic power is turned off.

6.3.3.1 On-Line Dynamic Tests - Where downtime is not critical, the spare parts list can be reduced and signal tracing techniques can be utilized to troubleshoot modules. This type of procedure is performed as follows: remove suspected module; insert module extender into the module connector; insert suspected module into the module extender; and perform signal tracing procedure with an oscilloscope while the equipment is operated in a routine which exercises the module circuits.

6.3.4 Repair

For minimum system downtime, replace defective modules and/or system components that have been located during system troubleshooting procedures. When system downtime is not critical and module troubleshooting procedures are employed, perform repairs using good shop practices. Remove defective components by cutting the component leads and removing the leads from the printed board with a solder sucker. When soldering semiconductor devices, use a heat sink and the smallest soldering iron adequate for the work. Perform all soldering operations in the shortest possible time to prevent damage to components. Replace defective components with components of equal or greater quality or closer tolerance.

6.3.5 Validation Test

Following the replacement of any electrical component, a test should be performed to assure the correction of the malfunction and to make necessary adjustments. This test should be taken from the preventive maintenance procedure most applicable to the portion of the system in which the malfunction was located. Normally, the diagnostic program serves this purpose.

When time permits, it is suggested that the entire preventive maintenance task be performed as a validation test. The reasons for this are as follows: other components may be marginal; while the equipment is down and available, preventive maintenance can be performed and need not be rescheduled for the normal period.

6.3.6 Log Entry

Corrective maintenance procedures are not completed until they are recorded in the maintenance log. Record all data indicating the symptoms given by the malfunction, the method of malfunction location, and any other information which would be helpful in maintaining the equipment in the future.

CHAPTER 7

ENGINEERING DRAWINGS

This chapter contains a list of the engineering drawings supplied with the BA10 system. The engineering drawings are located in Volume IV of the Peripheral Device Engineering Drawing Set. Should any discrepancy exist between the drawings in this manual and those supplied with the equipment, assume the latter drawings to be correct. Module, power supply, and power control panel schematics are contained in Volume III of the PDP-10 Maintenance Manual.

Refer to Tables 7-1, 7-2, 7-3 and 7-4 for the associated drawing numbers and titles.

7.1 DRAWING TERMINOLOGY

The engineering drawing numbers for the BA10 system contain six fields of information, separated by hyphens. A typical example of a drawing number is shown below:

D BS CR10 0 IOCB B

D — Drawing Size
BS — Drawing Code
CR10 — Option Number
0 — Manufacturing Variation
IOCB — Drawing Title Abbreviation
B — Revision Indicator

The drawing size, option number, and the drawing title abbreviation are self-explanatory. The manufacturing variation letter identifies the variation that the drawings reflect. For example: 0 reflects drawings applicable to all variations; A reflects the 60 Hz equipment; etc. The drawing code identifies the type of drawing. A list of the common drawing codes follows.

BS - Block Schematic or Logic Diagram
CL - Cable List
CS - Circuit Schematic
FD - Flow Diagram
IC - Interconnection Drawing
KS - Key Sheet
MU - Module Utilization
RS - Replacement Schematic
SD - System Diagram
PL - Parts List

Signal names on the drawings provide a cross reference to the drawing where the signal originates. Two typical examples of signal names are shown below.

Example 1:

CRST DATA MISSED (1)

Descriptive Signal Name

Drawing Title Abbreviation
(CARD READER STATUS)

Example 2:

— CRCN READ CARD

Descriptive Signal Name

Drawing Title Abbreviation
(CARD READER CONTROL LOGIC)

Signal Active when in the FALSE condition

7.2 LOGIC SYMBOLS

The DEC standard logic symbols are shown at the input of most circuits to specify enabling condition required to produce a desired output. These symbols represent either standard DEC logic levels or standard DEC pulses. All pulses in the BA10 are R-series pulses.

Typical engineering symbols are shown in Figure 7-1.

7.3 LOGIC LEVELS

With the exception of card reader and plotter interface signals, all logic signals are either standard DEC logic levels or standard DEC pulses. A standard DEC logic level is either a ground (0 to -0.5V) or -3V (-2.5 to -4.0V). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond (—◇) indicates that the signal is a level and that ground represents assertion; a solid diamond (——◆) indicates that the signal is a level and that -3V represents assertion.

All logic levels applied to the conditioning-level inputs of capacitor-diode gates must be present either 100 or 400 ns (depending on the module used) before an input triggering pulse is applied to the gate.

The standard DEC negative pulse is indicated by a solid triangle (——▶) and goes from ground (0 to -0.5) to -3V (-2.5 to -4.0V). The standard DEC positive pulse, indicated by an open triangle (——▷), goes from -3V to ground. The width of the standard pulses used in this equipment is either 100 or 400 ns, depending on the module and application.

Occasionally, the trailing edge transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (——◆▷) is drawn to indicate this fact. The triangle is drawn solid if the negative (ground to -3V) transition triggers circuit action. The shading of the diamond is opposite that of the triangle to indicate triggering on the trailing edge.

Any other signal is nonstandard and is indicated by an arrowhead (——>) pointing in the direction of signal flow.

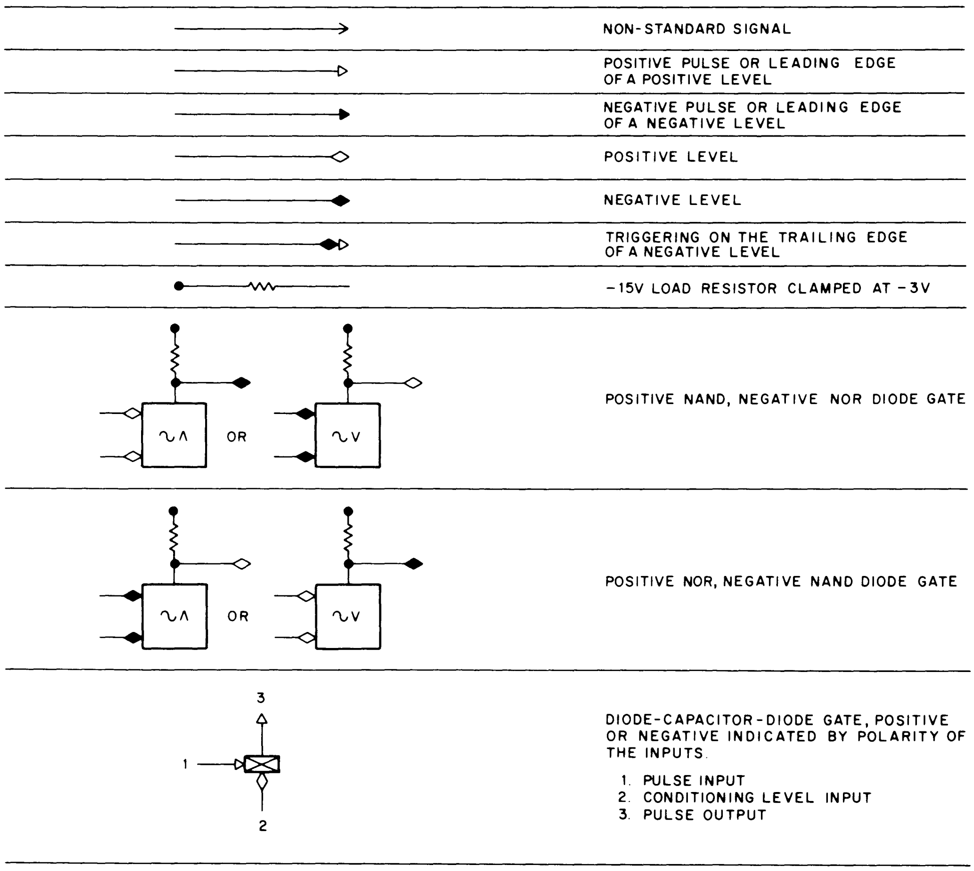
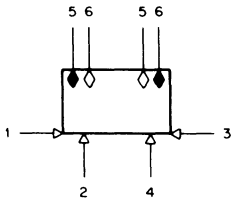


Figure 7-1 DEC Standard Logic Symbols



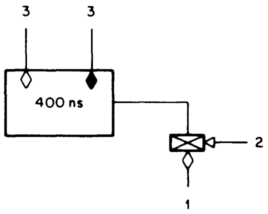


Figure 7-1 DEC Standard Logic Symbols (Cont)

7.4 FLIP CHIP PULSES

FLIP CHIP circuit operation in the card reader system uses the DEC R-series pulses. The pulse produced by the R-series modules starts at -3V, goes to ground (-0.2V) for 100 or 400 ns, then returns to -3V. This pulse is idealized in Figure 7-2.

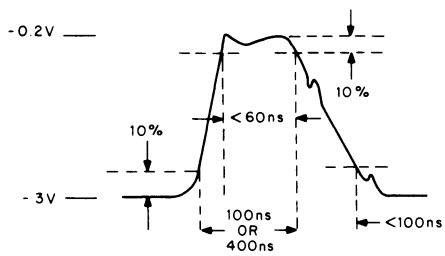


Figure 7-2 R-Series Pulse

7.5 ENGINEERING DRAWING LISTS

The following tables list the BA10 Engineering drawings contained in Volume IV of the Peripheral Device Engineering Drawing Set.

Table 7-1
BA10 Engineering Drawings

Drawing Number	Title	Revision
D-IC-BA10-0-AC	Wiring AC Power 50-60 Hz	
D-BS-BA10-0-IOB	Interface	
D-BS-BA10-0-IOCA	I/O Bus Control	
D-MU-BA10-0-MU	Module Utilization	

Table 7-2
CR10 Engineering Drawings

Drawing Number	Title	Revision
D-BS-CR10-0-CRBF	Card Reader Buffer	
D-BS-CR10-0-CRBR	Card Reader Buffer Register	
D-BS-CR10-0-CRCN	Card Reader Control Logic	A
D-BS-CR10-0-CRST	Card Reader Status	
D-BS-CR10-0-IOCB	I/O Control	
D-CL-CR10-0-CRCL	Interface Indicator Cable List	
D-FD-CR10-0-CRFD	CR10 Card Reader Flow Diagram	

Table 7-3
LP10 Engineering Drawings

Drawing Number	Title	Revision
D-BS-LP10-0-IOCC	I/O Bus Control	
D-BS-LP10-0-LPBF	Line Printer Buffer	
D-BS-LP10-0-LPCC	Line Printer Column Counter	
D-BS-LP10-0-LPCN	Line Printer Control	
D-BS-LP10-0-LPDA	Line Printer Data	
D-BS-LP10-0-LPI	Line Printer Interface	

Table 7-3 (Cont)
LP-10 Engineering Drawings

Drawing Number	Title	Revision
D-BS-LP10-0-LPIN	Line Printer Indicators	
D-BS-LP10-0-LPST	Line Printer Status	
D-CL-LP10-0-LPCL	Interface Indicator Cable List	
D-FD-LP10-0-LPFD	LP10 Line Printer Flow Diagram	
D-FD-LP10-0-LPF1	LP10 Line Printer Flow Diagram	
D-FD-LP10-0-LPF2	LP10 Line Printer Flow Diagram	

Table 7-4
XY10 Engineering Drawings

Drawing Number	Title	Revision
D-BS-XY10-0-CONT (2 sheets)	XY10 Plotter Control	
D-BS-XY10-IOB	Interface	
D-BS-BA10-0-IOCA	I/O Bus Control	
D-BS-XY10-0-IOCD	I/O Control	
D-BS-XY10-0-PLCN	CalComp Plotter Interface	A
D-BS-XY10-0-PLST	Plotter Status	
D-FD-XY10-0-PLFD	XY10 Plotter Flow Diagram	

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