RJP04 moving head disk subsystem maintenance manual

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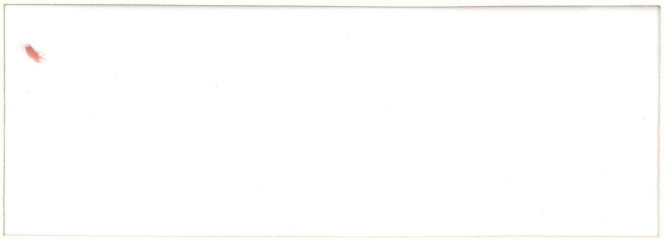

DEC-11-HRJPA-B-D

RJP04 moving head disk subsystem maintenance manual

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CHAPTER 1
SYSTEM AND PHYSICAL DESCRIPTION

1.1 GENERAL

This manual describes the RJP04 Moving Head Disk subsystem manufactured by Digital Equipment Corporation. The RJP04 subsystem consists of an RH11 Device Controller and from one to eight RP04 Disk Drives. The RH11 interfaces with any PDP-11 processor via the Unibus and controls one to eight RP04 Drives.

1.1.1 Scope

This manual is designed to provide Digital Field Service and customer maintenance personnel with sufficient installation, operation, and servicing information to install and maintain the RH11. Because the RH11 is used with the RP04 Drives, a description of the RP04 is included in this manual. Detailed information on the RP04 Drive can be found in the *RP04 Device Control Logic Maintenance Manual* (DEC-00-HRP4M-A-D).

1.1.2 Related Documentation

Table 1-1 lists related documentation that supplements the information in this manual.

Table 1-1
Related Documentation

Title	Document Number
PDP-11 Peripherals Handbook	112.00973.2908
RP04 Device Control Logic Maintenance Manual	DEC-00-HRP4M-A-D
Digital Logic Handbook	058.00173.2505

1.2 DISK FILE SYSTEM

Figure 1-1 shows the major components of a PDP-11 system containing an RH11 Device Controller and one to eight drives. The processor and memory components can be any of several types in the PDP-11 family since all of these components are equipped with the standard Unibus interface. This manual describes the RH11 Device Controller as it interfaces with the RP04 Drives.

1.2.1 Unibus

The Unibus provides the interface between the processor, memory, and the RH11 Controller. All data transfers between memory and the RH11 are accomplished via the NPR data transfer facilities of the Unibus.

The RH11 contains two Unibus ports: one designated as a control port and the second as a data port. Data may be transferred through either port using the NPR transfer facility. For normal operation, with memory connected to Unibus A as shown in Figure 1-1, the data port is not used, and the control port serves for both control and data transfers. When memory is connected to Unibus B, a programmable port select bit can cause data to be routed through the data port. Figure 1-2 shows a system configuration using multiport memory and both the control port and data port.

A third configuration which may be employed occurs in a multiprocessor environment. Figure 1-3 shows the RH11 system interfaced to a Unichannel 15 system and a remote processor. In this type of configuration, the PDP-15 can direct the PDP-11 to transfer data from common memory to the disk. The data could then be transferred to another memory bank associated with the remote processor on Unibus B.

Figure 1-4 shows a dual controller configuration with a single processor; Figure 1-5 shows a dual controller configuration with two processors.

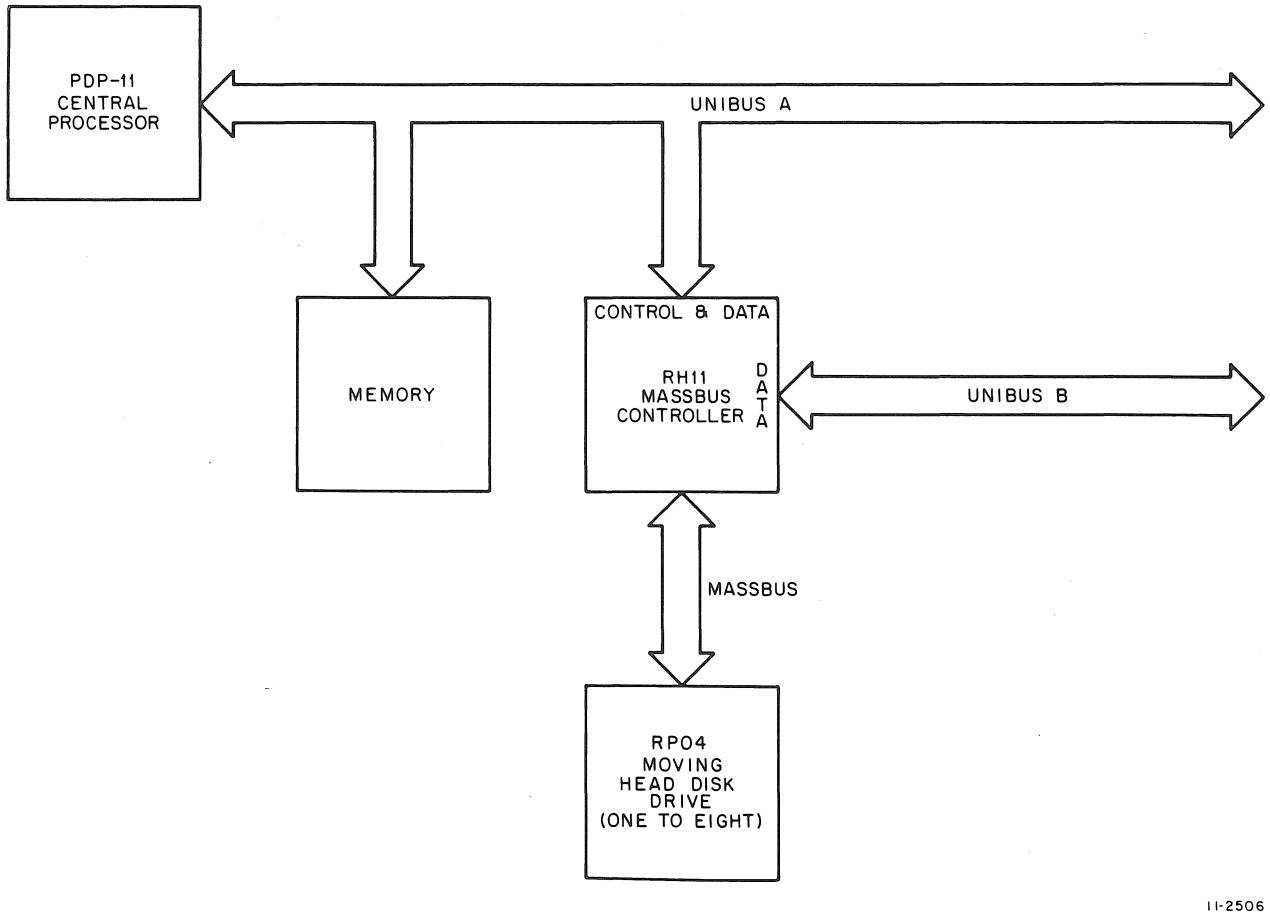


Figure 1-1 RH11 Simplified System Diagram

1.2.2 Massbus

Massbus is the name of the interface between the RH11 Controller and the RP04 Drive. The Massbus provides a parallel data path between the RH11 and the disk devices, and has a total maximum external cable length of 60 ft between drives. Normally, a 25-ft cable connects the RH11 to the first RP04 and 2-ft cables connect one RP04 to the next. The Massbus comprises two sections: an asynchronous control bus and a synchronous data bus for high-speed data transmission.

The purpose of the asynchronous control bus is to:

1. Transmit commands and information from the controller to the drive for the purpose of reading or writing drive registers
2. Notify the controller when an Attention condition exists in one or more drives (refer to Chapter 3).
3. Transmit status information from the drive to the controller, and
4. Provide a master reset to all drives from the controller.

The purpose of the synchronous data bus is to transmit blocks of data at high speed between the controller and drives and to control the initiation and termination of block transmissions.

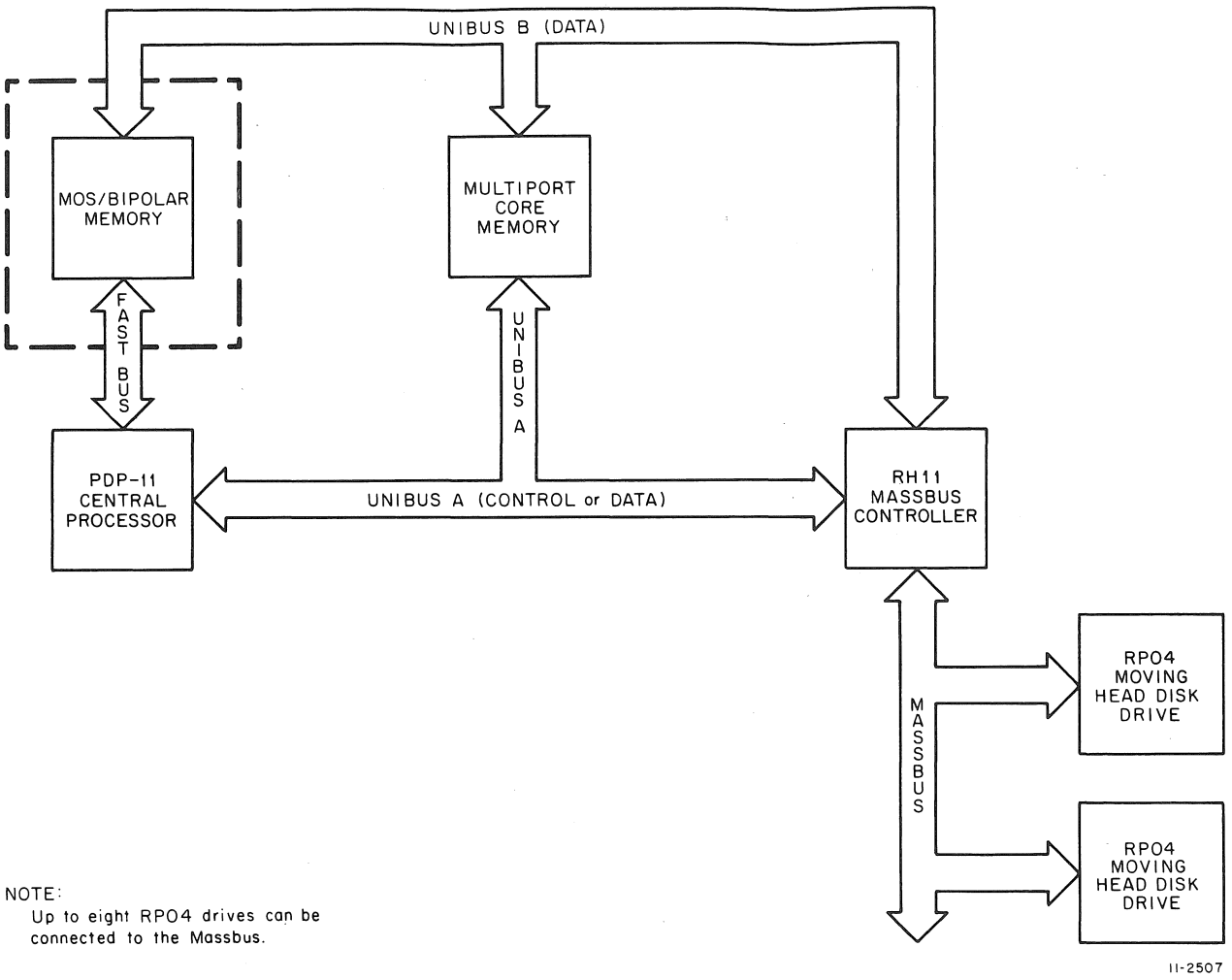


Figure 1-2 RH11 Multiport System

1.3 RH11 CONTROLLER

The RH11 Controller, in conjunction with the RP04, provides an extremely fast and reliable mass storage system that can be employed in timesharing or real-time data storage applications. The following major functions are performed by the RH11:

1. Interfaces with one or two Unibus cables
2. Communicates directly with the main memory to fetch and store data
3. Communicates with the central processor to receive commands, provides error and status information, and generates interrupts
4. Interfaces with one to eight drives.

The RH11 is divided into two major functional groups: the register and control path and the DMA (direct memory access) data path (Figure 1-6).

The register and control path allows the program to read from and/or write into any register contained in the RH11 and the selected RP04 Drive. There are a total of 4 registers in the RH11, 15 registers in each drive, and 1 shared register that is partially contained in the RH11 and partially contained in the selected drive.

The DMA data path functionally consists of a 66-word by 18-bit first-in, first-out memory and associated control logic. The major function of this memory (hereafter referred to as the Silo) is to buffer data in order to compensate for fluctuations in NPR latency time on the Unibus.

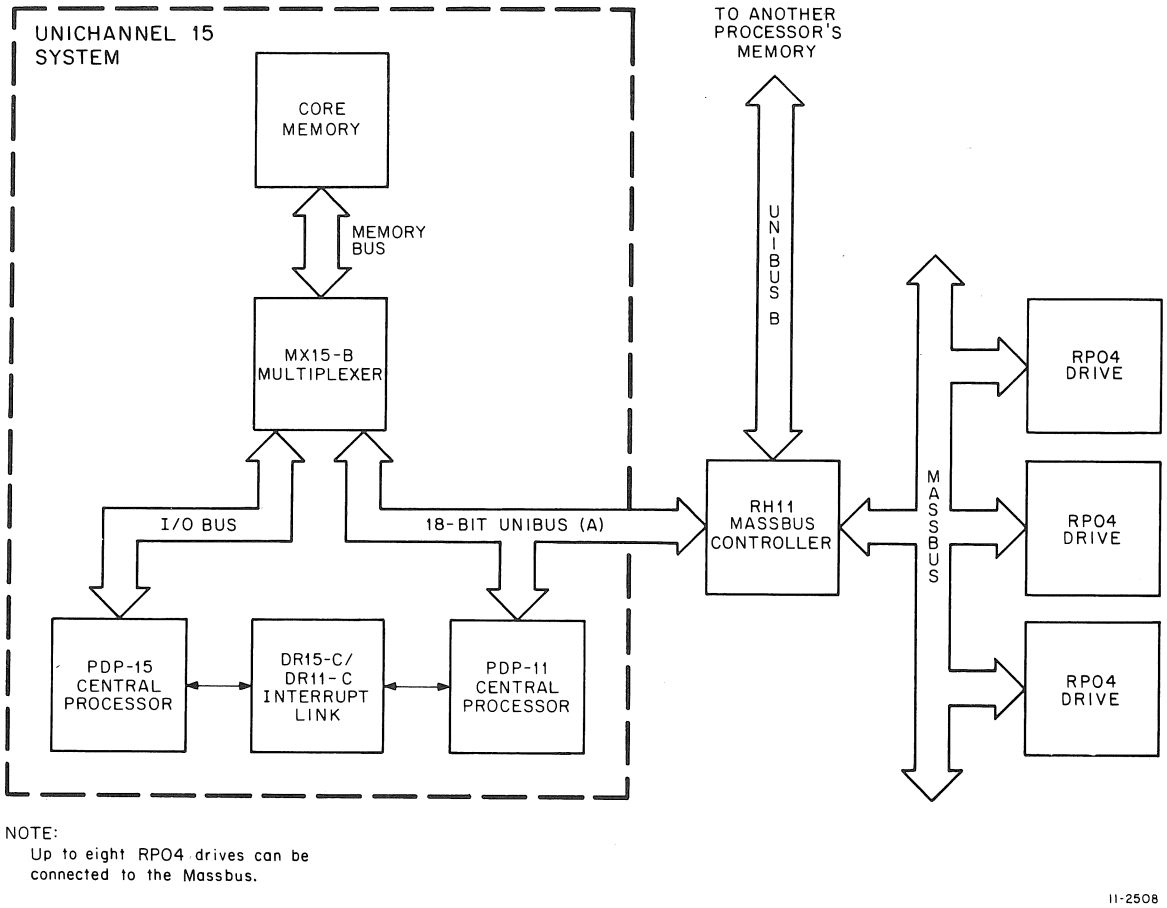


Figure 1-3 RH11 Combined With Unichannel 15 System

1.3.1 Register and Control Path

When a PDP-11 instruction addresses the RH11 to read or write any device register in the RH11 or in the drive, a Unibus cycle is initiated and this data is routed to or from the RH11 (refer to Chapter 3 for a detailed description of the registers). If the register to be addressed is local (contained within the RH11), the register control logic immediately gates the data to or from the appropriate register. If the register to be accessed is remote (contained in one of the RP04 Drives), the register control logic initiates a Massbus control bus cycle. Accesses to registers in a drive via the control bus do not interfere with DMA data transfers that may be going on at the same time. Local RH11 registers specify parameters such as bus address and word count while the drive registers specify parameters such as desired disk address, status information, etc.

1.3.2 DMA Data Path

The DMA data path functionally consists of the Massbus data bus, a Silo memory, and the Unibus NPR logic. The Silo memory compensates for fluctuations in NPR latency times by buffering data between the Unibus and Massbus data bus during DMA transfers.

Figure 1-6 shows a simplified block diagram of the DMA data path. A single Unibus configuration is shown with Unibus A serving as both the control port and the data port.

The three data transfer commands that can be performed by the RH11 and RP04 are Write, Read, and Write-Check. Before these data transfers occur, the program specifies a memory address (MA), a cylinder address (CA), a desired sector/track address (DA), and a word count (WC). The memory address represents the starting memory location which the data will be written into or read from. This address occupies the 16 bits of the RPBA register and bits 9 and 8 of the RPCS1 register (Chapter 3). The state of the PSEL bit in the RPCS1 register determines over which Unibus the transfer will take place.

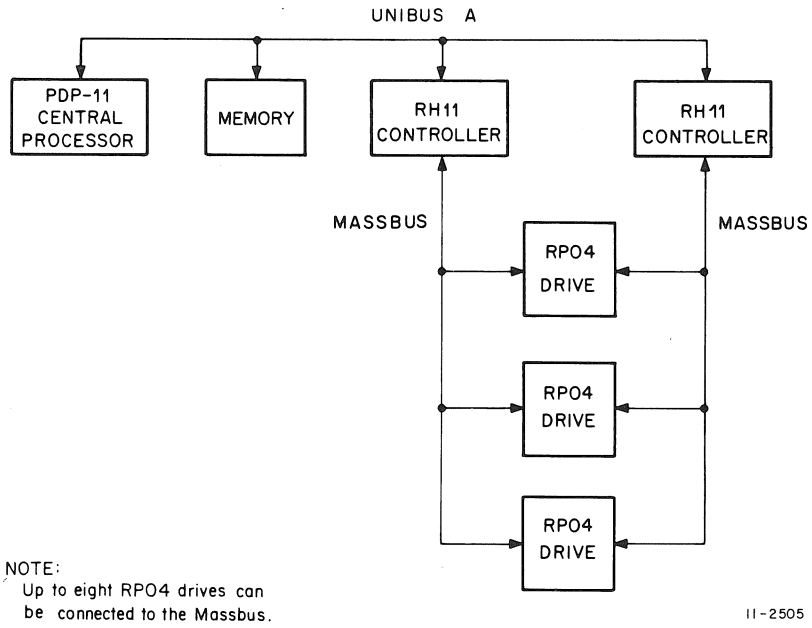


Figure 1-4 Dual Controller Option (With One Processor)

The desired cylinder address is the cylinder address where the head is to be positioned. This address occupies bits 09 through 00 in the RPDC register. The desired sector/track address is the disk sector and track address and represents the starting location on the disk surface where the data is to be written or read from. This address is located in the RPDA register.

The word count is a count of the number of words to be transferred to or from the disk. The negative (2's complement) of this number is loaded in the Word Count (RPWC) register and is incremented toward 0 for each data word transferred into or from memory. At the normal completion of a transfer, the appropriate number of words have been transferred, and the RPWC register contains 0.

1.3.2.1 Write Operation – In a write operation, the data words are transferred from memory to the disk via the RH11. The data path functionally consists of the Unibus NPR logic, the Silo memory, and the Massbus data bus. The program initially selects a drive and loads the bus address, word count, and desired addresses (sector, track, and cylinder). The program then loads a Write command code (with the GO bit set) into the RPCS1 Control and Status register. Unibus NPR cycles are initiated by the RH11, and the data words from memory are transferred to the input buffer (IBUF) of the Silo.

For each data word transferred, the word count is incremented by 1 and the bus address is incremented by 2. The data words are clocked into and "bubble" through the Silo. When the first data word reaches the top, it is automatically clocked into the Silo output buffer (OBUF). When the Silo is filled and a word is in OBUF, the RH11 asserts the RUN signal, which signals the drive to begin writing data on the disk.

After the RUN signal is asserted, the disk begins searching for the rotational position corresponding to the value in the Desired Address (RPDA) register. When this rotational position is found, the disk begins sending SCLK (sync clock) pulses to the RH11 and starts receiving data words from the RH11 via the Massbus data bus.

At the end of a transfer of each sector, the disk asserts the EBL (end of block) pulse and looks at the RUN signal. If the RUN signal is still asserted, the disk continues to receive the next sector of data and writes it on the disk surface. If the RUN signal is negated at the end of the EBL pulse, the drive disconnects from the Massbus data bus.

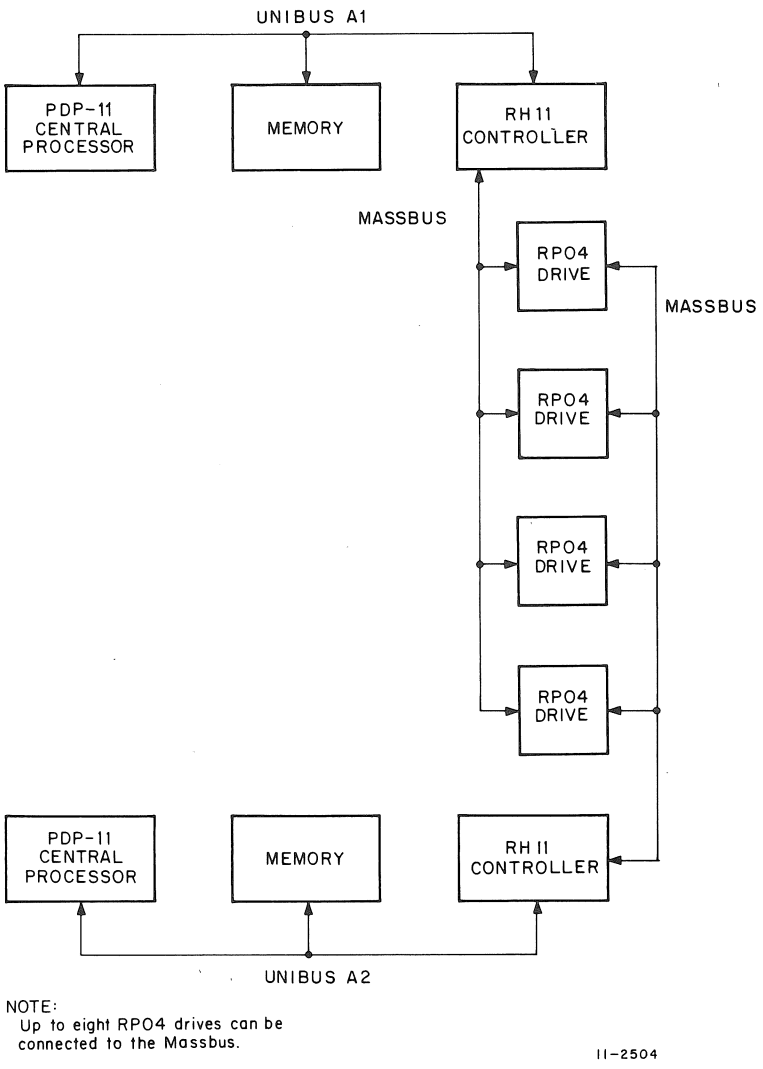


Figure 1-5 Dual Controller Option (With Dual Processor)

When less than a sector is transferred, the remainder of the sector will be written with 0s. The reason for this is that the RH11 negates the RUN signal at word count overflow; however, the disk does not respond to the negation of RUN until the end of EBL time, and therefore, the RH11 sends 0s on the Massbus data bus when word count overflow occurs.

Note that during a write operation, the Silo is filled or word count overflow occurs before the RH11 signals the drive to begin writing.

1.3.2.2 **Read Operation** – In a read operation, data words are transferred from the RP04 Drive to memory via the RH11 Controller. The data path functionally consists of the Massbus data bus, the Silo memory, and the Unibus NPR logic. The program initially selects a drive and loads the bus address, word count, and desired sector, track, and cylinder addresses. The program then loads a Read command code (with the GO bit set) into the RPCS1 Control and Status register (Chapter 3). The RH11 immediately asserts the RUN line. The RP04 Drive begins searching for the rotational position corresponding to the value in the Desired Address (RPDA) register. When the position is found, the disk begins sendig SCLK pulses to the RH11, along with the data words. The data is clocked into IBUF and is then gated into the Silo.

When the first data word has "bubbled" to the top of the Silo and has been clocked into OBUF, Unibus NPR cycles are initiated. Each time a word is transferred to the Unibus, the word count stored in the Word Count (RPWC) register is incremented by 1 and the bus address is incremented by 2.

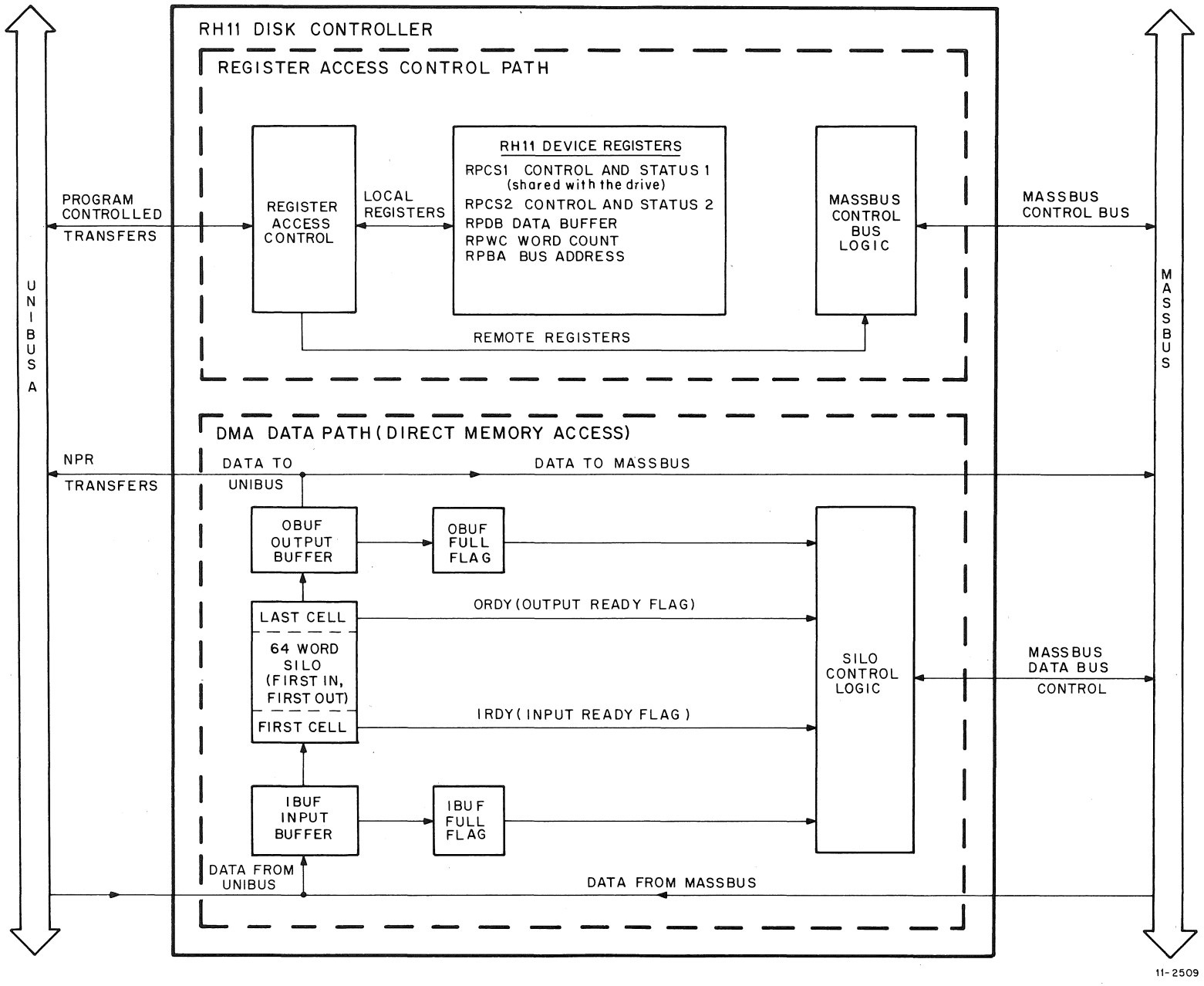


Figure 1-6 RH11 Simplified Data Path Diagram

NOTE

The RH11 may perform either single-cycle or back-to-back memory references per NPR request.

At the end of each sector, the drive asserts the EBL pulse and looks at the RUN signal. If the RUN signal is still asserted, the disk continues sending the next sector of data to the RH11 via the Massbus data bus. If the RUN signal is negated at the end of the EBL pulse, the disk disconnects from the Massbus data bus and the transfer is terminated.

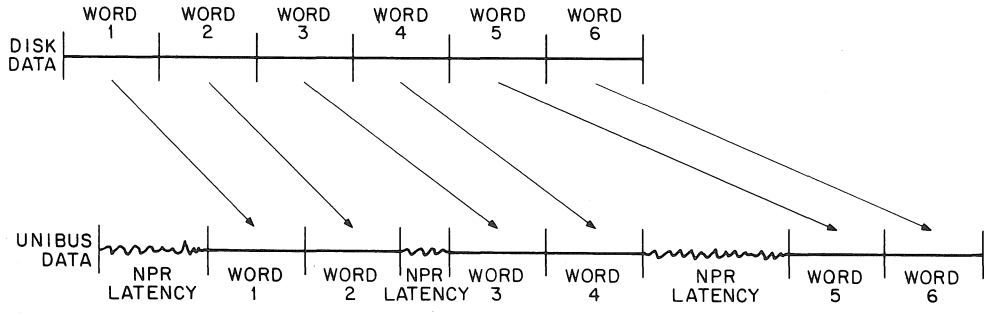
If the value initially stored in the RPWC register is less than the number of words in a full sector, the remaining words in the sector will be disregarded by the RH11. After word count overflow occurs, the RH11 stops performing Unibus data transfers and waits for the next EBL pulse. When EBL is received from the disk, the RH11 transitions to the ready state.

1.3.2.3 Write-Check Data Transfer – The third type of transfer is a Write-Check and is initiated when a Write-Check function is specified in RPCS1 and the GO bit in this register is set. In this operation, a block of data which has previously been written onto the disk is read from the disk. The data is compared to the data in memory originally used to write on the disk. The comparison is accomplished by Exclusive OR gates, and if any of the bits fail to compare, a Write-Check Error occurs. This method allows automatic verification that the data on the disk surface agrees with the contents of memory.

1.3.2.4 Data Transfer Rates – The data transfer rate from the drive is determined by a clock in the drive. The RP04 has an 18-bit format and a 16-bit format. The basic data transfer rate for the 18-bit format is a burst rate of 2.79 μs per word. The basic data rate for the 16-bit format is a burst rate of 2.48 μs per word. The Unibus data transfer rate depends on NPR latency time and memory cycle time. Figure 1-7 shows the data transfer sequence for a read operation, and Figure 1-8 shows the sequence for a write operation. Figure 1-9 shows the data transfer sequence for a read header and data command and Figure 1-10 shows the data transfer sequence for a write header and data command. For lengthy data transfers, the average Unibus data transfer rate is equal to the average disk data transfer rate. Statistical fluctuations in NPR latency times are absorbed by the buffering in the Silo.

NOTE

By inserting a single-cycle jumper in the RH11, it is possible to perform one memory cycle for each NPR. If the jumper is left out, the RH11 will perform back-to-back memory cycles before releasing the Unibus, unless only one word remains to be transferred.



NOTE:
Average data transfer rate is 2.96 μsec for the 16-bit format (3.25 μsec for the 18-bit format). This rate includes data and header.

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Figure 1-7 Read Command Data Transfer

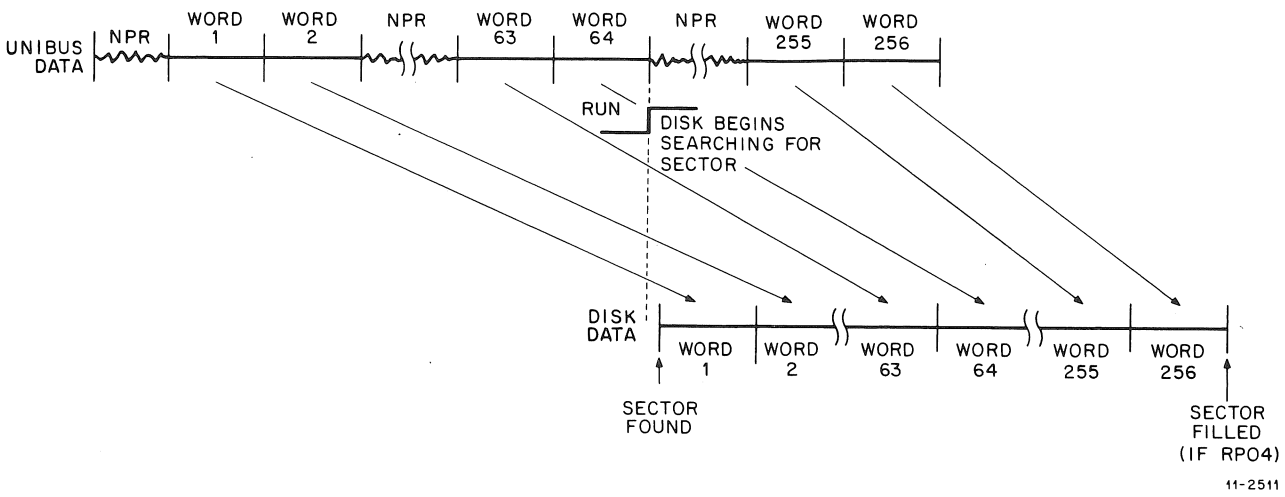


Figure 1-8 Write Data Transfer Sequence

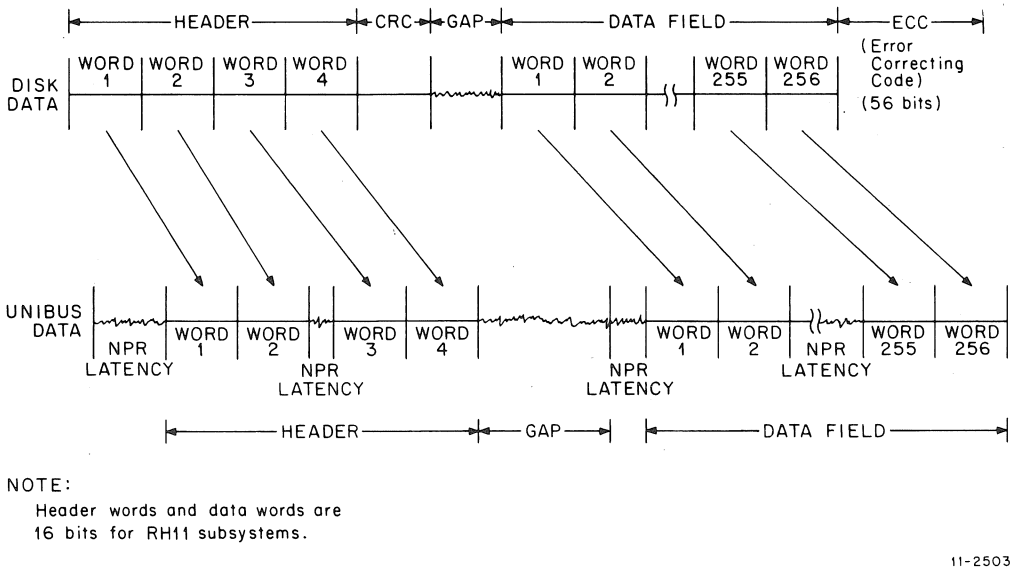


Figure 1-9 Read Header and Data Command Transfer

1.4 RP04 DRIVE

The RP04 Drive is a large capacity, high performance, direct access disk file which will accommodate one removable disk pack of the IBM 3336 type. The disk pack contains 10 magnetic disks, each 14 inches in diameter. The middle surface is prerecorded with positioning signal information for servo tracking and is a read-only surface. This leaves 19 surfaces available for recording. The 19 surfaces can store approximately 44 million 16-bit words or approximately 40 million 18-bit words. Total subsystem capacity using eight RP04 disk files is 352×10^6 16-bit words. The 16-bit format contains 22 sectors per track while the 18-bit format contains 20 sectors per track.

There is one head per surface which enables the RP04 to store or retrieve information at any location on a rotating disk pack. Information is recorded on the lower and upper surface of each disk (except for the servo surface at the middle of the disk pack).

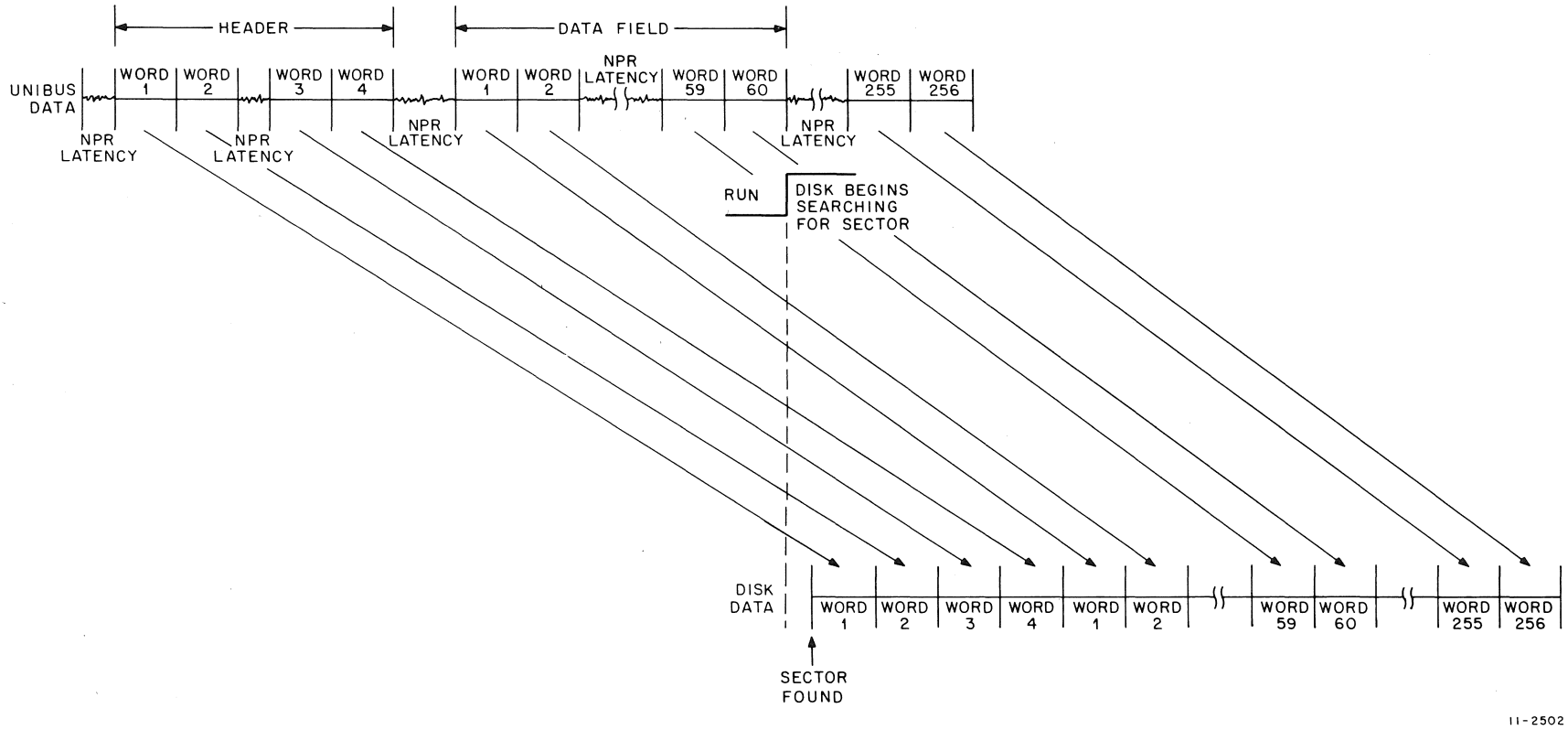


Figure 1-10 Write Header and Data Command Transfer (Pack Format Command)

With the dual controller option, the drive can be connected to two RH11 controllers, allowing access to the drive from two separate computer systems or from one computer system via two separate paths.

The RP04 drive performs the following functions.

1. Records and plays back data in two format modes
2. Calculates error correction information
3. Generates gaps and synchronization marks on the recording medium
4. Provides clock signals to synchronize data transmission between drive and controller
5. Maintains error and status indicators and generates an Attention signal when exceptional conditions occur
6. Locates data by address
7. Performs dual controller arbitration
8. Provides mechanisms for maintenance and diagnostic testing.

1.5 RJP04 SYSTEM SPECIFICATIONS

This paragraph defines the parameters of the RH11 Massbus Controller and the RP04 Drive.

1.5.1 Unibus NPR Latency

NPR latency time is from the assertion of a Unibus NPR by the RH11 until the RH11 takes control of the Unibus (asserts BBSY). The acceptable average NPR latency time is calculated as follows:

> Average data word time of the disk minus time to transfer one word to or from memory plus the time for the RH11 to issue the next NPR.

If the jumper in the RH11 is cut for two memory cycles per NPR, average acceptable NPR latency time is doubled, and is calculated as follows:

> Twice the average data word time of the disk minus time to transfer two words to or from memory plus the time for the RH11 to issue the next NPR. For example, if the average data word time of the disk is 2.48 μs (16-bit format) and the time to transfer two words to or from memory is 2 μs plus 0.2 μs to request the Unibus again, then the average acceptable NPR latency = (2 X 2.48) μs - (2 + 0.2) μs = 2.94 μs.

If the actual NPR latency consistently exceeds the acceptable average NPR latency during a lengthy read or write operation, the 66 words of data buffering in the RH11 (Silo plus IBUF and OBUF) will eventually be insufficient. This condition is signaled by a Data Late Error (DLT) condition.

1.5.2 Data Format

Data words are recorded on the disk in 16-bit format. Normally, for the RJP04 system, only 16 bits per word are transmitted between the controller and memory. To accomplish an 18-bit transfer via the Unibus, the Bus PA and Bus PB lines may be used as data bits BUS D16 and BUS D17, respectively. Both Unibus A and Unibus B are jumper selectable in the RH11 for this 18-bit mode. When a Unibus is not selected for 18-bit mode, the RH11, when reading, sends logical 0s on the Unibus PA and Unibus PB lines, and, when writing, sends 0s to the disk in bits 16 and 17 of the Massbus data bus.

In addition, the RH11 checks parity error conditions on the Unibus in the normal 16-bit mode when performing a write operation. A PDP-11 memory parity error is indicated when Unibus PA is negated and Unibus PB is asserted during an NPR data transfer from memory.

1.5.3 Error Correcting Code (ECC)

The RP04 contains Error Correcting Code logic which will generate, detect, and correct an error by reconstructing a portion of the data (limited by the capability of the selected code). The ECC employed in the RP04 is called a Burst Error Correcting Code.

Within the fixed specified code word length, the Burst Error Correcting Code will correct an error which must fall within the specified length of the burst (11-bit burst). The actual location of that burst within the data field is immaterial to the operation of the ECC logic. Any errors outside the specified burst length will be detected but not corrected.

The RP04 logic will find the burst within which the read error is included and determine the actual location of the burst within the data field. The ECC Pattern register contains the actual error burst and the ECC Position register contains the address for determining the actual location of the error burst within the data field. Both registers are located in the RP04. The actual correction of the data field will be done by the processor under software control.

During a read, write, or write-check operation, both data errors and unusual drive conditions signal the RH11 via the Exception (EXC) line, which sets the TRE (Transfer Error) bit after the read/write operation is complete. During non-data transfer operations, the drive can signal unusual conditions or completion of non-data transfer operations by the Attention (ATTN) line. This line is shared by all drives connected to the RH11.

During a read, write, or write-check operation, errors in the RH11 (such as DLT, Unibus parity error, etc.) also set the TRE bit and cause the operation to be aborted.

Interrupts are generated as a result of the ATTN line being asserted or by completion of a read or write data transfer.

1.5.4 RH11 Massbus Controller Specifications

Mechanical

Consists of a double hex-height system unit, which will mount in a BA11-FA, BA11-FB, BA11-BA, or BA11-BB mounting box (not supplied). Module usage is as follows:

RH11 Logic
2 hex-height, 2 double-height modules
Massbus Controller Transceivers
3 double-height modules
Unibus Cable Slots
4 double-height cable slots
Power Fail
2 single-height modules

Electrical

Power Requirements (RH11)
+5.0 ± 0.25 Vdc at 16.0 A max
−15.0 ± 1.5 Vdc at 0.58 A max

Logic Voltage
H ≈ +3 V, L ≈ 0 V

Environmental

Temperature
32° – 122° F (0° – 50° C) Class C

Relative Humidity
8% to 90%, no condensation

Vibration Shock
1.89 g rms, 10–300 Hz
20 g, half sine, 30 ms duration, any plane

Data Transfers Memory/Controller

Accomplished via the NPR facility of the Unibus. Data can be transferred on either of two Unibuses (program selected). An 18-bit data path is optional (uses Unibus PA and Unibus PB lines as data).

Data Transfer Controller/Disk

All controller/disk transfers are accomplished as 18-bit parallel words over the synchronous section of the Massbus.

Data Rates

RP04 (16-Bit Format)
2.48 μs/word (burst rate)
2.96 μs/word (average rate for multiple sector transfers)

RP04 (18-Bit Format)
2.79 μs/word (burst rate)
3.25 μs/word (average rate for multiple sector transfers)

Number of Drives Per Controller

Can handle up to eight RP04 Drives

Maximum Controller/Drive Cable Length

40-foot individual round Massbus cable (external)
60-foot total round Massbus cable (external)

1.5.5 RP04 Drive Specifications

The RP04 Drive is a high performance, direct access, single head per surface drive which enables a data processing system to store or retrieve information at any location on a rotating disk pack. The RP04 is connected to the RH11 Controller via the Massbus interface.

Features

Error detection and correction capability hardware which is permanently installed

Two sector formats available:
20 sectors per data track (256 18-bit words per data field of each sector)
22 sectors per data track (256 16-bit words per data field of each sector)

Remote stand-by operation

Options

Dual controller capability

Mechanical Specifications

Mounting

Mounted in a free-standing cabinet, approximately 40 inches high, 31 inches wide, and 32 inches deep. The width includes a 10-inch chassis attached to the side of the basic cabinet.

Weight

600 lb

Electrical Specifications

Power Requirements

dc – None

ac – 208/230 Vac ± 10%, 3-phase, 60 Hz ± 1%, or 380 Vac ± 10%, star with neutral, 50 Hz ± 1%, 3-phase – options include 240/408/220/420 Vac.

Starting current surge – less than 30 A

Environmental Specifications

Operating Temperature Range

60° F min, 90° F max

Non-operating Temperature Range

50° F min, 110° F max

Drive Cooling (Internal)

Forced Air

Maximum Wet Bulb Temperature

78° F

Heat Dissipation

7000 Btu/hour nominal
5500 Btu/hour nominal

Relative Humidity

20% min, 80% max (no condensation)

Vibration

0.25 g from 50 to 500 Hz

Shock

Operating: 3 g for 10 ms, 3 pulses in vertical direction only

Shipping: 6 g for 30 ms, 3 pulses in vertical direction only

Maintainability

The basic maintainability philosophy for the RP04 Drive is to provide on-line diagnostic capability. In addition to software diagnostics, an off-line hardware exerciser will also be provided.

Read/Write

Number of Read/Write Heads

19 (plus 1 read head for the servo)

Cylinders Per Disk Pack

411

Tracks Per Cylinder

19

Total Number of Tracks

7809 per disk pack

Data Bits Per Track, Maximum

107,520 (unformatted)

Data Bits Per Cylinder, Maximum

2,042,880 (unformatted)

Data Bits Per Disk Pack, Maximum

840,000,000 (unformatted)

Data Rate (Nominal)

6,448,000 bits/second

Data Words Per Disk Pack (Formatted Capacity)

43,980,288 (22-sector pack, 16-bit words)
39,982,080 (20-sector pack, 18-bit words)

Data Compatibility

The RP04 Drive allows for disk pack interchangeability between PDP-10/PDP-11/PDP-15 systems through software-controlled format and data word width settings.

Access Times

One Cylinder Seek

7 ms

Average Seek

27 ms

Maximum Seek

50 ms

Average Rotational Latency Time

8.33 ms

Operation

Start-up Time (Brush Cycle and Head Load)
15 seconds

Disk Rotational Speed
3600 rpm, ±2.5% (counterclockwise)

Stop Time (Retract Heads and Stop Disk Rotation)
15 seconds

Disk Drive Motor
1 hp induction, 208/230 Vac, 3-phase

Bit-Cell Time
155 ns

Disk Pack

Type
RP04P Pack (IBM 3336 Type)

Disk Diameter
14 inches

Number of Disks
10 magnetic disks (not including upper and lower protective disks)

Magnetic Recording Surfaces
19 (uppermost surface is numbered zero)

CHAPTER 2
MASSBUS INTERFACE

2.1 GENERAL

The Massbus provides the interface between the RH11 Controller and the RP04 Drives. The total external Massbus cable can be up to 60 ft in length, and up to eight drives may be connected in a daisy-chain configuration. The Massbus consists of two sections: a data bus section and a control bus section. These buses are described in the following paragraphs.

2.2 DATA BUS

The data bus section of the Massbus consists of a 19-bit (18 data bits plus parity bit) parallel data path and 6 control lines (Figure 2-1). The control lines are described in the following paragraphs.

Parallel Data Path – The parallel data path consists of an 18-bit data path designated D00 through D17 and an associated parity bit (DPA). The data path is bidirectional and employs odd parity. Data is transmitted synchronously, using a clock generated in the drive.

RUN – After a data transfer command has been written into the Control register of a drive, the drive connects to the data bus. The controller asserts the RUN line to initiate the function. At the end of each sector, on the trailing edge of the EBL (end of block) pulse, RUN is strobed by the drive. If it is still asserted, the function continues for the next sector; if it is negated, the function is terminated.

Occupied (OCC) – This signal is generated by the drive to indicate "data bus busy." As soon as a valid data transfer command is written into a drive, the drive asserts OCC. Various errors may prevent a drive from executing a command. The controller will time out in these cases due to no assertion of OCC or of SCLK, and the MXF (Missed Transfer) error will be set in the controller. OCC is negated at the trailing edge of the last EBL pulse of a transfer.

End of block (EBL) – This signal is asserted by the drive for 2 μs at the end of each sector (after the last SCLK pulse). For certain error conditions, where it is necessary to terminate operations immediately, EBL is asserted prior to the normal time for the last SCLK. In this case, the data transfer is terminated prior to the end of the sector.

Exception (EXC) – This signal is asserted by the drive when an abnormal condition occurs in the drive during a data transfer. The drive asserts this signal to indicate an error during a data transfer command (Read, Write, or Write-Check). EXC is asserted at or prior to assertion of EBL and is negated at the negation of EBL.

Sync Clock (SCLK), Write Clock (WCLK) – These signals are the timing signals used to control the strobing of the data in the controller and/or in the drive. During a read operation, the RH11 strobes the data lines on the negation of SCLK and the drive changes the data on the assertion of SCLK. During a write operation, the controller receives SCLK and echoes it back to the drive as WCLK. On the assertion of WCLK, the drive strobes the data lines; on the negation of WCLK, the controller changes the data on the data lines.

2.3 CONTROL BUS

The control bus section of the Massbus consists of a 17-bit (16 bits plus parity) parallel control and status data path, and 14 control lines (Figure 2-1), which are described below.

Parallel Control – The parallel control path consists of a 16-bit parallel data path designated C00 through C15 and an associated parity bit (CPA). The control lines are bidirectional and employ odd parity.

Drive Select [DS(2:0)] – These three lines transmit a 3-bit binary code from the controller to select a particular drive. The drive responds when the select (unit) number in the drive corresponds to the transmitted binary code.

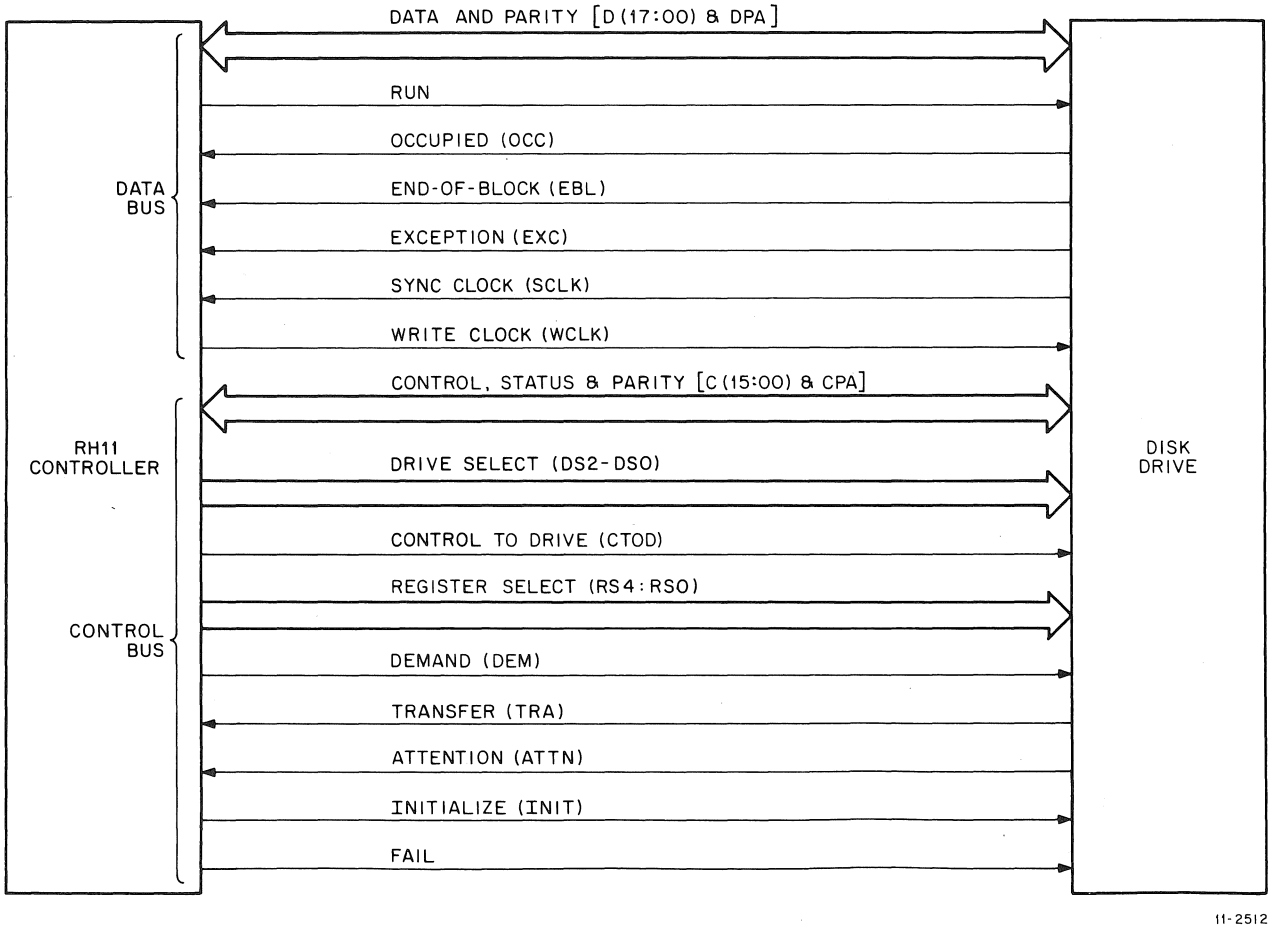


Figure 2-1 Massbus Interface Lines

Controller-to-Drive (CTOD) – This signal is generated by the controller and indicates the direction in which control and status information is to be transferred. For a controller-to-drive transfer, the controller asserts CTOD. For a drive-to-controller transfer, the controller negates this signal.

Register Select [RS (4:0)] – These five lines transmit a 5-bit binary code from the controller to the selected drive. The binary code selects one of the drive registers.

NOTE

Sixteen registers are contained in the RP04 and are designated by RP codes 00 through 17_8. Four registers are contained in the RH11. Table 2-1 lists the registers and their locations. If a register code higher than 17_8 is detected by the RP04 hardware, an Illegal Register (ILR) error occurs in the drive.

Table 2-1
RH11/RP04 Registers

Massbus Address (Octal)	Register	Mnemonic	Type
	Drive Registers		
00	Control (shared)	RPCS1	Read/write
01	Drive Status	RPDS	Read only
02	Error Register 1	RPER1	Read/write
03	Maintenance	RPMR	Read/write
04	Attention Summary	RPAS	Read/write
05	Desired Sector/Track Address	RPDA	Read/write
06	Drive Type	RPDT	Read only
07	Look-Ahead	RPLA	Read only
10	Error Register 2	RPER2	Read/write
11	Offset	RPOF	Read/write
12	Desired Cylinder Address	RPDC	Read/write
13	Current Cylinder Address	RPCC	Read only
14	Serial Number	RPSN	Read only
15	Error Register 3	RPER3	Read/write
16	ECC Position	RPEC1	Read only
17	ECC Pattern	RPEC2	Read only
	Controller Registers		
	Word Count	RPWC	Read/write
	Bus Address	RPBA	Read/write
	Status	RPCS2	Read/write
	Data Buffer	RPDB	Read/write

Demand (DEM) – This signal is asserted by the controller to indicate a transfer is to take place on the control bus. For a controller-to-drive transfer, DEM is asserted by the controller when data is present and settled on the control bus. For a drive-to-controller transfer, DEM is asserted by the controller to request data and is negated when the data has been strobed off the control bus. In both cases, the RS, DS, and CTOD lines are generated and allowed to settle before assertion of DEM.

Transfer (TRA) – This signal is asserted by the selected drive in response to DEM. For a controller-to-drive transfer, TRA is asserted after the data has been strobed and is negated after DEM is negated. For a drive-to-controller transfer, TRA is asserted after the data has been gated onto the bus and negated after the negation of DEM is received.

Attention (ATTN) – This line is shared by all eight drives attached to a controller; it may be asserted by any drive as a result of an abnormal condition or status change in the drive. An ATA status bit in each drive is set whenever that drive is asserting the ATTN line. ATTN may be asserted due to any of the following conditions:

1. An error while no data transfer is taking place (asserted immediately).
2. Completion of a data transfer command if an error occurred during the data transfer (asserted at the end of the data transfer).
3. Completion of a mechanical motion command (Seek, Calibrate, etc.) or of a search command.
4. As a result of the medium-on-line (MOL) bit changing states (except in the unload operation). In the dual controller configuration, a change in state of MOL will cause the assertion of ATTN to both controllers.

The ATA bit in a drive may be cleared by the following actions:

1. Asserting INIT on the Massbus (affects all eight drives).
2. Executing a reset instruction.
3. Causing Unibus A INIT by a console operation.
4. Writing a 1 into the CLR bit (controller clear).
5. Writing a 1 into the Attention Summary register (in the bit position for this drive). This clears the ATA bit; however, it does not clear the error.

6. Writing a valid command (with the GO bit asserted) into the RPCS1 register if no error occurs. Note that clearing the ATA bit of one drive does not always cause the ATTN line to be negated, because other drives may also be asserting the line.

NOTE

There are three cases in which ATA is not reset when a command is written into the Control register (with the GO bit set). These are: (1) if there is a Control Bus Parity error on the write, (2) if an error was previously set, or (3) if an illegal function (ILF) code is written.

Initialize (INIT) – This signal is asserted by the controller to perform a system reset of all the drives. It is asserted when a 1 is written into the CLR bit (bit 05 of RPCS2) and when Unibus INIT is asserted on Unibus A. When a drive receives the INIT pulse, it immediately aborts the execution of any current command and performs all actions described for the Drive Clear command.

NOTE

In the dual controller configuration, a drive will honor an INIT pulse only from the controller which has seized the drive, or from either controller if the drive is in the unseized state. In addition, the ATA and VV bits, which exist independently on each port of the RP04, can be cleared only from their respective controller.

FAIL – When asserted, this signal indicates a power-fail condition has occurred in the controller. While FAIL is asserted, the drive inhibits reception of the INIT and DEM signals at the drive.

2.4 COMMAND INITIATION

To initiate a command in a drive via the Massbus, the controller (or the central processor via the controller) writes a word into the RPCS1 register. The function code and GO bit are transferred to the selected drive. If the command specified is valid and the GO bit is asserted, the selected drive executes the command.

Commands are of two types: non-data transfer commands (such as Drive Clear, Seek, etc.) and data transfer commands (such as Read, Write, and Write-Check). The command function code bits (05 through 00 including GO in RPCS1) are 01_8 through 47_8 for non-data transfer commands and are 51_8 through 77_8 for data transfer commands (not all are valid functions).

2.4.1 Non-Data Transfer Commands

Non-data transfer commands affect only the state of the drive. The controller merely writes the command word (with GO bit set) into the drive's Control register. At the completion of the command execution, the drive typically asserts the ATTN line to signal its completion.

If the non-data transfer command code written into the drive is not recognized by the drive as a valid command, the drive will immediately signal an error by asserting the ATTN line. The Illegal Function (ILF) error is set.

2.4.2 Data Transfer Commands

When any data transfer command code (with the GO bit set) is written into the drive's Control register, the controller expects data transfer on the data bus to begin soon thereafter. The controller resets its RDY (Controller Ready) bit as soon as the data transfer command code is written into a drive. The drive normally responds by asserting the OCC line. The controller asserts RUN and then data is transferred to or from the specified drive, after the proper address (sector, track, cylinder) is found.

If a Class B error occurs in a drive during a data transfer command, the drive asserts the EXC line. This line remains asserted until the trailing edge of the last EBL pulse. The RH11 Controller always negates the RUN line when it detects EXC asserted, so that the data transfer is terminated at the end of the sector in which the error was signaled.

2.5 READING AND WRITING DRIVE REGISTERS

The process of reading or writing drive registers is accomplished via the asynchronous (control bus) portion of the Massbus (Figure 2-1). The RH11 initiates the action by selecting a drive (DS2–DS0), selecting a register (RS4–RS0) in that drive, selecting a direction of transfer (CTOD), and either reading or writing the register via the 17 bidirectional control lines [C(15:00) and CPA]. After a deskew delay to allow the control lines to stabilize, the RH11 asserts DEM. The drive, upon receiving the DEM assertion, checks the CTOD line to ascertain whether a read or write is to occur.

If a register read operation is specified, the drive will gate the contents of the specified register onto the control bus and will issue TRA. When the RH11 receives TRA, it will gate the control lines onto the Unibus. After a deskew delay, the RH11 asserts SSYN to the processor. When the processor receives the control data and SSYN, it clears MSYN. The clearing of MSYN negates SSYN and DEM. The negation of DEM causes TRA to be negated and completes the operation.

If a register write operation is specified, the RH11 gates the control data onto the control bus when it issues DEM. The drive will transfer the data from the control bus into the specified drive register and assert TRA, which causes the assertion of SSYN in the RH11. SSYN is transferred to the processor and causes MSYN to be cleared. The clearing of MSYN causes SSYN and DEM to be negated. The negation of DEM causes TRA to be negated to complete the operation.

The Massbus structure allows a register read operation (asynchronous control bus) to occur while a data transfer (synchronous data bus) is taking place. Any attempt by the RH11 to write a register in a drive performing a data transfer operation (except for the Maintenance and Attention Summary registers) will cause the RP04 Drive to set the Register Modification Refused (RMR) error bit (Chapter 3).

2.6 DATA TRANSFER

Before a data transfer takes place, the selected unit, desired sector/track address, cylinder address, bus address, and word count are specified by the program. The program then transfers the Read or Write data transfer command (with the GO bit asserted) to the RPCS1 register.

Upon receipt of the data transfer command, the drive will assert OCC, indicating that the data bus is busy. The RH11 logically connects to the Massbus data bus by asserting RUN and then waits for SCLK pulses from the drive. For a Write data transfer, each WCLK pulse causes a word to be written into a data register in the drive logic; for a Read data transfer, each SCLK pulse causes a word to be transferred to the Massbus. When a sector of words has been written onto or read from the disk, the disk sends an EBL pulse to the RH11. If the RUN line is still asserted at this time, a sector of data words is transferred. If the RUN line is negated, the data transfer is terminated.

2.7 MASSBUS PHYSICAL DESCRIPTION

The Massbus consists of 56 signals, including data, control, status, and parity. These signals are routed externally to all cabinets via a round BC06S Massbus 60-pair cable (Figure 2-2). Standard cable length from the RH11 cabinet to the first drive is 25 ft and from drive to drive (daisy chain) is 2 ft. On special order, 40-ft and 10-ft cable lengths can be substituted. Under all conditions, the total external cable length must not exceed 60 ft. Figure 2-3 shows the cable routing for a dual-port subsystem.

At the RH11 cabinet, the BC06S cable plugs into an AD-7009861 Receptacle Housing Assembly, which is mounted in a connector panel at the lower rear of the cabinet. This connector panel has cut-outs for four Receptacle Housing Assemblies in order to accommodate up to four RH11s and associated cabling. The other side of the Receptacle Housing Assembly accepts three BC06R, 20-pair, flat-conductor cables from the RH11.

At the RP04 cabinet end, the BC06S cable connects to another AD-7009861 Receptacle Housing Assembly, which is mounted at the rear of the DCL. The internal end of this assembly accepts the flat BC06R Massbus cable that is internal to the RP04. The output connector of the last drive is terminated with a 7009933 Terminator Pack Assembly.

Table 2-2 shows the Massbus signals and their associated pin assignments.

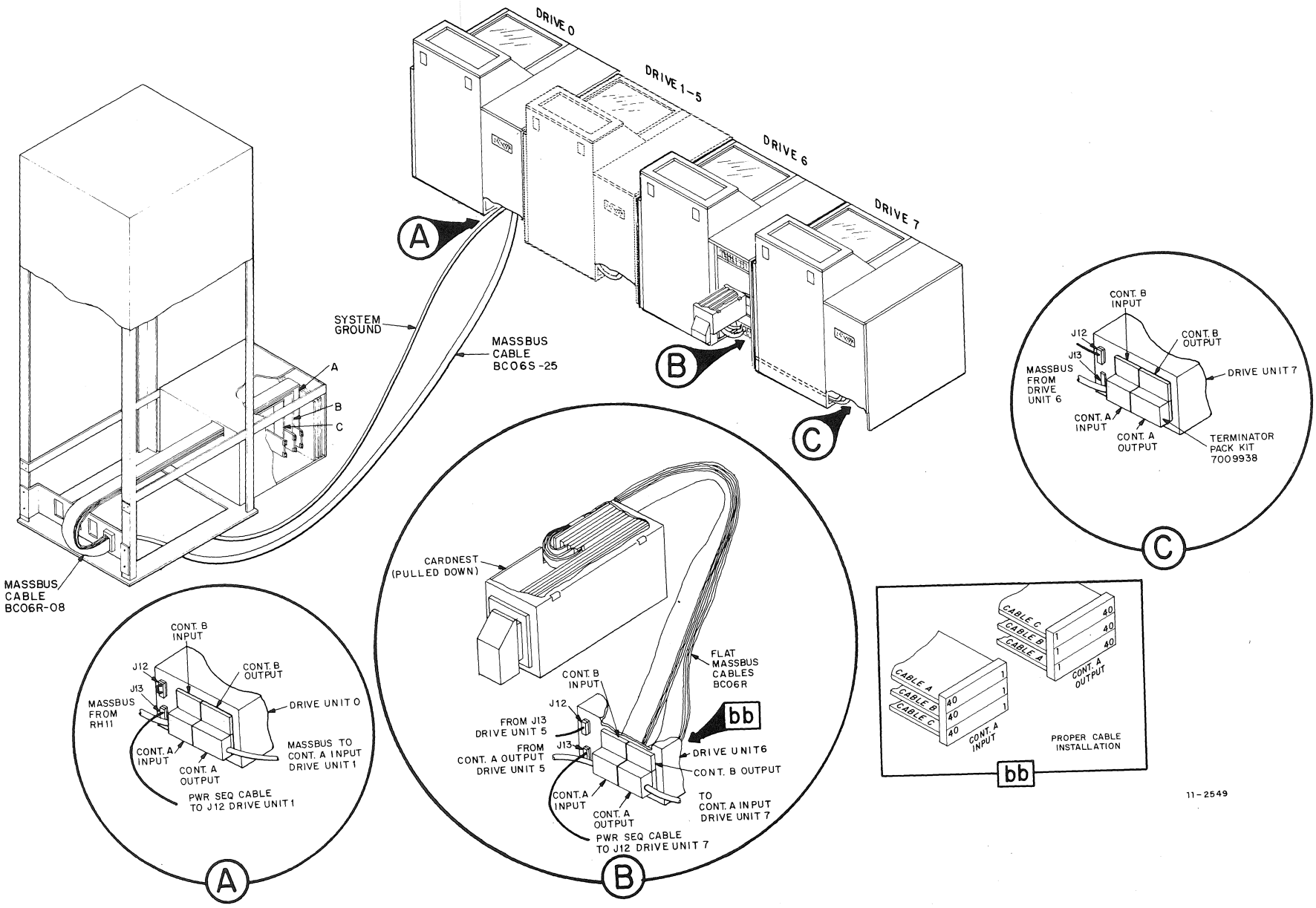


Figure 2-2 Single-Port Subsystem Cable Routing

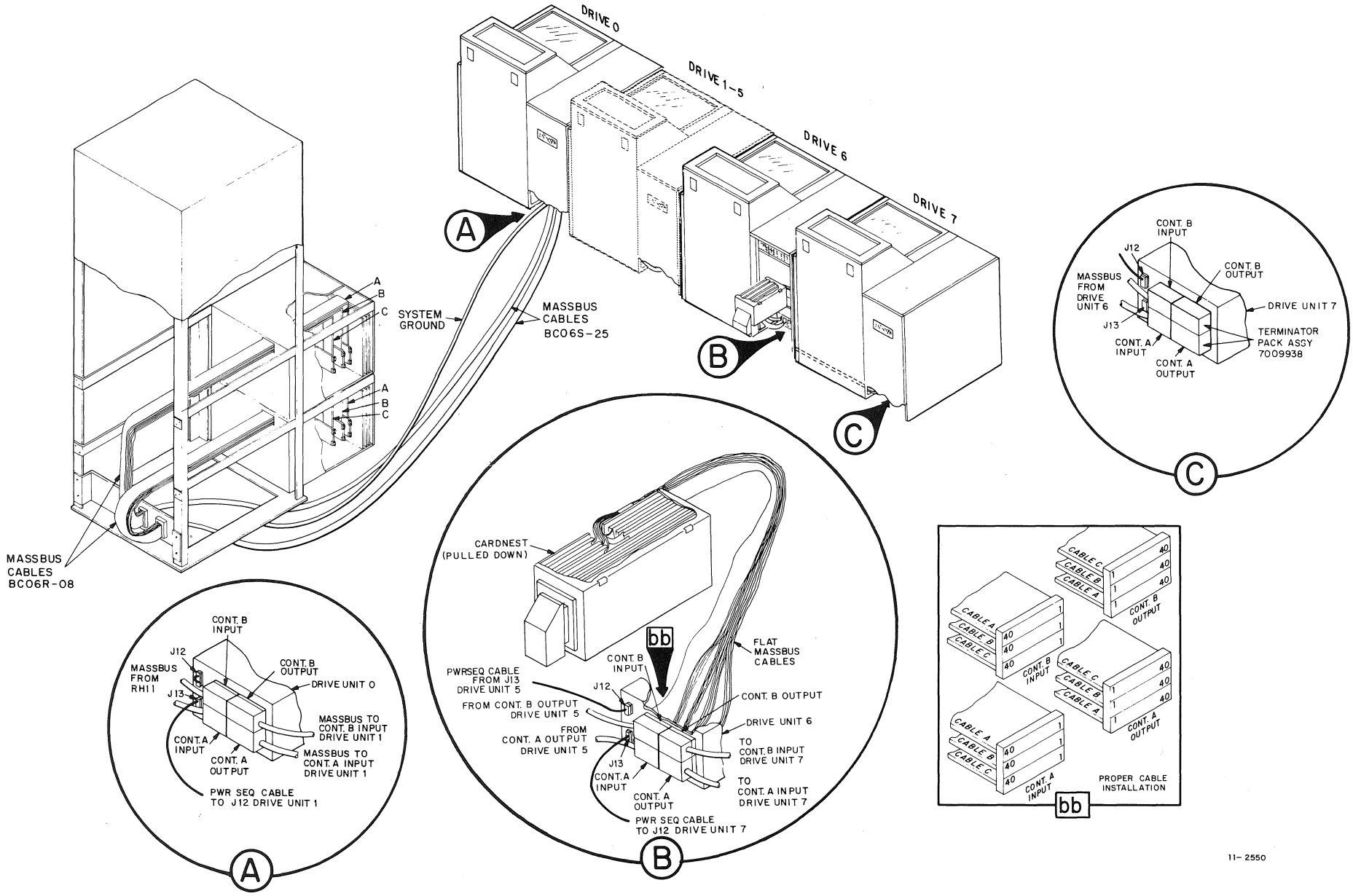


Figure 2-3 Dual-Port Subsystem Cable Routing

Table 2-2
Massbus Signal Cable Designations

Cable	Pin*		Polarity	Designation
Massbus Cable A	A	1	-	MASS D00
	B	2	+	
	C	3	+	MASS D01
	D	4	-	
	E	5	-	MASS D02
	F	6	+	
	H	7	+	MASS D03
	J	8	-	
	K	9	-	MASS D04
	L	10	+	
	M	11	+	MASS D05
	N	12	-	
	P	13	-	MASS C00
	R	14	+	
	S	15	+	MASS C01
	T	16	-	
	U	17	-	MASS C02
	V	18	+	
	W	19	+	MASS C03
	X	20	-	
	Y	21	-	MASS C04
	Z	22	+	
	AA	23	+	MASS C05
	BB	24	-	
	CC	25	-	MASS SCLK
	DD	26	+	
	EE	27	+	MASS RS3
	FF	28	-	
	HH	29	+	MASS ATTN
	JJ	30	-	
	KK	31	-	MASS RS4
	LL	32	+	
	MM	33	-	MASS CTOD
	NN	34	+	
	PP	35	+	MASS WCLK
	RR	36	-	
	SS	37	+	MASS RUN
	TT	38	-	
	UU	39		SPARE
	VV	40		GND

Table 2-2 (Cont)
Massbus Signal Cable Designations

Cable	Pin*		Polarity	Designation
Massbus Cable B	A	1	-	MASS D06
	B	2	+	
	C	3	+	MASS D07
	D	4	-	
	E	5	-	MASS D08
	F	6	+	
	H	7	+	MASS D09
	J	8	-	
	K	9	-	MASS D10
	L	10	+	
	M	11	+	MASS D11
	N	12	-	
	P	13	-	MASS C06
	R	14	+	
	S	15	+	MASS C07
	T	16	-	
	U	17	-	MASS C08
	V	18	+	
	W	19	+	MASS C09
	X	20	-	
	Y	21	-	MASS C10
	Z	22	+	
	AA	23	+	MASS C11
	BB	24	-	
	CC	25	-	MASS EXC
	DD	26	+	
	EE	27	+	MASS RS0
	FF	28	-	
	HH	29	+	MASS EBL
	JJ	30	-	
	KK	31	-	MASS RS1
	LL	32	+	
	MM	33	-	MASS RS2
	NN	34	+	
	PP	35	+	MASS INIT
	RR	36	-	
	SS	37	+	MASS SP1
	TT	38	-	
	UU	39		SPARE
	VV	40		GND

*Alternate pin designation schemes

Note: Massbus cables are to be installed per markings on the cable.

Table 2-2 (Cont)
Massbus Signal Cable Designations

Cable	Pin*		Polarity	Designation
Massbus Cable C	A	1	-	MASS D12
	B	2	+	
	C	3	+	MASS D13
	D	4	-	
	E	5	-	MASS D14
	F	6	+	
	H	7	+	MASS D15
	J	8	-	
	K	9	-	MASS D16
	L	10	+	
	M	11	+	MASS D17
	N	12	-	
	P	13	-	MASS DPA
	R	14	+	
	S	15	+	MASS C12
	T	16	-	
	U	17	-	MASS C13
	V	18	+	
	W	19	+	MASS C14
	X	20	-	
	Y	21	-	MASS C15
	Z	22	+	
	AA	23	+	MASS CPA
	BB	24	-	
	CC	25	-	MASS OCC
	DD	26	+	
	EE	27	+	MASS DS0
	FF	28	-	
	HH	29	+	MASS TRA
	JJ	30	-	
	KK	31	-	MASS DS1
	LL	32	+	
	MM	33	-	MASS DS2
	NN	34	+	
	PP	35	+	MASS DEM
	RR	36	-	
	SS	37	+	MASS SP2
	TT	38	-	
	UU	39	H	MASS FAIL
	VV	40		GND

*Alternate pin designation schemes

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 GENERAL

Twenty 16-bit registers (Figure 3-1) interface the RH11 Device Controller to the RP04 Drive. These registers are loaded and read under program control via Unibus A (the control port of the RH11). Data is sometimes transferred over a second Unibus (Unibus B) called the data port of the RH11. The disk system is monitored by status and error indicators in these registers. Four of the registers are located entirely in the RH11 and 15 are located entirely in the RP04 Drive. One register is shared by both the RH11 and the RP04. Bits 15 through 13 and 10 through 6 of this register are stored in the RH11, while bits 12, 11, and 5 through 0 are generated by the RP04.

Table 3-1 shows the various subsystem registers and their respective addresses.

3.2 TRACK FORMATTING

Figure 3-2 shows the data formatting for the RP04 Drive. The data track on the disk contains 22 sectors (16-bit words), each containing a header and a data field. The first sector following the index pulse is sector 0. All data sectors are fixed length; if the actual size of useful data information is less than the amount of space on the data field, the remainder of the data field will be filled with 0s until 256 words have been written.

3.2.1 Header Format

A disk pack should be formatted and the format verified before any real data is written on it. Once formatted, individual or groups of sectors should not be reformatted unless absolutely necessary.

Figure 3-3 shows the header format, which consists of the following five words:

Word 1 – This word contains the desired cylinder address. The RP04 has 411 cylinders (requiring 9 bits). This word also contains one bit (bit 12) to be written on the disk surface to identify the format mode of operation (18-bit or 16-bit format).

Word 2 – The low order five bits of this word contain the desired sector address. The least significant five bits of the upper byte of this word contain the desired track address. Each cylinder on the RP04 contains 19 data tracks.

Word 3 – This word is the first key word and exists with every header.

Word 4 – This word is the second key word and exists with every header.

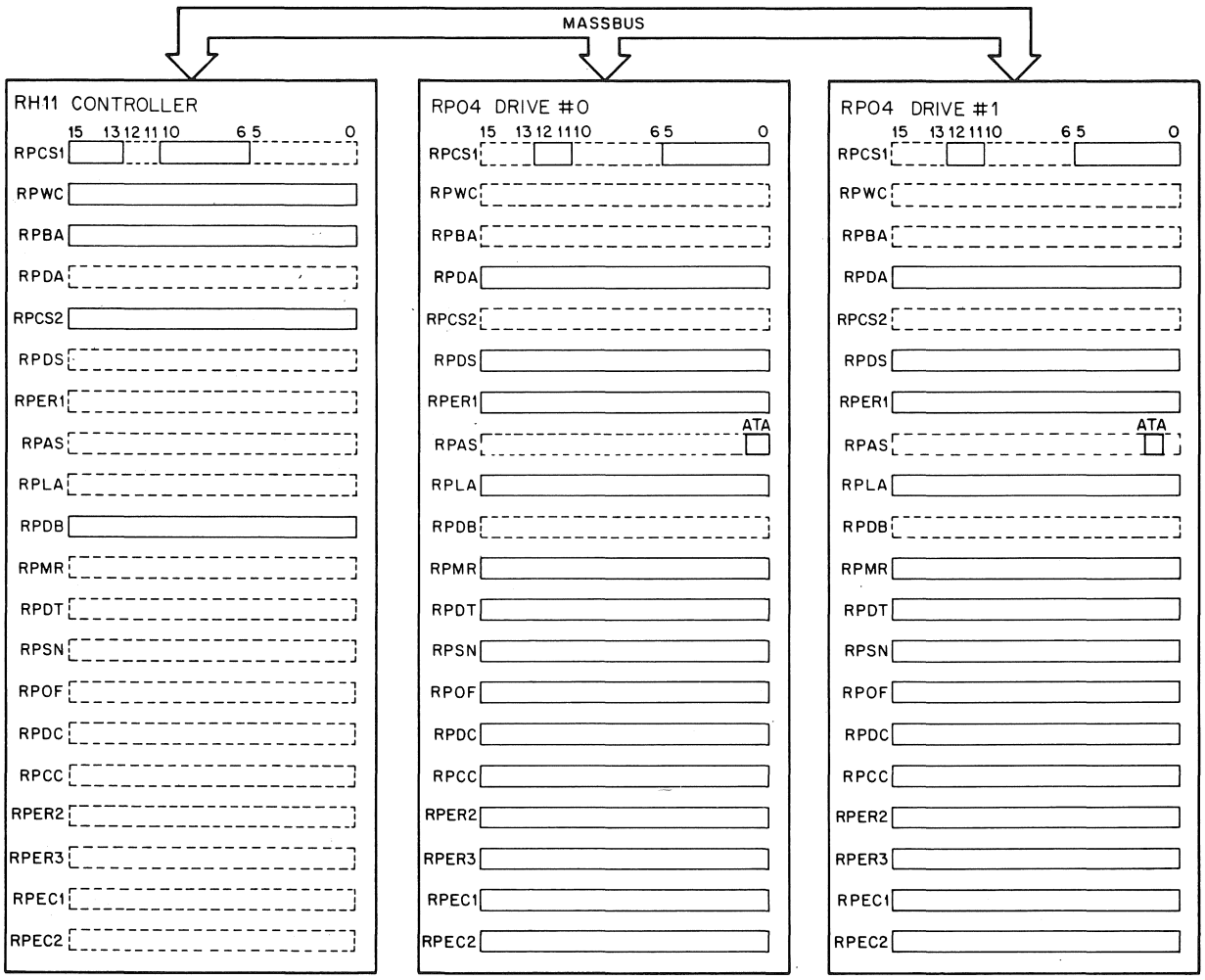
NOTE

The two key words are completely transparent to the device. If the software utilizes these words, information should be provided to the RP04 Drive during a header format operation.

Word 5 – This is the CRC word which is generated and checked by the device logic. This word is not available to the software.

3.2.2 Header Field Handling

3.2.2.1 Normal Header Compare – During a normal header compare, the RP04 compares only the first two words of the header and then checks the CRC word for error. An error in the header field is indicated by turning on the appropriate error bit in the Error register (format error, header compare error, or CRC error). A header error, however, is only valid when the sector count field of the RPLA Look-Ahead register and the sector field of the Desired Sector/Track Address register (RPDA) have already matched. It is immaterial where an error occurs in the header field since the RP04 cannot determine its location in the field. However, if the software reads the header into main memory using a Read Header and Data command, it would be possible to locate the error in the header field.



MASSBUS ADDRESS	NOMENCLATURE	UNIBUS ADDRESS
00	RPCS1 – CONTROL AND STATUS REGISTER 1	776700
–	RPWC – WORD COUNT REGISTER	776702
–	RPBA – BUS ADDRESS REGISTER	776704
01	RPDA – DESIRED ADDRESS REGISTER	776706
–	RPCS2 – CONTROL AND STATUS REGISTER 2	776710
05	RPDS – DRIVE STATUS REGISTER	776712
02	RPER1 – ERROR REGISTER 01	776714
04	RPAS – ATTENTION SUMMARY PSEUDO REGISTER	776716
01	RPLA – LOOK-AHEAD REGISTER	776720
–	RPDB – DATA BUFFER	776722
03	RPMR – MAINTENANCE REGISTER	776724
06	RPDT – DRIVE TYPE REGISTER	776726
10	RPSN – SERIAL NUMBER REGISTER	776730
11	RPOF – OFFSET REGISTER	776732
12	RPDC – DESIRED CYLINDER ADDRESS REGISTER	776734
13	RPCC – CURRENT CYLINDER ADDRESS REGISTER	776736
11	RPER2 – ERROR REGISTER 02	776740
15	RPER3 – ERROR REGISTER 03	776742
16	RPEC1 – ECC POSITION REGISTER	776744
17	RPEC2 – ECC PATTERN REGISTER	776746

NOTES:

1. RPCS1 shared between RH11 and RP04; bits 15–13 and 10–6 are stored in the RH11; bits 13–11 and 5–0 are generated by the RP04.
2. Each drive is assigned an attention summary bit in the bit location corresponding to its unit number.
3. Location of registers denoted by solid lines; dashed lines are for reference only.

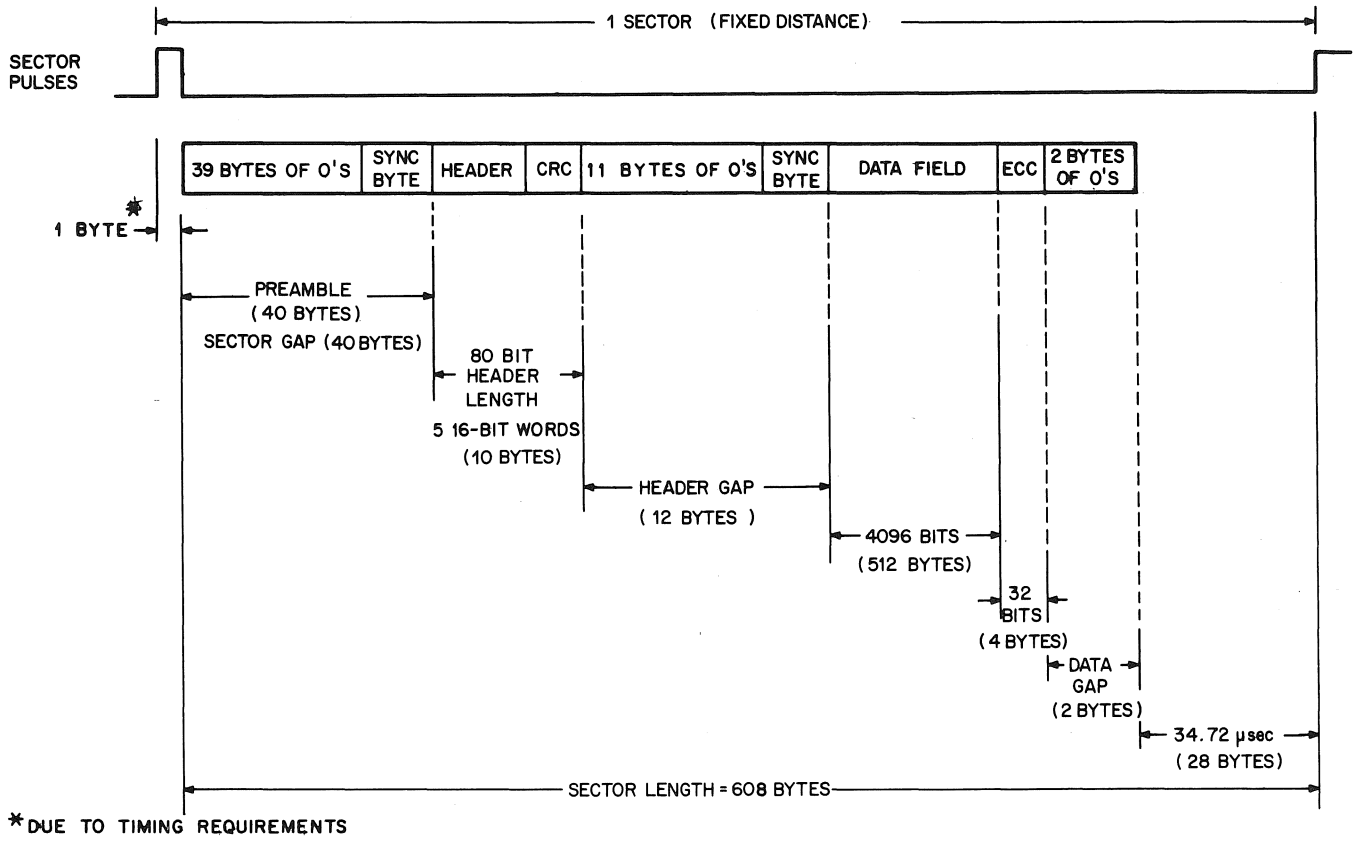
11-2501

Figure 3-1 RJP04 Subsystem Registers

Table 3-1
RH11 and RP04 Device Registers

Mnemonic	Register Name	Unibus Address	Massbus Address	Mode	Function
RPCS1	Control	776700	00*	Read/write	Contains function code, GO bit
RPWC	Word Count	776702	*	Read/write	Contains 2's complement of number of words to be transferred
RPBA	Bus Address	776704	*	Read/write	Contains memory address of location where data transfer is to begin
RPDA	Desired Sector/Track Address	776706	01	Read/write	Contains disk sector and track address where transfer is to occur
RPCS2	Status	776710	*	Read only	Contains RH11 status indication
RPDS	Drive Status	776712	05	Read/write	Contains all non-error status plus error summary bit
RPER1	Error Register 01	776714	02	Read/write	Contains individual error indications
RPAS	Attention Summary	776716	04	Read/write	Contains one bit per drive attention summary status
RPLA	Look-Ahead	776720	07	Read only	Contains current position as a sector number and fraction of a sector block
RPDB	Data Buffer	776722	*	Read/write	Contains input and output connection to silo for maintenance
RPMR	Maintenance	776724	03	Read/write	Contains control and diagnostic information
RPDT	Drive Type	776726	06	Read only	Contains drive characteristic indications
RPSN	Serial Number	776730	10	Read only	Contains lowest four digits of DEC drive serial number
RPOF	Offset	776732	11	Read/write	Contains bits for control of offset of movable heads
RPDC	Desired Cylinder	776734	12	Read/write	Contains address of cylinder for seek-
RPCC	Current Cylinder	776736	13	Read only	Contains cylinder address corresponding to current arm position
RPER2	Error Register 02	776740	14	Read/write	Contains detailed error bits
RPER3	Error Register 03	776742	15	Read/write	Contains detailed error bits
RPEC1	ECC Position	776744	16	Read only	Contains position of burst error
RPEC2	ECC Pattern	776746	17	Read only	Contains the burst error

*RH11 registers (RPCS1 is shared by RP04 and RH11).



NOTES: 1) WITH SECTOR TYPE FORMAT, NO ADDRESS MARK RECORDING IS NECESSARY.

2) IN REGARD TO THE HEADER, THERE IS ERROR DETECTION RATHER THAN ERROR CORRECTION. THE LAST HEADER BYTE WILL BE A CRC BYTE FOR ERROR DETECTION PURPOSES.

3) THE 34.72 µsec GAP AT THE END OF THE DATA SECTOR MUST BE GUARANTEED UNUSED.

4) THE DATA FIELD IS A FIXED BLOCK OF DATA OF 256 16 BIT WORDS.

11-2500

Figure 3-2 Detailed Sector Format

3.2.2.2 **Header Compare Inhibit** – The header compare may be inhibited by setting the HCI (Header Compare Inhibit) bit (RPOF, bit 10). If the RP04 detects that this bit is asserted, it will ignore the header compare logic and CRC correction and will send only the data field (designated by the sector count) to main memory.

In extended operation, with the HCI bit asserted, the RP04 will continue reading or writing only data fields (as long as the RUN line remains set) and will ignore header compares or header field errors.

3.2.2.3 **Key Field** – Two rules for formatting a disk pack are:

1. The value of key words in formatting should be known and set up at format time.

   The key words should be static (not subject to change).

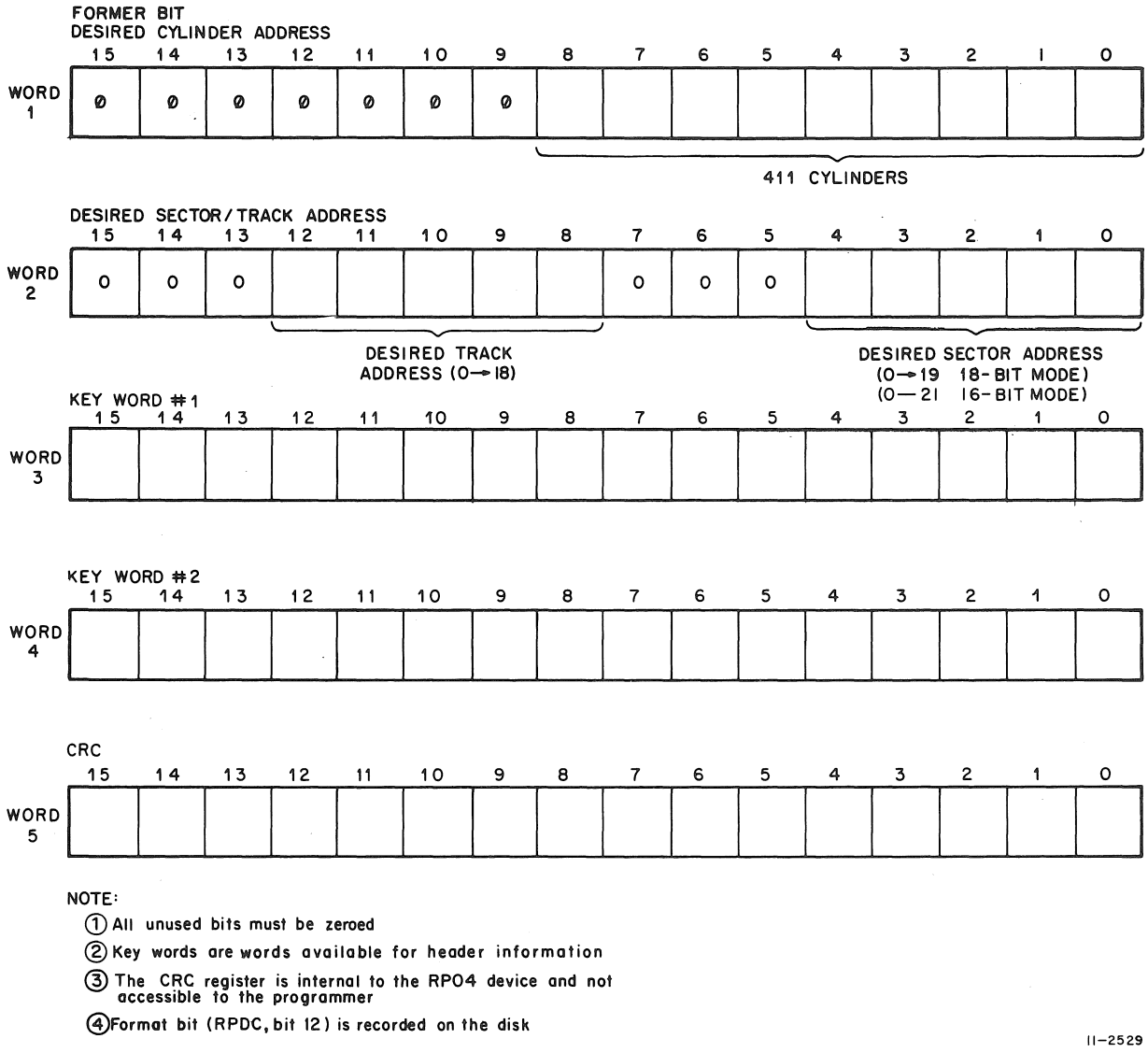


Figure 3-3 Header Format

Key words can be used for:

1. Alternate addressing scheme (special hardware)
2. Access right indications (system only, system write only, etc.)
3. Data structure versus data block (bit map, directory)
4. Data verification and security (software or special hardware).

3.2.2.4 Key Field Handling – The RP04 identifies the header by examining only the first two words of the header and then checks the CRC word for an error. The CRC check examines the first five words of the header, while the header compare only compares the first two words of the header.

The RP04 Drive will normally read the first two words, and then check the format bit, cylinder, sector, and track. After the fifth word, the RP04 checks the CRC. If no header error is detected, the RP04 outputs the data into the main memory as if the key did not exist. The software, by examining the data, determines if this block of data is the one required.

NOTE

The RP04 logic sends the data field on the basis of the normal header compare only (the first two words) because the system time required to compare the key and return that data would guarantee loss of that sector and a disk revolution during a normal read data operation.

If the software is willing to lose a disk revolution, it is possible to handle the key field in the following sequence:

1. Issue a Read Header and Data command to the desired sector. The RP04 device will transfer the entire header and data field to the controller, as soon as it detects a sector count/sector field compare and will terminate the command. The RP04 device logic will compare the header words, and initiate a Format Error (FER), Header Compare Error (HCE), or Header CRC (HCRC) error if a header error occurs.

2. The software will compare the header field portion of the sector (including the key) in main memory and, if the compare is successful, it can issue a Read command to that sector.

3. On the next revolution, the RP04 device will make a normal header compare (first two words) and will transfer the data field to main memory.

The possible loss of a revolution each time a key needs to be looked at on a sector may result in significant throughput reduction if done frequently. It is possible, however, to use a key on the header of the first of *many* sectors to be read. In this way, the system throughput reduction can be minimized.

An alternative method is for the software to place the key one sector *ahead* of the actual sector. Through a Read Header and Data command, the software could read and verify the key and still have the time to have the data field belonging to the next sector transferred, if a key compare is made.

3.2.2.5 **Key Words Update** – The software may desire to update the key words of a header. This update is accomplished as follows. In the normal format operation, the controller issues a Write Header and Data command. The RP04 will generate gaps, write header words received through the Massbus, and write 256 words containing all 1s supplied by the controller under the control of the system software.

First Revolution – Issue a Read command to that sector using the old key or no key at all. The RP04 will read the data field into main memory.

Second Revolution – Issue a Write Header and Data command and format that sector normally. This time the header field will contain new key words. The old data field will be filled with 256 words of 1s supplied by the software.

Third Revolution – Issue a Write command to that sector and write the data field from main memory. This data field may be the same as the old one or may be altered.

NOTE

The software may update the key words of a header in *one* revolution by issuing a Write Header and Data command and reformatting the entire sector by rewriting the header with the new key words. In this case, the software will send actual data words instead of 1s after the generation of the header gap by the RP04. There is a significant risk, however, in using this approach since the software must rely only on the sector count field/desired sector field compare to reformat the sector. If the sector count field is out of sequence, the wrong sector will be reformatted.

3.2.2.6 **Header Compare Error Handling** – Upon receiving a Read or Write command, the RP04 logic will normally begin searching the headers as they pass under the head.

The sector count field must be in sync with the data on the track. This occurs following a successful head load. Syncing the sector counter with the index pulse is required only once, following the head load.

If any header error is detected (FER, HCE, or HCRC) during an implied Search, Read, or Write command, the RP04 will abort.

The emphasis, from the software point of view, is on the desired sector address match primarily and then on the actual recorded header information. Consequently, the RP04 Drive will have an exclusive OR condition (X-OR) between the desired sector field of the Desired Sector/Track Address register and the sector count field.

As long as the desired sector field and the sector count field do *not* match, header verification will not be initiated. When the desired sector is equal to the sector count field, the following conditions occur:

1. If the recorded header (first two words) matches the desired format bit and the Desired Cylinder and Desired Sector/Track Address registers *without* a CRC error, the data field associated with that header is the required one.

2. If the desired sector field and sector count field match, but a CRC error is detected, the HCRC bit will be set and no transfer of any kind will take place. The EXC line will also be set by the RP04 Drive logic. In addition to the HCRC bit being set, the HCE error bit may be set, indicating a header compare error.

NOTE

The FER, HCE, and HCRC error bits will be cleared when a Drive Clear command or an Initialize (INIT) pulse is received.

3.2.3 Data Format

The RP04 can operate in 16-bit mode or in 18-bit mode. Figure 3-4 shows the 16-bit formatted sector and the sector timing relationships.

The 34.72-μs gap at the end of the sector is required to compensate for mechanical tolerances in the RP04. The total unformatted capacity of an RP04 data track is 107,520 bits and, based on a 4864-bit sector length, the maximum number of sectors is 107,520/4,864 = 22 sectors + 512 spare bits.

3.3 FUNCTION CODES

The programmer initiates operations by selecting a drive, selecting the Control register (776700), and loading the register with a function code and GO bit. The function code specifies a specific command. The RP04, upon assertion of the GO bit and RUN, proceeds to execute the command. The commands can be divided into three categories: data transfer commands, positioning commands, and housekeeping operations. These commands and their corresponding function codes are listed on the following page.

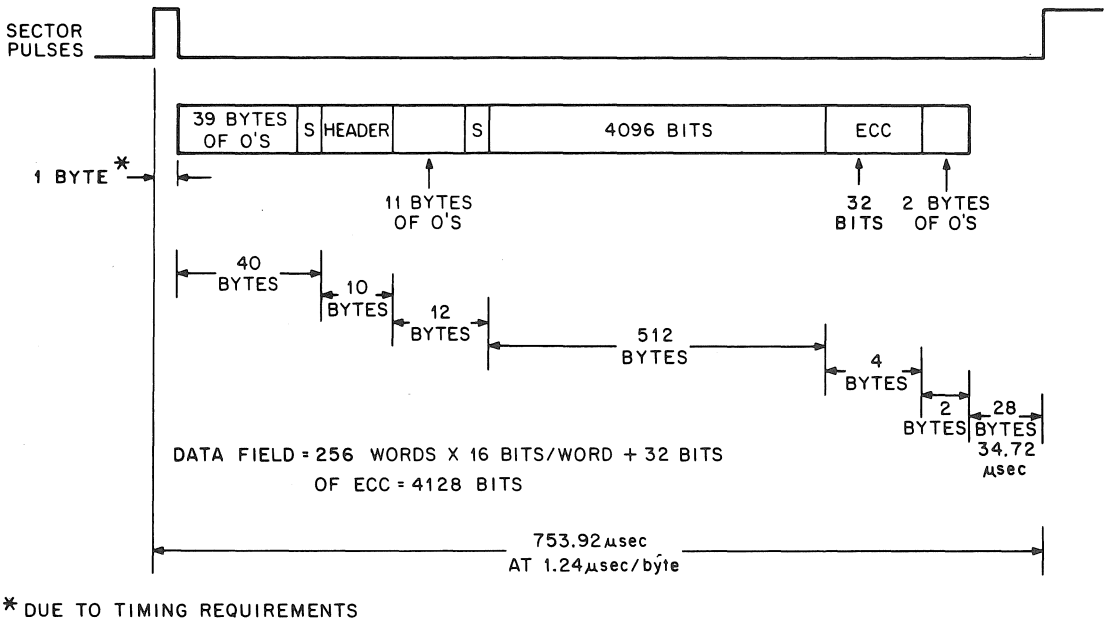


Figure 3-4 Sector Timing (16-Bit Mode)

Data Transfer Commands	Function Code
Write Check Data	51
Write Check Header and Data	53
Write Data	61
Write Header and Data (Format)	63
Read Data	71
Read Header and Data	73

Positioning Commands	Function Code
Unload (Standby)	3
Seek	5
Recalibrate	7
Offset	15
Return to Centerline	17
Search	31

Housekeeping Operations	Function Code
No-op	1
Drive Clear	11
Release	13
Read-in Preset	21
Pack Acknowledge	23
(Initialize (Massbus INIT pulse)	

Data Transfer Commands – These commands involve data transfer to or from the disk and usually take less than 1 ms for the transfer of a sector. However, the commands may involve access time consuming many milliseconds. The data transfer commands are described below.

Write Check Data – Transfers to the controller the 256-word data field which, in turn, compares it to the corresponding words in memory.

Write Check Header and Data – Transfers to the controller the header field and data field which, in turn, compares it to the corresponding words in memory.

Write Data – Writes the 256-word data field of the sector with the words supplied by the controller, and generates the ECC word.

Write Header and Data (Format Operation) – Writes the sector header with the four words supplied by the controller and generates the CRC word. Writes the data field of the sector with the words (256) supplied by the controller, and generates the ECC word.

Read Data – Transfers to the controller the 256-word *data field in the sector.*

Read Header and Data – Transfers to the controller 4 words of sector header data, and the 256 words in the data field.

Positioning Commands – Positioning commands are mechanical movement commands used to position the heads over the disk pack and take milliseconds to complete. These commands assert the ATTN line after their normal completion. The positioning commands are described below.

Unload – Places the drive in the Standby state. The heads are retracted, the spindle cycled down, and the STANDBY light lit. The command completes when the drive is brought back on line (up to speed and heads loaded). It is at this time that the ATTN line is asserted.

Seek – Causes the heads to be moved to the cylinder address specified by the desired cylinder. The current cylinder is made equal to the desired cylinder address following the completion of the command.

Recalibrate – Positions the heads over cylinder zero, and sets the Current Cylinder Address register to zero. The command takes approximately 500 ms to complete.

Offset – A "micro" seek. It allows the heads to be moved off the track centerline. It is used in error recovery processing and takes 10 ms to execute regardless of the offset value.

Return to Center Line – Used to explicitly return to the track centerline after an offset operation.

Search – Combines the Seek command with a search for the desired sector address and can be considered a synchronization command between the software and the desired disk address.

Housekeeping Commands – Housekeeping commands are used to place the drive logic into a known or initial state and usually take a few microseconds to complete. The housekeeping commands are listed below.

No-op – Does not perform any operation.

Drive Clear – The following registers and conditions within the RP04 are cleared:

- Status Register – ATA and ERR
- All three Error registers
- Attention Summary register
- ECC Position and Pattern registers
- Diagnostic mode bit

Release Command – Performs a drive clear function and releases the drive for use by the other port. ATTN is never raised after the completion of the housekeeping commands unless there is a persistent error condition.

INIT Pulse – Performs the same functions as the Drive Clear command but does not require the drive to be ready.

Read-in Preset – Sets the VV (volume valid) bit, clears the Desired Sector/Track Address register, clears the Desired Cylinder Address register, and clears the FMT, HCI, and ECI bits in the Offset register. Clearing the FMT bit causes the RP04 to be in 18-bit mode.

Pack Acknowledge – Sets the VV bit for the command controller. This command must be issued before any data transfer or positioning commands can be given if the pack has gone off-line and then on-line (i.e., MOL changes state). It is primarily intended to avoid unknown pack changes on a dual controller drive.

3.4 DATA TRANSFER COMMANDS

Data transfer command codes are designated by 51_8 through 77_8 (always odd since the GO bit must be asserted to execute a data transfer command). Other command codes (01_8 through 47_8) are called non-data transfer commands. Only data transfer commands cause the RH11 to become busy (RDY bit negated). While the RH11 is busy, no further data transfer commands may be issued (see PGE bit 10 in RPCS2). Non-data transfer commands, however, may be issued at any time and to any drive which is not busy (DRY asserted).

Partial sector data transfer commands are handled by the RH11 in the following manner. During a partial sector read data transfer, the RH11 stops transfers to memory, even though the RP04 continues transfers to the RH11 until the end of the sector is reached. During a partial sector write data transfer, the RH11 stops fetching the words from memory while the RP04 continues writing 0s into the remainder of the sector. The RH11 supplies the zero data words and WCLK signals for the completion of the sector.

NOTE

Data transfer commands never raise the ATTN line upon completion of the transfer unless an error has occurred.

All data transfer commands have seek and sector search functions implied. When the desired cylinder does not equal the current cylinder during the execution of the data transfer, a Seek will be issued to the desired cylinder (implied seek, ATTN not asserted). The device will then search the desired track for the desired sector and, when found, will start the data transfer to or from the RH11 Controller. On all commands except the Write Header and Data command (which is the format operation) and the Search command, a match of the sector header must be made before the data transfer is started. If the Header Compare Inhibit (HCI, bit 10 in Offset register) bit is set, the header will be compared and checked, but, like the Write Header and Data command, the transfer will be started based on the prerecorded sector pulses. With the HCI bit set, header errors will not be reported. With the HCI bit cleared (header compare enabled), the transfer will be aborted if a header error is detected.

The desired sector, track, and cylinder addresses are updated after the transfer of a sector. Therefore, at the end of a transfer the disk is set up to transfer the next sequential sector. This allows multiple sector transfers and spiral transfer across tracks and cylinder. When the desired cylinder address changes during a transfer, the implied seek is performed and is termed a mid-transfer seek. Note that the data bus is tied up for the complete transfer, including any and all seek and search time. The RP04 does not lose its "sync" on sector pulse during a seek and therefore does *not* have to wait for the index pulse to start its sector search.

3.4.1 Read Command

In the normal Read command execution, the controller will raise the Read command and RUN line, following the asynchronous loading of the proper control registers at the interface.

Before the read operation can actually begin, the RP04 Drive will:

1. Check for correct format.

2. Check if the positioner is addressing the required cylinder. If it is, the RP04 Drive will begin searching for the required sector. If not, the device logic will initiate a Seek command.

3. When the correct sector count/desired sector field match and the entire header is identified without a header error, the RP04 will begin looking for the sync byte located at the end of the header gap.

   When a positive identification is made on the sync byte, the RP04 will read the next 16 bits or 18 bits (depending on the mode of operation) and will place the first word in the data buffer, while the second word is being read off the disk pack. When the data buffer contains word 0, the RP04 will assert SCLK.

   NOTE

   The manipulation of data bits into words (16 bits or 18 bits) will be done by the RP04 Drive internally.

While (1) and (2) are taking place, the controller is waiting for the assertion of SCLK. If an implied Seek command is required, the waiting period can be extensive. The data is shifted into the data shift register serially. At the same time, the device logic is shifting the same data bits through the ECC hardware.

If a Class B error occurs during the seek operation (implied seek or mid-transfer seek), the command will be terminated after the completion of the seek operation.

The RP04 Drive keeps track of the number of bytes transferred since the data length is always fixed. If the *actual* valid data is less than 256 words, the RP04 is expected to supply the entire 256 sync clocks and will fill the remainder of the data field with 0s so that the data field always contains 256 words.

Upon recognizing the SCLK assertion, the RH11 prepares to receive a data word. At the trailing edge of SCLK, the RH11 will strobe the data lines, strobing the data into its data buffer. After 2.48 μs from the trailing edge of SCLK (if in 16-bit mode), the device logic will place another word on the data lines and assert SCLK again. The data transfer will continue in the same way until the last word has been sent to the RH11 (last assertion of SCLK).

3.4.1.1 Examining ECC for Error – The SCLK will reset for the last time when the 256th word has been output to the RH11. The Read command on this sector is not finished until the ECC bytes, always located at the end of the data field, have been read and serially shifted into the ECC hardware. Following the shifting of the ECC bytes, the device logic will examine the contents of the ECC hardware for errors.

If the ECC hardware indicates an error (with ECC correction enabled), the RP04 will go into the error recovery procedure, depending on the status of the ECI bit (RPOF, bit 11). If the ECC correction is enabled, the controller *must wait* until the correction results are available before assertion of the EBL pulse for the sector in error. The presence or absence of an ECC error will be determined approximately 5 μs after the fall of the last SCLK. If no ECC error exists, the operation will terminate normally. If the RUN line is asserted when the RP04 detects the EBL pulse, the RP04 Drive logic will begin looking for the new sector address specified by the Desired Cylinder and Desired Sector/Track Address registers. (The sector field of the Desired Sector/Track Address register was incremented at the rise of the last EBL pulse.)

The Read command is terminated due to an ECC error condition in the two cases described in the following paragraphs.

Case A: Error Correction Code Inhibit (ECI) Bit Is Reset – If an ECC error is detected with the ECI bit reset, the RP04 immediately goes into the ECC correction procedure. At the same time, the RP04 logic will set the Data Check (DCK) error and assert the EXC line before the error correction procedure begins. The error correction process requires a minimum of 7 ms before it is completed and the results are available. When the results are available, the device will transfer the error pattern and its location within the data field to the appropriate ECC registers. The ATA bit will also set at the trailing edge of EBL and EXC.

If the error was not ECC correctable, the device will set the ECC Hard Error bit (RPER1, bit 6) and the EXC and ATTN lines. Therefore, with the DCK and the ECH bits set, the device logic will proceed to a normal termination with the EBL pulse.

NOTE

Throughout the error correction procedure, the sector counter is in sync and is incrementing normally.

If the RH11 keeps the RUN line asserted when it detects the EBL pulse, the RP04 device logic will begin looking for the new sector address specified by the Desired Cylinder and Desired Sector/Track Address registers. (The sector field of the Desired Sector/Track Address register was incremented at the rise of the last EBL pulse.)

Case B: Error Correction Code Inhibit (ECI) Bit Is Set – If the ECI bit is set and an error occurs, the operation will terminate with the DCK and EXC bits set and the RP04 will not go into the error correction process.

If the RUN line remains high during the fall of the EBL pulse (with DCK set), the command will continue for the next sector without a loss of revolution. The DCK bit and EXC line will remain set until the RH11 issues a Drive Clear command or an INIT pulse.

3.4.1.2 **Read with Implied Seek** – When a Read command is issued, the RP04 first examines the contents of the header registers (Desired Cylinder and Desired Sector/Track Address) and compares the Desired Cylinder register with the Current Cylinder Address register to determine if the positioner is over the desired cylinder.

If the current and desired cylinder addresses are *not* the same, the RP04 logic will initiate a Seek to the proper cylinder. Upon completion of this Seek command, the device will begin a header compare operation to look for the desired sector.

The search will begin with the first sector pulse. Throughout the seek operation, the sector count field remains in sync with the rotating disk due to a servo clock. Consequently, no need exists to resync the sector count at the completion of a seek operation. When the proper header has been identified, the RP04 will check for a header error and for a match in the desired sector field/sector count field. If a header error did not occur, the RP04 logic will read the first data word, place it in the data buffer, and assert SCLK. The data transfer will take place as described in Paragraph 3.4.

3.4.1.3 **Spiral Read Capability** – During an extended read operation, the software continues reading through data tracks (spiral read). This spiral effect can occur in two cases: when the cylinder is the same and the track address is incremented, and when both the track and cylinder addresses are changed. These cases are described in the following paragraphs. A 22-sector format is assigned (16-bit mode).

Same Cylinder – Change Track Address – The RP04 samples the RUN line at the trailing edge of the EBL pulse during the end of the 21st sector transmission on track x. If the RUN line stays high, the RP04 logic will increment the track field of the Desired Sector/Track Address register to (x + 1). Within 34.72 μs between the last byte of sector 21 on track x and the leading edge of sector 0 (index pulse) on track (x + 1), there is enough time for the head address to switch before the next read on sector 0 is initiated. The Read command will continue normally on the new data track.

The reading of sectors will continue through all the data tracks of the cylinder presently being addressed (and, if necessary, to the next cylinder) if the RUN line is high during the fall of the EBL pulse. The command will terminate at the fall of the last EBL pulse with the RUN line being unasserted. At the end of the transmission, the track field will reflect the address of the track from which the next sector will be extracted. If the cylinder address has not changed, the Desired Cylinder Address register will remain unchanged. The sector field of the Desired Sector/Track Address register reflects the last sector transferred, plus one.

Change Track Address, Change Cylinder Address (Mid-Transfer Seek) – With a DCA (Desired Cylinder Address) other than 410, a head address of 18 (last track on the cylinder), and a sector address of 21, the trailing edge of the EBL pulse on sector 21 will again sample the status of the RUN line.

If the RUN line is asserted, the RP04 will increment the Desired Cylinder Address register by one and initiate a seek operation. In addition, the track field is reset, thus automatically selecting track 0. The sector field is also reset to sector 0. The sector counter is guaranteed to stay in sync with the rotating disk during the seek operation, due to the servo clock supplied by the RP04 logic.

While the RH11 is waiting for a SCLK from the data field of the next sector, the RP04 logic will initiate a one-cylinder seek operation (7 ms). Following a seek completion, the device logic will wait for sector 0. The elapsed time between the last sector on the previous cylinder and the first sector on the new cylinder is one complete revolution (16.7 ms). The RH11 will then receive a new SCLK after 16.7 ms plus 72 μs (sector gap, header, and header gap time). The RP04 will continue reading sectors through different tracks and different cylinders for as long as the RUN line remains asserted during the fall of the EBL pulse.

3.4.1.4 **Termination Conditions** – There are two termination procedures in the case where there is both a track address change and a cylinder address change.

1. *RUN Line Reset* – If the RUN line is reset, the RP04 will terminate the data transfer at the fall of the EBL pulse in the current sector. The rise of the EBL pulse unconditionally increments the sector field and track field of the Desired Sector/Track Address register to the next sector address. Upon termination of the multisector Read command, therefore, the contents of the Desired Cylinder and Desired Sector/Track Address registers will reflect the address of the next sector following the last sector transferred.

   NOTE

   If the RUN line is reset at the fall of the EBL pulse of track 18 and sector 21, the desired cylinder address will increment by one but *no* mid-transfer seek will be initiated.

2. *Entire Pack To Be Read* – If the entire pack is read, the data transfer will always terminate (unconditionally) when sector 21, on track 18 and cylinder 410 (last cylinder on the 3336 disk pack) has been transferred. The RP04 logic will raise the EBL pulse following the ECC check on sector 21. If the RUN line is high at this time, the AOE (Address Overflow Error) bit is set.

   The Last Sector Transferred (LST) bit is set at the rise of the EBL pulse when terminating the transfer. This bit (RPDS, bit 10) is reset by the RP04 logic when a new function command is received. After the last sector has been read, the contents of the RP04 registers are as follows (provided no address overflow error occurred):

   Cylinder Address Register = 411 (Illegal address)
   Desired Sector/Track Address Register
   Desired Track Field = 0
   Desired Sector Field = 0 (Was incremented at the last rise of the EBL pulse)

NOTE

Upon initiation of a data transfer command, the data is blocked for 45 μs to compensate for settling time of the read amplifier. If a sector pulse is encountered within this period, it will not be recognized. Consequently, the sector block associated with this sector pulse cannot be recognized until the next revolution.

3.4.1.5 Error Handling – If an ECC error is detected during the transfer of data, the RP04 logic will *stop* the transfer and go into the error correction procedure, provided the ECC is enabled. When the error correction procedure is finished, the software can continue reading sectors by issuing a *new* Read command. If the intent is to read multiple sectors, the RUN line should remain asserted, since the address on the registers already reflects the address of the next available sector. However, a rotational delay of one revolution is incurred.

If the RUN line is still asserted at the fall of the EBL pulse of sector 21, track 18, cylinder 410, the RP04 logic treats this condition as an error condition. Consequently, the RP04 will set the AOE bit, raise the ATTN line, and set the LST status bit. The following error conditions are also associated with the read mode.

Address Overflow Error (AOE, RPER1, Bit 9) – This bit is set after the Desired Cylinder Address register overflows (exceeds address 410) during a spiral data transfer. With the AOE bit set, the RP04 will terminate the operation when the last sector has been processed. This bit is set if the RUN line remains asserted following the fall of the last EBL pulse.

Drive Timing Error (DTE, RPER1, Bit 12) – This bit is set during the read mode, when a failure has occurred in the clocking or timing circuits in the drive. A failure in the clocking or timing circuits can no longer guarantee the logic remaining in the proper sequence. Consequently, the RP04 will *abort* the command as soon as this error is detected. The software should try to reread this sector where the error occurred.

Invalid Address Error (IAE, RPER1, Bit 10) – This bit is set if a read is attempted on a nonexistent cylinder address, track address, or sector address (contents of the corresponding RP04 interface register in error). With this error bit set, the RP04 Drive will terminate the command before execution.

Operation Incomplete, (OPI, RPER1, Bit 13) – This bit is set if the read or write operation fails to complete within three index pulses from the initiation of the command. The RP04 Drive will keep trying for as long as the software wishes. Each time a Drive Clear command or an INIT pulse is reinitiated by the RH11, the device logic will reset the OPI bit and other error bits (if present), and execute the command.

NOTE

Any of the error bits discussed above that are associated with the read mode will also cause the composite error (ERR) bit (RPDS, bit 14) and the Attention Active (ATA) bit in the RPAS register to set. The error conditions can only be reset through a Drive Clear command or an INIT pulse.

3.4.1.6 Offset Recovery Procedure – In addition to ECC, the RP04 offers further data recovery attempts by offsetting the positioner in small increments around the vicinity of the questionable data track. Even though the logic for offsetting the positioner is available to the programmer at any time, the software can only use this capability on an unrecoverable type error on the track centerline. The offset operation is time consuming and its use is limited.

Figure 3-5 shows the available positioner offset increments in the RP04 as well as the method for providing the offset address to the RP04 Drive.

Bit Location	Cylinder Difference (Normal Mode)	Off-Set Address (Off-Set Mode)
0	1	25 Microinches
1	2	50 Microinches
2	4	100 Microinches
3	8	200 Microinches
4	16	400 Microinches
5	32	800 Microinches
6	64	Not Used
7	128	Reverse Direction
8	256	Not Used

RECOMMENDED OFFSET POSITIONS:

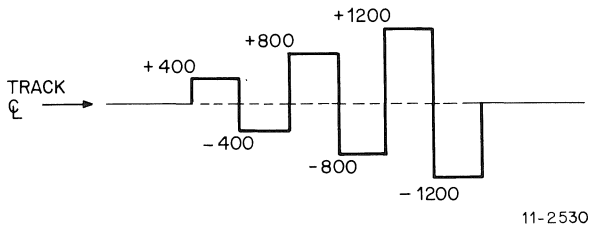


Figure 3-5 Positioner Offset Settings

The nine lines used to provide the offset information are the *same* nine lines used to provide the cylinder difference address to the positioner during a normal seek operation.

Writing a word into the Offset register with the proper function code in the Control register (RPCS1) will initiate an offset operation. The Offset register presents the offset address and direction information, as shown in Figure 3-5. Rather than advancing forward in three positions and in reverse in three positions, it is recommended that the positioner go back and forth as shown in the figure. The recommended number of tries in each offset position is two.

NOTE

The positioner is under control of the software and the software ultimately determines the positioning sequence.

While the positioner is moving in the offset mode, the positioner Operation In Progress (PIP) bit (RHDS, bit 13) will be set. At the completion of the offset movement, the RP04 will:

Reset PIP status bit
Set the DRY bit
Reset the GO bit
Raise the ATTN line.

If the controller issues a Seek command or a Write command instead of another Offset command, the device logic *will return* the positioner to track centerline before executing a Seek command to another cylinder or a Write command to the same cylinder.

3.4.1.7 Read Header and Data Command – The Read Header and Data command allows an entire sector (header and data field) to be read. The RP04 requires 260 SCLKs (4 SCLKs for the header words and 256 SCLKs for the data field) to transfer the entire sector.

During the transferring of the four header words, the RP04 logic also checks for header miscompare and/or CRC errors. The appropriate error bits are set if a format error (FER), header compare error (HCE), or header CRC error (HCRC) is detected.

A header error in this case will *not* interrupt the data transfer. The RP04 Drive will transfer the entire data field associated with the header. The data field will also be checked for read errors (through ECC) if the ECI bit is reset.

NOTE

The Read Header and Data command may be issued following a format operation; in this case, the data field may have been filled with 1s, and an ECC check will determine the condition of the data field recording space.

3.4.2 Write Command Execution

When the controller detects the assertion of SCLK, it will immediately assert WCLK, indicating to the RP04 that word 0, already on the data lines for a period of time, is valid. The device logic will receive the assertion of WCLK (370 ns maximum cable delay) and will strobe word 0 from the data lines into the data buffer at this time. In 16-bit mode, the RP04 will strobe 16 Massbus data lines.

Upon recognizing the negation of the SCLK, the controller immediately resets WCLK. At the negation of WCLK, the RH11 places the second word on the data lines. Approximately half a word time from the trailing edge of SCLK, the RP04 again asserts SCLK to indicate it is prepared to accept another word.

NOTE
SCLK has a period of approximately 2.5 μs.

The above process will continue until 256 words have been transferred to the RP04 from the RH11.

3.4.2.1 **Writing of ECC** – Following the negation of the last SCLK, the RP04 Drive will require approximately 7.5 μs to write the ECC bytes before it raises the EBL pulse.

Four ECC bytes (two words) are required to be written at the end of each data field. This amounts to two word times or approximately 5.0 μs (for 4 bytes). In addition to ECC, the device logic will write *two* bytes of 0s at the end of the data field, following the ECC bytes; this requires another 2.5 μs, for a total of 7.5 μs.

3.4.2.2 **Termination** – Seven and one-half microseconds after the last data word (word 255) is strobed by the device, the EBL pulse is asserted for 1.5 μs, indicating the completion of the particular sector data field update.

The RH11 sees the EBL pulse and adjusts the RUN line accordingly. The RP04 looks at the RUN line at the trailing edge of the EBL pulse. It will terminate the command if the RUN line is low, or will continue on to the next sector if the RUN line is asserted.

The assertion of the EBL pulse by the device will also cause the sector field of the Desired Sector/Track Address register (RPDA) to increment to the next sector address. The sector count will increment at the rise of the next sector pulse.

NOTE
Even though the actual valid data field may be smaller than 256 words, the RP04 *will expect* the controller to send 256 WCLK signals and the appropriate data to fill the remainder of the data field.

This is essential for proper ECC operation. The device logic will, therefore, *always* assume a fixed data length of 256 words (16-bit or 18-bit words).

3.4.2.3 **Write Lock Operation** – The RP04 can be placed in the WRITE PROTECT mode through a manual switch on the RP04 control panel. The status of the device will be indicated by the illumination of the manual switch. When the indicator is ON, an attempt to issue a Write command on a write-locked device will cause the Write Lock Error (WLE) bit to set on Error register 01. To remove the write lock condition, the manual switch must be placed in the WRITE PERMIT mode.

The Write Lock Error and all other error bits are cleared with a Drive Clear command or with an INIT pulse.

3.4.2.4 **Write Error Conditions** – During the write mode, a number of device errors, such as Loss of Write Current, AC Unsafe, and Write Current Without Write Command, will cause the device to unconditionally go into the WRITE PROTECT mode, in the middle of a write operation. Under those circumstances, the RP04 will also *retract* the heads.

The above emergency conditions will cause the following to occur:

1. The EXC line will be set, indicating an error occurred during data transmission.
2. The ATTN line will be set.
3. The Drive Unsafe (UNS) bit will be set in the Error register. Depending on the nature of the UNS bit, the heads may be retracted from the pack.
4. The composite error (ERR) bit will be set on the Drive Status register because the UNS bit is on.
5. The Error registers will include all the pertinent error bits.

Other Write command errors in the Error register are:

1. *Parity Error (PAR)* – Data and control bus parity errors are ORed into a single bit. This bit is set when a parity error is detected during the write operation over the synchronous or asynchronous bus lines (odd parity). The detection of a parity error will cause the RP04 to:

   - Set the EXC line.
   - Set the PAR bit in Error register 01.

   The device will continue accepting data to the end of the sector. At the trailing edge of EBL, the RP04 will sample the RUN line and take the following action:

   - If the RUN line is high, the RP04 will maintain the PAR bit set and continue writing the next sector (Class A error).
   - If the RUN line is low, the Write command will be terminated with the appropriate error bits set.

2. *Header Compare Error (HCE)* – This bit is set during the write mode, when the contents of a header (first two words) do not match the contents of the Desired Cylinder and Desired Sector/Track Address registers. With the HCE bit set, the RP04 will not continue the operation (Class B type error).

3. *Address Overflow Error (AOE)* – This bit is set during the write mode after the Desired Cylinder Address register (RPDC) overflows (exceeds address 410) during a spiral write operation. With the AOE bit set, the RP04 will terminate the operation when the last sector is written.

4. *Drive Timing Error (DTE)* – This bit is set during the write mode when a failure has occurred in the clocking or timing circuits in the drive. A failure in the clocking or timing circuits can no longer guarantee the logic remaining in the proper sequence. Consequently, the RP04 Drive will abort the command as soon as this error is detected. The software should try to regenerate the sector where the error occurred.

5. *Invalid Address Error (IAE)* – This bit is set if a write is attempted to a nonexistent cylinder address, track address, or sector address (contents of the corresponding RP04 register in error). With this error bit set, the RP04 will terminate the command before execution.

6. *Operation Incomplete (OPI)* – This bit is set during a Write command, if the write operation fails to complete within three index pulses from the initiation of the command. The RP04 will continue trying for as long as the software wishes. Each time a Drive Clear command or an INIT pulse is reinitiated by the RH11, the device will reset the OPI and other error bits (if present) and execute the command.

NOTE

Any of the above discussed error bits associated with the write mode will cause the ERR and the ATA bits to set and the EXC line to be asserted.

7. *Format Error (FER)* – This bit is set when the prerecorded flag bit on the header field is not equal to the corresponding flag bit in the Offset register. This error usually occurs where the wrong pack was mounted on the RP04 device. With this bit set, the RP04 will immediately abort the command by resetting the GO bit and setting the ATTN line.

8. *HCRC Error* – This bit is set if a CRC error is detected after the header compare process. With the HCRC error bit set, the RP04 will not execute the Write command. This command must be reinitiated with a loss of one revolution.

   The HCRC error will reset when a Drive Clear command or an INIT pulse is received.

9. *Write Clock Fail (WCF)* – This bit is set if the WCLK signal is not received by the drive during a write operation. Upon recognizing this error condition, the RP04 will abort the command.

3.4.2.5 Multisector Write Operation – The RP04 Drive will update sectors as long as the RUN line remains asserted.

NOTE

On a write operation, the headers will not be rewritten.

The multispiral write and its termination are similar to that described for the multisector read operation (see Paragraph 3.4.1.3).

3.4.2.6 Write Check Commands – The Write Check Data and Write Check Header and Data commands are used by the RH11/RP04 subsystem for data verification. These commands cause the data in memory to be compared, word by word, with the data read from the disk.

Write Check Data (51_8) – With respect to the RP04 Drive, the execution of this command is identical to the Read Data command. The RH11 compares the data on the disk to the data read from memory. Upon receiving the 51_8 function code, the RP04 will enable the same logic required to execute a Read Data command.

Write Check Header and Data (55_8) – For the RP04, the Write Check Header and Data command is identical to the Read Header and Data Command (see Paragraph 3.4.1.7). Upon receiving the 55_8 function code, the RP04 will enable the Read Header and Data command logic.

NOTE

Although these two commands are treated as normal Read commands for the RP04, they employ different function codes to command the RH11 to verify from memory rather than write into memory.

3.5 POSITIONING COMMANDS

The positioning commands are those commands which cause the RP04 positioner to move in any direction (see Paragraph 3.3).

3.5.1 Unload (Standby)/Cycle-Up Operation (03_8)

An Unload command is a special command in the RP04 instruction repertoire that will cause the RP04 to retract the heads and cycle down the spindle (but *not* power down the machine). The Unload command allows the software to indicate that the program requires a disk pack change to continue. This change can take place any time during the actual job execution or at the end of the job.

In a multiprogram environment, it is possible that more than one job is running simultaneously on eight RP04 dual controller devices. The software can issue the Unload command to the specified drive, which eliminates the necessity of the operator having to know when a pack change is required and of having to print this on the console. In addition, the RP04 control panel has a STANDBY light which illuminates as soon as the RP04 recognizes the command.

Upon recognizing the Unload command, the RP04 device will:

1. Set the PIP bit
2. Reset the DRY bit
3. Initiate head retraction
4. Reset the MOL bit
5. Illuminate the STANDBY indicator on the control panel.

When the spindle comes to a stop, the operator may exchange the disk pack and press the STANDBY button on the RP04 control panel, which will:

1. Turn off the STANDBY indicator on the control panel (light will go off on the STANDBY button).
2. Begin the cycle-up procedure. The cycle-up procedure consists of: brush cycle, spindle up to speed, and load heads.

When the device cycles up and the positioner is settled in the recalibrate position (addressing cylinder 0) the RP04:

3. Sets the MOL bit
4. Sets the DRY bit
5. Resets the PIP bit
6. Sets the ATA bit.

The RP04 is now ready to accept another command.

NOTE

Throughout the entire unload sequence, the GO bit will be set. The device will *not* accept another command until the cycle-up procedure is complete.

3.5.2 Seek Command (05_8)

The RP04 Drive can cause a seek operation in the following ways:

1. Seek Command
2. Implied Seek: A normal Read or Write command causes the RP04 to examine the positioner location and initiate a seek if the proper cylinder is not addressed.
3. Mid-Transfer Seek: During a normal *extended* (spiral) Read or Write Data command, a seek operation to the next cylinder will automatically be iniitated by the device logic if the last sector on the cylinder's last track has been read or written and the RUN line remains asserted.

The following paragraphs describe these seek operations in detail.

3.5.2.1 Seek Command Initiation (05_8) – The software will load the Desired Cylinder Address register (RPDC) with the pertinent information for reading from or writing on a sector on the data pack. The software will load the Control register with a seek function code and the GO bit to begin the operation.

When the GO bit is set, the contents of the appropriate registers are assumed valid. The device logic will first compare the contents of the Desired Cylinder Address register with the Current Cylinder Address register by a subtraction process. If the output of the subtract logic is other than zero, a seek will take place.

NOTE

The comparison of the Desired Cylinder Address register with Current Cylinder Address register is done automatically.

3.5.2.2 Seek Command Execution – The Seek command is initiated when the GO bit is set in the Control register (RPCS1, bit 0). The setting of the GO bit will cause the actual positioner movement to begin, and will cause the PIP bit (RPDS, bit 13) to set and the DRY bit to reset. The DRY bit, when reset, indicates a busy condition to the controller.

NOTE

Each time an attempt is made by the controller to write into the Desired Cylinder Address register (RPDC) while a seek is in progress, the RP04 will not accept the information and will assert the RMR bit (RPER1, bit 02).

3.5.2.3 Seek Command Termination – The device logic will wait for the seek operation to complete. Upon completion of the seek, the positioner is on target, settled, and the device is ready to accept another command. Consequently, the RP04 will:

1. Reset the PIP bit
2. Set the DRY bit
3. Set the ATA bit

Before another command is accepted, the RP04 will transfer the contents of the Desired Cylinder Address register into the Current Cylinder Address register so that the Current Cylinder Address register reflects the actual address of the cylinder that the positioner is addressing.

When the contents of the Desired Cylinder Address register are transferred to the Current Cylinder Address register, the subtract logic should be equal to zero. Following the cycle up, the RP04 will wait for the first index pulse to reset the sector counter for synchronizing the control logic.

NOTE

Upon completion of the Seek command, it will not be necessary to resync the sector counter. The device supplies a constant sector clock (1.24 μs/period), which is the basis for the generation of timing. Even during the positioner's actual movement, this clock will operate and be in sync with the rotating medium.

3.5.2.4 Incomplete Seek Handling – The device logic normally waits for the seek completion. Due to a positioner malfunctioning, the seek operation may *not* complete. The device will monitor the seek timing and will time out in 85 ms if the seek has not completed, and will:

1. Set the Seek Incomplete (SKI) error bit
2. Set ATA bit
3. Reset PIP bit (indicating device positioner is not busy)
4. Set RDY bit (indicating the device is ready to execute a command).

The above conditions will indicate to the software that:

1. The seek operation did *not* complete.
2. The exact positioner location is *unknown*.

SKI will always cause the RP04 to determine that the drive is unsafe to operate. The software can attempt to diagnose the trouble by looking at the Error registers.

The RP04 has already issued a Recalibrate command *internally* upon detecting a seek incomplete, and the positioner is on its way back. A second Recalibrate command is not necessary. The device will wait for the completion of the recalibrate before setting the RDY bit and raising the ATTN line.

A successful completion of a recalibrate operation will:

1. Clear the Current Cylinder Address register
2. Set the ATA bit.

NOTE

Since an error exists in the Error register (SKI error bit is set), the software must issue a Drive Clear command to clear the error before retrying.

The software can now retry by issuing another Seek command.

3.5.2.5 Implied Seek Operation – In addition to the actual Seek command execution, the RP04 has the capability of performing a seek operation indirectly (implied seek) when a read or write function code is in the Control register.

The implied seek operation is similar to the Seek command (see Paragraph 3.5.2.2) with the following exceptions:

1. In an implied seek, the function code in the Control register is a Data Transfer command.

2. The ATTN line is not asserted and the PIP bit will not be set for an implied seek.

At the completion of the seek operation, the RP04 immediately looks at the sector count/desired sector field compare logic for sector identification. Once the comparison is made, the RP04 will compare headers, and, if no header or CRC error is detected, a normal read or write operation will take place.

At the completion of the implied seek, the DRY bit will stay *reset* and no ATA bit will be set. The software will *not* be notified that a seek operation took place before data transmission was initiated.

When an implied seek is involved, the software may have to wait a maximum of 66.7 ms or an average 35.33 ms from the time the command was issued until the rise of the first data transfer.

3.5.2.6 Error Condition Handling – The software must be aware, in general, that an implied seek is possible upon issuing a Read or Write command. This is important because it is possible to encounter an incomplete seek operation during an implied seek execution.

For an incomplete implied seek operation, the RP04 will:

1. Set the Seek Incomplete (SKI) error bit

2. Set the ATA bit

3. Set the RDY bit

4. Assert EBL and EXC lines.

The data transfer command (Read or Write) will be aborted, and the RP04 will wait until the interrupt is serviced.

NOTE

Upon setting the SKI error bit, it is essential for the RDY bit to set in order to allow a Recalibrate command, Drive Clear command, or INIT pulse to clear the error condition.

If the positioner trouble is *not* catastrophic (UNS bit is not set), the RP04 will automatically issue a Recalibrate command. Until the recalibrate operation is complete, the RP04 will maintain a busy status but the EBL and EXC lines will be asserted to indicate forced termination.

A successful completion of a recalibrate operation will:

1. Reset the Current Cylinder Address register

2. Set the ATA bit.

The software can retry the operation (following a drive clear) as follows:

1. Reissue the data transfer command (Read or Write) with the implied seek

2. Issue a Seek command first, before issuing the data transfer command.

3.5.2.7 Mid-Transfer Seek Operation – On an extended read or write, the RP04 can perform one-cylinder seeks (spiral read/write) when the last sector on the last data track on the cylinder is read and the software wishes to continue (RUN line remains asserted).

For example, if the Desired Sector/Track Address register contains a track address of 18 and a sector address of 21 (22-bit sector mode), and RUN line is high at the fall of the EBL pulse, the RP04 will:

1. Increment the Desired Cylinder Address register by one

2. Reset the desired track field of the Desired Sector/Track Address register

3. Reset the desired sector field of the Desired Sector/Track Address register.

The incrementing of the Desired Cylinder Address register will automatically initiate a seek unless the RUN line is unasserted at the fall of the last EBL pulse.

A one-cylinder seek in the RP04 requires 7 ms. Assuming 0.8 ms/sector, the one-cylinder seek corresponds to about nine sectors; when the one-cylinder seek is complete and the RP04 resumes the read operation, the next sector on the new cylinder's track 0 to be encountered will be sector 10. The sector address on the Sector Address register is for sector 0.

Since one revolution in the RP04 requires 16.7 ms, the 7 ms required for a one-cylinder seek is less than half a revolution. To address sector 0 on track 0 of the new cylinder, the software must wait for a full revolution (16.7 ms).

On an extended read or write operation where a mid-transfer seek is involved, the RUN line remains asserted for a complete revolution before the first SCLK from sector 0 of track 0 of the new cylinder. This time is required whether or not: (1) sector 0 is addressed using the mid-transfer seek approach; or (2) the software terminates the data transfer command on track 18, sector 21 of the previous cylinder, initiates a seek to the next cylinder, and reissues the data transfer command to continue the operation.

Using the mid-transfer seek, the operation is done automatically. Without the mid-transfer seek, a few commands (control and data transfer) would be required, but the data bus would be free during the seek.

NOTE

It is possible for a data transfer operation to begin with an implied seek (usually more than one cylinder) followed by mid-transfer seeks for as long as the RUN line remains high at the fall of each EBL pulse. During a mid-transfer seek operation, the PIP bit will *not* be used.

3.5.2.8 Termination – With mid-transfer seeks, it is possible to transfer data across cylinder boundaries without having to issue a Seek command to change cylinder addresses. If the sector being operated is the last addressable sector on the data pack, the conditions will be as follows:

Cylinder Address Register = 410 (maximum)
Desired Sector/Track Addressed Register
Track Field = 18 (maximum)
Sector Field = 21 (maximum on a 22-sector pack)

After transferring that sector, the RP04 will raise the EBL pulse following the ECC check on sector 21. Simultaneously, the RP04 will set the Last Sector Transferred bit (RPDS, bit 10). If the RUN line remains asserted, the address overflow error (RPER1, bit 9) will be set.

3.5.2.9 Error Handling – A mid-transfer seek error is similar to that described for the Seek command in Paragraph 3.5.2, except that the EBL pulse and the EXC line are asserted in this case since no data transfer will take place.

3.5.3 Recalibrate Command (07_8)

A Recalibrate command can be issued by the software when a mispositioning has been suspected (headers do not compare). This command will cause the RP04 positioner to position the heads over cylinder 0. A Recalibrate command is normally issued by the software after a possible seek error is detected and is also automatically performed with each head load sequence.

Neither a Drive Clear command or an INIT pulse will cause a recalibrate operation. Upon recognizing a Recalibrate command and the GO bit set, the RP04 will:

1. Set the PIP bit
2. Reset the DRY bit
3. Initiate the recalibrate operation.

NOTE

During recalibration, the contents of all registers associated with positioning are ignored. When the positioner is addressing cylinder 0 and is settled in that position, the RP04 will reset the PIP bit, set the DRY bit, and set the ATA bit. At this point, the RP04 is ready to accept a new command.

In addition to causing the positioner to return to cylinder 0, the Recalibrate command will clear the Current Cylinder Address register and the Offset register (except for the HCI, ECI, and FMT 22 bits). For a power-up/cycle-up case, the RP04 will automatically execute Recalibrate and Drive Clear commands prior to issuing DRY to the RH11. The Drive Clear command clears the Maintenance register as well as other registers during power up.

In the event of device errors, the appropriate error bits in the Error registers are set and may cause the UNS bit (RPER1, bit 14) to set, depending on the error. The SKI bit will also be set to indicate an incomplete recalibration operation.

The RP04 specifications for positioner timing are as follows:

One-cylinder seek	7 ms
Average seek	27 ms
Maximum seek	50 ms
Average rotational latency time	8.33 ms

The duration of a recalibrate operation is approximately 500 ms maximum.

3.5.4 Offset Command (15_8)

The Offset command involves moving the positioner in small increments from the track centerline in either the forward or reverse direction. This operation offers additional data recovery attempts over that provided by the ECC capability when an ECC error is detected.

The RH11 issues an Offset command, which uses the contents of the Offset register to determine the offset. Nine lines are required by the RP04 to specify the offset direction and address. If an ECC hard error occurs, three offset positions (±400, ±800, ±1200 μin.) should be used, as shown in Table 3-2. However, it will be up to the software to establish the offset values. Following the -1200 μin. try, any seek, read, or write to *another* cylinder will automatically cause the positioner to return to centerline prior to executing the command.

At the completion of the offset and when the positioner is settled, the device logic will:

1. Reset the PIP bit
2. Set the DRY bit
3. Set the ATA bit.

Upon recognizing the above conditions, a Read command should be issued to the cylinder and track in order to recover the data.

To understand the offset operation, assume that the data recovery at +400 μin. offset was not successful. The number of tries on this position is immaterial at this point. Consequently, the programmer should reload the Offset register with a new offset value and direction (-400 μin.), and the GO bit should be set. The RP04 will initiate the offset operation and:

1. Set the PIP bit
2. Reset the DRY bit.

At the completion of the offset operation, the RP04 will:

1. Reset the PIP bit
2. Set the DRY bit
3. Set the ATA bit.

With the positioner offset at -400 μin. from centerline, the programmer should issue a Read command to recover the data from the sector in error.

Table 3-2
Offset Positions

Position	Code Word OF0 – OF7 and Offset Address (μin.)								Value/Direction
	OF7 DIR	OF6 –	OF5 800	OF4 400	OF3 200	OF2 100	OF1 50	OF0 25	(μin.)
1st offset	0	0	0	1	0	0	0	0	+400
2nd offset	1	0	0	1	0	0	0	0	-400
3rd offset	0	0	1	0	0	0	0	0	+800
4th offset	1	0	1	0	0	0	0	0	-800
5th offset	0	0	1	1	0	0	0	0	+1200
6th offset	1	0	1	1	0	0	0	0	-1200
Return to centerline									

Now assume that the data recovery at -400 μin. *was* successful. The Read command would terminate as normal. The positioner will now remain in the -400 μin. offset position. The software can proceed with another command in three ways:

1. *Seek to Another Cylinder (Command, Implied or Mid-Transfer Seek)* – Upon recognizing a seek operation to another cylinder, the RP04 will automatically return the positioner to track centerline before initiating the seek operation. Initiating the return of the positioner to centerline is done as follows:

   - Set PIP bit
   - Reset the DRY bit.

   After the positioner returns to the track centerline, the RP04 will execute the Seek command. At the completion of the Seek command, the RP04 will clear the Offset register.

2. *Read to Another Track of the Same Cylinder* – If the software issues a Read command to another data track on the *same* cylinder, the positioner will perform the Read command while in the offset state.

3. *Write on Another Track on the Same Cylinder* – The RP04 will *not* permit a Write command to be executed with the positioner in the offset state. Upon recognizing a Write command, the RP04 will return the positioner to track centerline automatically before executing the write operation.

   NOTE

   Any incomplete offset will cause the Seek Incomplete (SKI) bit to set and an automatic recalibrate to occur.

4. Execute a Return to Centerline command.

3.5.5 Return to Centerline (RTC) Command (17_8)

The RP04 will not allow the software to initiate a Write command while the positioner is in offset. The software can cause an RTC command to take place in one of the following ways:

1. *RTC Command* – From an offset position, the software can issue an RTC command through the Control register. Upon the termination of this command (approximately 10 ms), the positioner will be addressing the track centerline (null position). Following the completion of an RTC command, the ATTN line will be set.

2. *Automatic RTC Execution* – If a Write command is issued to the RP04 in the normal mode, with the positioner in offset, the RP04 will automatically perform an RTC before the new Write command can be executed. Upon returning to track centerline, the device will execute the Write command (following the completion of the RTC operation).

   NOTE

   An automatic RTC will also be performed by the RP04 if a Seek or Recalibrate command is issued while the positioner is in offset.

An automatic execution of an RTC will *not* set the ATTN line at the completion of the RTC operation.

Since the RTC command is a mechanical positioning operation, the SKI error bit will be set if a positioning error is detected. An automatic recalibrate will occur following the positioning error.

3.5.6 Search Command (31_8)

When a Search command is issued, the device compares the sector counter with the Desired Sector/Track Address register (RPDA). When they match, the RP04 will assert the ATTN line, causing an interrupt to the system.

The software should not specify the sector block which is to be read, but should specify one sector (or more) before it, so that the system can issue the appropriate command and read the required sector. The RP04 will assert the ATTN line to indicate a sector address match. This is the only time the ATTN line is used to indicate a sector address match. During a normal Read or Write command, the ATTN line is not used even though a header search may be occurring.

The purpose of the Search command is similar to that of the Look-Ahead register feature which allows the software to look ahead and optimize the disk revolution.

An unsuccessful completion of a Search command occurs when a sector count/desired sector address match is not made during a search operation. In this case, the OPI bit is set after two index pulses have been encountered.

3.6 DUAL CONTROLLER OPTION

The dual controller option in the RH11/RP04 subsystem provides the capability for two controllers to access the same RP04 Drive. Figure 3-6 shows the dual controller configuration. Note that the eight RP04 Drives are daisy chained and that the two controllers can be attached to the same or to two different central processors.

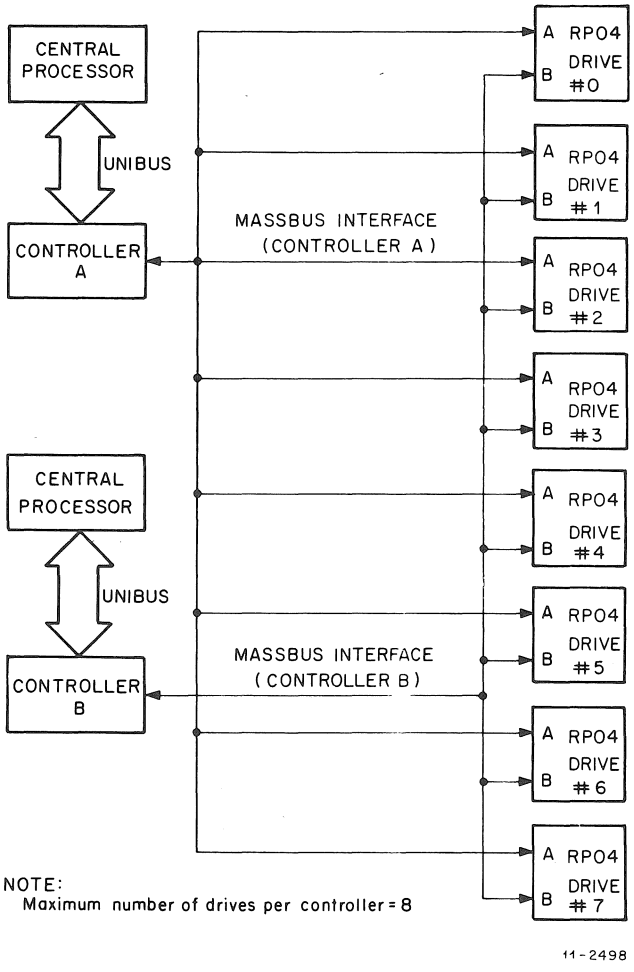


Figure 3-6 Dual-Controller Configuration

NOTE

It is possible for the two central processors to be a PDP-11 and a PDP-10 since both can interface to the Massbus. The PDP-11 must operate in 16-bit mode while the PDP-10 can operate in 16-bit or 18-bit mode.

A drive with the dual controller option has three operational states determined by the setting of the CONTROLLER SELECT switch:

1. Drive connected to Controller A (A switch position).
2. Drive connected to Controller B (B switch position).
3. Programmable (A/B switch position).

When the drive is connected to Controller A, *only* Controller A can read or write the drive's registers (except for the Attention Summary register). Similarly, when the drive is connected to Controller B, *only* Controller B can read or write the drive's registers.

In the programmable state, the drive is not connected to either controller, but its registers can be read or written on a first come, first served basis.

3.6.1 Unseized Operation

The unseized state occurs when the drive is not connected to either controller and the CONTROLLER SELECT switch is in the A/B position.

The drive can be switched to the alternate controller by the CONTROLLER SELECT switch on the RP04 control panel, or it can switch to the alternate controller when in the unseized state if:

1. The alternate controller *writes* into any register (including illegal registers)
2. The alternate controller *reads* the Control register
3. The alternate controller writes the ATA bit associated with a specific drive in the Attention Summary register.

As an example, if the drive is in the unseized state and Controller A reads the Control register, it will seize the drive.

3.6.2 Seized Operation

Seized operation occurs when the drive is logically connected to one controller.

NOTE

The drive is seized by Controller A when the CONTROLLER SELECT switch is in A position, by Controller B when the CONTROLLER SELECT switch is in B position, or by either controller when the CONTROLLER SELECT switch is in A/B position.

If the drive is seized by Controller B, for example, *writing* any drive register from Controller A is ignored by the device logic; however, the drive will store the fact that Controller A has requested use of the drive in the Port Request flip-flop. Every request by Controller A to read the Control register (RPCS1) will cause the RP04 to send 0s (accompanied by the TRA pulse) to the controller, indicating that the device is reserved by the other controller. Since the system operates with odd parity, the RP04 will force a one parity bit with each transmission of 0s through port A.

NOTE

If the drive is seized by Controller B, the Drive Present (DPR) bit will be set for Controller B and reset for Controller A. No special handling is required by the RP04 to process the DPR bit, because, if Controller A requests a read of the Control register (RPCS1), the RP04 will send all 0s (accompanied by the TRA pulse). The same situation occurs for the DRY bit (0s sent to Controller A, indicating that the device is busy).

If, upon cycling up (indicated by setting of the MOL bit), the device recognizes the CONTROLLER SELECT switch to be in the A/B position, it will set the Programmable (PGM) bit. Although the RP04 may be occupied by one controller or the other, the status of the PGM bit is not physically altered.

The RP04 contains the following Status register and Control register bits for dual controller operation.

Status Register (RPDS)

- Programmable (PGM) – This bit is set when the CONTROLLER SELECT switch on the RP04 control panel is in A/B position and indicates that the drive is equally available to both controllers.
- Drive Present (DPR) – This bit is set for the controller which has seized the drive. If the second controller attempts to access the Status register, the RP04 will transmit all 0s (accompanied by the TRA pulse) and cause the DPR bit to appear reset. The DPR bit indicates that the drive is ready to communicate with the controller which has seized it.
- Drive Ready (DRY) – This bit is set for the controller which has seized the drive and is set on the completion of an operation. The DRY bit is the complement of the GO bit which is set at the initiation of an operation. If the second controller attempts to access the Status register, the RP04 will transmit all 0s (accompanied by the TRA pulse) and will cause the DRY bit to appear reset (indicating device busy).
- Volume Valid (VV) – The RP04 implements two Volume Valid bits: VV-A and VV-B. These are used to indicate when a disk pack may have been changed; therefore, the program should not assume anything about the identity of the pack. VV-A is accessible to Controller A only; VV-B is accessible to Controller B only. The status of either bit is displayed in bit 6 of the Status register (RPDS). Bit 6 of the Status register can be examined by each controller and will indicate the pack status for that controller. If Controller A issues a Pack Acknowledge command, the VV bit for Controller A is *set*. If Controller B does not issue a Pack Acknowledge command, the VV bit for Controller B is *reset*.

Control Register (RPCS1)

- Device Available (DVA) – This bit will be set in the Control register which has seized the drive. If the second controller attempts to access the Status register, the RP04 will transmit all 0s (accompanied by the TRA pulse). This will cause the DVA bit to appear reset to the second controller.
- Pack Acknowledge Command (23_8) – Upon recognizing this command in the Status register, the RP04 will set the VV bit for the controller issuing the command.

3.6.3 Switching to Other Controller and Time-Out

When a controller terminates its operation, it must issue a Release command to release the drive.

NOTE

The RP04 will time out if it is occupied by a controller and a Release command is not received from that controller 1 second after termination of the last command transmitted to the RP04. In this case, the device is returned to the unseized state. The 1-second time-out does not apply if the controller is selected via the CONTROLLER SELECT switch.

Assume Controller B has seized the drive and Controller A has requested it. When Controller B issues the Release command, the RP04 will:

1. Set the PGM bit in the Drive Status register
2. Maintain the DPR bit set to Controller A
3. Set the Drive Available (DVA) bit for Controller A
4. Set the ATA bit to Controller A.

Upon recognizing the ATTN line being asserted, Controller A will take advantage of the interrupt and will initiate a command to the RP04. With the drive seized by Controller A, Controller B will receive the same responses that Controller A was receiving when it requested the drive.

3.6.4 Returning to the Unseized State

Upon recognizing the Release command from Controller B, the RP04 will check the Port A Request flip-flop to determine if the RP04 has been requested by Controller A. If this flip-flop is not set, the device logic will return to the unseized state (PGM is already set) and the DVA bit is set in the Control register. If the flip-flop is set, Controller A will seize the drive and bypass the unseized state.

3.6.5 Device Seize from Unseized State

When the RP04 is unseized by either controller, it is equally available to both. If a controller reads a drive register (including illegal registers), the RP04 will immediately connect to that controller for the duration of the register read operation. This constitutes a momentary transition.

If a controller writes any register (including illegal registers), the RP04 will immediately connect to that controller and remain seized to that controller until a Release command or a 1-second time-out is received.

Table 3-3 shows the controller action and the corresponding RP04 responses to each action. For example, if Controller A attempts to read the Control register and the drive is in the unseized state with the CONTROLLER SELECT switch in the A/B position, the RP04 will immediately switch to Controller A, set the DVA bit, and read the function code. If the drive is already seized by Controller A, the RP04 will merely set the DVA bit and read the function code. If the drive is already seized by Controller B, Controller A will read all 0s.

3.6.6 Manual CONTROLLER SELECT Switch

The CONTROLLER SELECT switch on the RP04 control panel is a three-position switch designated A, B, and A/B. With the switch in position A, the RP04 is seized by Controller A; with the switch in position B, the RP04 is seized by Controller B; and with the switch in position A/B, the RP04 will be totally programmable and either controller can access the RP04 as dictated by the software. In the A and B positions, the RP04 is dedicated only to the controller selected and is not alterable by the software.

To avoid accidental activation of the switch, the logic is implemented to allow switching to occur only when the machine is cycled up (indicated by the setting of the MOL bit).

For single controller operation, the switch is interlocked to Controller A and manipulating the switch has no effect on the system.

3.6.7 Attention Summary Bits

The RP04 implements two ATA flip-flops: ATA-A and ATA-B. When Controller A has seized the RP04, the ATA-A bit is displayed in the ATA position of the Status register; ATA-A is accessible to Controller A only. When Controller B has seized the RP04, the ATA-B bit is displayed in this bit position; ATA-B is accessible to Controller B only.

The ATA-A bit is always accessible to Controller A regardless of the setting of the CONTROLLER SELECT switch; similarly, the ATA-B bit is always accessible to Controller B.

Reading of the Attention Summary register by either controller will receive the normal response. Even though Controller A is selected, Controller B can read the RP04 registers; however, zeros will be read back to Controller B, indicating that this controller is not logically connected to the drive.

Table 3-3
Register Accesses on Dual Controller Operation

Action Performed by Controller A	Drive Response with Respect to Controller A		
	Drive in Programmable	Drive Seized by A	Drive Seized by B
Read the Control register.	Immediately switches to state A; reads the function code.	DVA = 1; reads the function code.	DVA = 0; reads all zeros.
Write the Control register.	Immediately switches to state A; loads the function code.	Loads the function code. (Switches to neutral if the function is release.)	The function code is ignored.
Read the Status register.	Reads the status bits; PGM = 0; DPR = 1. No change of state.	Reads the status bits; PGM = 1; DPR = 1.	Reads all zeros; PGM = 1; DPR = 0.
Read any other drive register.	Reads the register; no change of state.	Reads the register.	Reads all zeros.
Write any other drive register.	Immediately switches to state A; loads the register.	Loads the register.	The word is ignored.

NOTES

1. It is assumed that the CONTROLLER SELECT switch is in A/B position.

2. If Controller A has seized the drive, and Controller B requests it, the drive will switch to Controller B as soon as a Release command is issued. When this occurs, the ATTN line is asserted.

3.6.8 START/STOP and STANDBY Switches

The RP04 contains two cycle-up control switches: START/STOP and STANDBY.

When the drive is first powered up (logic power applied), the spindle is stopped and the heads are unloaded. The Volume Valid status bits (both VV-A and VV-B) are reset by the drive whenever the RP04 cycles up.

NOTE

The Pack Acknowledge command (or the Read-In Preset command) causes VV-A to set (if the command was executed from Controller A) or causes VV-B to set (if the command was executed from Controller B).

If VV-A is reset, the only valid commands from Controller A are Pack Acknowledge, Read-In Preset, and Drive Clear. (The same is true for VV-B and Controller B.) Drive Clear does not cause VV to be set.

NOTE

If ERR is set, the only valid command is Drive Clear.

Whenever the drive makes the transition from the spindle stopped-heads unloaded state to the spindle up-heads loaded state, ATA-A and ATA-B are both set, and VV-A and VV-B are both reset. (If the drive is seized by Controller A, ATA-B remains set and is visible in the Attention Summary register on Controller B.)

The expected response from Controller B, assuming the drive is first seized on A, would be:

1. Processor B reads the Attention Summary register and sees ATA-B.

2. Processor B writes the Attention Summary register, clears ATA-B, and causes Request B to be set.

3. Processor B reads the Status register, sees all 0s, but knows that Request B is set. (If Controller B seizes the drive in step 2, processor B will see the appropriate status in step 3.)

The STANDBY switch has no effect until the Unload command is initiated. Upon initiation of this command, the heads will unload and the spindle will power down. If, in this condition (STANDBY light on), the START/STOP switch is pressed, there is no change of state in the drive. The only condition that will allow the spindle to power up and the heads to load is the pressing of the STANDBY switch.

Whenever the drive makes the transition from the standby state to the spindle up-heads loaded state, it resets both VV-A and VV-B, and sets both ATA-A and ATA-B.

Whenever the drive makes a transition from the spindle up-heads loaded state to the spindle down-heads unloaded state, the MOL bit is reset and the ATA bit is set.

If an Unload command has not been initiated, the spindle is down, and the heads are unloaded, the controller may be seized, but the 1-second time-out applies. (Note that the time-out does not apply while in the standby state.)

3.6.9 Persistent Error Handling

Assume that the RP04 is seized by Controller A and a persistent error occurs which cannot be cleared by a Drive Clear or an Initialize command.

If Controller B has requested the RP04, the RP04 will eventually be seized by Controller B through the 1-second time-out. The ATA bit will be set, but it will have a double meaning. Controller B will determine that an error condition also exists by reading the Status register and discovering the ERR bit set.

If Controller B has *not* requested the RP04, the RP04 will revert to the unseized state through the 1-second time-out. In this case, Controller B will receive no ATTN when the drive goes to the unseized state from Controller A. Controller B will be notified of the error condition when it attempts to seize the drive (by writing the drive registers).

NOTE

In the event of a persistent error, the software can clear the ATTN bit by writing a 1 into it.

Subsequent addressing of the Attention Summary register by the Controller will *not* cause the ATTN bit, belonging to the drive with the persistent error, to be asserted. Any attempt to write on any of the other drive registers, however, will cause the ATTN line to be asserted.

3.6.10 Initialize in Dual Controller Operation

The RP04 Drive will honor an Initialize command issued separately from either controller under the following conditions:

1. An Initialize issued by Controller A will clear ATA-A and set VV-A but has no effect on Controller B. The converse is true for an Initialize issued by Controller B. (ATA-B will clear and VV-B will be set), with no effect on Controller A.

2. If the device is seized by Controller A and an Initialize is initiated by Controller B, the Initialize from Controller B is ignored. Conversely, if the device is seized by Controller B and an Initialize is initiated by Controller A, the Initialize from Controller A is ignored.

3. When the device is in the unseized state, an Initialize from either controller will be accepted.

3.7 ERROR CORRECTING CODE PROCESSING

The RP04 contains error correcting code (ECC) logic which will generate, detect, and correct an error by reconstructing a portion of the data. A burst error correcting code is employed which will correct an error that falls within the specified burst. The actual location of the burst within the data field is immaterial. Any error outside the burst field will be detected but not corrected. The hardware treats this as an ECC hard error (noncorrectable).

The RP04 hardware contains an ECC Position register and an ECC Pattern register. The ECC Position register contains the address of the first bit of the error burst within the data field, which identifies the exact location of the error burst to the software.

NOTE

The data words are designated as bits 1 through 16, not 0 through 15. Consequently, if the second data word contained an error burst, the contents of the ECC Position register would contain 17, and not 16.

The data field in each sector includes a 32-bit ECC redundancy check. If no error is detected in the data field after the last word has been read, the Read command will normally terminate without any time delay.

If any error has been detected in the data field (and ECC hardware is enabled), the procedure to correct this error is accomplished by the ECC hardware, which will go through a routine to isolate the 11-bit error burst in the data field. The exact location of this burst is available to the software.

NOTE

If an error has occurred and has been detected by the ECC hardware following transmission of the data block, the Data Check (DCK) error bit will be set and remain set throughout the entire correction process (providing the ECI bit is reset).

The software will then take the ECC burst pattern and will proceed to find the bits in error and correct them by inverting their state as shown in Figure 3-7.

The software will count the data bits in the data stream starting with bit 1 of word 1. When it reaches a count of 2055, as shown in Figure 3-7, it will stop. The next 11 bits represent the error burst or the segment of bits containing the error. These bits are compared with the 11-bit error burst on a bit-by-bit basis. For each 1 bit in the error burst, the corresponding bit in the data field is complemented. (Actually, the bits are exclusively ORed.) After the 11 bits have been examined and the appropriate bits corrected, the rest of the data field is correct.

NOTE

The 11-bit error burst contained in the ECC Pattern register consists of bits 0 through 10 of the data word. The remaining high-order bits (11 through 15) are always zeros.

Figure 3-8 shows an example of the error correction process. It is assumed that the data field is all 0s and an error burst of five 1s occurred in bits 14 through 18. The RP04 hardware loads the ECC Position register with a value equal to 8. This value is calculated by the hardware and indicates that the 11-bit error burst begins with bit 8 in the data field. Consequently, the software should count 8 bits beginning with word 0 of the data field in memory and extract the next 11 bits, including bit 8.

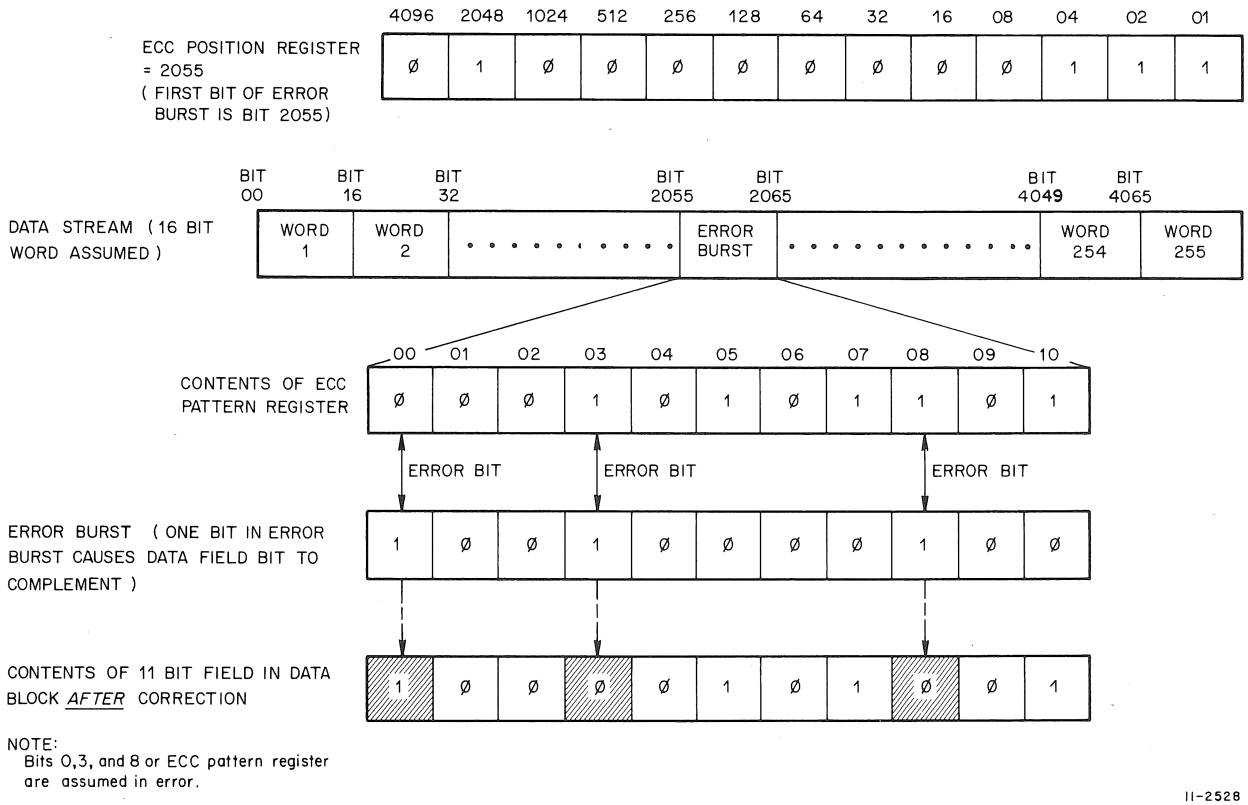


Figure 3-7 Example of Error Correction Process

The error burst is exclusively ORed with the contents of the ECC Pattern register, which was loaded with a pattern calculated by the RP04 hardware. For each 1 in the ECC Pattern register, the corresponding data bit in the data field is complemented, which corrects the bits in the error. This process is accomplished by the software.

NOTE

If the error burst is located within the first 11 bits of word 0, the ECC Pattern register will display the error bits in their actual position. In this case, the contents of the ECC Position register will be 1.

Figure 3-9 shows a second example where the data field is assumed to be all 0s, and an error burst of 1s occurred between bits 11 through 16. The RP04 hardware loads the ECC Position register with five (calculated by the RP04 hardware), indicating that the error burst begins with bit 5 of the data field. The software counts to bit 5, extracts the next 11 bits, including bit 5, and exclusively ORs these bits with the contents of the ECC Pattern register, which was also calculated and loaded by the RP04 hardware. For each 1 bit in the ECC Pattern register, the corresponding bit in the data field is complemented as shown.

3.7.1 Noncorrectable Errors

Using the burst error method described, two types of errors will be detected but not corrected:

1. Any error field larger than the 11-bit burst
2. Two isolated dropped bits (for example, a bit in word 1 and a bit in word 23).

If an uncorrectable error occurs, the RP04 will indicate this by asserting the ECH Hard Error bit (RPER1, bit 06). The software may desire to reread and, depending on the nature of the error, the second read may be successful. For an ECC uncorrectable error, the contents of the ECC Position register and the ECC Pattern register are insignificant.

The ECC field in the sector block always follows the 256-word data block. The data block is guaranteed to be 256 words in length regardless of whether the 16-bit mode or 18-bit mode is employed. After transmitting the required 256 data words, the RP04 logic will inhibit communication with the RH11 for approximately 5 μs until the ECC field is shifted through the ECC register for a possible read error detection.

3.7.2 Error Correction Techniques

Error correction in the RP04 can be enabled or inhibited by the Error Correction Inhibit (ECI) bit (RP04, bit 11). If this bit is asserted, the RP04 logic will inhibit error correction when an error is detected. The read operation will continue as if no error occurred. If this bit is negated, the RP04 logic will enable the ECC circuitry when a read error is detected.

Optimum system performance dictates that the ECI bit should be enabled on the first read operation. With ECC enabled, five possibilities could arise:

1. Correctable error on first pass
2. Noncorrectable error on first pass
3. Noncorrectable error on any pass after first pass
4. Correctable error in offset position
5. Noncorrectable error after 28 attempts.

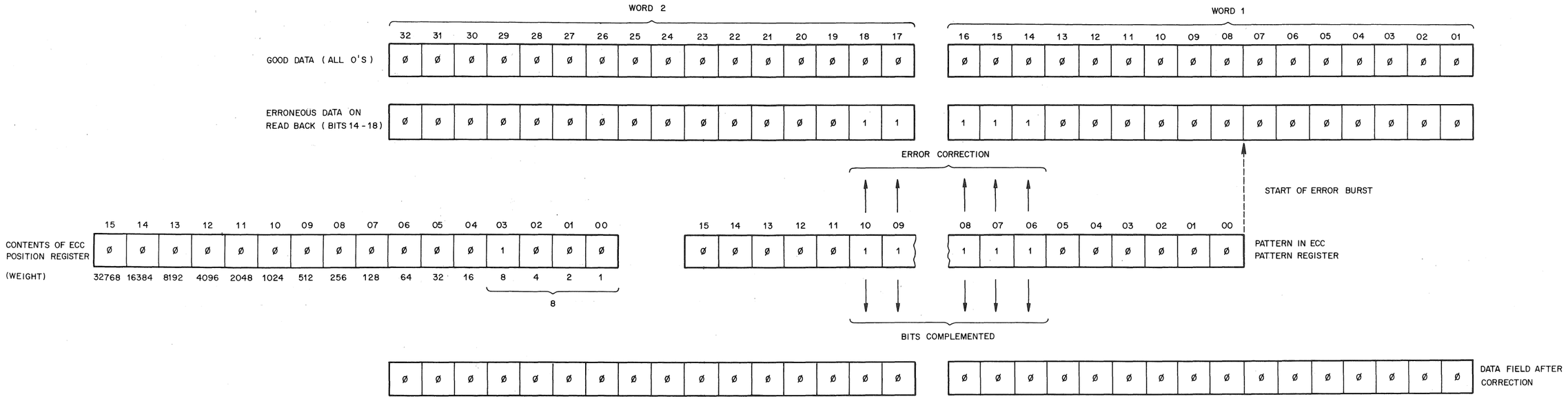
These cases are described in the following paragraphs, and assume that ten sequential sectors are to be read from the disk, with a read error occurring in sector 5.

Correctable Error on First Pass – The procedure for this case is:

1. Read sectors 1 through 5.
2. Correct sector 5 by the ECC logic.
3. Lose one revolution (as a result of the error correction).
4. Reinitiate the GO bit by reloading the Control register (RPCS1).
5. Read sectors 6 through 10.

NOTE

The EBL pulse at the end of sector 5 automatically increments the desired sector field of the Desired Address register (RPDA) to sector 6. As a result of this, only the GO bit and RUN line need to be asserted during the extra revolution to recover the data in sectors 6 through 10.



NOTES:
1. NUMBER IN ECC POSITION REGISTER IS DETERMINED BY RP04 HARDWARE.
2. PATTERN IN ECC PATTERN REGISTER IS DETERMINED BY THE RP04 HARDWARE.
3. SOFTWARE TAKES VALUES IN (1.) AND (2.) AND PERFORMS ERROR CORRECTION.
4. ALL 1s IN ERROR BURST CAUSE CORRESPONDING BITS IN DATA FIELD TO BE COMPLEMENTED (EXCLUSIVE OR).

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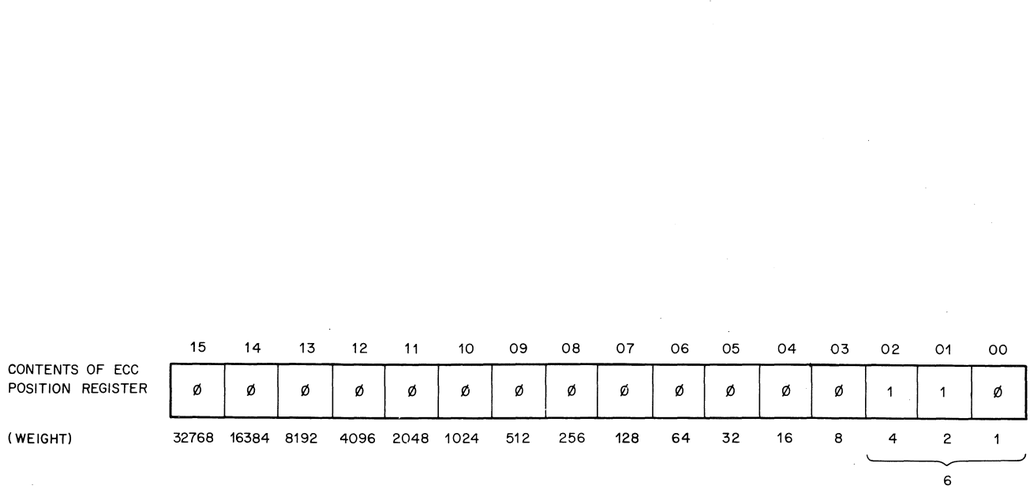
Figure 3-8 Example of Five-Bit Error Correction



NOTES:
1. NUMBER IN ECC POSITION REGISTER IS DETERMINED BY RP04 HARDWARE.
2. PATTERN IN ECC PATTERN REGISTER IS DETERMINED BY THE RP04 HARDWARE.
3. SOFTWARE TAKES VALUES IN (1.) AND (2.) AND PERFORMS ERROR CORRECTION.
4. ALL 1s IN ERROR BURST CAUSE CORRESPONDING BITS IN DATA FIELD TO BE COMPLEMENTED (EXCLUSIVE OR).

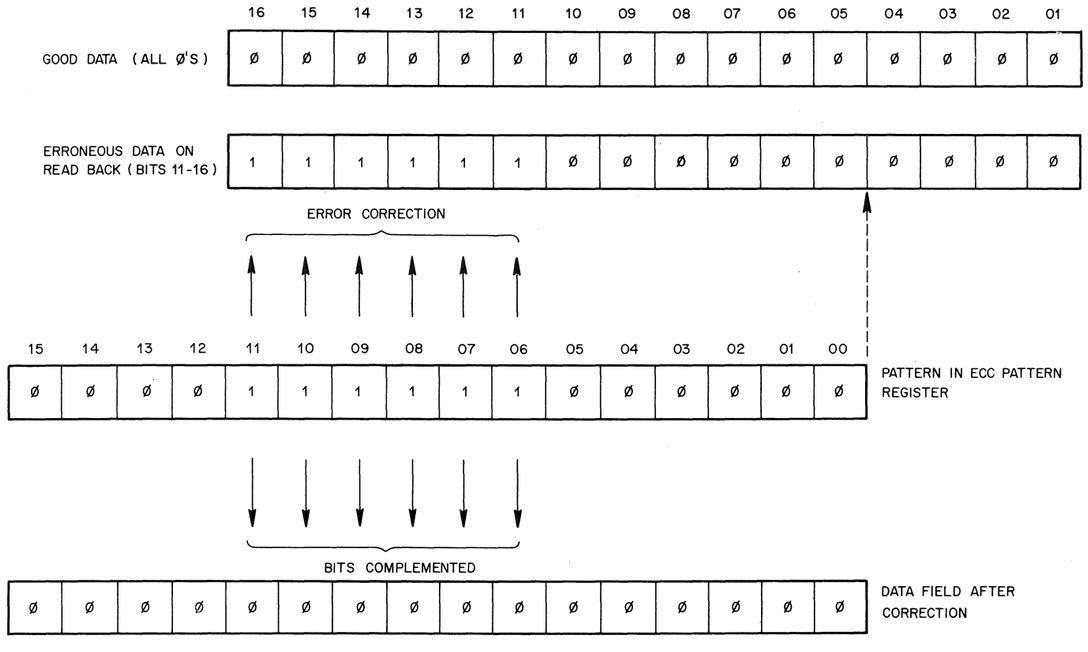


Figure 3-9 Example of Six-Bit Error Correction

Noncorrectable Error on First Pass – This case occurs as a result of an ECC hard error (RPER1, bit 06 asserted) occurring at the end of the ECC process. Even though sector 5 is not corrected in this case, the Desired Address (RPDA) register is still incremented, and is now addressing sector 6. The procedure is as follows:

1. Read sectors 1 through 5.
2. Attempt to correct the ECC hard error in sector 5.
3. Lose one revolution (due to error correction attempt). During this revolution, reload the Desired Address (RPDA) register and reinitiate the Read command by reasserting the GO bit and the read function code.
4. Attempt to reread sectors 1 through 10 on the second revolution. (ECC is still enabled.)
5. Attempt to correct the error in sector 5. Assume that it is successfully corrected.
6. Lose a second revolution (due to error correction).
7. Reassert the GO bit by loading the Control register (RPCS1).
8. Read sectors 6 through 10.
9. Terminate the command.

This example assumed that ECC was successful on the second try. However, two disk revolutions (approximately 33.4 ms) were lost in addition to the time required to reload the appropriate Control registers.

It is possible that on the second pass of reading sectors 1 through 10 that sector 5 may come up with no read errors, depending on the type of error discovered. There is a good probability that the data would be recovered on the second pass without the need for ECC. Typical errors of this type are isolated dropped bits within the same record or a speck of dirt under the head on that spot, which disappeared on the second revolution.

Noncorrectable Error on Any Pass After the First Pass – In this instance, an ECC hard error (RPER1, bit 06) occurs for the second time. This case is similar to the "noncorrectable error on first pass" case except that another disk revolution will be lost. Figure 3-10 represents a flow diagram of the procedure. The software should attempt to recover the data (using ECC) 16 times before the offset recovery procedure is employed.

There are six recommended offset positions (±400, ±800, and ±1200 microinches). It is recommended that two tries of each position (with ECC enabled) be attempted for a total of 12 attempts. Consequently, the software should attempt to recover a read error for a total of 28 tries (16 tries in the null position and 12 tries in the offset position), before the error is declared unrecoverable.

NOTE

The actual number of revolutions lost during the 28 tries could be in excess of 28 if the read error was corrected the second time around in the sixth and last offset position.

Most errors that are corrected occur with the RP04 in the null position. If the error is not corrected by the third try using ECC, additional attempts in the null position and offset position are not likely to be successful.

Correctable Error in Offset Position – If an error is corrected while in offset, it is usually an indication that the entire data track is generated by a head which was not precisely aligned in relation to other heads. It is probable that the rest of the sectors, in this case, will be recovered in the offset position as well. Therefore, with the positions still in offset, the software should reinitiate the GO bit during the next revolution and read sectors 6 through 10. The Desired Address register has already incremented to sector 6.

NOTE

A Read command to the same track or another track on the *same* cylinder can be executed in offset or in the null position by issuing a Return to Centerline (RTC) command.

Noncorrectable Error After 28 Attempts – Assuming that the read error on sector 5 cannot be recovered after 28 unsuccessful attempts with ECC and offset, the software should take the following steps to recover.

1. After the 28th unsuccessful attempt to recover the error, the software should declare the error uncorrectable to the user.

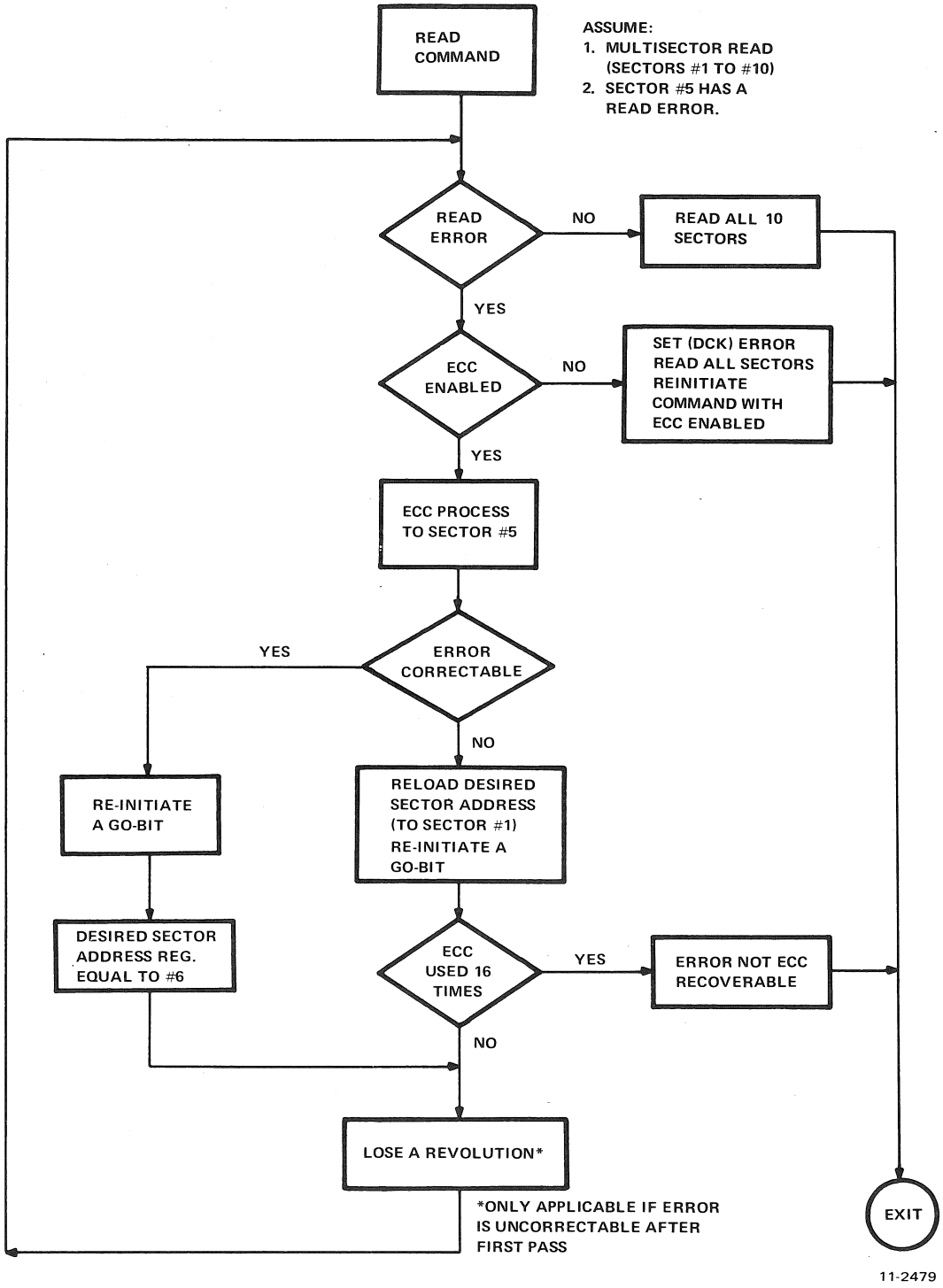


Figure 3-10 Uncorrectable Error Flow Chart Example

2. Issue an RTC command to the RP04. Since the last twelve attempts were made in the offset state, assume that offsetting the positioner will not help in data recovery.

NOTE

An RTC command requires 10 ms for execution versus 16.7 ms for a disk revolution. Consequently, it is possible to execute an RTC and reassert the GO bit (the RPDA register has already incremented to sector 6) during the same revolution (28th attempt) and read sectors 6 through 10.

3. Terminate the command.

If the software wishes to recover sector 5 in spite of the unrecoverable error, the following steps should be taken:

1. Load the Desired Address register with the address of sector 5.

2. Set the Error Correction Inhibit (ECI) bit in the Offset register.

3. Issue a Read command and assert the GO bit. The ECC hardware will indicate a read error, the DCK (Data Check) bit is asserted, the EXC and ATA lines are asserted, but the RP04 will not enter the error correction routine.

3.8 ERROR CLASSIFICATION AND DATA RECOVERY

The RP04 has six different categories of errors, which are tabulated in Table 3-4. All error bits (with the exception of the head load sequence monitoring status bits in category D) cause the ERR bit in the Drive Status register (RPDS) to set. The ERR bit is set in most cases by the Unsafe (UNS) bit in the RPER1 register.

When the ERR bit sets, the software should attempt to recover. The data recovery procedure for each of the six categories is described below.

Category A – If a category A error occurs, the RP04 Drive takes the following action:

1. If the heads are not loaded, they will not be permitted to load.

2. If the error occurs in the middle of the operation, the RP04 will immediately deselect the heads and disable all commands. This is clearly an unsafe condition.

Any of the category A error bits will cause the UNS bit to set in Error register 01 (RPER1) which, in turn, will cause the ERR bit to set in the RPDS register.

If the error occurs prior to head loading, the software should initiate a Drive Clear command or an Initialize and attempt to recover the data again.

If the error occurs during operation, the standard procedure for the device to indicate an unsafe condition is to immediately raise the EBL pulse and EXC line for a minimum of 1.5 μs. Following the negation of EBL and EXC, the RP04 will normally:

1. Reset the GO bit

2. Set the DRY bit

3. Set the ATA bit

4. Raise the ATTN line.

Again in this case, the software should retry by initiating a Drive Clear command or an Initialize.

In either case, however, the software should try to recover three times; if the UNS condition persists, this is considered a hard error and maintenace personnel should be notified.

Category B – The behavior of the device when a category B error occurs is similar to that of category A *except* that if the category B error occurs during operation, the device will *automatically* retract the heads.

The software should attempt to recover as in category A. A Drive Clear command or an Initialize will cause the heads to reload automatically in addition to clearing the appropriate error conditions.

If the heads load successfully, the DRY bit will be set and the software can retry. If the heads do *not* load following three attempts, maintenance personnel should be notified.

Table 3-4
RP04 Error Bits Classification

Category	RP04 Error Bits	RP04 Reaction
A	Write Current Unsafe (WCU, RPER2) Current Sink Failure (CSF, RPER2) Write Select Unsafe (WSU, RPER2) Current Switch Unsafe (CSU, RPER2) Transition Detector Failure (TDF, RPER2) Transitions Unsafe (TUF, RPER2) Write Ready Unsafe (WRU, RPER2) Multiple Head Select (MHS, RPER2) No Head Selection (NHS, RPER2) PLO Unsafe (PLU, RPER2)	These bits cause the unsafe (UNS) bit in RPER1 to set. Category A bits: 1. Prevent head load 2. Deselect the heads 3. Disable the Read, Write, Seek, and Offset commands.
B	30 Volts Unsafe (30VU, RPER2) AC Unsafe (ACU, RPER2) Pack Speed Unsafe (PSU, RPER3) Velocity Unsafe (VUF, RPER3) AC Low (ACL, RPER3) Any Unsafe Except Read/Write (UWR, RPER3) DC Low (DCL, RPER3)	These bits cause the UNS bit in RPER1 to set. Category B bits: 1. Retract the heads 2. Prevent head load 3. Deselect the heads 4. Disable Read, Write, Seek, and Offset commands.
C	Disk Pack Rotation Error (PRE, RPER3) Motor Sequence Error (MSE, RPER2) Failsafe Enabled (FEN, RPER2)	These bits cause the UNS bit in RPER1 to set. Category C bits: 1. Retract the heads 2. Prevent head load 3. Deselect the heads 4. Disable, Read, Write, Seek, and Offset commands. These bits require manual intervention.
D	Seek Incomplete (SKI, RPER3) Off Cylinder (OCYL, RPER3)	Category D bits: 1. Automatically recalibrate 2. Set the ERR bit in the RPDS register.
E	Drive Forward 5 in./sec (DF5, RPDS) Drive Forward 20 in./sec (DF20, RPDS) Drive to Inner Guard Buffer (DIGB, RPDS) Go Reverse (GRV, RPDS) Difference Less than 64 (DL64, RPDS) Difference Equals 1 (DE1, RPDS)	These bits are the head load sequence monitoring bits and are listed in the order in which they occur. By reading the RPDS register, it can be determined how far the head load sequence has progressed.
F	Index Error (IXE, RPER2) Any error bit in RPER1, RPER2, or RPER3 registers	Any of these bits sets the ERR status bit in the RPDS register. The IXE bit does not require a Drive Clear or an Initialize and will reset itself on the next valid index pulse.

Category C – The errors in this category cannot be corrected without operator (manual) intervention. The RP04 reaction when these errors occur is the same as described for categories A and B. In addition to restarting the device, it may be necessary to reset the circuit breaker, depending on the problem. Maintenance personnel should be notified if a category C error occurs.

Category D – When the RP04 detects a Seek Incomplete (or Off Cylinder) error, it will *automatically* recalibrate. To reset the error condition, the software should issue a Drive Clear command or Initialize the drive.

NOTE

Issuing a Recalibrate command internally or an Initialize is mandatory for the RP04, since the recalibrate action will actually clear the SKI error internally. The software need not issue a Recalibrate command in this case.

Following the recalibrate completion, the software should again attempt to recover the data.

The SKI and OCYL error bits will cause identical reactions from the RP04 Drive. SKI or OCYL are not considered unsafe conditions for the drive, unless other error bits are also set.

Category E – These bits are *not* error bits unless the head loading sequence is interrupted. The expected reaction by the software has already been described. None of the bits in category E alone will cause an error.

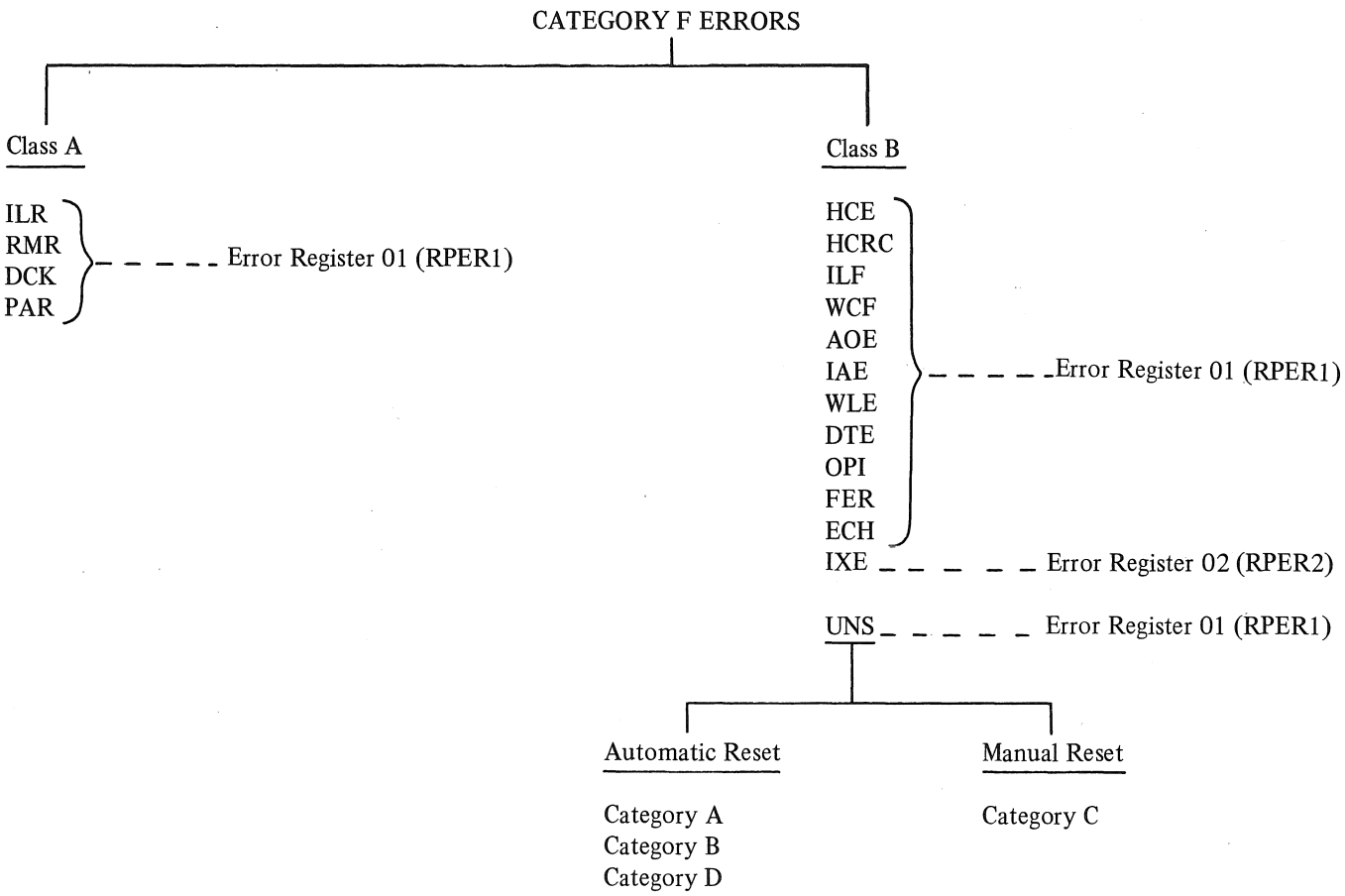
Category F – This category of errors includes essentially all RP04 Drive errors, directly or indirectly. Under this category, there is a further classification of errors as shown in Table 3-5.

- Class A: EXC is asserted immediately but transfer to the end of the current sector is completed and normal EBL is asserted.
- Class B: Both EBL and EXC are asserted immediately. Data transfer stops.

For both class A and B errors, EXC is negated and ATTN is asserted at the trailing edge of EBL.

With the exception of unsafe type errors discussed under the various categories, all others can be cleared through a Drive Clear command or an Initialize operation before another attempt is made by the software.

Table 3-5
Category F Classification of Errors



CHAPTER 4
PROGRAMMING DEFINITIONS AND SPECIFICATIONS

4.1 GENERAL

This chapter describes some of the Massbus signals, clearing methods, and interrupt conditions, and each bit in the RH11 Massbus Controller and RP04 Drive. Also included is an RH11/RP04 register summary chart, which is convenient for rapidly locating a specific bit in one of the subsystem registers.

4.2 DEFINITIONS

This paragraph describes some of the Massbus signals which are used in generating status information.

- Attention (ATTN) – The ATTN line is a shared line which connects from all drives in common to the RH11 Controller. Each drive asserts ATTN (and sets its own ATA bit) whenever it has an error condition (ERR asserted) or has finished executing any movement command.

  The logical expressions for these statements are:

  $ATTN \leftarrow ATA_0 + ATA_1 + \ldots + ATA_7$

  $ATA_i \leftarrow ERR_i +$ completion of a movement command.

  $ERR_i \leftarrow$ any drive error asserted (RPER).

  (i represents the unit select code of a drive, 0 through 7).

- Exception (EXC) – The EXC line connects from the controller to the drive which is performing a data transfer. It is asserted by the drive if an error occurs during the transfer. This line is used to distinguish errors in the drive performing a data transfer from errors signaled by the ATTN line. (A drive which is performing a data transfer never asserts ATTN while the data transfer is underway.)

- End of Block (EBL) – The EBL line is pulsed by the drive performing a data transfer at the end of each sector. The RH11 examines the EXC line only during the EBL pulse.

- Clearing Methods

  Controller Clear – Controller Clear is the action of writing a 1 into the CLR control bit (bit 5 of RPCS2). This causes the following to be cleared:

  All controller errors (RPCS2, bits 15 through 8, RPCS1, bits 15 through 13)

  Silo buffer

  RPBA Unibus Address register and A16, A17

  Unit select U(02:00), IE, PSEL, BAI, and PAT bits

  Errors, function code, and DA register in all drives connected to the RH11 (by assertion of the Massbus INIT signal).

RH11 Error Clear – RH11 Error Clear is the action of writing a 1 into the TRE bit (bit 14 of RPCS1). This causes all controller errors to be cleared (RPCS2, bits 15 through 8 and RPCS1, bits 14 and 13).

Drive Clear – Drive Clear is a command code (11_8) which causes errors, the function code, and the DA register to be cleared in the drive selected by U(02:00).

Table 4-1 shows the various methods used to clear the disk system.

4.3 PROGRAMMING NOTES

This paragraph describes miscellaneous features of the RH11/RP04 subsystem not described in other sections of this manual.

The TRE (Transfer Error) bit is located in the RH11 and is associated only with error conditions during data transfers and error conditions in the controller. The ERR bit is a summary error bit which is located in each drive. Writing a 1 into TRE (RH11 Error Clear) does not affect ERR in any drive. Similarly, a Drive Clear command does not affect TRE in the RH11.

RDY is the "ready" indicator for the RH11 Controller. When RDY is asserted, the RH11 is ready to accept a data transfer command. DRY is the "ready" indicator for each drive. To successfully initiate a data transfer command, both of these bits must be asserted. However, a non-data transfer command (e.g., Search, Drive Clear) may be issued to a drive any time DRY is asserted, regardless of the state of the RDY bit.

When a data transfer command is successfully initiated, both RDY and DRY become negated. When a non-data transfer command (such as Search) is successfully initiated, only the DRY bit becomes negated. Some non-data transfer commands (such as Drive Clear) take so little time to execute that the program will never see the negation of the DRY bit.

The assertion of RDY after the execution of a data transfer command will not occur until the DRY bit is set and the

Table 4-1
Results of Program-Controlled Clearing

ACTION	Clear All RH11 Errors	Clear Silo	RESULTS		
			Clear BA, U(02:00), IE, PSEL, PAT, BAI A16, A17	Assert Massbus INIT	Clear ERR and errors in the drive
Unibus A INIT (Reset instruction execution or console reset)	X	X	X	X	X (all 8 drives)
Controller Clear (Bit 5 in RPCS2 ← 1)	X	X	X	X	X (all 8 drives)
Issue a Data Transfer command (with GO = 1)	X	X			
RH11 Error Clear (Bit 14 in RPCS1 ← 1)	X				
Drive Clear (Function code with GO = 11_8)					X (selected drive only)

controller (RH11) is done. RDY is asserted on the completion of the last Unibus NPR memory cycle and the negation of RUN at the trailing edge of EBL.

If any command other than Drive Clear is issued to a drive which has ERR asserted, the command is ignored by the drive. If a data transfer command is issued to a drive which has ERR asserted, the drive does not execute the command, and the Missed Transfer Error (MXF, bit 9 in the CS2 register) occurs in the RH11.

4.4 INTERRUPT CONDITIONS

The RH11 generates an interrupt in the PDP-11 CPU due to the following conditions:

1. Upon termination of a data transfer (if Interrupt Enable is set when the RH11 becomes ready).

   Interrupt = (RDY ← 1) · (IE)

2. Upon assertion of Attention or occurrence of a controller error (while the controller is not busy and Interrupt Enable is set).

   Interrupt = (SC ← 1) · (RDY) · (IE)

3. When the program writes 1s into it and RDY at the same time.

   Interrupt = (IE ← 1) · (RDY ← 1)

CAUTION

READ-MODIFY-WRITE instruction (BIS, BIC, etc.) with IE bit set will cause an immediate interrupt.

4.5 TERMINATION OF DATA TRANSFERS

A data transfer which has been successfully started may terminate in the following ways:

1. Normal Termination – Word count overflows to 0 and the RH11 becomes ready (RDY ← 1) at the end of the current sector.

2. Controller Error – An error occurs in the CS2 register as indicated below:

   Bit 15 DLT (Data Late)
   14 WCE (Write Check Error)
   13 UPE (Unibus Parity Error)
   12 NED (Nonexistent Drive)
   11 NEM (Nonexistent Memory)
   10 PGE (Program Error)
   9 MXF (Missed Transfer Error)
   8 MDPE (Massbus Data Parity Error)

   Any of these errors sets TRE. The RH11 terminates the data transfer immediately, but waits for the EBL pulse at the end of the current sector before becoming ready.

3. Drive Error – An error occurs in the drive. The drive sets ERR in the RPDS register and at least one bit in the RPER register. The drive also asserts EXC, which causes TRE to set when the next EBL pulse occurs. The RH11 becomes ready after the EBL pulse.

   After the EBL pulse, the drive disconnects from the Massbus data bus and, because ERR is set, ATTN is then asserted.

   In some cases of severe drive errors, the EBL pulse may be artificially generated by the drive before the normal end of the sector.

4. Program-Caused Abort – By performing a Controller Clear or a Reset instruction, the program can cause Massbus INIT to be asserted by the RH11, which aborts all operations on all drives attached to the controller. Status and error information is lost when this is done. The RH11 and RP04 become ready immediately.

4.6 CONTROL (RPCS1) REGISTER (776700)

This register is utilized by the RH11/RP04 to store the disk commands and operational status. The function (command) code designates a function for the drive selected in bits 02 through 00 of the RPCS2 register. Setting the GO bit will cause the drive to recognize the function code in the Control register. The actual execution of the command, however, will not begin until the RUN line is asserted (except for mechanical motion commands).

The RP04 Drive will handle data transfer commands, positioning commands, and housekeeping operations. These are described in Chapter 3.

Figure 4-1 shows the bit format and Table 4-2 defines the bit usage for the RPCS1 register.

Table 4-2
Control (RPCS1) Register (776700) Bit Assignments

Bit		Set By/Cleared By	Remarks
15	SC (Special Condition) Read only	Set by TRE or ATTN or Massbus Control Parity Error. Cleared by Unibus A INIT, Controller Clear, or by removing the ATTN condition.	SC = TRE + ATTN + MCPE
14	TRE (Transfer Error) Read/write	Set by DLT, WCE, UPE, NED, NEM, PGE, MXF, MDPE, or a drive error during a data transfer. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or by loading a data transfer command with GO set.	TRE = DLT + WCE + UPE + NED + NEM + PGE + MXF + MDPE + (EXC · EBL)
13	MCPE (Massbus Control Bus Parity Error) Read only	Set by parity error on Massbus control bus while reading a remote register (located in the drive). Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or by loading a data transfer command with the GO set.	Parity errors which occur on the Massbus control bus while writing a drive register are detected by the drive and cause the PAR error (RPER1 register, bit 03) to set.
12	Not used	Always read as a 0.	
11	DVA (Drive Available) Read only	Set when device is not busy on other port. Reset by device from other port when device is busy on that port.	This bit is used in dual controller configurations.
10	PSEL (Port Select) Read/write	When PSEL = 1, data transfer is via Unibus B; when PSEL = 0, data transfer is via Unibus A. Cleared by Unibus A INIT, Controller Clear, or by writing a 0 in this bit position.	A Unibus select control bit. This bit cannot be modified while the RH11 is performing a data transfer (RDY negated).
9 8	A17 A16 (Unibus Address Extension Bits) Read/write	Upper extension bits of the BA register. Cleared by Unibus A INIT, Controller Clear, or by writing 0s in these bit positions.	Control bits. These bits cannot be modified while the RH11 is performing a data transfer (RDY negated).
7	RDY (Ready) Read only	RDY normally = 1. During data transfers, RDY = 0.	When a data transfer command code ($51_8 - 77_8$) is written into RPCS1, RDY is reset. At the termination of the data transfer, RDY is set (Paragraph 4.3).

Table 4-2 (Cont)
Control (RPCS1) Register (776700) Bit Assignments

Bit	Set By/Cleared By	Remarks
6 IE (Interrupt Enable) Read/write	IE is a control bit which can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted (Paragraph 4.4). Cleared by Unibus A INIT, Controller Clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.	A program-controlled interrupt may occur by writing 1s into IE and RDY at the same time.
5 – 0 F4–F0 and GO bit Read/write	F4–F0 and the GO bit are function (command) code control bits which determine the action to be performed by the RH11 and RP04 as shown in the chart below.	The function code bits are stored in the selected drive. Data transfer commands, defined as F4 • (F3 + F2), always cause the RH11 to become busy.

F4	F3	F2	F1	F0	GO	Octal	
0	0	0	0	0	1	01	No Operation
0	0	0	0	1	1	03	Unload (Standby)
0	0	0	1	0	1	05	Seek Command
0	0	0	1	1	1	07	Recalibrate
0	0	1	0	0	1	11	Drive Clear
0	0	1	0	1	1	13	Release (Dual Port Operation)
0	0	1	1	0	1	15	Offset Command
0	0	1	1	1	1	17	Return to Centerline
0	1	0	0	0	1	21	Read-In Preset
0	1	0	0	1	1	23	Pack Acknowledge
0	1	1	0	0	1	31	Search Command
1	0	1	0	0	1	51	Write Check Data
1	0	1	0	1	1	53	Write Check Header and Data
1	1	0	0	0	1	61	Write Data
1	1	0	0	1	1	63	Write Header and Data
1	1	1	0	0	1	71	Read Data
1	1	1	0	1	1	73	Read Header and Data

The GO bit (RPCS1, bit 0) must be set to cause the controller or drive to respond to a command. The GO bit is reset by the drive after command execution.

Cleared by Unibus A INIT or Controller Clear (will abort command execution in all drives).

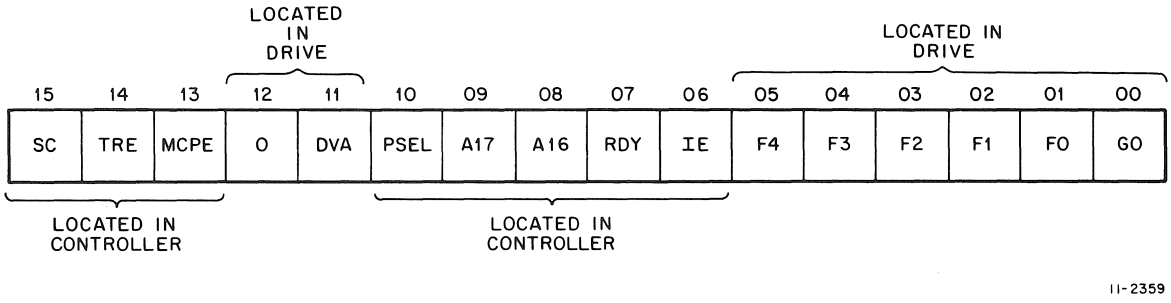


Figure 4-1 Control (RPCS1) Register (776700) Bit Usage

4.7 WORD COUNT (RPWC) REGISTER (776702)

This register is loaded by the program with the 2's complement of the number of words to be transferred. During a data transfer, it is incremented by 1 each time a word is transmitted to or from memory. A maximum of 64,000 words can be transferred at one time.

Figure 4-2 shows the RPWC bit format, and Table 4-3 provides a description of each bit.

4.8 UNIBUS ADDRESS (RPBA) REGISTER (776704)

This device register is used by the RH11 to address the memory location in which a transfer is to take place.

The RPBA register forms the lower 16 bits of address which combine with RPCS1, bits 09 and 08, to create the 18-bit memory address. This register should be loaded by the program with the starting memory address. Each time a DMA transfer is made, the register is incremented by 2. If the BAI (Bus Address Increment Inhibit) bit (bit 03 of RPCS2) is set, the incrementing of the RPBA register is inhibited and all transfers take place to or from the starting memory address. Figure 4-3 shows the RPBA bit usage, and Table 4-4 provides a description of each bit.

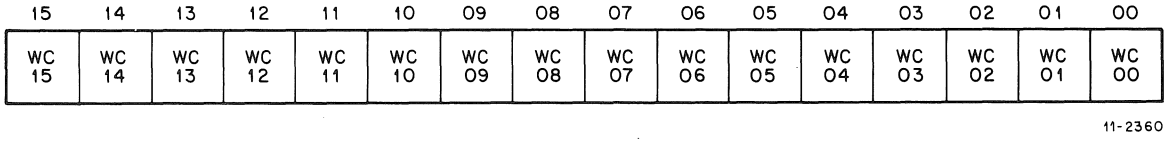


Figure 4-2 Word Count (RPWC) Register (776702) Bit Usage

Table 4-3
Word Count (RPWC) Register (776702) Bit Assignments

	Bit	Set By/Cleared By	Remarks
WC	(15:00) (Word Count) Read/write	Set by the program to specify the number of words to be transferred (2's complement form). This register is cleared only by writing 0s into it.	Incremented for each data transfer.

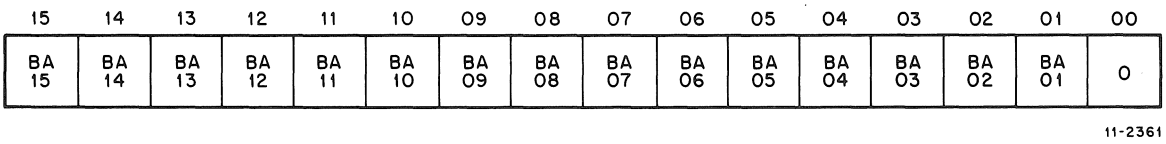


Figure 4-3 Unibus Address (RPBA) Register (776704) Bit Usage

Table 4-4
Unibus Address (RPBA) Register (776704) Bit Assignments

Bit		Set By/Cleared By	Remarks
00	Not used	Always read as a 0.	
01–15	BA(01:15) (Unibus Address) Read/write	Loaded by the program to specify the starting memory address of a transfer. Cleared by Unibus A INIT or by Controller Clear.	The BA register is incremented by 2 by the RH11 after each transfer of a word to or from memory.

4.9 DESIRED SECTOR/TRACK ADDRESS (RPDA) REGISTER (776706)

This device register is used by the drive to address the sector and track on the disk to or from which a transfer is desired. The RPDA register is associated with the drive whose unit number appears in RPCS2 (02:00). Before a transfer, the RPDA should be loaded by the program with the address of the first block to be transferred. The RPDA is incremented each time a block of data has been transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred. The RPDA register is also incremented each time an error is detected and EBL is generated. At the end of a transfer, RPDA contains the address of the next block (not yet transferred).

The RPDA register contains a five-bit sector address providing for 20 sectors per data track (18-bit format) or for 22 sectors per data track (16-bit format). The register also contains a five-bit track address providing for 19 data tracks. The sector and track addresses are non-contiguous; however, when the sector count fills up with a count of 19 or 21 (depending on format), the next word read or written will cause the track address to increment and the sector address to clear. When the sector address and track address reach their full counts, the next word will cause both sector and track addresses to increment to 0.

The Invalid Address Error (IAE, RPER1, bit 10) is set when the address in the Desired Sector/Track Address register is invalid (greater than that indicated) and a search operation is initiated.

The RPDA register can only be loaded with a word. Any attempt to write a byte causes the entire word to be written. Any attempt to write in this register while the drive's GO bit is asserted will cause an RMR (Register Modify Refused) error (RPER1, bit 02) and the register is not modified. Figure 4-4 shows the Desired Sector/Track Address register bit usage, and Table 4-5 provides a description of each bit.

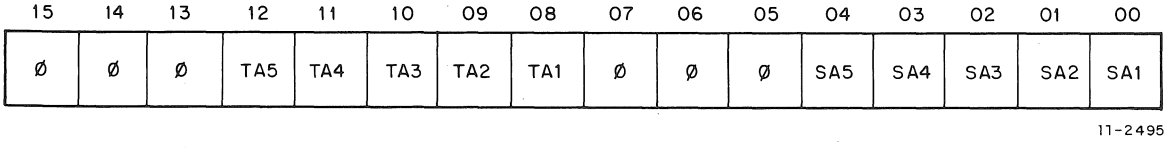


Figure 4-4 Desired Sector/Track Address (RPDA) Register (776706) Bit Usage

Table 4-5
Desired Sector/Track Address (RPDA) Register (776706) Bit Assignments

Bit		Set By/Cleared By	Remarks
15–13	SP (Spare)	Always 0s.	Spare bits for future expansion.
12–08	TA (05:00) (Track Address) Read/write	Set by the program to specify the track on which a transfer is to start. Cleared by Unibus A INIT, Controller Clear, or by performing a Drive Clear function.	Incremented by the drive when sector 21 (16-bit format) or sector 19 (18-bit format) is reached.
07–05	SP (Spare) Read/write	Always 0s.	Spare bits for future expansion.
05–00	SA (05:00) (Sector Address) Read/write	Set by the program to specify the sector on which a transfer is to start. Cleared by Unibus A INIT, Controller Clear, or by performing a Drive Clear function.	Incremented by the drive after each sector has been transferred.

4.10 STATUS (RPCS2) REGISTER (776710)

This register indicates the status of the controller and contains the drive unit number U(02:00). The unit number specified in bits 02 through 00 of this register indicates which drive is responding when registers are addressed that are located in a drive.

These are: RPCS1, bits 5 through 0, 12 and 11

RPDA	RPDB	RPDC
RPDS	RPMR	RPCC
RPER1	RPDT	RPER2
RPAS	RPSN	RPER3
RPLA	RPOF	RPEC1
		RPEC2

Figure 4-5 shows the RPCS2 bit usage, and Table 4-6 provides a description of each bit.

4.11 DRIVE STATUS (RPDS) REGISTER (776712)

This register contains the various status indicators for the selected drive. The status indicators displayed are those of the drive which is specified by the unit select bits (02:00) of the RPCS2 register. The register is a read-only register. Figure 4-6 shows the RPDS bit usage, and Table 4-7 provides a description of each bit. Writing into this register will not cause an error, and will not modify any of the status bits.

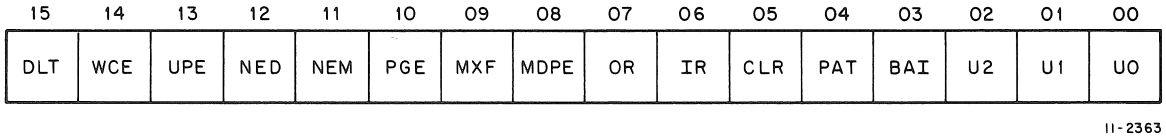


Figure 4-5 Status (RPCS2) Register (776710) Bit Usage

Table 4-6
Status (RPCS2) Register (776710) Bit Assignments

Bit		Set By/Cleared By	Remarks
15	DLT (Data Late) Read only	Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer. Also set when the controller is performing a data transfer operation over the second Unibus (PSEL = 1) and a Unibus B INIT is received on that port. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	DLT causes TRE. Buffering is 66_{10} words deep in the controller, and a DLT error indicates a severely overloaded bus. Can also be set by the program reading or writing the RPDB register (Paragraph 4.15).
14	WCE (Write Check Error) Read only	Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	WCE causes TRE. If a mismatch is detected during a Write-Check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RPBA (and extension) is the address of the word following the one which did not match (if BAI is not set). The mismatched data word from the disk is displayed in the data buffer (RPDB).
13	UPE (Unibus Parity Error) Read/write	Set if the Unibus parity lines indicate a parity error while the controller is performing a Write or Write-Check command. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	UPE causes TRE. When the Unibus is selected to do 18-bit data transfers, the UPE error is disabled. When a Unibus parity error occurs, the RPBA register contains the address +2 of the memory word with the parity error (if BAI is not set). This bit may be set by program control for diagnostic purposes.
12	NED (Nonexistent Drive) Read only	Set when the program reads or writes a drive register in a drive [selected by U(02:00)] which does not exist or is powered down. (The drive fails to assert TRA within 1.5 μs after assertion of DEM.) Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	NED causes TRE.
11	NEM (Nonexistent Memory) Read only	Set when the controller is performing a DMA transfer and the memory address specified in RPBA is nonexistent (does not respond to MSYN within 10 μs. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	NEM causes TRE. The RPBA contains the address +2 of the memory location causing the error.

Table 4-6 (Cont)
Status (RPCS2) Register (776710) Bit Assignments

Bit		Set By/Cleared By	Remarks
10	PGE (Program Error) Read only	Set when the program attempts to initiate a data transfer operation while the RH11 is currently performing one. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	PGE causes TRE. The data transfer command code is inhibited from being written.
09	MXF (Missed Transfer) Read/write	Set if the drive does not respond to a data transfer command within 250 ms. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	MXF causes TRE. This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive which has ERR set, or if the drive fails to initiate the command for any reason (such as a parity error).
08	MDPE (Massbus Data Bus Parity Error) Read only	Set when a parity error occurs on the Massbus data bus while doing a read or write-check operation. Cleared by Unibus A INIT, Controller Clear, RH11 Error Clear, or loading a data transfer command with GO set.	MDPE causes TRE. Parity errors on the Massbus data bus during write operations are detected by the drive and cause the PAR error (RPER1 register, bit 03).
07	OR (Output Ready) Read only	Set when a word is present in RPDB and can be read by the program. Cleared by Unibus A INIT, Controller Clear, or by reading DB (Paragraph 4.15).	Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to read the DB register before OR is asserted will cause a DLT error.
06	IR (Input Ready) Read only	Set when a word may be written in the DB register by the program. Cleared by reading the DB (Paragraph 4.15).	Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to write the DB register before IR is asserted will cause a DLT error.
05	CLR (Controller Clear) Write only	When a 1 is written into this bit, the RH11 and all drives are initialized (Paragraph 4.2).	Unibus A INIT also causes Controller Clear to occur.
04	PAT (Parity Test) Read/write	While PAT is set, the RH11 generates even parity on both the control bus and data bus of the Massbus. When clear, odd parity is generated. Cleared by Unibus A INIT or Controller Clear.	While PAT is set, the RH11 checks for even parity received on the data bus but not on the control bus.

Table 4-6 (Cont)
Status (RPCS2) Register (776710) Bit Assignments

Bit		Set By/Cleared By	Remarks
03	BAI (Unibus Address Increment Inhibit) Read/write	When BAI is set, the RH11 will not increment the BA register during a data transfer. This bit cannot be modified while the RH11 is doing a data transfer (RDY negated). Cleared by Unibus A INIT or Controller Clear.	When set during a data transfer, all data words are read from or written into the same memory location.
02–00	U(2:0) (Unit Select) Read/write	These bits are written by the program to select a drive. Cleared by Unibus A INIT or Controller Clear.	The unit select bits can be changed by the program during data transfer operations without interfering with the transfer. The RP04 registers contain bits which come from the selected drive.

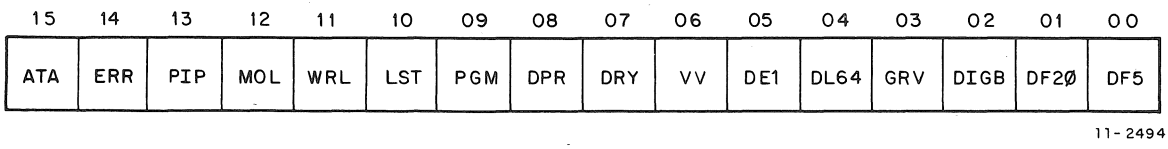


Figure 4-6 Drive Status (RPDS) Register (776712) Bit Usage

Table 4-7
Drive Status (RPDS) Register (776712) Bit Assignments

Bit	Set By/Cleared By	Remarks
15 ATA (Attention Active) Read only	An Attention condition in a drive will set the ATA bit and the ATA summary line (Paragraph 4.2). It is cleared by Unibus A INIT, Controller Clear, loading a command with the GO bit set, or loading a 1 in the RPAS register corresponding to the drive's unit number. The last two methods of clearing the ATA bit will not clear the error indicators in the drive. **NOTE** **The ATA bit will not set if the drive was switched from a neutral position. The ATA bit may be reset by writing a 1 into the Attention Summary register. Writing a 0 into the register has no effect.**	An Attention condition is caused by: any error in the error registers (except during data transfers); the completion operation; the completion of a start up cycle (with the MOL bit set); dual controller operation with drive presently available (drive was requested before but was not available); correct sector identification (Search command only). For dual controller operation, the ATA bit is asserted on both ports each time the drive cycles up. There are two ATA bits implemented in the RP04 ATA-A, which is accessible to Controller A, and ATA-B, which is accessible to Controller B. When the port switch is in Controller A, the ATA-A bit is displayed in the ATA bit position (bit 15) of the RPDS register. Accesses from Controller B will read all 0s except for the RPAS register. The reverse situation holds true when Controller B is selected.
14 ERR (Error) Read only	Set when one or more of the errors in the Error registers (RPER1, RPER2, or RPER3) in a selected drive is set. Cleared by Unibus A INIT, Controller Clear, or Drive Clear.	A composite error bit which is the logical OR of all the error conditions in the RPER1, RPER2, or RPER3 registers. This ERR bit is not cleared by loading a command other than Drive Clear. While ERR is asserted, commands other than Drive Clear are not accepted by the drive.

Table 4-7 (Cont)
Drive Status (RPDS) Register (776712) Bit Assignments

<table>
<tr><th colspan="2">Bit</th><th>Set By/Cleared By</th><th>Remarks</th></tr>
<tr><td>13</td><td>PIP
(Positioning
In Progress)
Read only</td><td>Set by the drive when a positioning command is accepted. These commands are Seek, Offset, Return to Centerline, Recalibrate, Unload, and Search. The PIP bit will not be set during implied seeks or mid-transfer seeks. Cleared when the moving function is completed. The DRY and ATA bits are also set at this time (normal termination).</td><td>This bit helps to distinguish the case of a drive being busy (DRY negated) while no data transfer is underway (RDY asserted in the RH11).

The following chart shows the state of the PIP bit in relation to the type of operation being performed.

<table>
<tr><th>Operation</th><th>DRY</th><th>PIP</th><th>ATA At End of Operation (No Error)</th></tr>
<tr><td>No operation</td><td>1</td><td>0</td><td>No</td></tr>
<tr><td>Unload (Standby)</td><td>0</td><td>1</td><td>Yes</td></tr>
<tr><td>Recalibrate</td><td>0</td><td>1</td><td>Yes</td></tr>
<tr><td>Drive Clear</td><td>1</td><td>0</td><td>No</td></tr>
<tr><td>Release</td><td>0</td><td>0</td><td>No</td></tr>
<tr><td>Search Command</td><td>0</td><td>1</td><td>Yes</td></tr>
<tr><td>Implied Search</td><td>0</td><td>0</td><td>No</td></tr>
<tr><td>Seek</td><td>0</td><td>1</td><td>Yes</td></tr>
<tr><td>Offset</td><td>0</td><td>1</td><td>Yes</td></tr>
<tr><td>Write Check</td><td>0</td><td>0</td><td>No</td></tr>
<tr><td>Write Data</td><td>0</td><td>0</td><td>No</td></tr>
<tr><td>Write Header and Data</td><td>0</td><td>0</td><td>No</td></tr>
<tr><td>Read Data</td><td>0</td><td>0</td><td>No</td></tr>
<tr><td>Read Header and Data</td><td>0</td><td>0</td><td>No</td></tr>
<tr><td>Implied Seek</td><td>0</td><td>0</td><td>No</td></tr>
<tr><td>Mid-Transfer Seek</td><td>0</td><td>0</td><td>No</td></tr>
<tr><td>Return to Centerline</td><td>0</td><td>1</td><td>Yes</td></tr>
<tr><td>Pack Acknowledge</td><td>1</td><td>0</td><td>No</td></tr>
<tr><td>Read-in Preset</td><td>1</td><td>0</td><td>No</td></tr>
</table>
</td></tr>
<tr><td>12</td><td>MOL
(Medium On-Line)
Read only</td><td>Set by the drive upon the successful completion of the startup cycle as follows:

1. Mount pack
2. Start spindle motor
3. Brush cycle
4. Motor up to speed
5. Load heads
6. Recalibrate

Cleared when the spindle is powered down or the device is switched off-line (with the spindle still up to speed) for diagnostic purposes.</td><td>With the positioner in recalibrate state (addressing cylinder 0), the device will generate a File-Ready condition, which is active only if the positioner is settled in recalibrate state. Upon recognizing this condition coming true, the drive will set the MOL bit. Whenever the MOL bit changes state (set or reset), the ATA bit is also set, except in the unload operation case.</td></tr>
</table>

Table 4-7 (Cont)
Drive Status (RPDS) Register (776712) Bit Assignments

Bit	Set By/Cleared By	Remarks
11 WRL (Write Lock) Read only	Set when the RP04 will not accept Write commands.	The RP04 Drive can be placed in WRITE LOCK mode through a manual switch on the RP04 control panel. The status of the device is indicated by the illumination of the manual switch. When the indicator is on, any attempt by the operating system to issue a Write command on a write-locked device will cause the Write Lock Error (WLE, bit 11 of RPER1) bit to set. To remove the write lock condition, the manual switch must be used to place the device in the WRITE PERMIT mode.
10 LST (Last Sector Transferred) Read only	Set by the drive on rising edge of EBL pulse when last addressable sector on the disk pack has been read or written. Cleared when a new function command is received.	If the last sector transferred happens to be sector 19 or 21, (depending on format) of track 18 (last track on the cylinder), the Desired Sector/Track Address register increments to 0 and the Desired Cylinder Address register increments by one. If the RUN line is reset at the trailing edge of EBL of track 18 and sector 19 or 21, the Desired Cylinder Address (RPDC) register will be incremented by one but no mid-transfer seek will be initiated. A mid-transfer seek will take place only if the RUN line was set in the above case. If the software wishes to read the entire pack, the data transfer will always terminate unconditionally when sector 19 or 21 on track 18 and cylinder 410 (last cylinder on the IBM 3336 disk pack) has been transferred. In this case, the device logic will raise the End of Block (EBL) pulse following the ECC check on sector 19. Upon terminating the transfer, the drive will set the LST bit. With this bit set, the Desired Cylinder Address register contains 411 (illegal address), and the Desired Sector/Track Address register contains 0 since it was incremented on the rising edge of the last EBL pulse.

Table 4-7 (Cont)
Drive Status (RPDS) Register (776712) Bit Assignments

Bit	Set By/Cleared By	Remarks
09 PGM (Programmable) Read only	Set when the CONTROLLER SELECT switch is in the A/B position, indicating that the device is accessible from either Port A or Port B. Cleared when the CONTROLLER SELECT switch is in PORT A or PORT B position.	If system configuration requires RP04 to be used as single controller device, this bit will always be reset. Dual controller operation consists of being able to access an RP04 Drive from two controllers. A drive with the dual controller option has three states: Connected to Controller A Connected to Controller B Neutral When the drive is connected to Controller A, only the controller connected to Controller A can access the drive's registers. Similarly, when the drive is connected to Controller B, only the controller connected to Controller B can access the drive's registers. In the programmable state, the drive is not connected to either controller, but either controller can read its registers. The PGM bit is interrelated to the Drive Present (DPR, bit 8), which is set when the drive is switched to the controller reading the register.
08 DPR (Drive Present) Read only	Always set for single controller operation. In dual controller operation, this bit is set for the controller which has seized the RP04 and is reset for the other controller. When the RP04 switches from one controller to a second controller and the ATA line (bit 15) is high, DPR is set. This indicates that the RP04 is connected to the asynchronous control bus of this controller. If the RP04 is in the programmable state (PGM bit = 1) when requested, DPR will be set and the drive will switch immediately, regardless of the ATA bit.	

Table 4-7 (Cont)
Drive Status (RPDS) Register (776712) Bit Assignments

Bit		Set By/Cleared By	Remarks
07	DRY (Drive Ready) Read only	Set at the completion of every command, data handling or mechanical motion. Cleared at the initiation of a command.	If this bit is reset, the RH11 cannot issue another command. When set, this bit indicates the readiness of the RP04 device to accept a new command. If a Read or Write command was issued, the setting of the DRY bit will indicate normal termination. If an error was made during the data transfer, the appropriate interface lines and error bits will also be set. If a mechanical movement command was issued, the ATA bit will also be set when DRY is set. If an error occurs during the mechanical movement, the appropriate interface lines and error bits will also be set. The DRY bit status during the various stages of RP04 operation is shown in the chart under bit 13 (PIP) in this table.
06	VV (Volume Valid) Read only	Set by the Pack Acknowledge or Read-In Preset command from either port. Cleared by the drive whenever it cycles up from the off state.	When reset, this bit indicates when the drive has been put off-line and on-line and a disk pack may have been changed. Therefore, the program should not assume anything about the identity of the pack. There are two VV bits: VV-A for accesses to Port A and VV-B for accesses to Port B. When the port switch is in Port A, the VV-A bit is displayed in the VV bit position of this register. Accesses from Port B will read all 0s except for the RPAS register. The reverse situation holds true when Port B is selected.
05	DE1 (Difference Equals 1) Read only	Set when the device has detected a value equal to 1 in the difference counter during a head load sequence. Cleared by a File Ready at the completion of a head load sequence.	
04	DL64 (Difference Less Than 64) Read only	Set when the device has detected a value less than 64 in the difference counter during the reverse seek of the head load sequence. Cleared by a File Ready at the completion of a head load sequence.	

Table 4-7 (Cont)
Drive Status (RPDS) Register (776712) Bit Assignments

Bit		Set By/Cleared By	Remarks
03	GRV (Go Reverse) Read only	Set when the device has detected the Go Reverse signal during a head load sequence. Cleared by File Ready at the completion of a head load sequence.	
02	DIGB (Drive to Inner Guard Band) Read only	Set when the drive has detected the drive to inner guard band signal during a head load sequence. Cleared by File Ready at the completion of a head load sequence.	
01	DF20 (Drive Forward 20 in./sec) Read only	Set by the drive when it has detected the DF20 signal during a head load sequence. Cleared by File Ready at the completion of a head load sequence.	
00	DF5 (Drive Forward 5 in./sec) Read only	Set when the drive has detected a DF5 signal while in the head load mode after a sequence start pulse was recognized. Cleared by File Ready at the completion of a head load sequence.	

4.12 ERROR (RPER1) REGISTER 01 (776714)

This register contains the error status indicators for the drive whose unit number appears in bits 02 through 00 of RPCS2. Bit 14 of the RPDS register (ERR) is a composite error indicator which represents the logical OR of all the bits in the RPER1 register.

The RPER1 register is a read/write register; thus, diagnostic programs may test the functioning of the error indicators by counting a 1 into them.

Writing 0s into this register should not be used as the normal way of clearing errors. The Drive Clear command should be used instead.

The RPER1 register can only be written as a word. Any attempt to write a byte will cause an entire word to be written. If the program attempts to write into this register while the drive is busy (GO bit is asserted), an RMR (RPER1 register, bit 02) error is set, and the contents of the register are not modified. Figure 4-7 shows the RPER1 bit usage, and Table 4-8 provides a description of each bit.

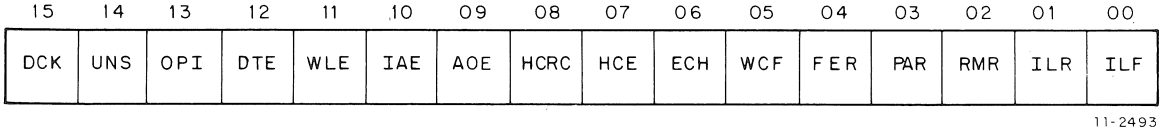


Figure 4-7 Error (RPER1) Register 01 (776714) Bit Usage

Table 4-8
Error (RPER1) Register 01 (776714) Bit Assignments

Bit		Set By/Cleared By	Remarks
15	DCK (Data Check) Read/write	Set during a read operation when the ECC hardware has detected an ECC error after the ECC bytes have been looked at. Cleared by a Drive Clear command, Unibus A INIT, Controller Clear, or by writing 0s into the register.	If Error Correction Code/Inhibit (ECI) bit is off, the RP04 will go into the error correction process. DCK will remain set. If ECI bit is on, the error correction process is inhibited even though an ECC error was detected at the end of a data transmission. EXC will be set at the completion of the error correction process and will last for the duration of EBL. If DCK is set, the data transfer on the present sector will terminate normally and, if the RUN line remains high at the trailing edge of the EBL pulse, the command will continue on the next sector.
14	UNS (Unsafe) Read/write	Set when the drive detects a condition which prevents it from operating. Cleared by a Drive Clear or by writing 0s into the register. If this does not cause the UNS condition to disappear, the RP04 must be powered down and cycled up to ensure clearing of all the errors including the UNS bit.	This bit is a composite error bit of the unsafe error conditions in the RPER2 and RPER3 registers. Any unsafe condition except a read or write unsafe denotes an emergency situation where the heads are automatically retracted and/or the drive cycled down. One example of "drive unsafe" is the drive error conditions that cause the RP04 to go to the WRITE PROTECT mode. With UNS set, the RP04 will not guarantee correct results on any of the operations. In most cases, clearing this bit requires field service intervention.
13	OPI (Operation Incomplete) Read/write	Set when a Read or Write command involving header search has not begun transmitting data (sync clocks) within three index pulses. OPI will also set during a search operation where a sector count match is not made after a maximum of three index pulses have been encountered. Cleared by a Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	In general, the OPI bit is used to indicate every case following a command initiation where there is inactivity for a maximum period of three index pulses. With OPI set, the GO bit will be cleared and the RP04 will be returned to the ready state (RDY bit set).

Table 4-8 (Cont)
Error (RPER1) Register 01 (776714) Bit Assignments

Bit		Set By/Cleared By	Remarks
12	DTE (Drive Timing Error) Read/write	Set when a failure has occurred in the clocking or timing circuits of the drive. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	A failure in the clocking or timing circuits can no longer guarantee the logic remaining in the proper sequence. Therefore, in both read and write operation, the RP04 will abort the command as soon as this error is detected. In the write operation, the software should try to regenerate the sector where the error occurred. The DTE bit will set in the case where the rising edge of a sector pulse is encountered before the data transmission is finished.
11	WLE (Write Lock Error) Read/write	Set when the operating system attempts to issue a write command on a write-locked device (device in WRITE PROTECT mode). A manual (WRITE PROTECT) switch can place the device in WRITE PROTECT mode during normal operation. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	
10	IAE (Invalid Address Error) Read/write	Set when the address in the Desired Cylinder register (RPDC) and the Desired Sector/Track Address register (RPDA) is invalid and a seek or search operation is initiated. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	The RP04 Drive format allows for 20 sectors per data track (18-bit format) or 22 sectors per data track (16-bit format). The RP04 will distinguish between the two formats and will set IAE if a sector greater than 19 (18-bit format) or a sector greater than 21 (16-bit format) is requested. IAE is also set if the cylinder and track addresses exceed the RP04 device capability.
09	AOE (Address Overflow Error) Read/write	Set when the Desired Cylinder register (RPDC) overflows during a read or write. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	Setting of this bit indicates that the Desired Cylinder Address register has exceeded cylinder address 410. With AOE set, the RP04 will terminate the operation when the last sector in cylinder 410 has been read or written.
08	HCRC (Header CRC Error) Read/write	Set by a CRC error in the header. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	It is possible for the cylinder address and sector/track address words of the header (first two words) to compare successfully but, because of an error in the two key words or the CRC word, the HCE bit will be reset and the HCRC bit will be set. If HCRC is set (independent of the status of HCE) during a Read/Write command, the RP04 will not make any data transfer. In the event of a CRC error during a Read Header and Data command, the entire sector will be transferred to the controller with the HCRC bit set and the errors will be recorded.

Table 4-8 (Cont)
Error (RPER1) Register 01 (776714) Bit Assignments

Bit		Set By/Cleared By	Remarks
07	HCE (Header Compare Error) Read/write	If the sector counter is equal to the desired sector field, the header associated with that sector is compared with the desired header words. If the header matches the desired cylinder and desired sector/track address, the header field is the required one. If the header does not match the desired cylinder and sector/track address, the HCE bit is set. If the sector address and sector count match but a CRC error is detected following the header compare, the HCE bit is reset and the HCRC bit is set. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	If the HCE bit is set during a Read/Write command, the RP04 Drive will not make any data transfer. In the event of a Read Header and Data command, however, the entire sector will be transferred to the controller, with the errors recorded. If both the HCE and HCRC bits are reset, there is no header error and the data transfer will occur.
06	ECH (ECC Hard Error) Read/write	Set when the conclusion of the error correction procedure indicates that the error was a noncorrectable ECC error. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	
05	WCF (Write Clock Fail) Read/write	Set during a write operation when the Write Clock signals are not received by the drive. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	Upon recognizing a WCF condition, the drive will abort the command.
04	FER (Format Error) Read/write	Set where the prerecorded (pack formatting) flag bit on the header is not equal to the corresponding flag bit in the Offset register (bit location 12, RPOF). Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	Error usually indicates that the wrong pack was mounted on the drive. With a Write command, an FER error can be catastrophic, FER will cause the command to abort at once. Only the Read Header and Data command can be used to retrieve the header information.
03	PAR (Parity Error) Read/write	Set when a parity error is detected during data transmission over the asynchronous control bus (odd parity) or over the synchronous data bus. Cleared by a Drive Clear command, an Initialize pulse, or by writing 0s into the register.	

Table 4-8 (Cont)
Error (RPER1) Register 01 (776714) Bit Assignments

Bit	Set By/Cleared By	Remarks
02 RMR (Register Modification Refused) Read/write	Set when a write is attempted into any register (except RPAS) during an operation. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	The following registers can be written into before or after an operation. Control register Error registers Maintenance register Attention Summary register Desired Sector/Track Address register Offset register Desired Cylinder Address register The remaining RP04 registers are read-only registers. During an operation, the Maintenance and Attention Summary registers can be written into. When RMR is set, the RP04 Drive will continue to normally execute the command in progress.
01 ILR (Illegal Register) Read/write	Set when the device control logic decodes a nonexistent register address from the register select lines (RS00–RS04). Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	Attempting to write into a read-only register will not cause the ILR to set. The bits received will be ignored and no other error will be flagged.
00 ILF (Illegal Function) Read/write	Set when the function code in the Control register does not correspond to an implemented command on this drive. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.	

4.13 ATTENTION SUMMARY (RPAS) REGISTER (776716)

This register allows the program to examine the attention status of all drives with only one register read operation. It also provides means for resetting the attention logic in a selected group of drives. The bit displayed in each of the eight low-order positions of this register is identical to the ATA bit displayed in RPDS for the corresponding drive. When fewer than eight drives are attached to the RH11, the bits corresponding to the missing drives are always 0.

A drive's ATA bit can be reset by loading a 1 into the bit position corresponding to the drive's unit number. (Loading a 0 has no effect.) This allows the program to inspect the RPAS register and later to reset the ATA bits which were set, without accidentally resetting other ATA bits which may have become set in the meantime.

For a program to use the RPAS without losing status information, the program must use the MOV instruction for all reads and writes of this register. An instruction that does a read-restore (such as BIS) may cause bits that became asserted between the read and the restore to be lost.

This register can be read or written at any time, regardless of whether any particular drive is busy. Note that a drive never asserts ATA during the execution of a command. The RPAS register can only be written as a word. Any attempt to write a byte will cause an entire word to be written. Figure 4-8 shows the RPAS bit usage and Table 4-9 provides a description of each bit.

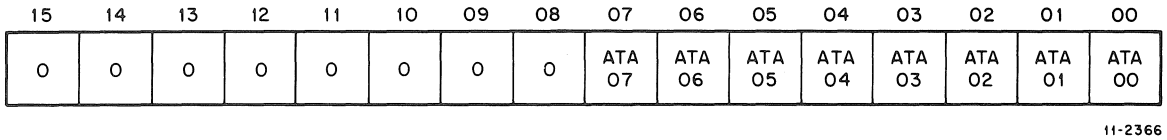


Figure 4-8 Attention Summary (RPAS) Register (776716) Bit Usage

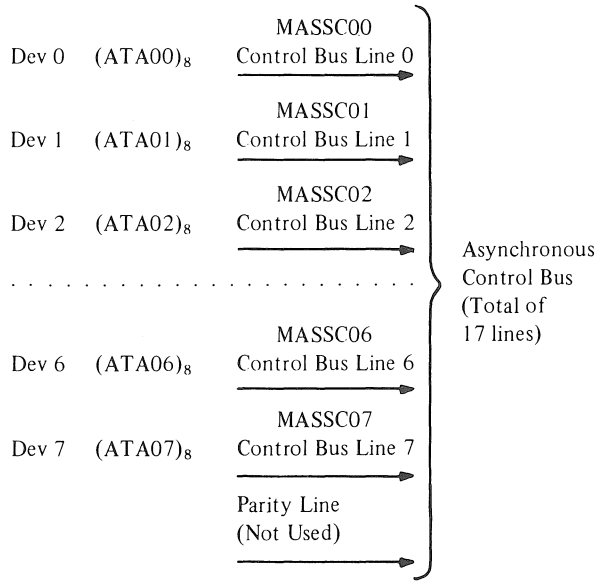
Table 4-9
Attention Summary (RPAS) Register (776716) Bit Assignments

Bit		Set By/Cleared By	Remarks
15:08	Not Used	Always read as a 0.	
07:00	ATA (07:00) (Attention Active) Read/write	Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by Unibus A INIT or Controller Clear. Individual bits are cleared by loading a function code with the GO bit in the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect.	Each drive's ATA bit is displayed individually in bit 15 of RPDS. Each drive responds in the bit position which corresponds to its unit number; e.g., drive 02 responds in bit position 02.

4.13.1 Read Capability

The controller will normally request Attention Summary status from all drives simultaneously by indicating a register 04 read on the Massbus Register Select lines (RS04–RS00).

When register 04 is selected, each device will ignore the fact that it may have been executing a data transfer command, and will place the output of its Attention Active flip-flop on its assigned bit position on the asynchronous control bus as follows:



The controller strobes the eight Attention Active (ATA) bits from the asynchronous control bus 1 μs after placing the RPAS address on the Register Select lines to see the results of the Attention Summary request.

NOTE

The normal Transfer (TRA) pulse used on the asynchronous bus will not be used in this case, since all the drives are responding simultaneously.

4.13.2 Write Capability

The Attention Summary flip-flop status of each device can be altered by the controller as follows:

Bit Written	ATA Before	ATA After
0	0	0
0	1	1
1	0	0
1	1	0

Writing a 1 in its assigned position causes a set ATA bit to be reset, while writing a 0 has no effect on the state of the ATA bit.

4.13.3 Attention Handling in Dual Controller Case

In a dual controller configuration, the Attention (ATTN) bit is set under the following conditions:

1. Upon powering up the device from the off state, ATTN will be asserted on both ports.

2. Upon powering up the device from the standby state (except from an Unload command), ATTN will be asserted to both controllers (even if the device is seized by one controller).

3. In case of a persistent error, the device will be forced to neutral state. Unless it has already been requested by the other controller, *no* ATTN will be generated until a request comes through.

4.13.4 Attention Handling on a Persistent Error (Single Controller)

A persistent error, just like any other error condition, will cause the ATTN line to be asserted. Unsuccessful attempts by the controller to clear the error will *not* work in this case; the ATTN will remain asserted.

The controller can reset the ATTN bit and free the Massbus ATTN line from that drive by writing a 1 into the Attention Summary register. (The error condition internal to the drive, however, will remain set.) If, at a later time, the same controller attempts to address the drive, the ATTN bit will again be asserted if the error persists.

4.14 LOOK-AHEAD (RPLA) REGISTER (776720)

This register presents the angular position of the disk relative to the read/write heads for the disk whose unit number appears in bits 02 through 00 of the RPCS2 register.

The purpose of this register is to provide the programmer with a means of optimizing disk access by minimizing rotational delays. The register contains a two-bit encoded extension field and a five-bit sector counter field.

Figure 4-9 shows the RPLA bit usage and Table 4-10 provides a description of each bit.

4.15 DATA BUFFER (RPDB) REGISTER (776722)

This register provides a maintenance tool to check the Silo data buffer in the RH11. A total of 66_{10} words is accepted before the Silo data buffer (DB) becomes full. If the program attempts to write into the data buffer while it is full or to read the data buffer when it is empty, a Data Late (DLT) error will be posted. Successive reads from the DB read out words in the same order in which they were entered into the Silo.

The IR (Input Ready) and OR (Output Ready) status indicators in the RPCS2 register are provided so the programmer can determine when words can be read from or written into the RPDB. IR should be asserted before attempting a write into DB; OR should be asserted before attempting a read from DB.

The RPDB register can be read and written only as an entire word. Any attempt to write a byte will cause an entire word to be written. Reading the RPDB register is a "destructive" readout operation: the top data word in the Silo buffer is removed by the action of reading the RPDB, and a new data word (if present) replaces it a short time later. Conversely, the action of writing the RPDB register does not destroy the contents of RPDB; it merely causes one more data word to be inserted into the Silo buffer (if it was not full). Figure 4-10 shows the RPDB bit usage, and Table 4-11 provides a description of each bit.

4.16 MAINTENANCE (RPMR) REGISTER (776724)

The Maintenance register is a 16-bit register which simulates various signals from the disk to allow diagnostic testing of the drive. This register is composed of two parts – a function bits section and a control bits section. Bits 09 through 06 are function bits and bits 05 through 00 are control bits.

The DMD bit (bit 0) must be set to place the drive in diagnostic mode. With the DMD bit set, the drive will handle the same command repertoire that it normally handles except that certain operations defined by the function bits may be initiated through the Maintenance register, and the results of these operations may be temporarily displayed in this register.

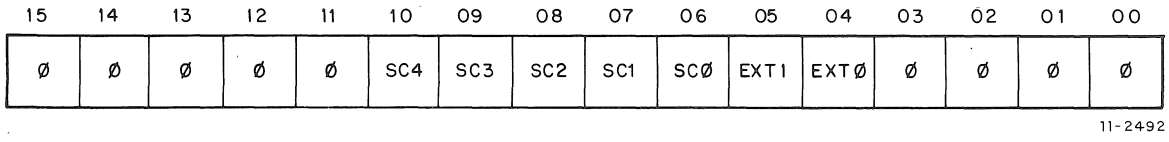


Figure 4-9 Look-Ahead (RPLA) Register (776720) Bit Usage

Table 4-10
Look-Ahead (RPLA) Register (776720) Bit Assignments

Bit		Set By/Cleared By	Remarks
15–11	Not Used	Always 0s.	
10–6	SC(4:0) (Sector Count) Read only		This five-bit register addresses the required sector on the data track through an exclusive-OR network with the RPDA register. The sector count is continually being incremented on the rising edge of each sector pulse and reflects the exact location of the data track in relation to the head. Each time the rising edge of the index pulse is encountered, the sector count field resets to zero. The maximum sector count is 21 for the 16-bit word format and 19 for the 18-bit data word format. If a sector count malfunction occurs during an operation, the RP04 will set the Operation Incomplete (OPI) error bit, after three index pulses, without a sector count/desired sector field match. A malfunctioning sector count field is a catastrophic error since the required sector cannot be recovered. The RP04 looks at every header on the data track. In the event of an error condition, no error is reported until after the sector counter matches the sector field, which is an indication that the desired sector has been found.
5–4	EXT (1:0) (Encoded Extension Field)		These two bits are used to specify the approximate location of the heads within a sector, as shown in the chart below. **EXT 1** / **EXT 0** / **Head Location** 0 / 0 / < 20% (in first 20% of sector) 0 / 1 / 20 to 40% 1 / 0 / 40 to 80% 1 / 1 / > 80% (in last 20% of sector) For example, if EXT 0 = 0 and EXT 1 = 1, the heads are from 40 to 80% past the beginning of the sector.
3–0	Not Used	Always 0s.	

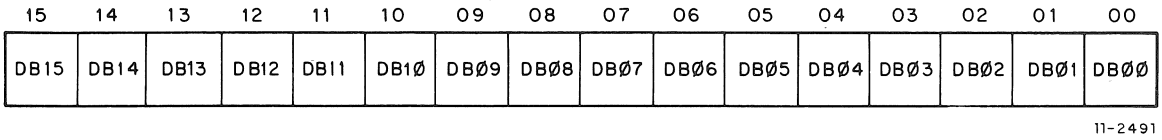


Figure 4-10 Data Buffer (RPDB) Register (776722) Bit Usage

Table 4-11
Data Buffer (RPDB) Register (776722) Bit Assignments

Bit	Set By/Cleared By	Remarks
15–00 DB(15:00) (Data Buffer) Read/write	When read, the contents of OBUF (internal RH11 register) are delivered. Upon completion of the read, the next sequential word in the Silo will be clocked into OBUF. When written, data is loaded into IBUF (internal RH11 register) and allowed to sequence into the Silo if space is available.	Used by the program for diagnostic purposes. When the register is written into, IR is cleared until the DB is ready to accept a new word. When the register is read, it will cause OR to be cleared until a new word is ready. During a write-check error condition, the data word read from the disk which did not compare with the corresponding word in memory is frozen in RPDB for examination by the program.

The Maintenance register provides wraparound capability within the drive without actually using the media to record or retrieve data. By using a program-controlled clock, the data is shifted through various registers and is routed back to memory without being written on the pack. The wraparound capability (which operates only in diagnostic mode) will not check the read/write electronics but could actually check the Data Serial Shift register.

Figure 4-11 shows the register bit usage and Table 4-12 provides a description of each bit.

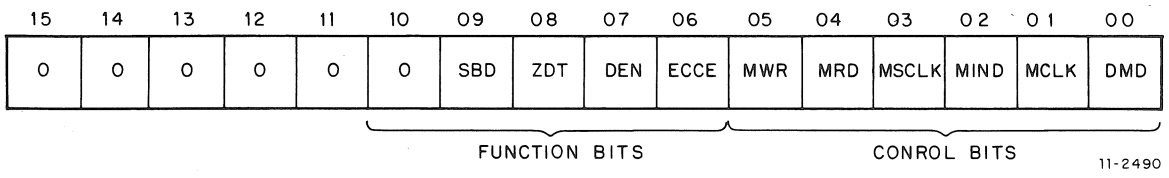


Figure 4-11 Maintenance (RPMR) Register (776724) Bit Usage

Table 4-12
Maintenance (RPMR) Register (776724) Bit Assignments

Bit		Set By/Cleared By	Remarks
15–10	Not Used		
09	SBD (Sync Byte Detected) Read/write	Set immediately following the sync byte detection for the header and data fields. Cleared by Unibus A INIT.	This bit will remain set for only half a maintenance clock pulse.
08	ZDT (Zero Detect) Read/write	Belongs to ECC logic and will set when the high-order 21 flip-flops in the ECC register are all zeros. Cleared by Unibus A INIT.	
07	DEN (Data Envelope) Read/write		This bit is a level which includes the 256 X 16 or 256 X 18 data bits and is used during both read and write operation.
06	ECCE (ECC Envelope) Read/write		This bit is a level which includes 32 bits of the ECC redundancy, and functions during both read and write operation.
05	MWR (Maintenance Write) Read/write	This bit is set by writing a 1 into it and is cleared by writing a 0 into it forming a data pattern.	In dynamic operation, the data from memory is supplied to the RP04 Data Buffer register via the RH11 Silo. The output of this buffer is applied to a shift register which shifts the data bits serially onto the disk pack. In diagnostic mode, the data from memory is applied to the RP04 Data Buffer via the RH11 Silo. The output of the Data Buffer is again applied in parallel to the shift register. Now, however, the output of the shift register is serially applied to this bit in the Maintenance register. The output of this bit position is applied to a second memory location under software control. By comparing the contents of the original memory location with the contents of this memory location, it can be determined that the write data path in the DCL is functioning properly. This method simulates the writing of data on the disk. Note that the disk pack was not included in the write data path.

Table 4-12 (Cont)
Maintenance (RPMR) Register (776724) Bit Assignments

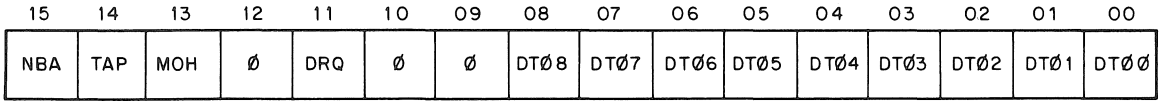
Bit		Set By/Cleared By	Remarks
04	MRD (Maintenance Read) Read/write	This bit is set by writing a 1 into it and is cleared by writing a 0 into it.	In dynamic operation, the data from the disk pack is serially applied to the shift register. The output of the shift register is applied to the RP04 Data Buffer register in parallel. The output of the Data Buffer is applied to memory via the RH11 Silo. In diagnostic mode, the data from memory is serially applied to this bit in the Maintenance register. The output of this bit is applied to the shift register. The output of the shift register is applied in parallel to the Data Buffer, which transfers the word to a second memory location via the RH11 Silo. By comparing the contents of the first memory location with the contents of the second memory location, it can be determined that the read data path in the DCL is functioning properly. This method simulates the reading of data from the disk pack. Note that the disk pack was not included in the read data path.
03	MSCLK (Maintenance Sector Clock) Read/write		Used in conjunction with the maintenance index pulse (bit 02) to check the device timing.
02	MIND (Maintenance Index) Read/write		The software supplies a pseudo-index pulse via the Maintenance register to check the timing generation logic. The rise of the pseudo-index pulse will reset the sector counter. The index pulse is assumed to be the sector pulse for sector 0. Following the index pulse, which normally resets the sector counter, the software must simulate sector clocks through the Maintenance register. There are a total of 13,440 sector clocks per revolution. For the 20 sector format mode, there will be 13,440/20 or 672 sector clocks per sector, and, for the 22 sector format mode, there will be 13,440/22 or approximately 609 sector clocks per sector. (Three sector clocks from each sector will be collected to form a longer tolerance gap on the last sector on each track.)

Table 4-12 (Cont)
Maintenance (RPMR) Register (776724) Bit Assignments

Bit		Set By/Cleared By	Remarks
02 (Cont)			To check the sector timing generation logic, the software can set the format bit and supply the appropriate number of clocks. Then, by a combination of reads from the Maintenance register and the Look-Ahead register (and other control registers, if applicable), the software can determine if the timing is working properly. To check index/sector clock interaction, a sector clock must be inserted under the index pulse envelope.
01	MCLK (Maintenance Clock) Read/write	Set by writing a 1 into this bit position. Cleared by writing a 0 into this bit position.	MCLK is actually the system-generated clock. The system can change the status of this bit from 0 → 1 → 0 → 1 . . . etc. by doing repeated writes on the Maintenance register, causing a square-wave clock to be generated. The pulse period of this clock is dependent on the system speed in altering the status of the clock bit. MCLK replaces the read data strobe or write data strobe which is generated by the drive. The advantage of the system clock is that between writes of the Maintenance register, the software can do reads to monitor the status of the function bits. The drive logic will slow down to the speed of the system clock.
00	DMD (Diagnostic Mode) Read/write	When set, this bit acts as an enable line to perform diskless operations and as an inhibit for the actual disk signals (PLO, index, sync clocks, data lines, etc.).	The Maintenance register is enabled by setting the DMD bit. This bit completely isolates the drive mechanism and analog circuitry from the disk control logic (DCL). The DMD bit must remain set as long as the Maintenance register is functioning. All Read/Write commands will function in the normal fashion except for the fact that the data will wrap around itself instead of actually being written on the disk. When initially setting the DMD bit, the writing function is treated similarly to any other register (GO bit reset, DRY bit set, and no errors). Once the DMD bit is set, the programmer can write the register.

4.17 DRIVE TYPE (RPDT) REGISTER (776726)

This register allows the program to distinguish between different classes of drives. The register is located in the drive whose unit number appears in bits 02 through 00 of RPCS2. Figure 4-12 shows the RPDT register bit usage and Table 4-13 provides a description of each bit.



NOTES:

1. **Since the contents of this register are permanent with the installation of an RP04 device, the register has been replaced by a set of jumper wires.**

2. **The RP04 has been given a specific drive type number so that it can be distinguished on the Massbus among other types of devices (RS03, RP05, etc.) attached to the same controller.**

   Single controller 020020_8
   Dual controller 024020_8

3. **For the RP04 Drive type:**

   NBA = 0
   MOH = 1 **Permanently (hardwired) for RP04 device.**
   TAP = 0

4. **DRQ = 1** **(Hardwired with dual controller option installed)**
   DRQ = 0 **(Hardwired without dual controller option installed)**

Figure 4-12 Drive Type (RPDT) Register (776726) Bit Usage

Table 4-13
Drive Type (RPDT) Register (776726) Bit Assignments

Bit		Set By/Cleared By	Remarks
15	NBA (Not Block Addressed) Read only		Since the method of formatting the RP04 Drive requires that the data be located by address on a data track, this bit is hardwired to the 0 state. Since the contents of this register are permanent in nature with the installation of an RP04 device, this register is represented by a set of jumpers.
14	TAP (Tape Drive) Read only		Used by magtape units only and is hardwired to the 0 state.
13	MOH (Moving Head) Read only		Since the RP04 is a moving head device, this bit is hardwired to the 1 state.

Table 4-13 (Cont)
Drive Type (RPDT) Register (776726) Bit Assignments

Bit		Set By/Cleared By	Remarks
12	Spare		
11	DRQ (Drive Request Required) Read only		Refers to the availability of the dual controller option with the RP04 Drive. The DRQ bit is hardwired as follows: DRQ = 1 Dual controller option available DRQ = 0 Dual controller option not available
10,9	Spares		
8–0	DT(08:00) (Drive Type Number) Read only		This field contains a unique number assigned to the RP04 Drive and is used to distinguish the RP04 from other device types on the Massbus (RS03, Tape, etc.) that may be attached to the same controller. The device type number for the RP04 (device number $20_8 - 27_8$) will be hardwired permanently in the logic.

4.18 SERIAL NUMBER (RPSN) REGISTER (776730)

The purpose of this register is to distinguish a drive from similar drives attached to the same controller. The serial number provides a means of distinguishing between different RP04s with identical characteristics and which are connected to the same controller. This information is useful during error logging of on-line software diagnostics to allow errors to be associated with a particular drive. The Serial Number register differs from the Drive Type register in that the drive type refers to different types of drives such as RP04s or RP04s with major options purchased from a different vendor.

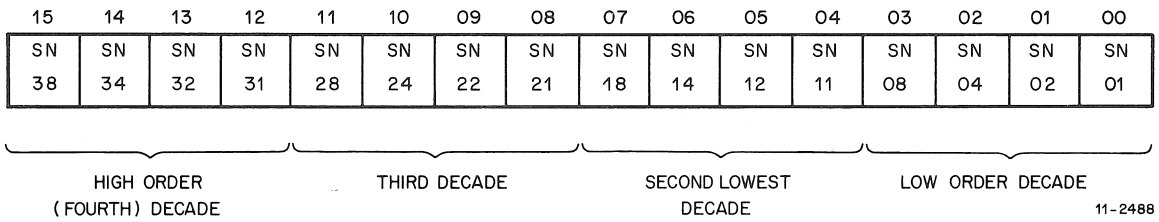
The Serial Number register is actually a jumper card with a maximum of 16 jumper wires. The serial number is established by cutting the proper wires at the factory or at installation time. The serial number of the drive itself is provided in BCD form without distinction between 50 or 60 Hz drives. The actual jumper card will be the same for all RP04 devices, but the number will be different for each RP04.

Figure 4-13 shows the RPSN register bit usage.

4.19 OFFSET (RPOF) REGISTER (776732)

The RP04, in addition to an error detection and correction capability, has the ability to offset the positioner in small increments from the track centerline in an effort to recover the data if recovery through ECC fails.

The positioner offsetting information is supplied to the RP04 directly from the software operating system. Figure 4-14 shows the Offset register bit usage and Table 4-14 provides a description of each bit.



NOTES:

1. **Not all decades may be required for identification.**
2. **The device serial number will be used in conjunction with the device type number.**

Figure 4-13 Serial Number (RPSN) Register (776730) Bit Usage

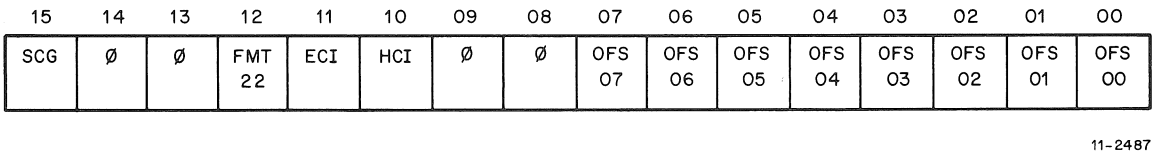


Figure 4-14 Offset (RPOF) Register (776732) Bit Usage

Table 4-14
Offset (RPOF) Register (776732) Bit Assignments

Bit		Set By/Cleared By	Remarks
15	SCG (Sign Change) Read/write		Used when a DDU and alignment (CE) pack are available to verify head alignment. Beginning from a known offset position and issuing continuous Offset commands toward the actual track centerline, the bit is guaranteed to change states when the head R/W gap is actually over the true track centerline.
14,13	Spares		
12	FMT 22 (Format Bit) Read/write	Set to a 1 when 16-bit/word format is used (16 bits/word X 256 words/sector). Set to a 0 when 18-bit/word format is used (18 bits/word X 256 words/sector). Cleared by Read-In Preset command.	This bit will be written in the cylinder address sector recorded on the data pack. Normally, this bit will be written during the format operation (write header and data). Upon reading a header from the pack, the recorded bit will be compared with bit 12 of the Offset register. If the bits do not compare, the Format Error (FER) bit will be set.

Table 4-14 (Cont)
Offset (RPOF) Register (776732) Bit Assignments

Bit		Set By/Cleared By	Remarks
11	ECI (Error Correction Code Inhibit) Read/write	Set when the software desires to inhibit error correction. If ECI is set, error correction code is disallowed; if ECI is reset, the error correction process is allowed. Cleared by Read-In Preset command.	If a data error is detected at the end of the data transmission in the read mode with the ECI bit reset, the RP04 device will immediately go into the ECC correction process. Prior to beginning the correction routine, the device will also set the Data Check (DCK) error bit, which will remain set until a Drive Clear command or an INIT pulse is received. The error correction process will require approximately 7 ms to complete before the results are available. When the results are available, the device will place the error pattern and the location of the error pattern within the data field in the appropriate ECC registers. The RUN line is expected to drop while the EBL pulse is high and, at the fall of the EBL pulse, the EXC line will also reset. The resetting of the EXC line will cause the ATTN line to set and the command will terminate. If the error was ECC noncorrectable, the RP04 will also set the ECC Hard Error (ECH) bit and will handle the EBL, EXC and ATTN lines as described above. If the ECI bit is set, the error correction process will be inhibited. The termination procedure will be done normally as if no data error occurred. Only the DCK bit will be set as soon as a data error is detected. This bit will remain set until a Drive Clear or an INIT pulse is received.
10	HCI (Header Compare Inhibit) Read/write	Set when the software desires to inhibit header compare. Cleared by Read-In Preset command.	When the RP04 sees this bit asserted, it will ignore the header compare logic and CRC check. With HCI set, the device logic depends only on the sector count field/desired address field comparison for sector identification. If the sector count field is out of sequence, the wrong sector may be affected. The meaning of the HCI bit is valid in both the Read and Write commands. It is strongly recommended, however, that the HCI bit be reset during a write operation.

Table 4-14 (Cont)
Offset (RPOF) Register (776732) Bit Assignments

Bit		Set By/Cleared By	Remarks
9,8	Spares		
7–0	OFS(7:0) (Offset Information) Read/write	Set under software control. Cleared by Read-In Preset command or at the completion of the offset operation.	The chart below shows the significance of the bits in the offset information field. Even though small increments exist, the RP04 manufacturer recommends that the offsettings for data recovery are as follows:

Position	Code Word OF0–OF7								Value/Direction (microinches)
	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0	
1st offset	0	0	0	1	0	0	0	0	+400
2nd offset	1	0	0	1	0	0	0	0	–400
3rd offset	0	0	1	0	0	0	0	0	+800
4th offset	1	0	1	0	0	0	0	0	–800
5th offset	0	0	1	1	0	0	0	0	+1200
6th offset	1	0	1	1	0	0	0	0	–1200
Return to Track Centerline									

In addition to an automatic Return to Centerline (RTC) operation when a Seek command is issued, the RP04 will provide a legal RTC command, which will return the positioner to track centerline. This command will enable the software to return the positioner to the centerline of the *current* cylinder.

If the last try on the 1200-μin. location is *not* successful, the error should be declared unrecoverable by the software. Two tries on each offset position are recommended.

With an Offset command in the Control register and the GO bit asserted, the RP04 will assume the contents of the Offset register are valid.

A 0 offset value is *not* valid. Putting a 0 in the Offset register will *not* guarantee the head's return to centerline.

It is possible for the offset address to appear as a binary combination of the OFS0 through OFS7 bits. The RP04 device will execute the offset to a position specified by the binary address in the Offset register.

The Offset register (except for FMT22, ECI, and HCI bits) will be cleared by issuing a Recalibrate, Write, Seek, or RTC command.

4.20 DESIRED CYLINDER (RPDC) REGISTER (776734)

This register is a read/write register and contains the address of the cylinder to which the positioner is to move. The desired cylinder address is loaded in the Desired Cylinder Address register via the Massbus interface.

The device logic will immediately compare the contents of the Desired Cylinder Address register with the Current Cylinder Address register through the subtract logic.

The Current Cylinder Address register reflects, at all times, the address of the cylinder which the positioner presently is addressing. The results of the subtraction between the two registers will specify the magnitude and direction of seek.

After the Desired Cylinder Address register has been loaded, a function code (Read, Write, or Seek command) specified, and the GO bit set in the Control register, the following events will take place:

1. If the subtract logic output equals 0, the *desired* cylinder address equals the *current* cylinder address and the positioner will *not* move.

2. If the subtract logic output is not equal to 0, the RP04 device will initiate a seek whose *direction* and *magnitude* are specified by the output of the subtract logic. Consequently, when the GO bit sets with a Read, Write, Search, or Seek command in the Control register, the contents of the Desired Cylinder Address register are presumed valid.

Prior to informing the controller that the seek was completed, the RP04 Drive will internally transfer, in parallel, the contents of the Desired Cylinder Address register into the Current Cylinder Address register, so that the Current Cylinder Address register reflects the actual cylinder the positioner is addressing.

Throughout the search portion of a Read or Write command and the actual data transfer, the Desired Cylinder Address register and the Current Cylinder Address register have identical contents.

If the command was a Seek command, the actual command termination would occur with the DRY bit set and the desired cylinder address transferred into the Current Cylinder Address register at the actual completion of the seek instruction.

Throughout the actual mechanical movement, the output of the subtract logic will be indicating the magnitude and direction of the seek. The device logic will actually do the decrementing of a cylinder difference counter and move the positioner to address the right cylinder.

The Desired Cylinder Address register will be cleared by the Read-in Preset command.

Although the Desired Cylinder Address register is a read/write register, the RP04 will not allow any writing in this register during a seek operation. Since the maximum number of cylinders in the RP04 is 411, only 9 bits are necessary to specify the Desired Cylinder Address register.

The Invalid Address Error (IAE) bit will be set when, upon asserting the GO bit, the contents of the Desired Cylinder Address register contain an address larger than 410.

Figure 4-15 shows the Desired Cylinder Address register bit usage.

4.21 CURRENT CYLINDER (RPCC) REGISTER (776736)

This register is a read-only register and operates in conjunction with the Desired Cylinder Address register described in Paragraph 4.20.

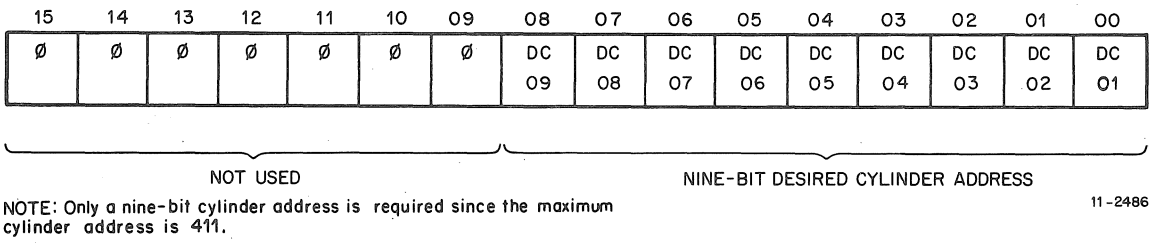
By monitoring this register, the software can determine the time required to execute the next Seek command based on the address in this register. This address reflects the exact position of the RP04 positioner whenever it is not in motion.

The Current Cylinder Address register will reset to zero:

1. On a recalibrate instruction

2. On a catastrophic error (where the device retracts the heads automatically)

3. Following the completion of the cycle-up process (heads loaded).



NOTE: Only a nine-bit cylinder address is required since the maximum cylinder address is 411.

Figure 4-15 Desired Cylinder Address (RPDC) Register (776734) Bit Usage

The Current Cylinder Address register will not reset to zero if

1. A Drive Clear command is issued
2. An initialize (INIT) pulse is received.

Figure 4-16 shows the Desired Cylinder Address register bit usage.

4.22 ERROR (RPER2) REGISTER 02 (776740)

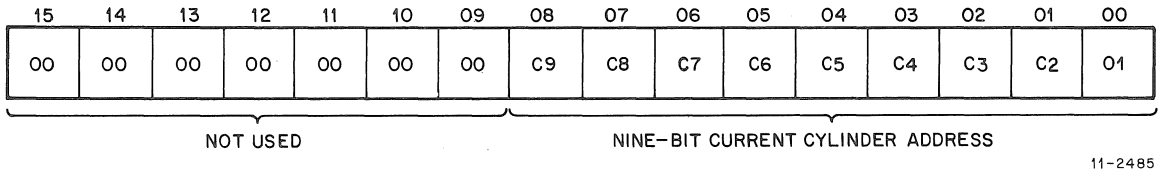
This register contains detailed error status information and is primarily used for monitoring the electromechanical performance of the drive rather than the Massbus interface. Whenever any of the bits in this register are set, the ERR bit in the Status (RPDS) register is set. In addition, the RP04 logic will cause the UNS bit in Error register 01 (RPER1) and the ATA bit in the RPAS register to set. Any of the errors in Error register 02 are considered catastrophic errors.

NOTE

All unsafe errors, with the exception of read/write unsafes, will cause the RP04 to: retract the heads from the pack area; prevent a head load from occurring; deselect all heads; disable the Read, Write, Recalibrate, Seek, and Offset commands.

All error bits will reset when a Drive Clear command or an INIT pulse is received. If the heads are retracted from the disk pack upon receiving a Drive Clear or an Initialize pulse, the RP04 will attempt to reload the heads *unless* the error persists.

Figure 4-17 shows the RPER2 bit usage and Table 4-15 provides a description of each bit.



NOTE:
Only a nine-bit current cylinder address is required, since the maximum cylinder address is 411.

Figure 4-16 Current Cylinder Address (RPCC) Register (776736) Bit Usage

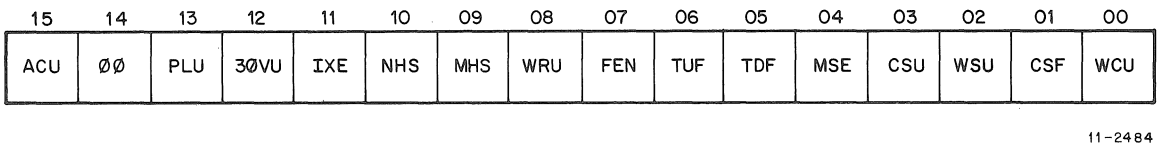


Figure 4-17 Error (RPER2) Register 02 (776740) Bit Usage

Table 4-15
Error (RPER2) Register 02 (776740) Bit Assignments

Bit		Set By/Cleared By	Remarks
15	ACU (AC Unsafe) Read/write	When set, this bit indicates that the RP04 has detected an interruption of ac power for the dc power supply. Cleared by a Drive Clear command or an INIT pulse.	
14	Not used		
13	PLU (PLO Unsafe) Read/write	Set when the RP04 has detected a loss of synchronization of the read/write phase-locked oscillator (PLO). Cleared by a Drive Clear or an INIT pulse.	
12	30 VU (30 Volts Unsafe) Read/write	Set when the drive has detected a loss of unregulated 30-volt dc power. Cleared by a Drive Clear or an INIT pulse.	This power is used by the +20.5-volt and +12.5-volt regulated power supplies.
11	IXE (Index Error) Read/write	Set when the RP04 detects a missing index pulse or an invalid index pulse. Cleared by the next valid index pulse.	
10	NHS (No Head Selection) Read/write	Set when the RP04 detects the absence of head selection when a Read or Write command is present. Cleared by a Drive Clear or an INIT pulse.	
9	MHS (Multiple Head Select) Read/write	Set when the RP04 has detected the concurrent selection of more than one head. Cleared by a Drive Clear or an INIT pulse.	
8	WRU (Write Ready Unsafe) Read/write	Set when the RP04 detects the presence of a Write command when the heads are not on the cylinder. Cleared by a Drive Clear or an INIT pulse.	
7	FEN (Failsafe Enabled) Read/write	Set when the RP04 detects an open circuit breaker in the 48-volt power driver supply. Upon detecting this error bit, the only way to reset it is to physically reset the circuit breaker and initiate a new start sequence.	The Failsafe Unload (FSU) circuit senses the voltage across the electromagnetic actuator (EMA) circuit breaker in the sequencer. As long as the circuit breaker is closed, there is no voltage across it so that the FSU circuit is disabled and -48-V power is stored in the Failsafe Reservoir (FSR). When the EMA circuit breaker opens, the voltage across it enables the FSU circuit, which uses the power stored at the FSR to actuate the EMA, retracting the heads and activating the Failsafe Enabled bit.

Table 4-15 (Cont)
Error (RPER2) Register 02 (776740) Bit Assignments

Bit	Set By/Cleared By	Remarks
6 TUF (Transitions Unsafe) Read/write	Set when the RP04 detects the absence of write transitions during a write operation. Cleared by a Drive Clear or an INIT pulse.	
5 TDF (Transitions Detector Failure) Read/write	Set when the RP04 detects write transitions without the presence of a Write command. Cleared by a Drive Clear or an INIT pulse.	
4 MSE (Motor Sequence Error) Read/write	Set if any of the following unsafe conditions are detected. SSR (Solid State Relay) failure Power Sequence Failure Brush in Pack error. Cleared by initiating a new start sequence successfully.	The SSR failure occurs when the RP04 has detected the presence of an ac voltage at the output of a de-energized SSR. The Power Sequence Failure occurs when the RP04 detects the loss of phase A or phase B voltage (with respect to phase C) after a start sequence. The Brush in Pack error occurs when the RP04 detects the brushes within the pack area when the disk is spinning at approximately 80% of its normal speed. A Motor Sequence error will disable the start sequence and initiate a stop sequence. This action results in a heads retracted condition and will prevent a head load. The Motor Sequence error bit is implemented such that if an SSR failure does *not* occur during startup, this error bit will indicate a Power Sequence Failure or Brush in Pack error while the drive motor is trying to get up to speed. **NOTE** **During power down, the Motor Sequence error bit will *not* be looked at to avoid getting a false indication of an error, since the state of the SSR cannot be predicted.**
3 CSU (Current Switch Unsafe) Read/write	Set when the RP04 detects an incorrect write current level during a write operation. Cleared by a Drive Clear or an INIT pulse.	
2 WSU (Write Select Unsafe) Read/write	Set when the RP04 detects that both even-side and odd-side heads are simultaneously enabled for writing. Cleared by a Drive Clear or an INIT pulse.	

Table 4-15 (Cont)
Error (RPER2) Register 02 (776740) Bit Assignments

Bit	Set By/Cleared By	Remarks
1 CSF (Current Sink Failure) Read/write	Set when the RP04 detects the current sink nonoperative without the presence of a Write command. Cleared by a Drive Clear or an INIT pulse.	
0 WCU (Write Current Unsafe) Read/write	Set when the RP04 detects the presence of write current without the presence of a Write command.	

4.23 ERROR (RPER3) REGISTER 03 (776742)

This register contains detailed error status information and is primarily used for monitoring the electromechanical performance of the drive rather than the Massbus interface. Whenever any of the bits in this register are set, the ERR bit in the Status (RPDS) register is set. In addition, the RP04 logic will cause the UNS bit in Error register 01 (RPER1) and the ATA bit in the RPAS register to set. Error bits 0, 1, and 3 are considered catastrophic errors.

NOTE

All unsafe error conditions, with the exception of read/write unsafes, will cause the RP04 to: retract the heads from the pack area; prevent a head load from occurring; deselect all heads; disable the Read, Write, Recalibrate, Seek, and Offset commands.

All error bits will reset when a Drive Clear command or an INIT pulse is received. If the heads are retracted from the disk pack upon receiving a Drive Clear or an Initialize pulse, the RP04 will attempt to reload the heads unless the error persists.

Figure 4-18 shows the RPER3 bit usage and Table 4-16 provides a description of each bit.

4.24 ECC POSITION (RPEC1) REGISTER (776744)

The RP04 has an ECC (error correction code) capability which will generate, detect, and correct an error by reconstructing a portion of the data. Within the specified code word length, which is fixed, the burst ECC code will correct an error which must fall within the specified length of the burst. The actual location of the burst within the code word (data field of a sector) is irrelevant.

Any errors outside the specified burst length will be detected but not corrected. The ECC hardware, in this case, will yield an ECC uncorrectable error. The RP04 logic contains the hardware to find the burst within which the read error is included and determine the exact location of the burst within the data field.

The ECC Pattern register contains the actual error burst and the ECC Position register contains the address for determining the actual location of the error burst within the data field.

NOTE

The actual correction of the data field is done by the software with the help of the ECC Position and ECC Pattern registers.

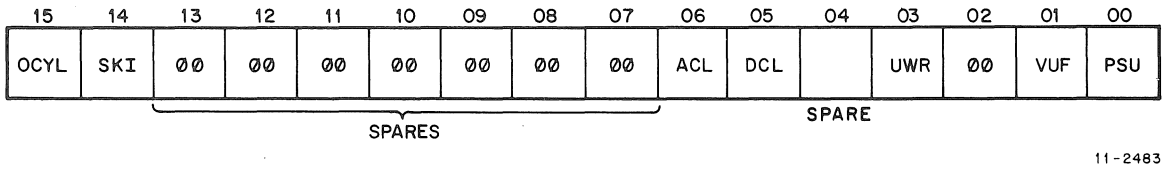


Figure 4-18 Error (RPER3) Register 03 (776742) Bit Usage

Table 4-16
Error (RPER3) Register 03 (776742) Bit Assignments

Bit		Set By/Cleared By	Remarks
15	OCYL (Off Cylinder) Read/write	Set when an invalid off cylinder condition is detected resulting in a Seek Incomplete. Cleared by a Drive Clear or an INIT pulse.	An off cylinder error will also cause an automatic recalibrate operation to occur.
14	SKI (Seek Incomplete) Read/write	Set when a seek operation fails to complete within 85 ms from a seek initiation.	Due to a positioner malfunction it is possible for the seek not to complete. The RP04 will assume a positioner hardware problem and will: Set the SKI bit Set the ATA bit Reset the PIP bit Set the RDY bit. This indicates to the software that the seek operation did not complete and the exact positioner location is unknown. A SKI condition will cause the RP04 to determine that the drive is unsafe to operate and will cause the UNS (RPER1, bit 14) bit to set. The software can diagnose the trouble by monitoring the Error register. The device logic has already issued a Recalibrate command *internally* upon detecting a Seek Incomplete, and the positioner is on its way back. A *second* Recalibrate command does not have to be issued by the software. The device will wait for the completion of the recalibrate before setting the RDY bit and raising ATTN. A successful completion of a recalibrate operation clears the Current Cylinder Address register and sets the ATA bit. **NOTE** **Since an error exists in the Error register (SKI error bit is set), the software must issue a Drive Clear command to clear the error before attempting to retry.**

Table 4-16 (Cont)
Error (RPER3) Register 03 (776742) Bit Assignments

Bit		Set By/Cleared By	Remarks
14 (Cont)			The path is now clear for the software to retry by issuing another Seek command. **NOTE** **The internal 85-ms Seek Time-Out one-shot will be triggered each time a Seek command is issued.** **Following the cycle-up progress, the RP04 will wait for the sector count to be in sync with the rotating medium before setting the Device Ready line. Following the initial syncing of the sector count field, it will not be necessary to resync the counter on every seek completion.**
13–7	Spares		
6	DCL (DC Low) Read/write	Set when the RP04 detects a loss of regulated 5 Vdc power, which powers the Massbus interface electronics. Cleared by a Drive Clear or an INIT pulse.	The detection of the DCL error condition will cause an automatic head retraction.
5	ACL (AC Low) Read/write	Set when the RP04 detects an interruption of primary ac power for the dc power supply which powers the Massbus interface electronics. Cleared by a Drive Clear or an INIT pulse.	The detection of the ACL error condition will cause an automatic head retraction.
4	Spare		
3	UWR (Any Unsafe Except Read/Write) Read/write	Set if any of the following unsafe conditions are detected (indicates a head retract has occurred): Pack Speed Unsafe 30 Volt Unsafe Velocity Unsafe Servo Unsafe AC Unsafe DC unsafe Cleared by a DC Clear or an INIT pulse.	DC Unsafe occurs when the RP04 has detected a failure of one of the regulated supply voltages. A DC Unsafe will: cause the heads to retract from the pack area; prevent a head load from occurring; deselect all heads; and disable the Read, Write, Recalibrate, Seek, and Offset commands.

Table 4-16 (Cont)
Error (RPER3) Register 03 (776742) Bit Assignments

Bit		Set By/Cleared By	Remarks
2	Spare		
1	VUF (Velocity Unsafe) Read/write	Set when the RP04 detects an excessive positioner velocity. Cleared by a DC Clear or an INIT pulse.	
0	PSU (Pack Speed Unsafe) Read/write	Set when the RP04 detects the pack speed to be below approximately 80% of normal while the heads are positioned within the pack area. Cleared by a Drive Clear or an INIT pulse.	

The ECC Position register contains the exact location of the error burst within the data field following the completion of the error correction procedure (refer to Paragraph 3.7).

Upon completion of the ECC process, the device will load this register with the necessary information. The EXC line is raised upon initiation of the error correction procedure and the ATA bit is set at the trailing edge of EBL and EXC.

Figure 4-19 shows the ECC Position register bit usage.

4.25 ECC PATTERN (RPEC2) REGISTER (776746)

This register is used in conjunction with the ECC Position register (Paragraph 4.24) and contains the actual error burst available at the completion of the ECC internal to the RP04 device logic error correction process.

The software will use the contents of the ECC Position register to find the actual location of the error burst in the data field. Then the error burst itself will determine the bits in error within the 11-bit field. Figure 4-20 shows the ECC Pattern register bit usage.

4.26 RH11/RP04 REGISTER SUMMARY

Figure 4-21 shows the bit assignments of the 20 registers in the RH11 and the RP04 Drive in a quick-look form. The registers are listed in sequential order by Unibus address.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
00	00	00	BLC 4096	BLC 2048	BLC 1024	BLC 512	BLC 256	BLC 128	BLC 64	BLC 32	BLC 16	BLC 08	BLC 04	BLC 02	BLC 01

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Figure 4-19 ECC Position (RPEC1) Register (776744) Bit Usage

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
00	00	00	00	BIT 00	BIT 10	BIT 09	BIT 08	BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00

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Figure 4-20 ECC Pattern (RPEC2) Register (776746) Bit Usage

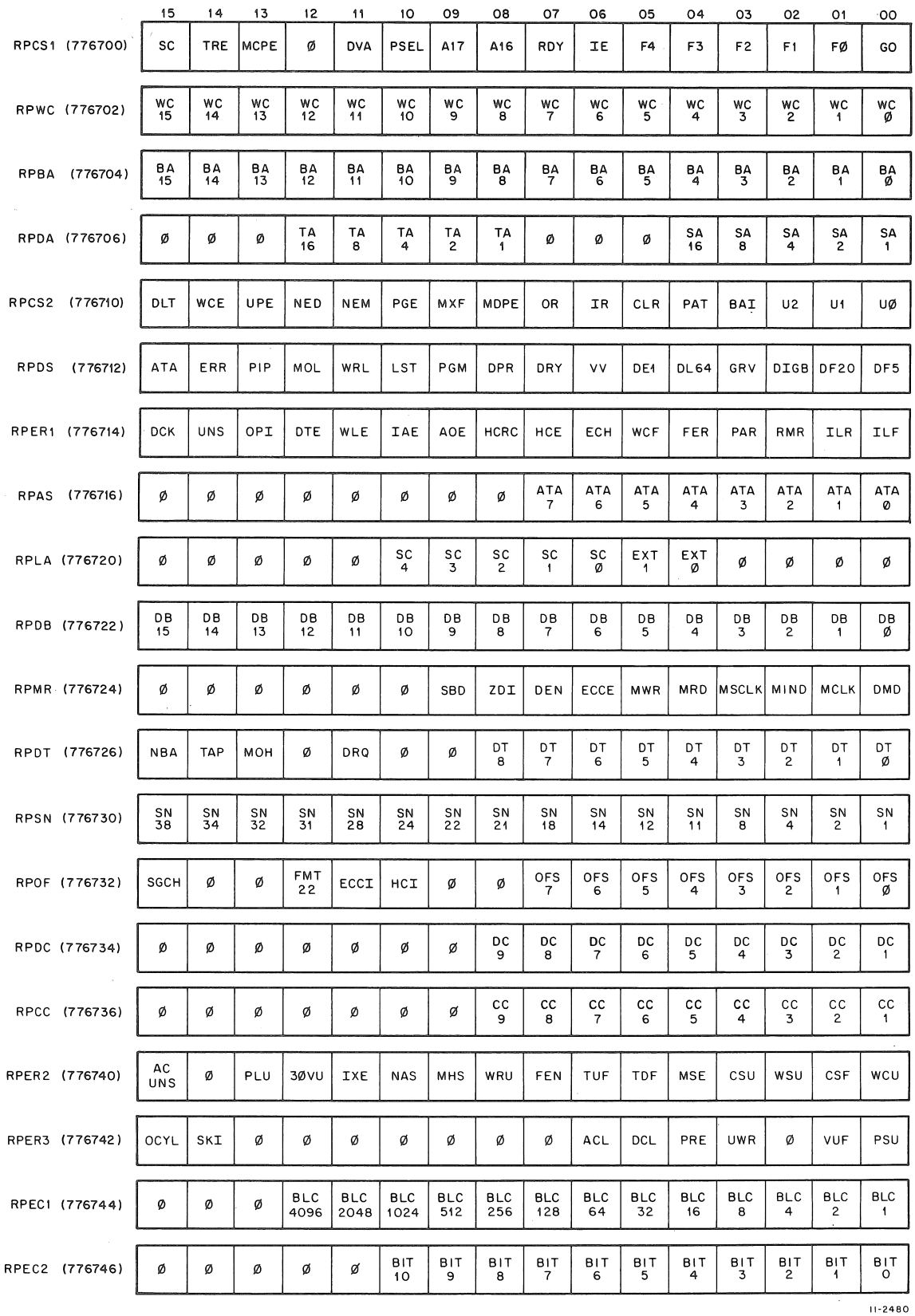


Figure 4-21 RH11/RP04 Register Summary

CHAPTER 5
THEORY OF OPERATION

5.1 GENERAL

This chapter describes the theory of operation of the RH11 Controller in two functional groupings – the register control path and the DMA path. These are described in detail in the following paragraphs.

5.2 REGISTER CONTROL PATH

The register control path provides the interface that enables the program to read from or write into any register in the RH11 or associated drive. Specific bits in these registers are designated as follows: 'read only' bits indicate that the program can read the status of these bits but cannot load them; 'write only' bits indicate that the program can load them but will read back a 0; 'read/write' bits indicate that the program may load them and read back the status.

The RH11 examines Unibus address bits 17 through 05 (17 through 06 if there are a total of more than 16 registers) to determine if the register being addressed is an RH11 register (Figure 5-1). The address field can be defined by a set of jumpers within the RH11. The Unibus address is compared with the set of jumpers and, if the two match, the addressed register is a valid RH11 register which enables the circuitry for a register function. If the Unibus address does not compare with the jumpers, the RH11 will not accept the address and will not initiate a data transfer with the processor.

5.2.1 Writing a Local Register

Unibus address bits 04 through 00 (05 through 00 if more than 16 registers are employed) select a cell in a read only memory (ROM) which specifies a unique register. The ROM outputs are register select signals (RSEL 04:00), two coded bits (M6 and M7), and a LOCAL/REM signal. Since this description involves accessing a local register (one contained in the RH11), LOCAL is generated at the output of the ROM as LOC/REM H. When this signal is unasserted or low and a register operation is being performed, a remote register is selected. Signals RSEL 01:00 and M6 and M7 are supplied to the register decoders to select one of the local registers. RSEL 04:00 is also supplied to the Massbus control logic, but is inhibited from the Massbus because a 'write local register' function is specified and REM remains unasserted.

Unibus control lines A0, C0, and C1 specify the direction of transfer and also specify byte or word addressing. When writing a register, the C0 and C1 lines are encoded for a DATO or DATOB (if byte addressing is specified). The A0, C0, and C1 control lines are supplied to a direction control network which generates IN, OUT, HI BYTE, or LO BYTE signals depending on the cycle desired. These signals are fed to the register decoder where they are used in decoding the various register enable signals.

The Unibus A data lines are connected to the RH11 and contain the data used to load the desired register.

When BUSA MSYN is received from the central processor (150 ns after the data, control and address are placed on the Unibus), a DEV SEL (device select) signal is generated which enables the register decoder to generate the appropriate enable signal for the register specified. Signal REG STR is created 85 ns later and is ANDed with the HI BYTE or LO BYTE signal and the specified register enable signal from the register decoder. The signals designated with IN are used for *writing* local registers; the signals designated OUT are used for *reading* local registers. For example, if it was desired to write into the WC (word count) register, the register decoders specify the WC IN L signal, which is ANDed with HI BYTE or LO BYTE and REG STR to generate a clock used to load the WC register. The data is clocked into the WC register at the time of REG STR. The trailing edge of this signal, which is 135 ns long, causes SSYN to be asserted. The central processor receives SSYN and lowers MSYN, which deselects the RH11 from the Unibus. The lowering of MSYN then causes SSYN to be lowered, and 75 ns after the lowering of MSYN, the address lines change and the cycle is completed.

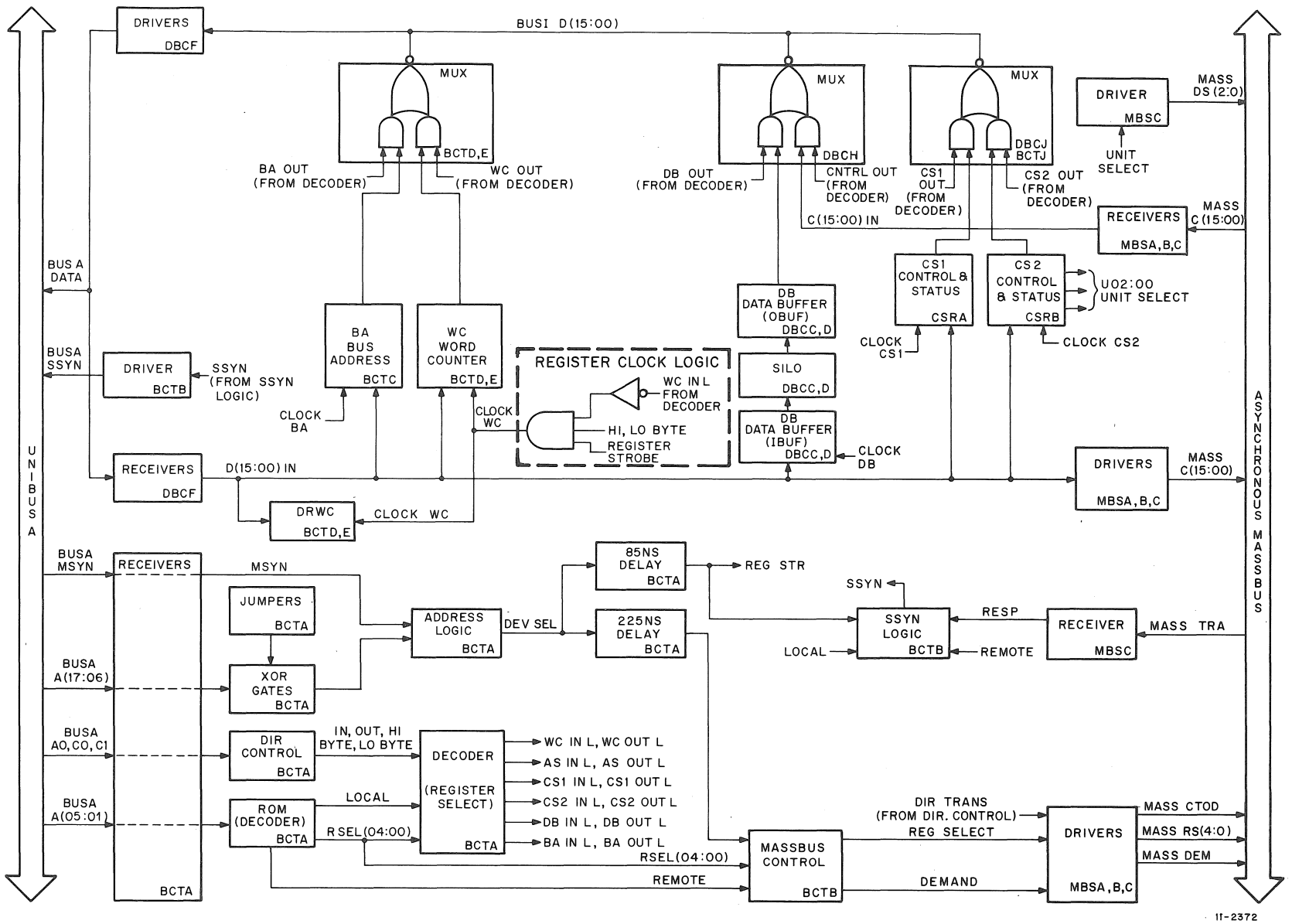


Figure 5-1 Register Control Path

5.2.2 Reading a Local Register

The process of reading a local register is the same as that described for writing a local register (Paragraph 5.2.1) with the following exceptions:

1. The C0 and C1 Unibus control lines are decoded for a DATI or DATIP operation.

2. When reading a local register, the register "OUT" signals of the register select decoders gate the contents of the register on the BUSI lines for transmission to the processor via Unibus A.

5.2.3 Writing a Remote Register (Figure 5-2)

A remote register is defined as a register located in the drive. The data path for writing a remote register is from Unibus A via data lines D00–D15 IN H on to the Massbus via control lines MASS C00–C15 H, where the data is received by the selected drive and loaded into the specified register in that drive. A CTOD (Controller to Drive) signal on the Massbus specifies the direction of transfer to the drive.

The upper address bits of the Unibus address are compared with a set of jumpers in the RH11 to enable the register selection logic, previously described. Unibus address bits 04 through 00 (05 through 00 if more than 16 registers are employed in the system) select a cell in the ROM (read only memory) which specifies a particular register. The outputs of the ROM are register select signals RSEL (04:00), two coded bits (M6 and M7), and the LOCAL/REM signal. The selected drive, whose unit number was preloaded by the programmer in the CS2 register, is specified by device select lines DS00 through DS02 on the Massbus.

When the MSYN signal is received over the Unibus by the RH11, the DEV SEL signal is enabled and a delay of 220 ns occurs before the RH11 issues DEM to the Massbus. This delay allows the select and data lines to settle and be decoded on the Massbus before the drive strobes the Massbus control lines. When the drive receives DEM and recognizes the unit address as its own and when the data has been clocked into the appropriate drive register, it issues transfer (TRA) to the RH11. When the RH11 receives TRA indicating that the drive has obtained the data, it issues SSYN to the processor. SSYN signals the processor that the slave (RH11) has finished the cycle, and the processor removes MSYN which, in turn, causes SSYN to go unasserted. Also MSYN going unasserted, removes the DEV SEL signal which causes DEM to drop. This action, in turn, causes TRA from the drive to go unasserted. The address and data is then removed from the Unibus and Massbus to complete the cycle.

5.2.4 Reading a Remote Register (Figure 5-3)

The process of reading a remote register is similar to that of writing a remote register with the following exceptions:

a. The data path for reading a remote register is from the drive to Massbus control lines C00 through C15 H, to the RH11 open-collector multiplexers (8234), to the BUSI lines, and then to the Unibus A data lines D00–D15.

b. Upon receipt of TRA when writing a remote register, SSYN is immediately sent to the CPU. When reading a remote register, however, SSYN is delayed 220 ns from transfer (TRA) to ensure that the data is present and settled on the Unibus.

5.3 DMA DATA PATH

Figure 5-4 is a block diagram of the DMA data path. The diagram shows three basic data flows – write, read, and write-check. These are briefly described below.

Write – Data is routed from the Unibus through two multiplexers (DMX and IMX) and into IBUF. The DMX multiplexer selects the data from Unibus A or Unibus B. If SEL BUS A is present, Unibus A is selected; if this signal is not asserted, Unibus B is selected. The IMX multiplexer selects the data from the DMX or from the Massbus depending on the function being performed. For a write function, the data at the output of IMX is from the Unibus and for a read or write-check function, the data is from the Massbus. The data words are gated into IBUF and bubble through the Silo to OBUF. For the write function, the data from OBUF is supplied to drivers and then to the Massbus data lines (MASS D00–D17).

Read – Data is routed from the Massbus data lines (MASS D00–D17) to IBUF through the IMX multiplexer. Just as in the write function, the data from IBUF bubbles through the Silo into OBUF. From OBUF, the data is gated onto Unibus A if SEL BUS A is present; otherwise, the data is gated onto Unibus B.

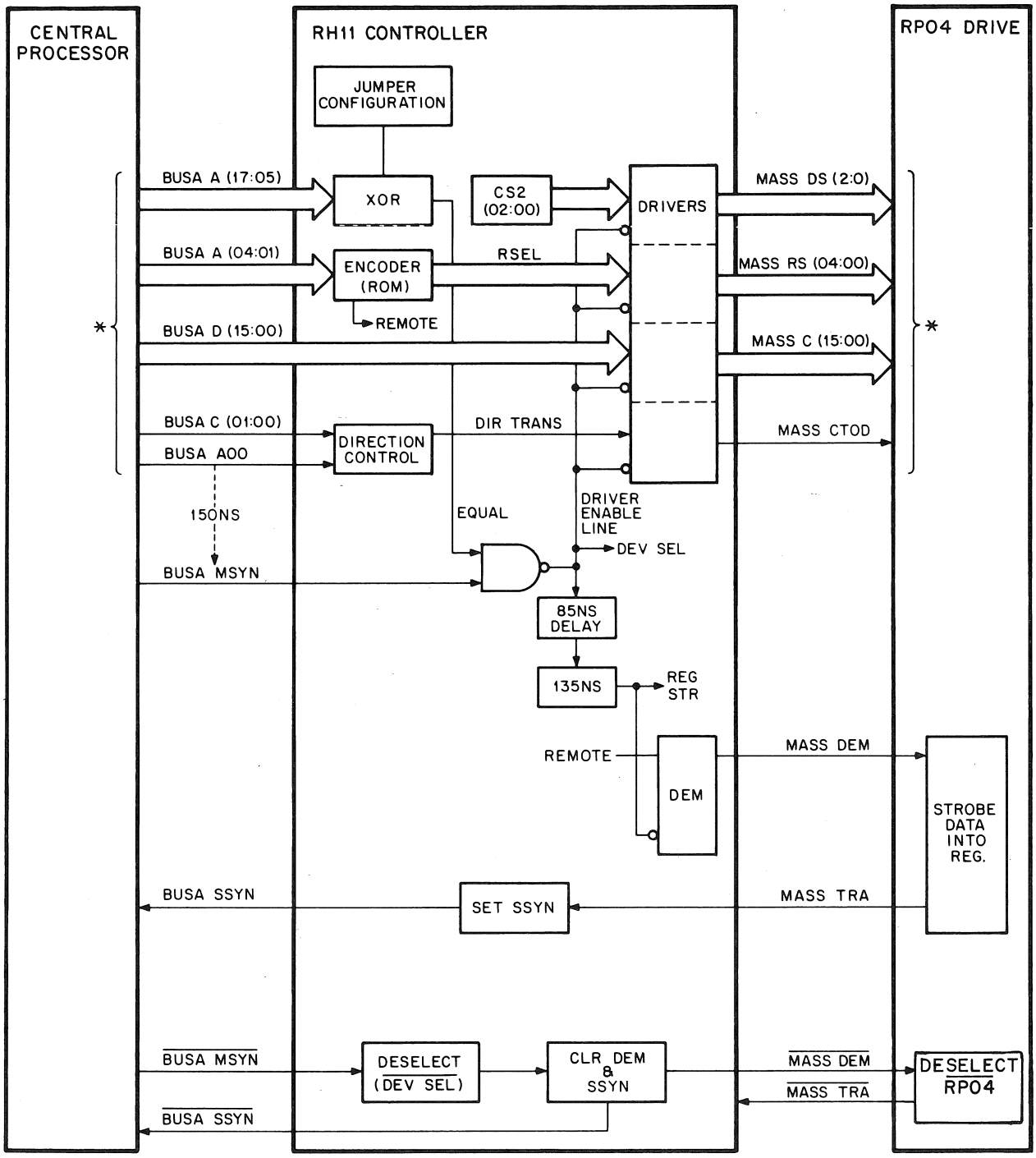
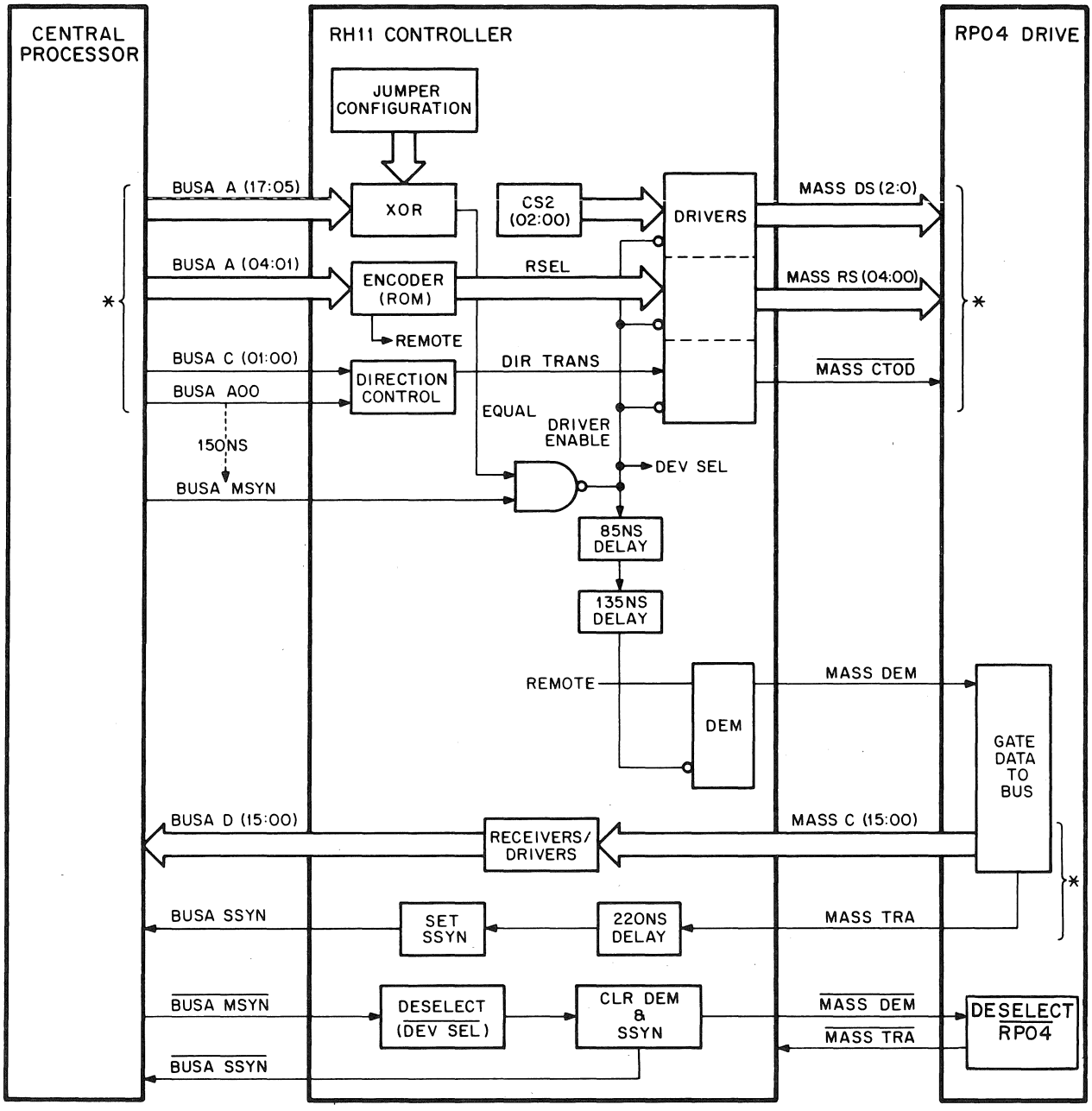


Figure 5-2 Writing Remote Register Interface



* ALL EVENTS WITHIN BRACKET OCCUR AT APPROXIMATELY SAME TIME.

11-2374

Figure 5-3 Reading Remote Register Interface

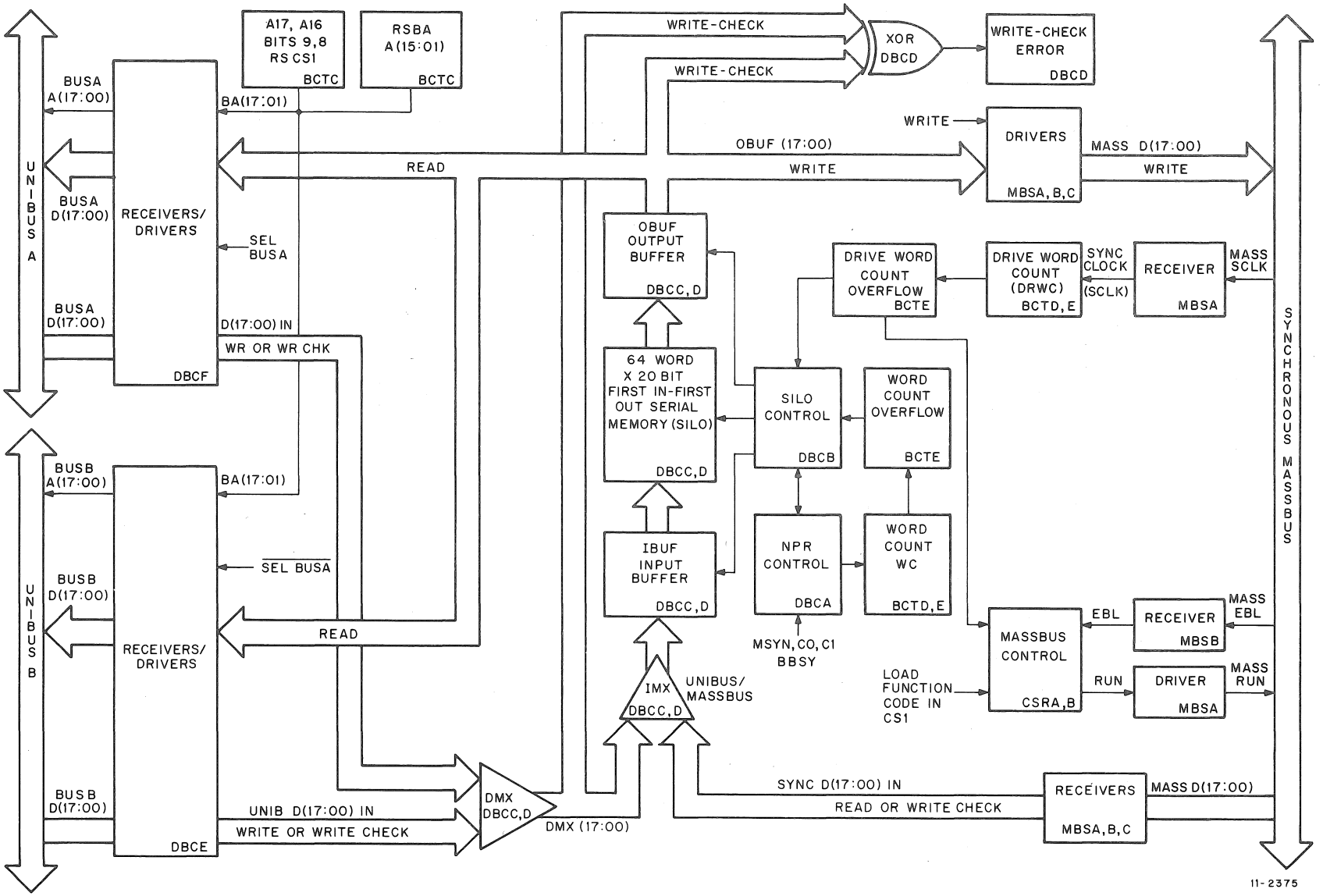


Figure 5-4 DMA Data Path Block Diagram

Write-Check – In the write-check function, the data that has previously been written onto the disk is compared with the contents of the memory locations that were the source of this data. In this way, errors in transmission can be easily detected. The data from the Massbus is fed through the IMX multiplexer into IBUF. From IBUF, the data bubbles through the Silo into OBUF and to a series of write-check Exclusive-OR gates. The second input to these gates is from the DMX multiplexer which contains data from the corresponding Unibus memory location. If the data from memory does not compare to the data read from the disk, a write-check error is flagged indicating a transmission error.

Figure 5-4 shows the bus address used to address memory on the Unibus. This is obtained from the BA register and from bits 9 and 8 of the CS1 register to form the 18 bit Unibus address. Both the word count (WC) and drive word count (DRWC) logic is shown. The word count keeps track of the number of words transferred between the Unibus memory and RH11 while the drive word count keeps track of the number of words transferred between the RH11 and the drive via the Massbus. When the WC register overflows, the RH11 ends the Unibus transfer; when the DRWC register overflows, the RH11 ends Massbus transfers.

In order to describe the data transfer operation of the RH11 in more detail, the following paragraphs present each function (read, write, write-check) as it interfaces between the Unibus and Massbus.

5.3.1 Write Block Transfer

Figure 5-5 is an interface diagram showing the action of the RH11 during a write data transfer. Initially, the desired address, bus address, selected unit, and word count are specified by the program. The desired address consists of the drive track and sector address desired to write on. This address is sent to the device and will be compared to the various sector addresses of the rotating disk. The bus address and word count are supplied to the RH11 and are monitored by circuitry in the RH11. The program, in this case, also specifies a write command code with the GO bit set (bits 5 through 0 of the CS1 register). The RH11 transfers the write command code and the GO bit to the selected drive and also examines the command code to enable the appropriate logic (memory reference, Silo control, data path, and Massbus control). The write command code and GO bit, which are sent to the drive, are stored in the drive's function register (bits 5 through 0 of CS1) and are decoded by the drive in order to determine the function to be performed.

NOTE

When a write command and the GO bit are loaded, the RH11 becomes busy and cannot accept another data transfer command.

The drive then waits for the RUN assertion from the Massbus before staring to search for the desired disk address where the data transfer will be initiated. The RUN signal is asserted by the RH11 when the Silo has been filled with a prescribed number of words, depending on the Silo capacity selected.

When the RH11 decoded the write command code from the program, it issued an NPR data request on the selected Unibus.

NOTE

The NPR request allows the RH11 to acquire bus mastership in order to transfer data directly to or from memory. This sequence is described in detail in Paragraph 6.7.

When bus mastership is granted to the RH11, the RH11 sends a memory address [stored in the bus address (BA) register and in bits 8 and 9 of the CS1 register] to memory via the Unibus. The RH11 asserts BUS MSYN 200 ns after the address is placed on the Unibus. The specified memory location responds with the data word in that location and the SSYN control signal. The data word is clocked into the IBUF register in the RH11, the WC register is incremented by 1, and the BA register is incremented by 2.

NOTE

The WC register is initially loaded with the 2's complement of the number of words to be transferred and is incremented toward 0 for each word transferred. The BA register is incremented by 2 since the RH11 is a word-oriented device and the PDP-11 memory system is byte-oriented.

If the first word of the Silo is empty at this time, the RH11 will initiate a second memory reference. If the first cell of the Silo is full or if this is the second memory reference of back-to-back NPRs, the RH11 will release control of the Unibus and will wait for IBUF to be empty before initiating another NPR request. When word count overflow occurs or an error is detected, the Unibus memory references are terminated.

NOTE

The RH11 can perform single-cycle or back-to-back memory references for each NPR request.

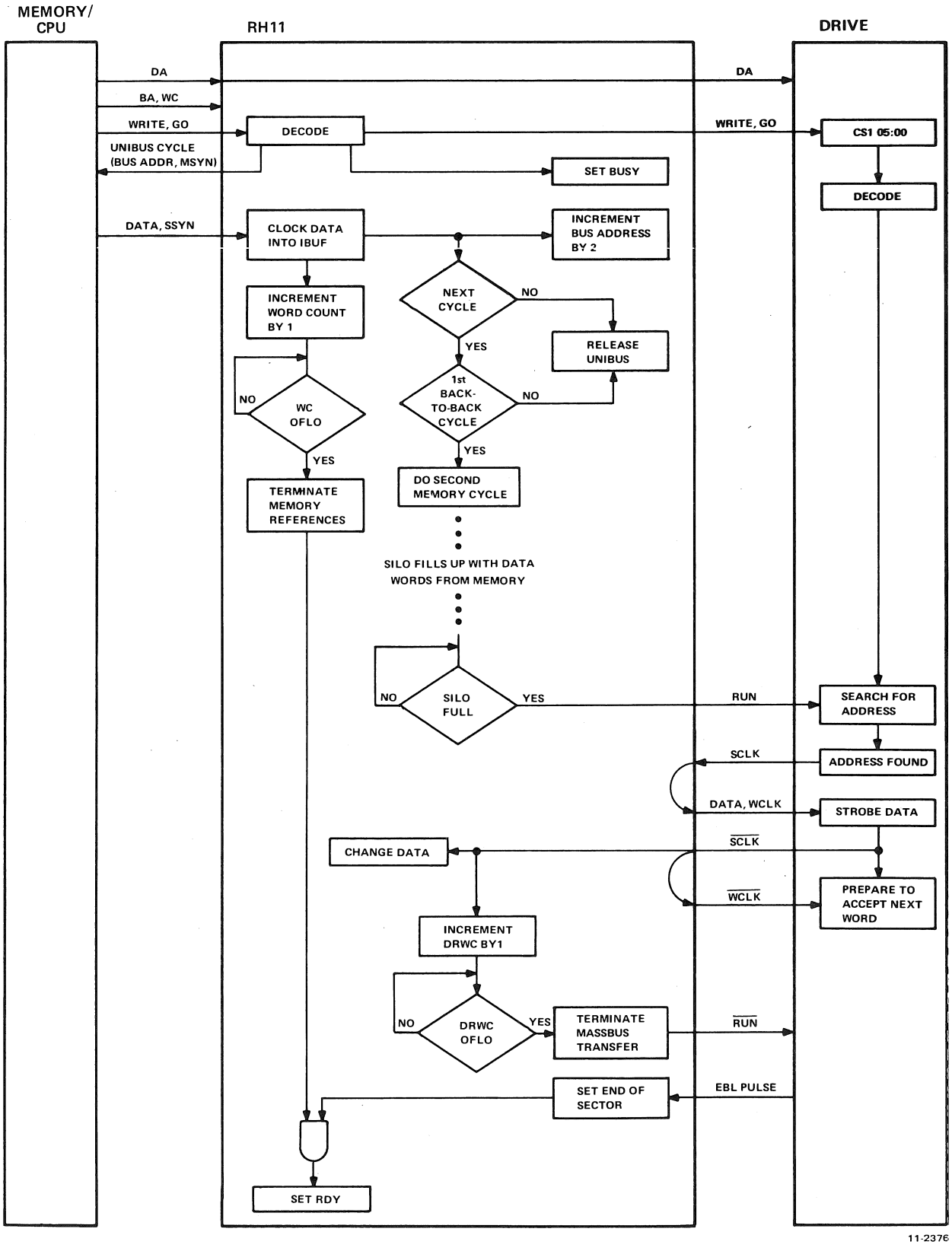


Figure 5-5 Write Cycle Interface Diagram

The data word which was clocked into IBUF from memory is automatically transferred to the bottom cell of the Silo if this cell is empty. If the cell is full, the data word in IBUF remains in IBUF until the data word in the bottom cell of the Silo has propagated to the next cell. Once a word is input to the Silo, it "bubbles" through the Silo to the last empty cell. Once a data word appears at the last cell of the Silo, it is clocked into the OBUF register, provided OBUF is empty. If OBUF is not empty, the data word remains in the last cell. Successive data words stack up in the Silo in a first in/first out (FIFO) sequence.

Each time a data word is input into IBUF, a start counter is incremented to determine how many words will be stacked in the Silo before the drive is signaled to begin the data transfer by the assertion of the RUN signal on the Massbus.

NOTE

There are four different Silo capacities which can be selected (Paragraph 6.19).

When the RUN signal is asserted on the Massbus and the drive has decoded a write command code, the drive starts to search for the desired address. When it has found the desired address, it issues synchronous clock (SCLK) signals on the Massbus. The SCLK is received by the RH11 and re-driven onto the Massbus as a write clock (WCLK) signal. The data word in OBUF is transferred to the drive on the leading edge of WCLK (leading edge of SCLK plus cable delay). The drive accepts the data word on the leading edge of WCLK. On the trailing edge of SCLK, the RH11 writes over the previous data word in OBUF with the word in the last cell of the Silo. A drive word count register (DRWC), which was initially loaded with the same value contained in the WC register, is incremented by 1 toward 0 for each word transferred. Successive words are transferred in this manner and when the required number of words are transferred, drive word count overflow occurs and the RUN line goes unasserted. If the number of words to be transferred is less than a complete sector, the drive is zero-filled in the remaining words in the sector. This action causes 0s to be loaded in the remainder of the sector by disabling the Massbus data drivers.

The drive signals completion of the sector with an EBL (End of Block) pulse. When the RUN signal is unasserted with the EBL pulse present, the data transfer is terminated and the RH11 transitions to the Ready state. If the number of words to be transferred is greater than a sector, the RUN line remains asserted at EBL time signaling the drive to continue transferring words to the next sector.

5.3.2 Read Block Transfer

Figure 5-6 is an interface diagram showing the action of the RH11 during a read data transfer. Initially, the desired address, bus address, selected unit, and word count are specified by the program as in the write block transfer. The program then loads a read command code with the GO bit set (bits 5 through 0 of the CS1 register). The RH11 transfers the read command code and the GO bit to the selected drive and also examines the command code to enable the appropriate logic (memory reference, Silo control, data path, and Massbus control). The read command and GO bit, which are sent to the drive, are stored in the drive's function register (bits 5 through 0 of CS1) and are decoded by the drive to determine the function to be performed.

NOTE

When a read command and the GO bit are loaded, the RH11 becomes busy and cannot accept another data transfer command.

The RH11 now asserts the RUN line on the Massbus to signal the drive to begin searching for the desired address specified. Once the drive has reached the desired address and begins to read the data, it presents a data word accompanied by SCLK on the Massbus. At the trailing edge of SCLK, the RH11 loads the data word into IBUF. In addition, the DRWC register is incremented. From IBUF, the data word automatically sequences through the Silo to the OBUF register. Successive words are transferred in this manner until the DRWC register overflows. When overflow occurs, the RUN line is negated and all remaining words in the sector are disregarded by the RH11. The drive indicates completion of the sector transfer by issuing an EBL (End of Block) pulse. If the RUN line is unasserted when EBL occurs, the data transfer is terminated and the RH11 becomes Ready as soon as the remaining Unibus memory references have been completed. If the number of words to be transferred is greater than the sector, the RUN line remains asserted at EBL time signaling the drive to continue transferring data words from the next sector.

The data words input to IBUF are propagated through the Silo. When the first data word reaches OBUF, an NPR request on the selected Unibus is issued and the WC register is incremented toward 0. This register is loaded with the 2's complement of the number of words to be transferred and incremented each time a word is loaded in OBUF.

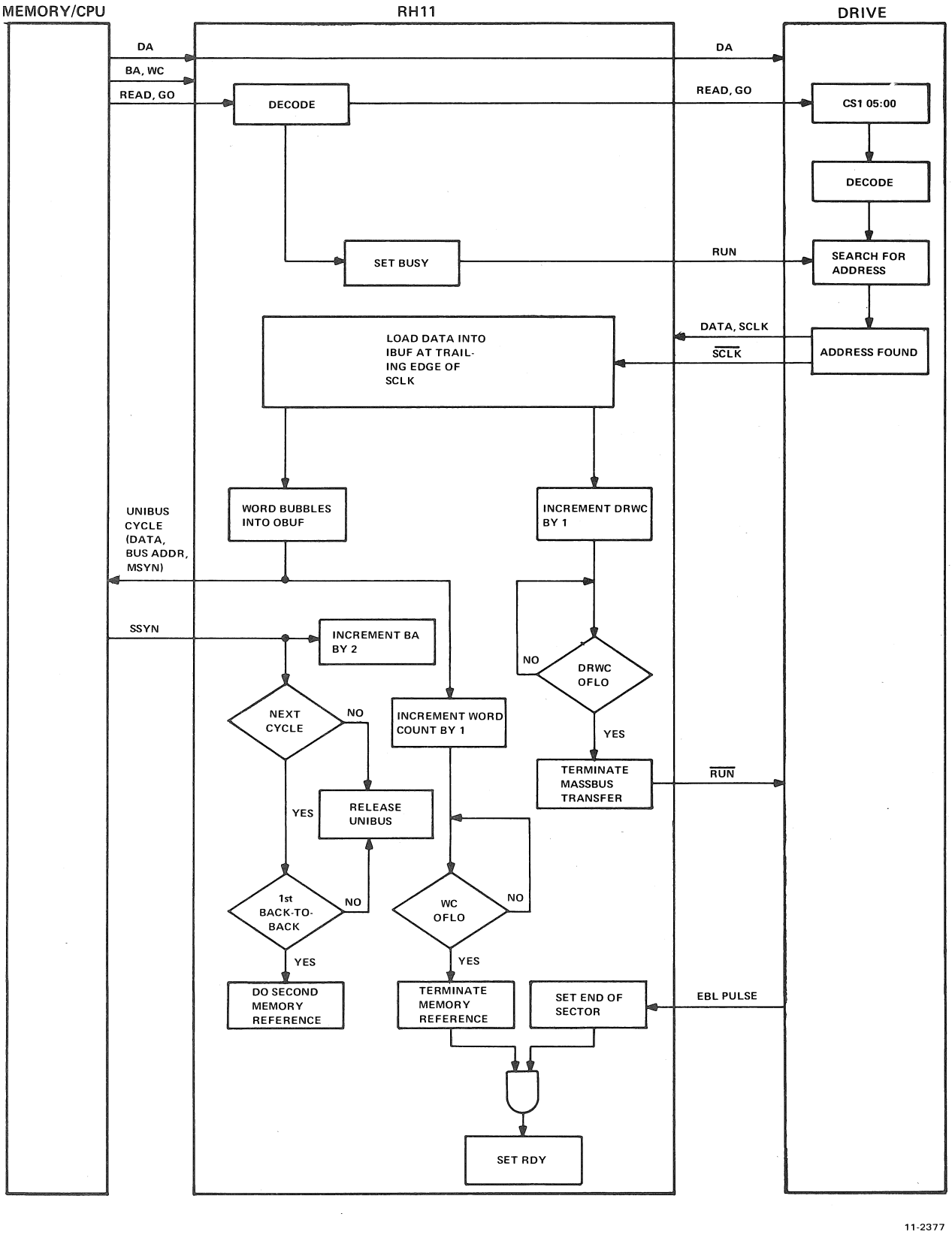


Figure 5-6 Read Cycle Interface Diagram

NOTE

The NPR request allows the RH11 to acquire bus mastership in order to transfer data directly to or from memory. This sequence is described in Paragraph 6.7.

When the RH11 acquires bus mastership, it sends a memory address (stored in the BA register and in bits 8 and 9 of CS1) and data (stored in OBUF) onto the Unibus. The RH11 issues BUS MSYN 200 ns after the data and address are placed on the Unibus. Memory acknowledges receipt of the data by asserting SSYN. The RH11 then removes MSYN and waits 75 ns before changing the data and address. After the data word has been transferred, the Bus Address register is incremented by 2 since the RH11 is word-oriented and the PDP-11 memory reference system is byte-oriented.

If there is a word in the top cell of the Silo when the data word is transferred from OBUF, the RH11 will maintain control of the Unibus for a second memory reference. If a word is not stored in the top cell of the Silo, or if this transfer is the second word of a back-to-back memory reference, the RH11 releases control of the Unibus and does not initiate a new NPR request until OBUF becomes full again.

NOTE

The RH11 can perform single-cycle or back-to-back memory references for each NPR request.

When word count overflow occurs or an error condition is present, the Unibus memory references are terminated. When the Unibus memory references are terminated and the drive reaches the end of the last sector, the RH11 transitions to the Ready state.

5.3.3 Write-Check Block Transfer

Figure 5-7 shows the interface diagram for a write-check operation. In a write-check operation, data written on the disk is validated by comparing it with the data in memory used to write it on the disk. This operation will reveal the addition or loss of any bits in the transmission process from memory to the disk via the RH11. This operation is similar to the read data transfer where the data is successively read from the disk, gated into IBUF (on the negation of SCLK), and propagated through the Silo. When the first data word reaches OBUF, an NPR request is initiated and a Unibus cycle allows the original data word from memory to be supplied to the RH11. The data word in OBUF is compared with its original counterpart from memory. If any bits do not compare, the WCE (Write-Check Error) bit is set and the word is 'frozen' in OBUF so that the program can examine the data word in error from the disk. If the bits do compare, the write-check operation continues until the final sector is checked or until an error is detected.

When the RH11 becomes bus master and requests a data word from memory, memory issues the data word on the Unibus accompanied by SSYN. When the RH11 receives SSYN, it waits 125 ns to deskew data on the Unibus and to allow the data to propagate through the XOR gates before MSYN is cleared.

5.4 WRITE FLOW DIAGRAM DESCRIPTION

Figure 5-8 is a detailed flow diagram of the write data transfer. Initially, the RH11 is in the Ready state and the program specifies the bus address, desired address, word count, and selected unit (specified in CS2). A Write command is loaded in bits 05 through 01 of CS1 and the GO bit is set in bit 00 of CS1. The Ready state in the RH11 is then cleared and the Silo is initialized. At this point the flow diagram divides into two asynchronous paths – one for the Unibus sequence of events and one for the Massbus sequence of events. The Unibus flow is discussed first inasmuch as a START signal, generated in this path, is necessary to initiate the Massbus flow.

5.4.1 Unibus Flow Description

When the Write command is loaded in CS1, DATA REQ is set. This signal asserts the BUS NPR line to request a Unibus cycle. The processor acknowledges the NPR by returning NPG (non-processor grant). The RH11, in turn, clears NPR and asserts SACK, indicating acknowledgment of the NPG. If a cycle is already in progress, the RH11 waits until BBSY and SSYN become negated. When this occurs, the RH11 asserts BBSY, indicating it is now bus master and negates BUS SACK. In addition, NPC MASTER is asserted which initiates the timing for the NPR cycles.

The Bus Address (BA) register and bits 9 and 8 of CS1 are then gated onto the Unibus in order to access the specified memory location. The C lines (C0 and C1) are encoded for a DATI cycle (data into the RH11, which is the master device). A delay of 200 ns is provided for deskewing on the Unibus. This deskew period allows the address and C lines on the Unibus to settle and also allows time for the memory to decode them.

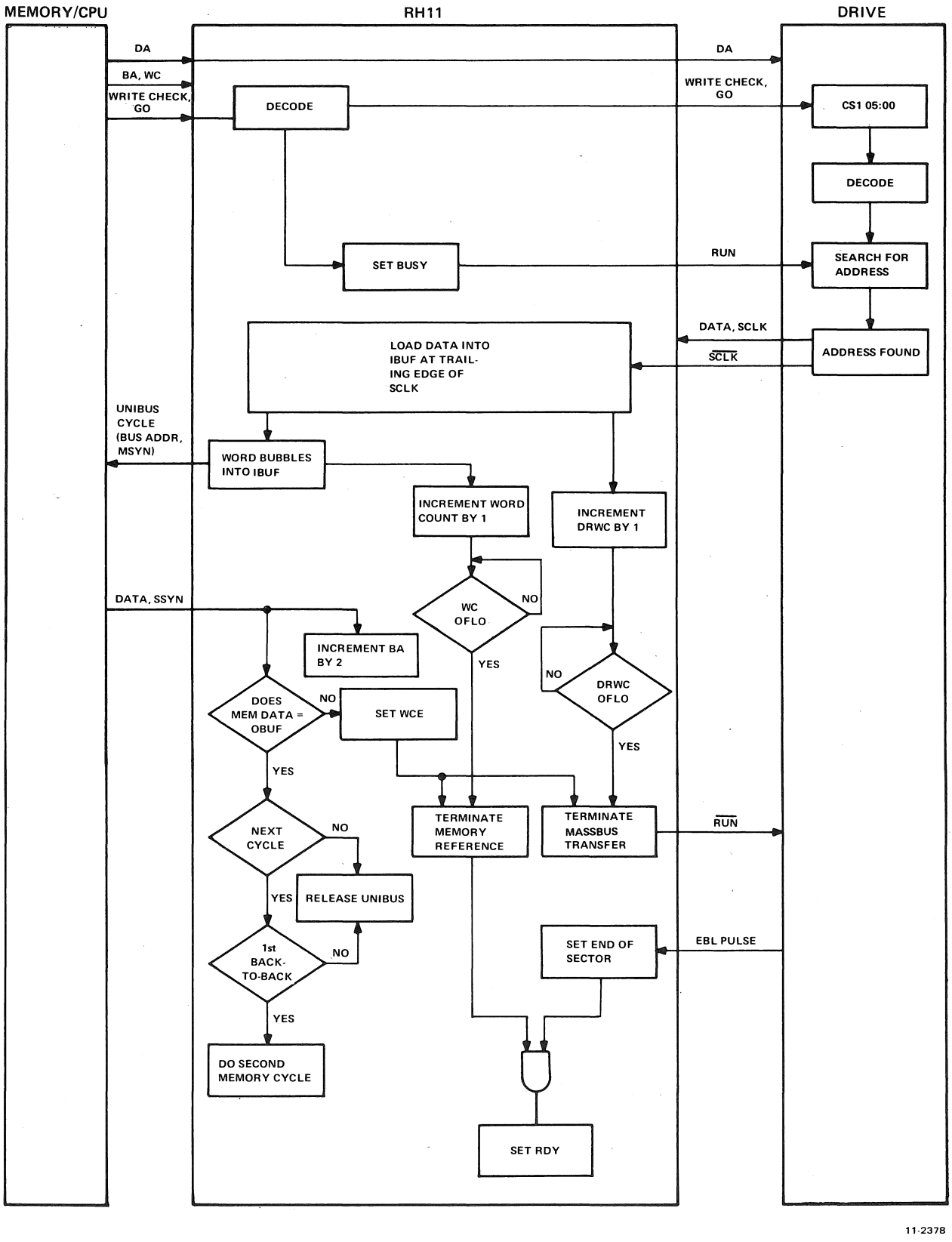


Figure 5-7 Write Check Cycle Interface Diagram

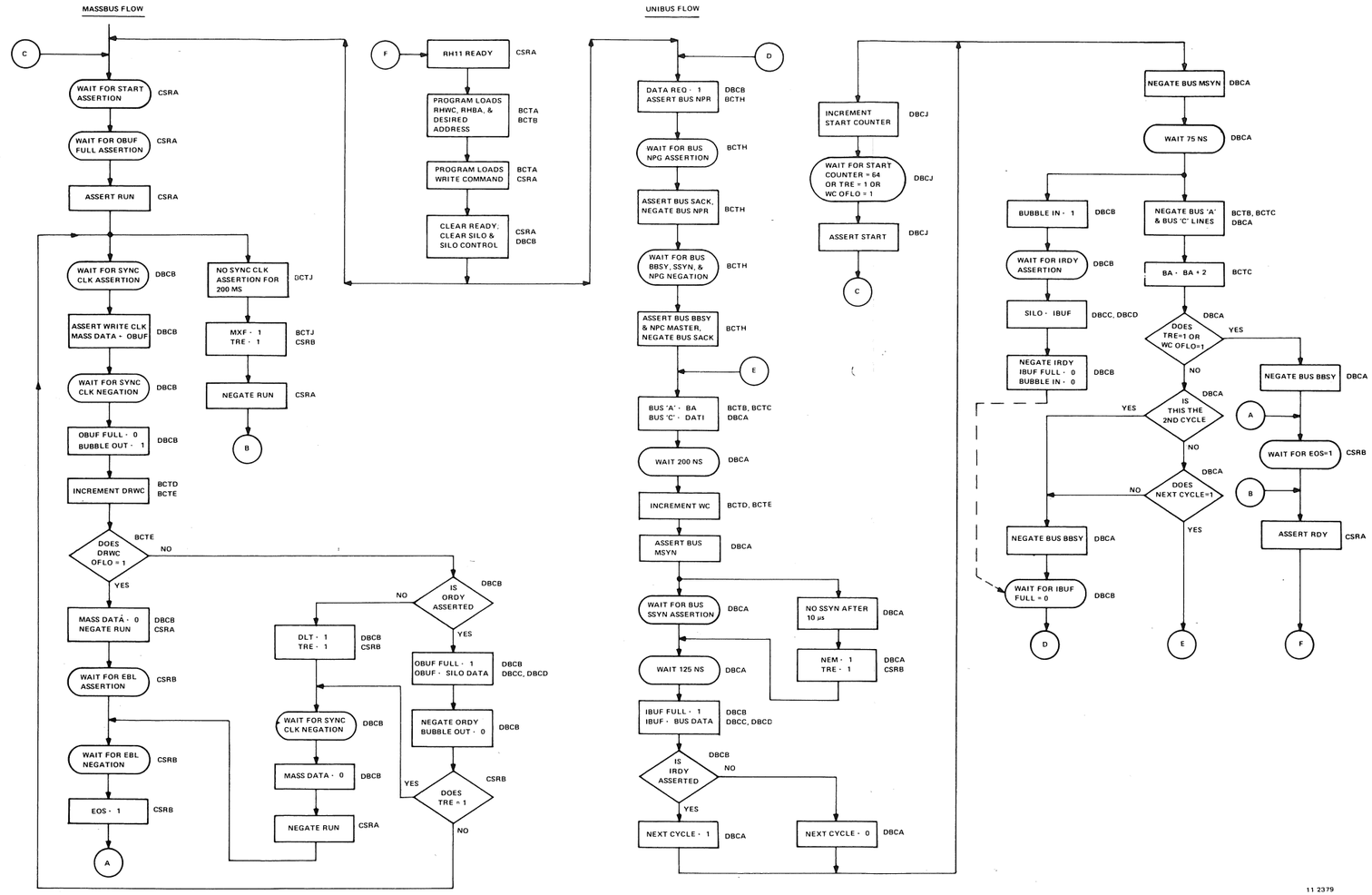


Figure 5-8 Write Command Flow Diagram

After the 200 ns deskew, the RH11 asserts BUS MSYN and increments the Word Count (WC) register. The RH11 then waits for SSYN to be returned from memory with the first data word. If SSYN does not occur within 10 μs of MSYN, the RH11 sets NEM (non-existent memory) error and TRE (transfer error). A 125 ns delay is provided for deskewing data on the Unibus and also provides time to allow the data to be internally gated to IBUF. After 125 ns, a DATA STR (data strobe) signal is generated. The leading edge of DATA STR clocks the data into IBUF and sets IBUF FULL. Also the status of the first cell in the Silo is checked (IRDY) and, if empty, NEXT CYCLE is set to allow back-to-back memory references.

The Unibus flow divides into two paths at this point. The first path checks to see if the START signal should be asserted; the second path provides the signals required to complete the present Unibus cycle and to start the new one. In addition, the second path allows the data from IBUF to be gated into the Silo and bubble up to the top; the second path will be described first, since the first path is used to initiate the Massbus flow when START is present.

MSYN is negated and a 75 ns delay is provided to allow the memory to deselect. This branch of the flow then divides into two simultaneously occurring operations. When BUBBLE IN is set, it triggers the logic to look for Input Ready (IRDY) at the input to the Silo. When IRDY is present, a SHIFT IN pulse is generated which clocks the data from IBUF into the Silo. If a word is in the first cell of the Silo, IRDY is inhibited until the word bubbles up to the next cell. When the Silo accepts the word from IBUF, it clears IRDY and the word begins to bubble up the Silo. When IRDY clears, BUBBLE IN and IBUF FULL clear. When the data reaches OBUF, it is ready to be transferred to the disk. However, the drive is not connected to the RH11 until the START signal is asserted.

This branch of the flow not only inputs data to the Silo but also shows the completion of the Unibus cycle. The Bus Address (BA) register is incremented by 2 to point to the next sequential memory word. The RH11 examines the WC for word counter overflow and also examines TRE. If word count has overflowed or if TRE is present, the second memory cycle is not performed, the address and C lines are removed from the Unibus, and BBSY is negated, which allows another device to become bus master. The RH11 waits for the drive to finish the transfer before going back to the Ready state. If TRE or word count overflow is not present, the status of NEXT CYCLE is checked and, if asserted during the first memory cycle of the back-to-back references, the flow then goes to point E to start the second memory cycle. If NEXT CYCLE is not asserted, or if it already is the second memory reference of a back-to-back cycle, BBSY is negated and the RH11 waits for IBUF FULL to clear before reinitiating an NPR sequence at point D in the flow diagram. The dotted input shown indicates that both parallel branches must complete before the flow can sequence to point D.

The first breakpoint in the flow previously described will now be discussed. It must be understood that this operation is occurring in parallel with what has just been described. DATA STR increments the START counter which counts up to 64. START is asserted when the counter reaches 64, or word count overflow occurs, or TRE sets.

NOTE

If TRE sets, START is asserted and generates the RUN signal which the drive is waiting for. On the first SYNC CLK from the drive, the RH11 sets an ERROR flip-flop. When ERROR is set, the synchronous bus data drivers are disabled, no more words are clocked out of OBUF, and RUN is negated at the next EBL pulse (which occurs at the end of the sector).

5.4.2 Massbus Flow Description

If the conditions causing the START assertion are not met, then this branch of the flow terminates until entered with the next Unibus memory cycle. When the START signal is asserted, the Massbus flow is initiated. With START asserted, the RH11 waits for OBUF FULL and then asserts the RUN line. By waiting for OBUF FULL, the RH11 ensures that a data word is available on the Massbus for the drive to accept.

When the RUN signal is set, the RH11 is connected to the drive and the RH11 now waits for the first SYNC CLK from the drive. If a SYNC CLK does not occur after 200 ms, the MXF (missed transfer) error is set which, in turn, sets TRE. This action clears the RUN line and returns the RH11 to the Ready state. When the SYNC CLK signal is received by the RH11, it is returned to the drive as a WRITE CLK signal. The data from OBUF has been gated on the synchronous bus data lines. On the trailing edge of SYNC CLK, OBUF FULL is cleared, BUBBLE OUT is set, and the Drive Word Count (DRWC) register is incremented. The DRWC register is checked for overflow. If there is overflow, the synchronous bus data drives are disabled which effectively writes 0s in the remaining word slots in the sector and the RUN signal is negated. The RH11 then waits for EBL. On the trailing edge of EBL, the RH11 sets the EOS (end of sector) and returns to the Ready state.

If drive word count overflow did not occur, the RH11 examines ORDY (output ready) at the trailing edge of SYNC CLK. This is done to ensure that a word is in OBUF in time for the next transfer. If ORDY is not asserted, a DLT (data late) error is raised which, in turn, causes TRE. The synchronous bus data drivers are disabled which causes 0s to be written in the remaining words in the sector. The RH11 then waits for the EBL signal from the drive, clears the RUN line, asserts the EOS signal, and returns to the Ready state.

If ORDY is asserted, the Silo data is clocked into OBUF and OBUF FULL is set. When the data word is gated from the Silo to OBUF, ORDY is cleared and BUBBLE OUT is cleared to prevent the next word in the Silo from being clocked into OBUF. When the next data word bubbles up to the top cell, ORDY is again asserted. If TRE is not present, the Massbus flow loops back and the RH11 waits for the next SYNC CLK from the drive, indicating the next word is to be transferred.

If TRE was set, the RH11 waits for the SYNC CLK negation before synchronizing the error condition. At this point the Massbus data drivers are disabled to cause a zero-fill in the rest of the sector. In addition, RUN is negated. At the trailing edge of EBL, End of Sector (EOS) is set and the RH11 returns to the Ready state.

5.5 READ FLOW DIAGRAM DESCRIPTION

Figure 5-9 is a detailed flow diagram of the read data transfer. Initially, the RH11 is in the Ready state and the program specifies the bus address, desired address, word count, and selected unit (specified in CS2). A read command is loaded in bits 05 through 01 of CS1 and the GO bit is set in bit 00 of CS1. The Ready state in the RH11 is then cleared, the RUN line is asserted which logically connects the RH11 to the drive, and the Silo and Silo control are initialized. At this point the flow divides into two asynchronous branches – the Massbus flow and the Unibus flow. The Massbus flow is described first because it is necessary to provide the first data word (ORDY assertion) to begin the Unibus flow.

5.5.1 Massbus Flow

The RH11 sits in a Wait state waiting to receive SYNC CLK signals from the drive.

NOTE

If there is no SYNC CLK after 200 ms, MXF error and TRE are set. The RUN line is cleared and the RH11 returns to the Ready state.

SYNC CLK is issued when the drive has found the address which matches the track and sector address set in the desired address register. The leading edge of SYNC CLK informs the RH11 that the drive has asserted a data word on the Massbus. On the trailing edge of SYNC CLK, the Drive Word Count (DRWC) register is incremented which indicates the number of words received from the synchronous bus. Also, the RH11 checks IBUF FULL.

If IBUF FULL is asserted indicating a word in IBUF, a DLT (data late) error is posted since there is no place to store the incoming data word. The RH11 then clears RUN. On the trailing edge of EBL, the EOS (End of Sector) is set and returns the RH11 to the Ready state.

If IBUF is not full, the data word from the Massbus is clocked into IBUF and the IBUF FULL flag is asserted. After a 150 ns delay (to allow the data in IBUF to be available to the Silo) the BUBBLE IN flip-flop is set. If Input Ready (IRDY) is not asserted (indicating the presence of a data word in the bottom cell of the Silo), the flow waits for IRDY to be asserted. As soon as IRDY is asserted, the BUBBLE IN flip-flop enables the data word to be clocked from IBUF into the Silo. When IRDY is negated, the IBUF FULL flag and BUBBLE IN are cleared, allowing a new word to be loaded into IBUF.

Each new data word from the drive is accompanied by SYNC CLK and on the trailing edge of each SYNC CLK, the drive word count is incremented indicating receipt of another word. The Drive Word Count register is loaded in parallel with the Word Count register. Both registers contain the 2's complement of the number of words to be transferred. DRWC register is now checked for overflow. If drive word count has not overflowed and there is no TRE, the flow loops back to point C and waits for the next SYNC CLK and the next data word. With TRE set or drive word count overflow, the RUN line is cleared. The RH11 waits for EBL, sets EOS on the trailing edge of EBL, and returns to the Ready state when the Unibus flow is completed.

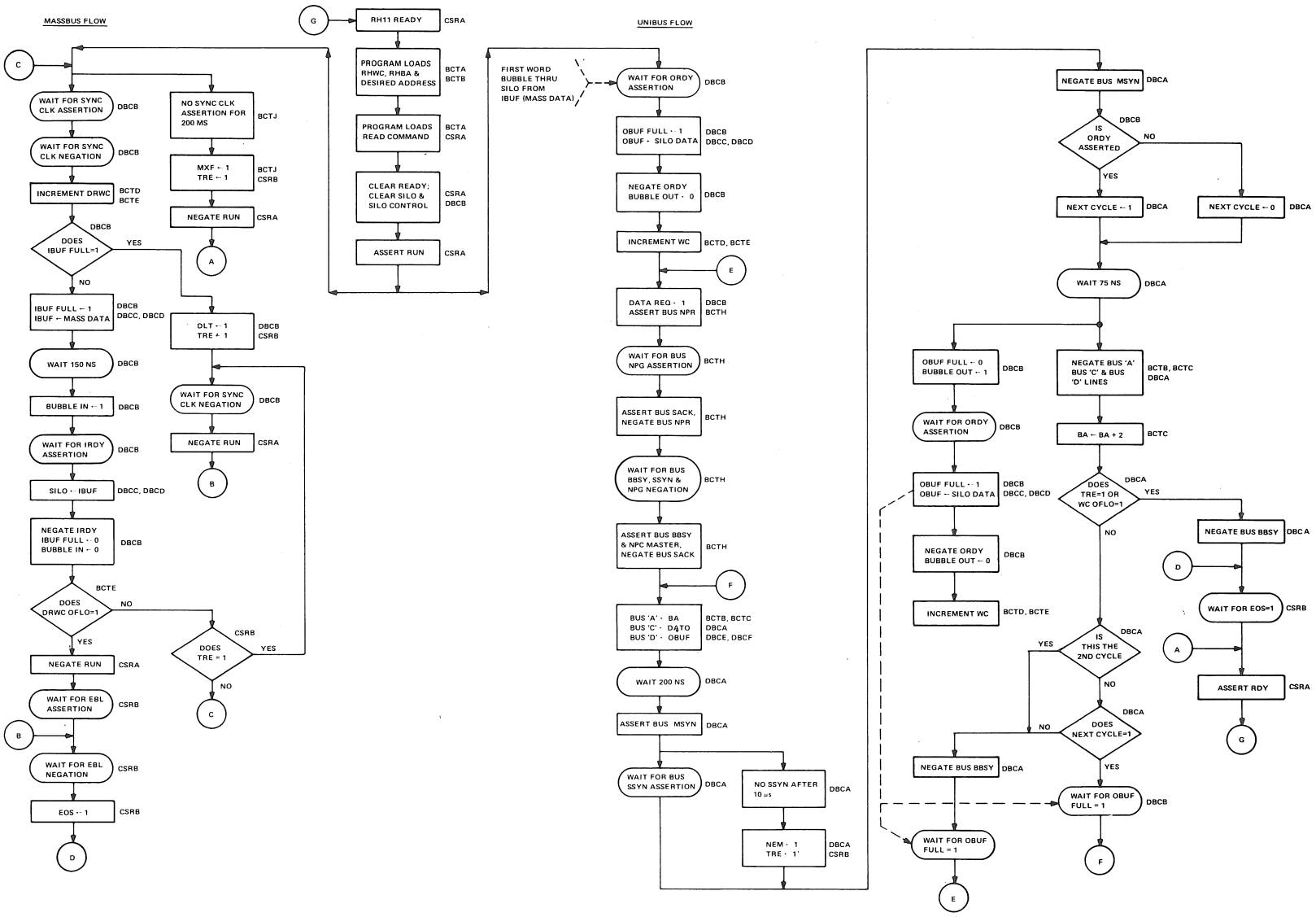


Figure 5-9 Read Command Flow Diagram

5.5.2 Unibus Flow

The Unibus flow is waiting for the first data word to be clocked to the top cell of the Silo. When this occurs, ORDY (output ready) is asserted. Since this is the first word, OBUF is not full and the data word is gated into OBUF, the OBUF FULL flag is asserted, BUBBLE OUT is cleared (previously initialized set), and ORDY is cleared. The word count is incremented. The condition of OBUF FULL being asserted causes DATA REQ to set, which enables the RH11 to assert BUS NPR. The RH11 waits for NPG (non-processor grant); upon receipt of NPG, the RH11 is the next device to gain control of the bus and asserts BUS SACK acknowledging receipt of NPG. BUS NPR is also cleared. The RH11 is waiting for BBSY and SSYN from the previous Unibus cycle to be removed. When this occurs, SACK is cleared and the RH11 asserts BBSY and becomes bus master.

The RH11 then asserts an NPC master signal, gates the bus address to the Unibus address lines, encodes the control lines (C0 and C1) for a DATO cycle, and gates the data from OBUF to the Unibus data lines. The RH11 now waits 200 ns to deskew the address, control, and data lines before BUS MSYN is asserted.

The RH11 asserts BUS MSYN and waits for memory to respond with SSYN. If the memory location specified by the bus address does not respond within 10 μs, the RH11 sets a NEM (non-existent memory) error, which causes TRE to set.

SSYN indicates that the memory has accepted the data word. At this time, MSYN is negated and the status of the Silo is checked (ORDY) to determine if another memory reference can be performed. If ORDY is asserted, NEXT CYCLE is set.

The RH11 then waits 75 ns after MSYN is negated before the address is removed or changed. The 75 ns deskew ensures that the memory is properly deselected. The flow now divides into two branches. The first branch finishes the Unibus cycle while the second branch allows data to bubble out of the Silo into the OBUF register. The first branch will now be described.

If a transfer error or word count overflow occurs, the address, control lines, and data are removed from the Unibus, the bus address is incremented by 2, BBSY is cleared, and the RH11 waits for the EOS produced by the trailing edge of EBL from the Massbus flow. If EOS is present with TRE or word count overflow, the RH11 goes to the Ready state. Both the Massbus and Unibus loops must complete before the RH11 goes to the Ready state. It is at this point that the two asynchronous loops merge in order to set Ready.

If there is no transfer error or word count overflow, the bus address is incremented, and if this is the second memory cycle or NEXT CYCLE is not set, BBSY is cleared. At this point, the flow stops and waits for OBUF FULL to set before looping back to point E and reinitiating an NPR cycle.

If the bus cycle was not the second one and the NEXT CYCLE flop is set, the RH11 waits for the next data word (OBUF FULL asserted) before starting the second back-to-back cycle. At this point, the flow loops back to point F.

The second branch, which begins after the 75 ns delay, allows data to be bubbled out of the Silo and into OBUF register. This is shown by OBUF FULL being cleared and BUBBLE OUT set to allow the data word in the top cell of the Silo to be transferred to OBUF. When ORDY is asserted, the Silo data is transferred to OBUF and OBUF FULL is set. The dotted lines indicate that this operation (OBUF FULL setting) allows the first branch to continue. When ORDY is negated, the BUBBLE OUT flip-flop is cleared and the WC register is incremented. The flow then ends until the next memory cycle causes this branch to be reentered.

5.6 WRITE CHECK FLOW DIAGRAM DESCRIPTION

Figure 5-10 is a detailed flow diagram of the write-check operation. This operation reads data from the device via the Massbus and stores the data in the Silo. When the data propagates through the Silo to OBUF, a Unibus cycle is performed to read the corresponding word in memory. This word is compared with the word from the drive which has propagated into OBUF. The comparison is accomplished by a series of Exclusive-OR gates. If the two words are equal (indicating no transmission errors), the OBUF FULL flag is cleared, and successive data words are compared until an error or until all words have been compared. If the two are not equal, the WCE (write-check error) bit is set which sets TRE, the word is frozen in OBUF, and the OBUF FULL flag remains asserted. Either the word read from the device and stored in OBUF or the word read from the Unibus could be in error. Since it is more difficult to access the word from the drive, this word is held in OBUF in the event of a WCE.

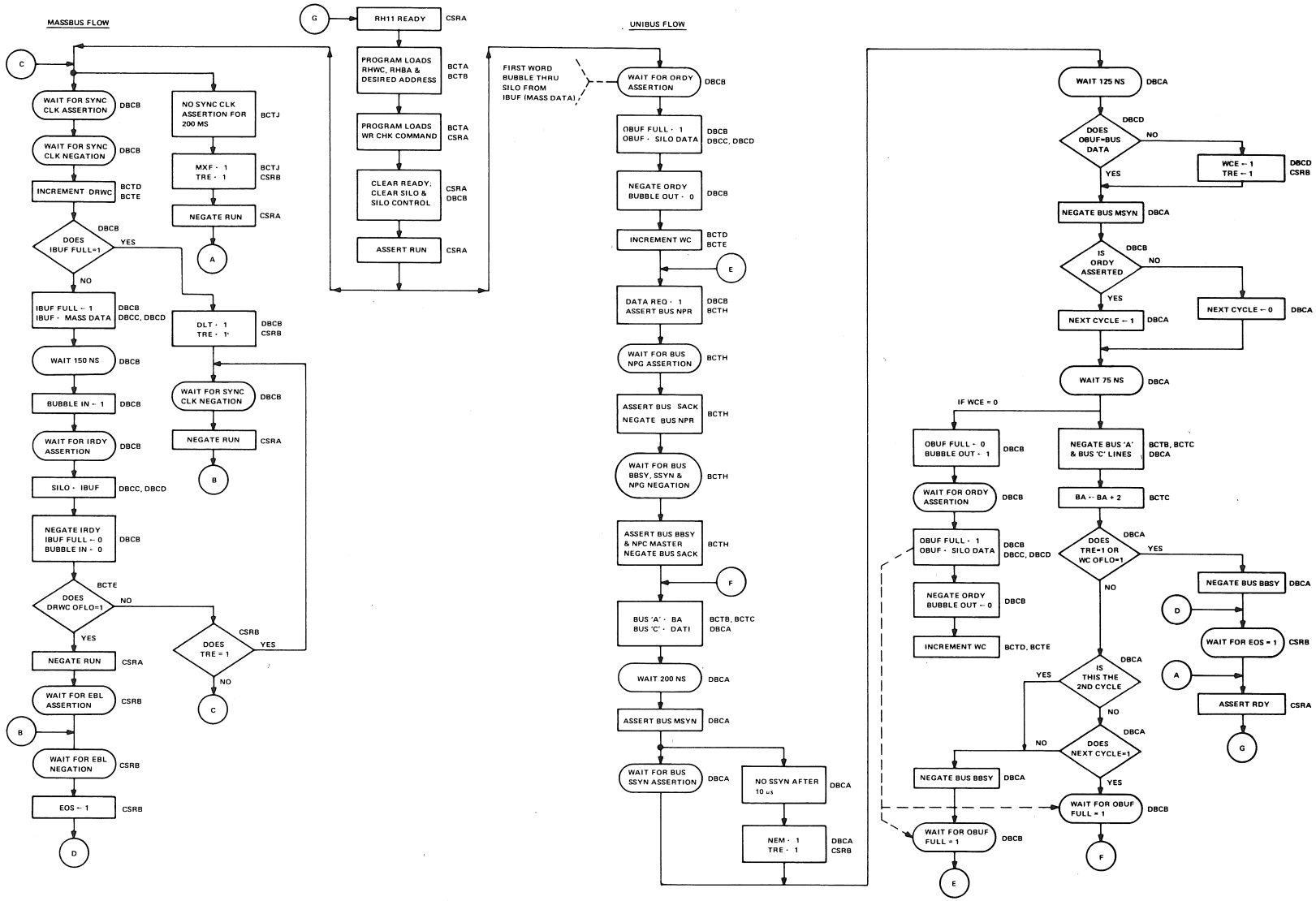


Figure 5-10 Write Check Command Flow Diagram

5.6.1 Massbus Flow Description

The description of the Massbus flow for the write-check operation is identical to the read operation (Paragraph 5.4.1).

5.6.2 Unibus Flow Description

The description of the Unibus flow for the write-check operation is similar to that for the read operation (Paragraph 5.5.2) with the following exceptions:

a. A DATI Unibus operation is performed to receive data from the specified memory location.

b. Upon receipt of SSYN from memory, the RH11 generates a 125 ns delay to deskew the data on the Unibus and to allow the data to propagate through the Exclusive-OR gates so that it may be compared with OBUF, and

c. If the data from memory and the data from the drive (stored in OBUF) do not compare, the WCE is posted and the parallel branch of the flow which transfers data from the Silo to OBUF is prevented from happening.

CHAPTER 6
DETAILED LOGIC DESCRIPTION

6.1 GENERAL

This chapter provides a detailed description of the RH11 logic diagrams. These descriptions should be used in conjunction with the flow diagrams in Chapter 5 to provide both an overall and detailed understanding of the RH11. The diagrams described in this chapter are tabulated in Table 6-1.

The M7295 module is designated BCT and is used for bus control; the M7296 module is designated CSR and is used for control and status; the M7294 module is designated DBC and is used for data path routing; and the M7297 module is designated PAC and is used for parity generation and checking.

Detailed timing diagrams (Figures 6-1, 6-2, 6-3, and 6-4) are also included in this chapter and may be used in conjunction with the detailed logic descriptions to show timing relationships between signals. Figure 6-1 is the Unibus timing diagram for a write operation; Figure 6-2 is the Unibus timing diagram for a read or write-check operation; Figure 6-3 is the Massbus timing diagram for a write operation; and Figure 6-4 is the Massbus timing diagram for a read or write-check operation.

6.2 BCTA LOGIC DIAGRAM

This diagram contains the register selection logic used by the program to select local RH11 registers or remote registers in the associated drive. The register address is supplied to 18 Unibus receivers (8838) via the Unibus. Bits 17 through 13 of the register address are asserted designating the I/O area. Bits 12 through 5 are fed to a series of jumper Exclusive-OR gates whose outputs are collector-ORed. If any of the output of these gates goes low, it forces the output line low as in the case where the Unibus address does not match the selected address of the RH11. The addresses to which the RH11 responds can be relocated by modifying the jumpers. If a jumper is left in, it represents a logic 0 and if it is cut, it represents a logic 1. The register address bits are asserted low on the Unibus. For example, address bit 12 is low at the input to the 8838 Unibus receiver. The output of this gate goes high. This is compared to the jumper intact which is low. The output of the Exclusive-OR gate, after inversion, is low and this drives the collector-ORed output line low to inhibit DEV SEL. On the other hand, if the jumper is out, (representing a 1), the Exclusive-OR gate compares two high inputs yielding a high output which enables the DEV SEL signal for that bit.

Bits 4 through 1 of the Unibus address are supplied to a 32-cell read only memory (ROM). A low logic level is supplied to the fifth address input to the ROM via the jumper selection at E3 and thereby allows 4 address bits to specify one of 16 cells in the ROM. The contents of the specified cell represents a specific pattern on the eight output signals (M0 through M7) of the ROM.

These outputs are used to provide the appropriate register signals. Each cell represents a different register address. If more than 16 registers are required for a particular RH11 system, the jumpers at E3 shown below the address jumpers are selected to feed bit 5 of the Unibus address to the ROM. As a result, one of 32 cells in the ROM can be specified, and Unibus address bit 5 is not compared at the Exclusive-OR gates which enable a DEV SEL signal.

Table 6-1
Listing of RH11 Logic Diagrams

Logic Print	Functions
BCTA	Register Selection
BCTB	Unibus A Address Drivers; SSYN; DEMAND
BCTC	Bus Address Register
BCTD	Word Count Register (07:00)
BCTE	Word Count Register (15:08)
BCTF	Interrupt Control
BCTH	NPR Control
BCTJ	MXF; Data Out MPX; MB INIT
BCTK	PROM Truth Table
CSRA	Control and Status Register CS1
CSRB	Control and Status Register CS2 and Error Status
DBCA	NPR Control Logic
DBCB	Silo Timing Control
DBCC	Silo Data Path (11:00)
DBCD	Silo Data Path (17:12)
DBCE	Unibus B Data Transceivers
DBCF	Unibus A Data Transceivers
DBCH	Unibus Parity Control and Data Out MPXs
DBCJ	Start Control and Data Out MPXs
PACA	Parity Control (Massbus Parity Detection and Generation)
MBSA	Massbus Transceiver (Massbus Cable A)
MBSB	Massbus Transceiver (Massbus Cable B)
MBSC	Massbus Transceiver (Massbus Cable C)
BUSA	Unibus A Cable Diagram
BUSB	Unibus B Cable Diagram
M9300	Unibus B Terminator
G727	Grant Continuity Module

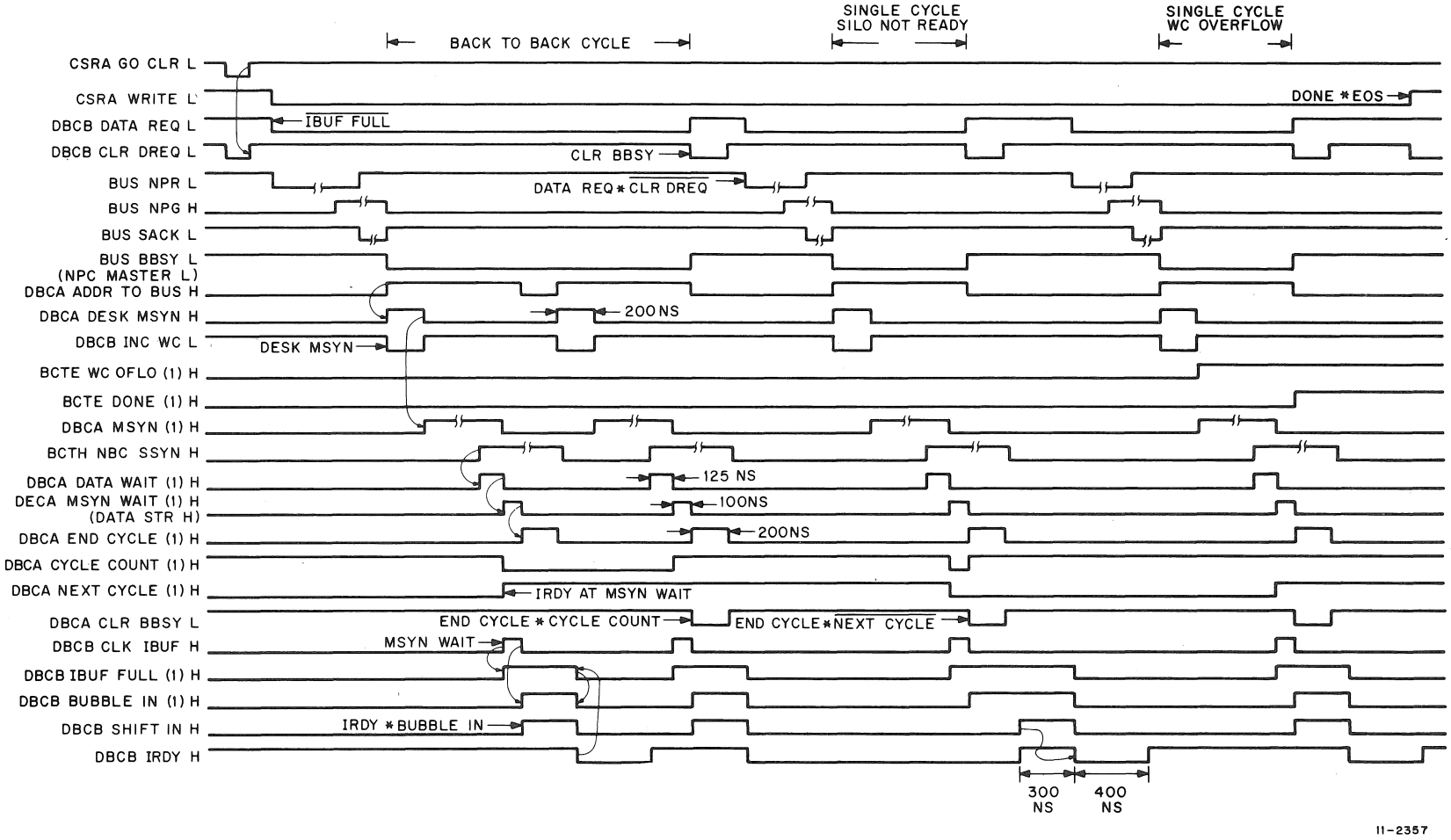


Figure 6-1 Write UNIBUS Timing Diagram

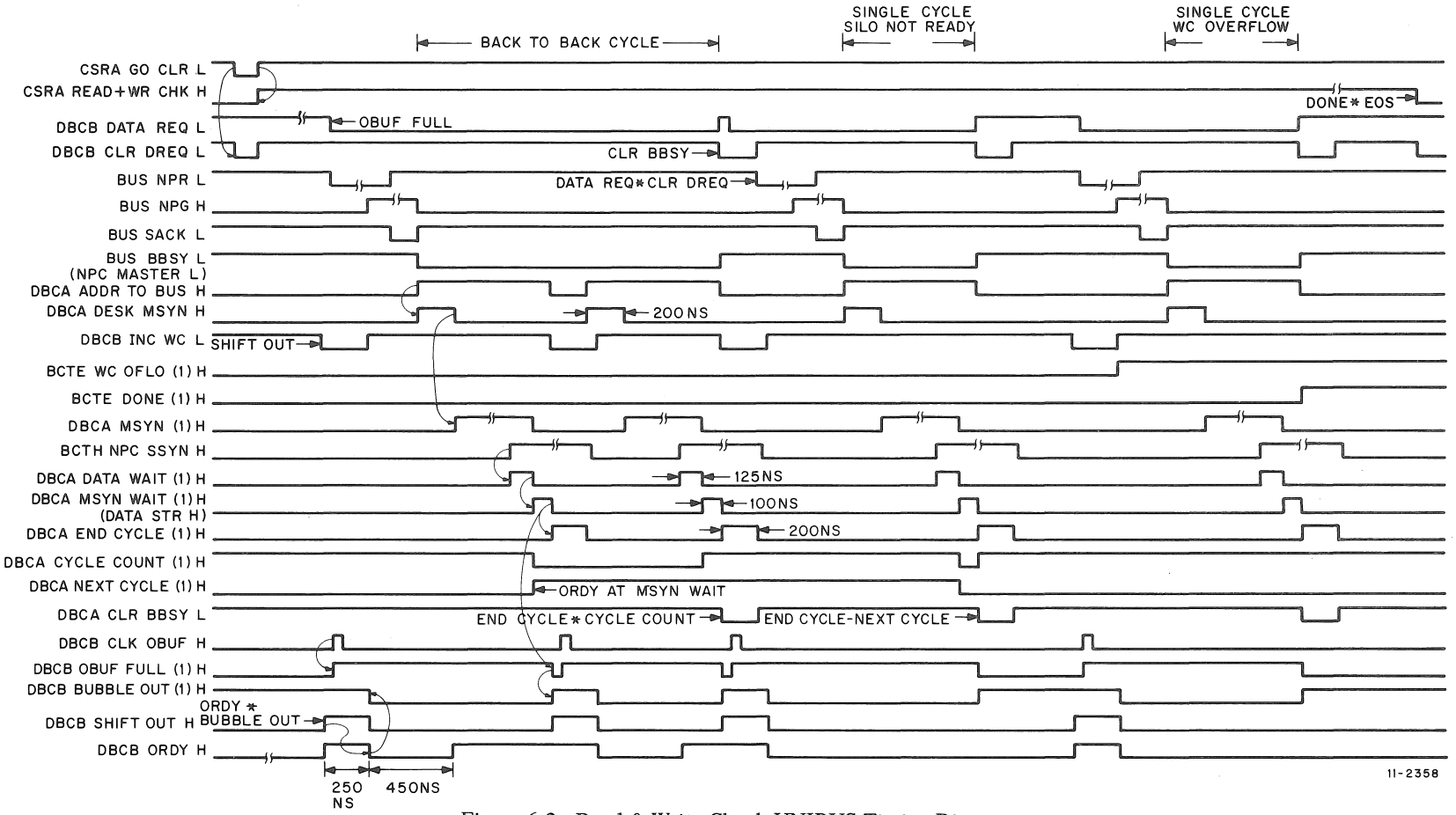


Figure 6-2 Read & Write Check UNIBUS Timing Diagram

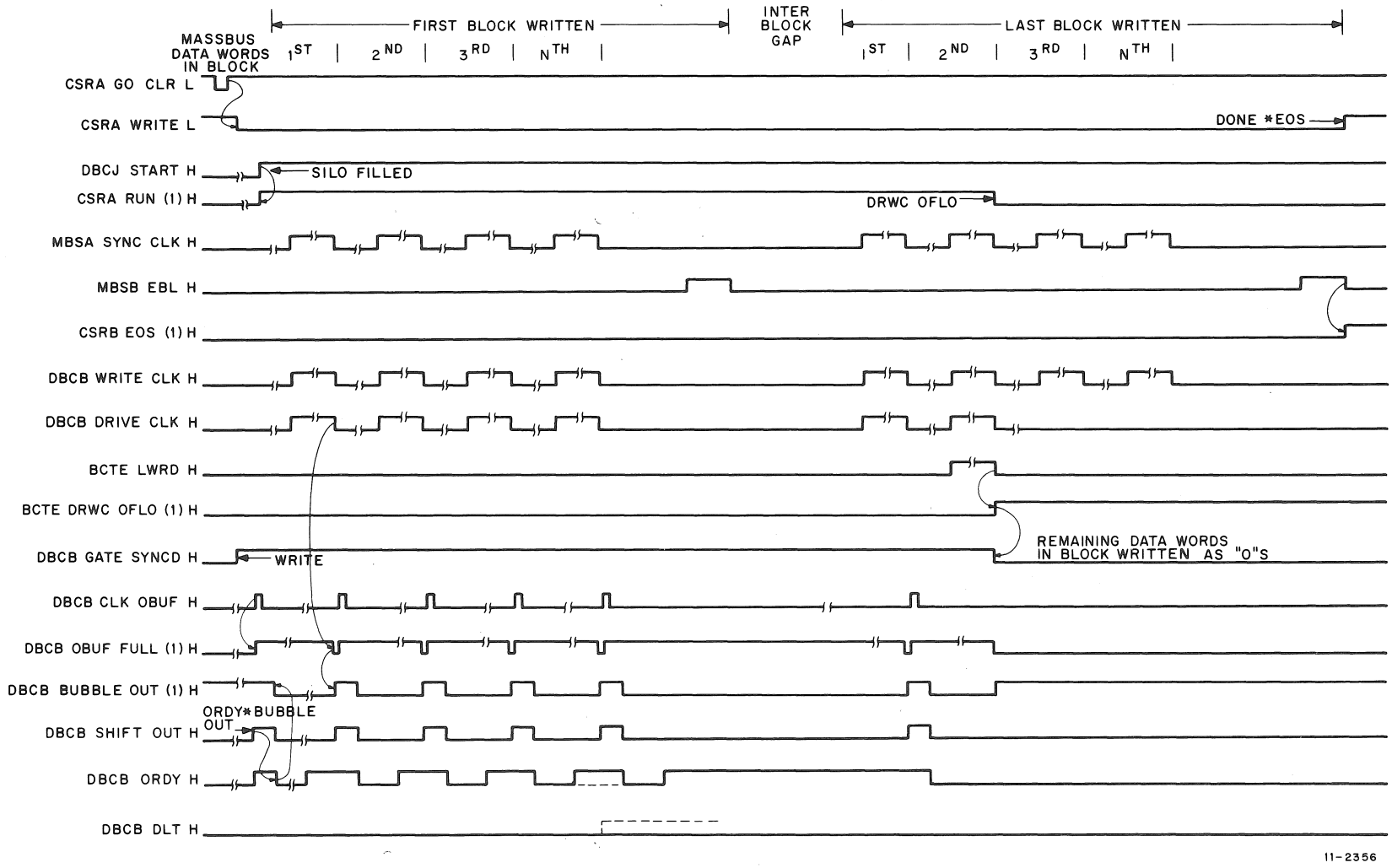


Figure 6-3 Write MASSBUS Timing Diagram

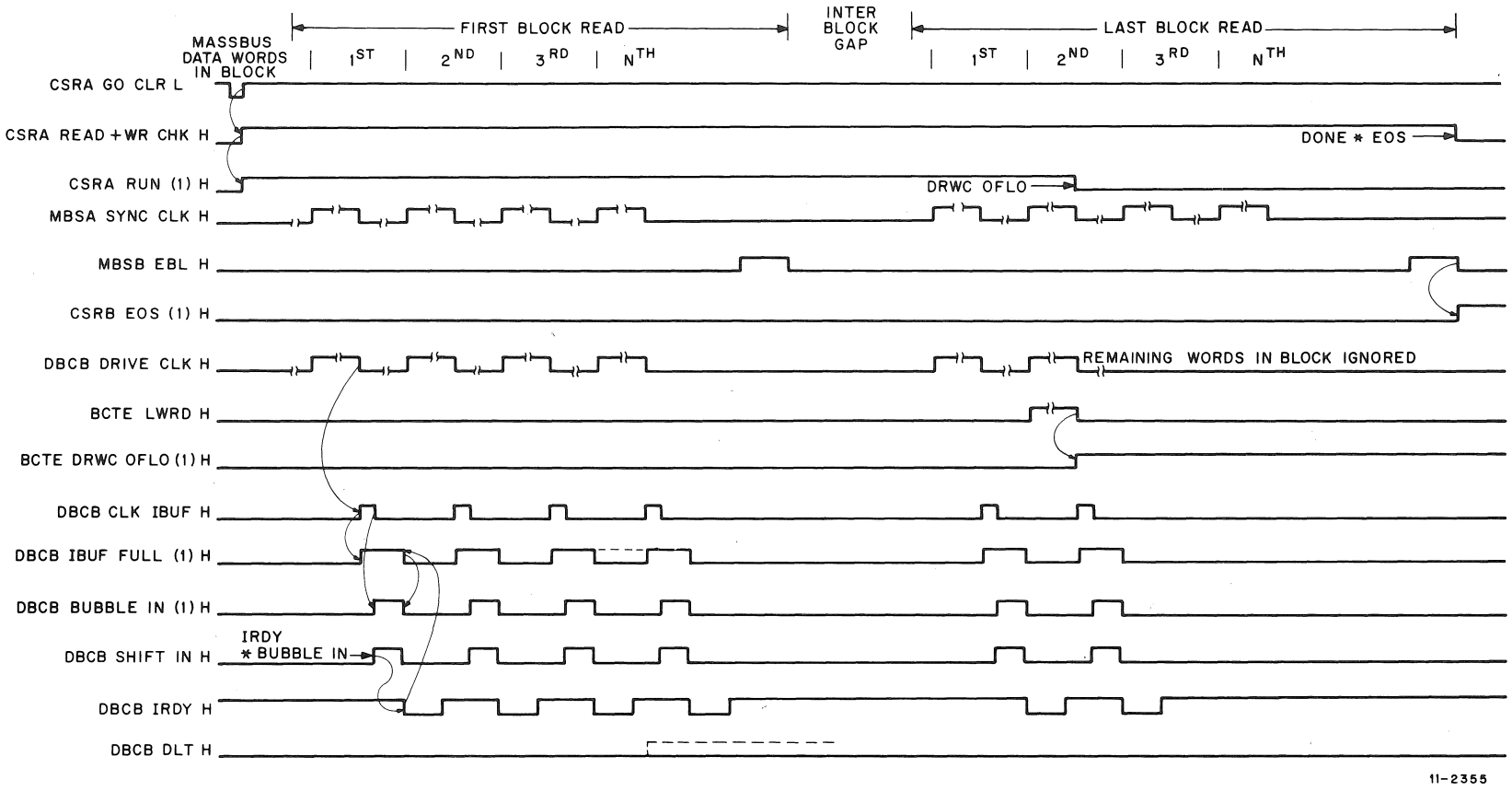


Figure 6-4 Read & Write Check MASSBUS Timing Diagram

In addition, the four most significant address bits which are applied to the ROM are compared against a jumper setting which define the exact number of registers used in the system. Each of these jumpers is weighted by the value assigned to it. If a jumper is removed, the RH11 will respond to the number of registers designated by the removed jumper. This number is added to the base address set by the address select jumpers on the Exclusive-OR gates. For example, if 12 registers are used in the system, the jumpers weighted 8 and 4 are removed. A Unibus address between the base address and the base address +11 words would be a valid register address. A Unibus address equal to or greater than the base address +12 words will cause the Logal REG output of the comparator to go unasserted, thus preventing the SSYN response.

NOTE

MSYN is delayed for 150 ns by the processor to allow the jumper Exclusive-OR gate decoder sufficient time to decode the address of the selected register. The MSYN signal then keys the DEV SEL signal which starts the register strobing sequence.

6.2.1 Local/Remote Register Selection

In addition to encoding the register address, the ROM asserts the LOC/REM H signal if a local register is being accessed. The Massbus handshaking sequence necessary to access a register located in a drive is inhibited in this case. If a remote register is being addressed, the LOC/REM H signal is not asserted (the Massbus handshaking sequence is enabled) and the DEMAND signal is initiated.

NOTE

The CS1 register is shared by the RH11 control and the associated drive. The LOCAL/REM H signal is not asserted to address this register. If LOC/REM H is asserted, the Massbus handshaking sequence is inhibited. This would prevent access to the portion of the CS1 register located in the drive.

6.2.2 RSEL Signals

The RSEL 04 through RSEL 00 signals from the output of the ROM are supplied to the Massbus which will be decoded in the drive to select a specific register. In addition, RSEL 00 and RSEL 01 are supplied to the lower of two 7442 BCD-to-decimal decoders and are used when the LOCAL/REM signal is asserted. The lower decoder decodes the CS2, DB, and BA registers and whether an input (from processor to RH11) or output (from RH11 to processor) function is to occur.

6.2.3 Decoder Inputs

Inputs D0, D1, and D2 to the decoder specify one of 8 outputs from 0 through 7 (outputs 3 and 7 are not used). RSEL 00 and RSEL 01 are applied to inputs D0 and D1 of the decoder, respectively, and specify one of the three above mentioned registers. BUSA C1 is applied to input D2 of the decoder and specifies an input or output function. When BUSA C1 L is asserted, the D2 input to the decoder is low enabling the register codes on outputs 0, 1, and 2. This indicates a DATO or DATOB where the data is transferred from the master (processor) to the slave (RH11). The register signal names incorporate the word "IN" denoting a 'write register' operation. When BUSA C1 L is not asserted, the D2 input to the decoder is high enabling the register codes on outputs 5, 6, and 7. This indicates a DATI or DATIP where the data is transferred from the slave (RH11) to the master (processor). The signal names are designated with the word "OUT" denoting a 'read register' operation. Input D3 is asserted low if the LOCAL REM H signal indicates a local register is addressed and DEV SEL H is asserted.

6.2.4 Decoder Outputs

With input D3 low, outputs 0 through 7 are enabled. If input D3 is not asserted, the outputs from 0 through 7 are inhibited and the decoder outputs are switched to 8 and 9 which are not used. Since the RSEL 04 through RSEL 00 signals are not used for selecting a drive register when the LOC/REM H signal is asserted, it is possible to redefine the two bottom bits of the ROM (RSEL 00 and RSEL 01) to be used as inputs to the decoder.

The upper decoder is similar to the lower one with a few exceptions noted below.

- Input D2 operates exactly the same as described for the lower decoder.
- ROM outputs M6 and M7 are used to decode the registers (WC, AS, CS1) associated with the upper decoder and are applied to inputs D0 and D1, respectively.
- Input D3 is enabled when DEV SEL L is asserted. LOC/REM H is not required since the M6 and M7 outputs of the ROM are not dual defined and may be used anytime.

6.2.5 Word or Byte Addressing

The logic network with the A0, C0, and C1 inputs determines whether word or byte addressing is required and whether an input or output function is occurring. The network implements the chart shown below.

C1	C0		
0	0	DATI	
0	1	DATIP	
1	0	DATO	
1	1	DATOB	if A00 = 0, low byte is specified. if A00 = 1, high byte is specified.

6.2.6 Control Lines

The C0 and C1 lines from the Unibus generate the DIR TRANS (direction of transfer) signal. When this signal is asserted, the direction of data transfer is from the RH11 to the drive register via the Massbus. When the signal is not asserted, the direction of data transfer is from the drive register to the RH11, and then to the Unibus to be made available to the program. The DIR TRANS signal is used to form the CTOD signal on the Massbus.

6.2.7 ODD BYTE L Signal

The ODD BYTE L signal is asserted when performing a DATOB to the high byte and is used to generate DIS DEM (disable demand). This is done to prevent the low (even) byte of the CS1 register from changing to the upper byte when the program is doing a byte operation (this is necessary since the Massbus does not implement byte operations and writeable bits in the low byte of CS1 are located in the drive).

6.2.8 Device Select (DEV SEL) Logic

The upper portion of BCTA shows the DEV SEL logic and the deskew demand logic. Bits 17 through 5 of the Unibus A address are used to generate DEV SEL L when MSYN occurs. MSYN is delayed from the address 150 ns to allow the address to be properly decoded by the jumper Exclusive-OR gates.

The negative-going edge of the DEV SEL L signal triggers one-shot multivibrator E63. The external components associated with this multivibrator are chosen to provide an 85 ns delay. Consequently, the negative-going edge of DEV SEL causes an 85 ns negative-going pulse at the 0 output of the one-shot. The positive-going trailing edge of this one-shot triggers a second one-shot with external components chosen for a delay of 135 ns. A positive-going pulse of 135 ns from the 1 output and a negative-going pulse of 135 ns from the 0 output are available.

6.2.9 Deskew Demand (DESK DEM)

The output of the second one-shot is designated DESK DEM (1) H or DESK DEM (0) H and provides a total delay of 220 ns before DEMAND is issued to the Massbus (see logic diagram BCTB).

6.2.10 Register Strobe (REG STR)

A REG STR signal is generated 85 ns after MSYN and is used for clocking the local registers.

6.2.11 Control Out (CTRL OUT) Signal

The CTRL OUT L signal is used when reading a remote register in the drive. CTRL OUT L is generated when the LOC/REM H signal is not asserted (remote mode), DEV SEL is asserted, and the BUSA C1 L signal is not asserted. This signal switches the multiplexer on logic diagram DBCH to gate the Massbus asynchronous data to the Unibus data lines making the register information available to the program.

6.2.12 Gate Control (GATE CNTL) Signal

The GATE CNTL H signal is used when writing into a remote register in the drive. GATE CNTL L is generated when DIR TRANS and DEV SEL signals are asserted and gate the Unibus data signals to the Massbus control lines.

6.3 LOGIC DIAGRAM BCTB

This sheet contains the DEMAND, SSYN, and NED logic and also contains the Unibus A address drivers used to gate the bus address to the Unibus.

6.3.1 Deskew Demand (DESK DEM) Logic

The DESK DEM (0) H signal from sheet BCTA is delayed 220 ns from MSYN and sets the SET DEM flip-flop. When set, this flip-flop causes DEMAND to be set, provided the TRANS (transfer) signal is not present on the Massbus. The TRANS signal is generated in the drive when the drive is ready to accept data or has data for transfer to the RH11.

6.3.2 Response from Drive

TRANS generates RESP L (response), indicating that the drive has responded to the controller. If no response occurs within 1.5 μs, a non-existent drive has been accessed. In this case, the NED (non-existent drive) flip-flop on BCTB is set.

6.3.3 SSYN Logic

The SSYN logic is used to determine when SSYN is sent to the Unibus. Each of the various methods of setting SSYN is described below.

Setting SSYN-Writing Remote Register (register electrically located in the drive) – When the program writes a remote register via the RH11, the unit select bits, the RSEL 04 through 00 signals, and the data are gated onto the Massbus. The unit select bits select the specified unit and the RSEL 04 through 00 signals select the appropriate register in that unit. If the RH11 is writing into a remote register, DIR TRANS H is asserted. After a 220 ns deskew period, the RH11 asserts DEMAND on the Massbus. When the drive sees DEMAND and recognizes its own unit select code and register address, it takes the data and issues TRANS which generates RESP in the RH11. Consequently, since DEMAND (1) H is asserted (accessing a remote register), DIR TRANS H is asserted (controller-to-drive transfer), and RESP L is asserted, gate E83 at zone D-6 generates SET SSYN L which is applied to the direct set input of the SSYN flip-flop.

NOTE

The Attention Summary register is a 1-bit pseudo register. When this register is accessed, more than one drive may respond. Therefore, the TRANS signal cannot be used to indicate the availability of data. In order to ensure that all drives have their respective Attention Summary bits loaded, a 1.5 μs delay is incorporated before the setting of SSYN.

Setting SSYN-Reading Remote Register – If the RH11 is reading a remote register (accepting data from the drive), the drive after recognizing its unit select code, register address, direction of transfer, and DEMAND, issues TRANS which generates RESP L in the RH11. Since DIR TRANS H is unasserted at this time (drive-to-controller transfer), a 200 ns one-shot multivibrator (E93) is fired. The external components are selected to provide the 200 ns pulse. This delay is designed to allow the data from the drive to propagate to the RH11 and onto the Unibus before SSYN is set. In other words, SSYN cannot be asserted on the Unibus until the data from the drive has been transferred to the Unibus and has stabilized. Consequently, when the one-shot fires, the 0 output goes low for 200 ns forcing the clock input to the SSYN flip-flop low for this period. At the end of 200 ns, the positive-going trailing edge of the 200 ns pulse sets SSYN which is asserted on the Unibus.

Setting SSYN-Access Local Registers – SSYN is set during the access of local registers as a result of REG STR H and DIS DEM H being asserted. REG STR H is generated 85 ns after MSYN on logic diagram BCTA and is used as a strobe input to the local register being accessed. Signal DIS DEM H indicates that the Massbus cycle is inhibited and a local register is being accessed. At the trailing edge of the REG STR signal, SSYN is set indicating that data has been accepted or is present on the Unibus when writing or reading a local register.

One-Shot Multivibrator (1.5 μs) – The 1.5 μs one-shot multivibrator (E93) shown in zone C-6 serves two purposes. First, it checks whether a non-existent drive has been accessed. The one-shot is fired when DEMAND is asserted. When the drive responds with TRANS which generates RESP L, the one-shot is cleared. As previously described, RESP L either generates SET SSYN L or DESK DATA L, depending on the state of the DIR TRANS H signal. Either of these signals direct clears the 1.5 μs one-shot, causing a positive-going edge at the output. This edge tries to clock the NED flip-flop set, but the same signal that direct clears the 1.5 μs one-shot also direct clears the NED flip-flop. When the RH11 issues DEMAND and receives TRANS from the drive, the 1.5 μs one-shot is cleared. In addition, the NED flip-flop is inhibited from setting. If the drive did not respond, the SET SSYN L and DESK DATA L signals are both inhibited from clearing the one-shot, causing the one-shot to time out. At this time, the positive-going edge clocks the SSYN flip-flop set. The NED flip-flop also sets if the register being accessed is not the Attention Summary register.

NOTE

The DEV SEL H signal is applied to the direct clear input of the one-shot and NED flip-flops. If set, the flip-flops are cleared after the Unibus cycle is completed and the addressed register has been deselected.

A second function of the one-shot is to provide a 1.5 μs waiting period to allow the Attention Summary register in the various drives to be properly read from or written into. In this case, the one-shot times out because the RESP signal is inhibited and at the end of 1.5 μs, SSYN is set. NED is not set since the flip-flop is set only when a register other than the Attention Summary register has been addressed and no RESP is received.

DIS DEM disables the DEMAND signal from being asserted on the Massbus and is generated under the following conditions:

1. If the LOC/REM H signal is asserted indicating local mode, DIS DEM is generated to inhibit the Massbus handshake sequence.

2. DIS DEM is generated if the access is to the odd byte (ODD BYTE L) in the CS1 register (CS1 IN L). The CS1 register is shared by the RH11 and the drive with the odd byte being in the RH11 and the even byte being in the drive. ODD BYTE L and CS1 IN L generate DIS DEM to inhibit the Massbus handshake sequence in order to prevent altering the even (low) byte of the CS1 register located in the drive when the program is doing a byte operation to the odd (high) byte in the RH11. This is necessary because the Massbus cannot differentiate byte from word operations.

3. The STOP DEM L signal is asserted when the processor tries to load a function code specifying a data transfer operation into the drive while the RH11 is already busy executing a data transfer function with that drive or some other drive. For example, if unit 0 is doing a read data transfer and the processor tries to do a read or write data transfer in unit 1, the STOP DEM L signal from CSRB prevents the function code from being transferred to unit 1; otherwise, there would be the OR condition of data from unit 0 and unit 1 on the synchronous Massbus and the program could not distinguish unit 0 data from unit 1 data.

In addition, the DEMAND signal is inhibited when the LEG REG (legal register) signal from BCTA is not asserted. This prevents a SSYN response by the RH11 which indicates to the processor that the Unibus address was not recognized by the RH11.

6.3.4 Gating Address Onto Unibus

The remainder of the sheet shows the Unibus drivers which gate the contents of the Bus Address (BA) register and A16 and A17 of CS1 onto the Unibus address lines. This is accomplished when the RH11 is bus master and doing NPR cycles. Signal ADDR TO BUS H is used to gate the address; signal SEL BUSA H from the CSR module (sheet A) is asserted when the PSEL bit in the CS1 register is cleared. At this time, the RH11 is connected to Unibus A. During NPR operations, if PSEL is asserted, the RH11 is connected to Unibus B. The RH11 is always powered up in the condition where PSEL is cleared indicating the RH11 is connected to Unibus A.

6.3.5 Data Buffer Out Clock

The DB OCLK H signal is used to release data at the output of the Silo when the DB register is read by the program. The BCTA CO L signal is used to inhibit the assertion of DB OCLK during Unibus DATIP operations. This is necessary so that a read-modify-write instruction does not falsely remove data from the Silo. DB register selection is used for maintenance purposes when verifying the operation of the 66-word Silo Buffer register. Signal DB OCLK is asserted when the RH11 responds with SSYN to the register operation (if not a DATIP) and is released when the processor removes MSYN.

6.4 LOGIC DIAGRAM BCTC

This sheet contains the logic for the 16-bit Bus Address register and the 2 extension address bits located in the CS1 register. The register functions as an up-down counter and consists of four 74193 chips, providing outputs labeled BUSB A01 L through BUSB A15 L. The inputs to the chips come from the Unibus A data receivers, shown on sheet DBCF. The register is loaded when the BA IN L signal, REG STR H, and HI BYTE or LO BYTE signal is available, depending on whether the high byte or low byte is to be loaded. If the register is to be loaded as a word, both HI BYTE H and LO BYTE H signals are asserted.

A fifth chip processes bits 9 and 8 of CS1 which are extension bits of the Bus Address register. These bits are designated A16 and A17. The chip is loaded when CS1 IN L, REG STR H, and HI BYTE H are asserted. The RDY signal must also be asserted to load this chip in order to prevent bits A16 and A17 from being changed unless the RH11 is in the Ready state, since other commands can be passed through the dynamic CS1 register to drives not doing transfers.

The 74193 chip has a load input. When this input goes low, the data on the input lines is loaded into the register. The chip also has a CLR input which clears the register to all 0s when CLR H is asserted. The register functions as an up-down counter which counts on the positive-going trailing edge of the ADDR TO BUS H strobe. If CNT DW (1) H is asserted, the register counts down; if CNT DW (0) H is asserted, the register counts up.

6.4.1 Clocking Bus Address Register

The ADDR TO BUS H clock can be inhibited by setting the bus address increment inhibit bit (BAI bit 08) in the CS2 register. When the BAI bit is set, it prevents the bus address from changing during transfers, and the transfers will always occur from that same memory location. This feature might be used when refreshing a display. Normally, BAI (0) H is asserted at the input to AND gate E88 in zone A-7 to enable the ADDR TO BUS H strobe used to increment or decrement the Bus Address register.

6.4.2 Address Bit 00

Address bit 00 is not implemented making the bus address always even (word addressing). This results in only three bits being implemented in the low-order 74193 chip. Since the carry and borrow lines are based on four bits in the chip, two external gates are employed as decoders – AND gate E21 in zone B-6 to detect a carry condition (all 1s) and NOR gate E20 in zone C-6 to detect a borrow condition (all 0s).

6.4.3 Count Down (CNT DW) Flip-Flop

A CNT DW flip-flop is shown in zone A-4 of the diagram and is employed for future capability when reverse write-check and reverse read operations may be implemented. When a reverse function code is loaded (defined by a combination of GO CLR and data bits D01 and D02), the CNT DW flip-flop sets, and reverse write-check and reverse read operations can be implemented. This function is not used with the RS04/RS03 disk.

6.4.4 Bus Address Outputs

The bus address outputs from the RSBA Bus Address register are multiplexed with the outputs of the RSWC Word Count register on logic diagrams BCTD and BCTE for transfer to the Unibus data lines when the register is read by the program.

The BA register and address extension bits (A16 and A17) are also driven onto the selected Unibus (A or B) when the RH11 is performing NPR transfers. This selects the memory location to be accessed by the transfer. The Unibus A address drivers are located on sheet BCTB, while the Unibus B address drivers are located on sheet BCTC.

6.5 LOGIC DIAGRAM BCTD, BCTE

Logic diagram BCTE contains the upper eight bits of the Drive Word Count register, the upper eight bits of the Word Count register and two quad-input multiplexer chips (8234) used to select the word count or bus address when the program reads these registers. Logic diagram BCTD contains a similar arrangement for the lower eight bits of the Drive Word Count and Word Count registers and contains an additional two quad-input multiplexer chips for selecting the lower bits of the Bus Address or Word Count register.

6.5.1 Word Count Registers

The Drive Word Count (DRWC) register counts words transferred between the RH11 and the Massbus and is invisible to the program. This register detects when the RUN line should be unasserted on the Massbus. The Word Count (WC) register is a programmable register which counts words transferred between the RH11 and memory on the Unibus. Both registers are loaded in parallel with the 2's complement of the number of words to be transferred and are incremented toward 0 for each transfer.

The load input to both registers is the logical AND of WC IN H (Word Count register specified), REG STR H and HI BYTE H and LO BYTE H. The Drive Word Count register is incremented by DRIVE CLK H on sheet BCTD. This signal is a synchronous clock and occurs if there is no word count overflow or no error condition. The Word Count register is clocked by the INC WC L signal from sheet DBCB. The registers count on the trailing edge (positive-going) of the DRIVE CLK signal and INC WC signal. A carry out of one chip of the Word Count register is rippled to the count input of the next successive chip. When a carry occurs out of the chip with the most significant bits, word count overflow occurs. The Drive Word Count register is configured in the same manner and when the carry occurs out of the chip with the most significant bits, drive word count overflow occurs. Note the absence of a clear input to both registers. Since the registers are preloaded at the start of a data transfer, a clear is not necessary.

6.5.2 Word Count or Bus Address Selection

The output from the Word Count register is applied to 8234 multiplexer chips. These chips switch either the contents of the Word Count register or Bus Address register to the output. When the S0 input is low, the B inputs (B0, B1, B2, etc.) are switched to the F outputs (F0, F1, F2, etc.). This condition occurs when the Bus Address register is selected from the register select logic on sheet BCTA. When the S1 input is low, the A inputs (A0, A1, A2, etc.) are gated to the F outputs. This condition occurs when the Word Count register has been selected by the register select logic on sheet BCTA. Since S0 and S1 are supplied from a decoder, both cannot be low at the same time. If both inputs are high, the output is disabled and floats high unless asserted by another chip wired in parallel. The multiplexer is open-collector and can be bused together with other

multiplexers. The output feeds an internal bus (BUSI) which is used to sum up data from all the registers and prepares it for input to the Unibus drivers which drive Unibus A.

6.5.3 Clear Logic

Zones D-3 and D-2 on BCTD contains the logic for both Unibuses which determine when a Clear signal is generated. BUSA INIT L or BUSA DC LO L, when asserted, generates INIT + DC LO L. The BUSA INIT L signal initializes the RH11 and the drive. The BUSA DC LO L indicates no power on the Unibus. INIT + DC LO L creates MB INIT H (Massbus initialize) which initializes the registers in the drive. Thus, a no-power condition on the Unibus is implemented to initialize the Massbus.

The three signals that follow generate CLR + GO CLR H and CLR. GO CLR is used to clear the NPR logic, and CLR is used to clear the RH11 and the associated drives.

1. INIT + DC LO L – This signal is the OR of BUSA initialize and DC LO L.

2. GO CLR L – This signal is asserted when a data transfer command is loaded with the GO bit in the CS1 register.

3. PG CLR L – This signal is asserted by setting the CLR bit in bit 05 of the CS2 register, and is used to clear the RH11 and the drive registers.

CLRB H is similar to the CLR H signal and is generated as a result of BUSB INIT or BUSB DC LO L. This signal does not clear the RH11 registers as they are not connected to Unibus B.

If data transfers are being performed on Unibus B when CLRB is asserted, a DLT (data late error) is posted to terminate the transfers.

On sheet BCTE the CLR + GO CLR H signal resets the WC, DRWC OFLO, and DONE flip-flops.

6.5.4 Word Count Overflow

When the Word Count register overflows, the carry output goes low and is applied to the WC OFLO flip-flop as a clock. The positive-going trailing edge of this signal clocks the WC OFLO flip-flop set.

When the WC OFLO flip-flop is set and the last data transfer is completed (trailing edge of DATA REQ), flip-flop E74 is set, causing the DONE assertion which indicates the completion of the data transfer on the Unibus.

If an error occurs (TRE asserted), then the DONE signal will be asserted at the end of the DATA REQ. The RH11 waits for the EOS (end of sector) before going to the Ready state. The DRWC OFLO flip-flop and Drive Word Count register function the same as the WC OFLO flip-flop and Word Count register. The carry output of the Drive Word Count register generates a LWRD H (last word) signal, indicating that the RH11 is not to anticipate receipt of another word. When the RH11 does a write data transfer, it normally makes sure that a word is available for transfer before the next SYNC CLK from the drive. When LWRD is generated, this operation is bypassed. LWRD is checked at the trailing edge of DRIVE CLK and will disable DLT (data late error).

6.6 LOGIC DIAGRAM BCTF

This diagram contains the interrupt control logic to prepare the Unibus to do an interrupt. The logic contained herein is similar to that on the M7821 Interrupt Control module which can be found in the *PDP-11 Peripherals and Interfacing Handbook.*

6.6.1 Interrupt Request

The interrupt control logic is initiated by INTR REQ H (interrupt request) and IE (1) H. The IE (Interrupt Enable) bit is set by the programmer by loading a 1 in bit 6 of the CS1 register. This allows interrupts to occur upon completion of an operation or upon detecting an error condition when INTR REQ H is asserted.

6.6.2 Bus Request

With the above conditions satisfied, BUSA BR L is asserted at the output of gate E65 in zone C-4. The other input to this gate is enabled because the SACK and BBSY flip-flops are reset. The BUSA BR L signal is applied to a priority jumper plug (zone D-6) configured at priority level 5. This causes BUSA BR5 L to be asserted at the output of the plug. The other BR outputs from the plug are unasserted at this time. BUSA BR5 L causes a bus request on the Unibus. When the processor is ready to allow the RH11 to become bus master, it returns BG IN H (bus grant) shown in zone C-8. This signal performs the following functions.

1. It is applied as a clock to the GRANT flip-flop. The positive-going edge tries to clock GRANT set. However, the set input to GRANT is disabled by BBSY being reset and IE (1) H and INTR REQ H being asserted. These conditions hold the input to NAND gate E47, pin 2 low, forcing the output high. The other input (pin 1) to the gate is from the BUSA NPR logic. With no NPR request, pin 1 is held high. AND gate E16 and inverter E64 which feed NAND gate

1. (Cont) are designed to improve the Unibus latency. The jumper at the input to gate E16, when cut, disables the circuit.

2. The BG IN H signal is used to direct clear the GRANT flip-flop when GRANT is negated. However, at this time, note that the GRANT flip-flop is still reset.

3. BG IN H also sets SACK 100 ns after the GRANT is received. The 100 ns delay is provided by the external components at the input to the 7408 AND gate in zone B-6. The delay provides the required time for the GRANT flip-flop to decide whether to block the grant or pass it on to the next device. Note that the set input to SACK is enabled as a result of the Bus Grant signal and because the GRANT flip-flop is still reset.

4. When the BG IN H signal is unasserted and SSYN IN H and BBSY IN H are unasserted indicating completion of the current cycle, BBSY is set. Note that the set input to BBSY is enabled since SACK is set.

Consequently, the interrupt control logic is initiated, a bus request is sent to the processor, a bus grant is returned from the processor, and the SACK flip-flop is set after a 100 ns delay. When the SACK flip-flop sets, the BUSA BR5 L signal goes unasserted and when the processor completes its current cycle, BBSY is set indicating that the RH11 has control of the bus. When BBSY sets, the set input to the GRANT flip-flop is enabled and the GRANT flip-flop will be set by the next BG IN H signal. The grant will be passed to the next device on the bus. In addition, setting BBSY causes the SACK flip-flop to clear, and also generates INTR MASTER L. This signal causes the BUSA INTR L signal on Unibus A to be generated and also gates the 7-bit interrupt vector to the Unibus. The vector is jumper selectable. If the jumper is left in, the corresponding bit is a 1; if the jumper is cut, the corresponding bit is a 0.

6.6.3 Interrupt Done

When the processor has accepted the interrupt vector, it returns SSYN IN H which generates INTR DONE H. This signal clears the latch in zone C-7 which allows the interrupt sequence to terminate. Also, INTR DONE H clears BBSY to allow another device to gain control of the bus.

6.7 LOGIC DIAGRAM BCTH

This diagram contains the NPR control logic necessary to initiate NPR requests and to gain control of the Unibus in order to do NPR cycles. The logic on this sheet is similar to the logic contained on the M7821 Interrupt Control module described in the *PDP-11 Peripherals and Interfacing Handbook.*

6.7.1 NPR Arbitration

The logic is initiated by DATA REQ H being asserted at the input to AND gate E15 (zone D-5). This signal is held asserted during the entire cycle for single cycle NPRs or is held asserted for both cycles when performing back-to-back NPR cycles. The other input to the AND gate is CLR DREQ L, which is normally held high during the cycle and enables the gate. The output of this AND gate qualifies AND gate E25 (zone B-3). The other two inputs to this gate are enabled by the SACK and BBSY flip-flops being reset. The output of AND gate E25, pin 12 is supplied to two gates (E33), (zone D-2) to raise an NPR request on the Unibus which has been selected. This sheet will be described assuming that Unibus A has been selected. In this event, the BUSA NPR L signal is asserted on the Unibus. The processor arbitrates the NPR requests and returns a BUSA NPG IN H signal when it wishes to to grant the bus to the RH11. The BUSA NPG IN H signal clocks the GRANT A flip-flop, but the flip-flop does not set since the three inputs to gate E7 (zone D-3) are high causing the D-input to the flip-flop to remain low. Consequently, the GRANT signal is blocked and is not passed to the other devices. The BUSA NPG IN H signal is also applied to multiplexer E26. Since Unibus A has been selected, the multiplexer inputs at pins A3 through A0 are present at the output. If Unibus B is selected, the inputs at pins B3 through B0 are present at the output. The BUSA NPG IN H signal clocks the SACK flip-flop after 100 ns. Since GRANT L is not asserted, the other input (pin 11) to E7 is high and provides a low input to the SACK flip-flop causing it to set. The 100 ns delay network consisting of the resistor and capacitor network at the input to AND gate E15 (zone C-5) ensures that the SACK flip-flop will not be prematurely set until the GRANT signal has been blocked. Setting the SACK flip-flop causes the BUSA SACK L signal to be asserted on the Unibus and also causes the RH11 to drop the BUSA NPR L signal. This acknowledges the fact that the RH11 has received the BUSA NPG IN H signal from the processor. SACK prevents the processor from further arbitrating NPRs.

6.7.2 Acquiring Bus Mastership

Multiplexer E26 monitors BBSY and SSYN for the selected Unibus (BUSA, in this case). When both BBSY and SSYN from the device currently acting as bus master are unasserted, NOR gate E32 (zone B-6) is qualified. This enables AND gate E15 (zone B-5). The other input to this gate qualifies the gate when the processor drops BUSA NPG IN H. The output of this gate clocks the BBSY flip-flop set since SACK is still asserted. When BBSY sets, it asserts BUSA BBSY L via gate E40 (zone B-2) and also asserts NPC MASTER L, indicating that the RH11 is now bus master. This initiates the sequencing logic for an NPR cycle (see sheet DBCA). The 0 output of the BBSY flip-flop disqualifies AND gate E25 (zone B-3) which keeps the BUSA NPR L signal unasserted. Also, when SACK ENB H and BBSY (1) H are asserted, the SACK flip-flop is cleared.

If a device on Unibus B desires to become bus master prior to the RH11 acquiring bus mastership, the logic in the RH11 must pass the grant to the next device. The BUSB NPG IN H signal clocks the GRANT B flip-flop set. Since the SEL BUSB H signal is unasserted, the D-input to the flip-flop is high and the flip-flop is set allowing the GRANT signal to be passed to the next device. When the BUSB NPG IN H signal is dropped by the processor, the clear input of the GRANT B flip-flop is brought low, thus removing the BUS NPG OUT signal to the next device.

6.7.3 Completion of NPR Cycle

The NPR cycle(s) is completed when CLR DREQ L is asserted, causing AND gate E15 (zone D-5) to go low. This action causes the NPR cycle to end and BBSY flip-flop to reset, releasing the bus to the next device.

6.8 LOGIC DIAGRAM BCTJ

This diagram contains the MB INIT logic, the logic used to gate out the high byte of the CS1 or the CS2 registers, and the logic to set the (Missed Transfer Error) MXF flip-flop.

6.8.1 MB INIT Signal

When an initialize (INIT) signal or a power fail condition (DC LO L) occurs on Unibus A, a MB INIT H (Massbus initialize signal) is generated and initializes all the drives. Both INIT and DC LO are guaranteed to be a minimum of 400 ns, and the assertion of either signal qualifies gate E87 (zone D-4) to produce MB INIT H.

Signal MB INIT H is also generated if the CLR bit in CS2 is set by the program. This causes a PG CLR L signal to be generated which fires 400 ns one-shot multivibrator E85 (zone D-6). The output of the one-shot is a 400 ns negative pulse which is used to enable the other input to gate E87 in zone D-4.

6.8.2 Gating High Byte of CS1/CS2

The two 2-to-1 multiplexers (E59 and E60) in the center of sheet BCTJ are used to gate out the high byte of the CS1 or CS2 register. CS1 OUT L, when asserted, gates the high byte of the CS1 register through the multiplexer and CS2 OUT L, when asserted, gates the high byte of the CS2 register through the multiplexer. The output of the multiplexer is the internal data bus (BUSI) which feeds Unibus A.

6.8.3 MXF Error Flip-Flop

The lower portion of sheet BCTJ shows the SET MXF and MXF flip-flops and a 250 ms one-shot. When the RH11 goes into the busy state (RDY H not asserted), the 250 ms one-shot (E85 in zone B-7) fires indicating that the RH11 is attached to the synchronous bus. The 250 ms one-shot is retriggered on every SYNC CLK signal from the drive. If the RH11 is busy, and a SYNC CLK pulse does not occur within 250 ms, the trailing edge of the 250 ms pulse clocks SET MXF flip-flop E86 (zone B-5) set which, in turn, causes MXF flip-flop E86 (zone B-3) to be direct set. Normally, the D-input to the SET MXF flip-flop is at ground which allows the flip-flop to set. If jumper W19 is cut, however, the high input applied to the D-input prevents the flip-flop from setting. This jumper is used for maintenance purposes. The MXF flip-flop can be set under program control by setting bit 9 (MXF error) of the CS2 register and by generating the appropriate gating signals (HI BYTE H, REG STR H, and CS2 IN L).

The 250 ms one-shot and the SET MXF flip-flop are direct cleared by the CLR H signal, the BUSY flip-flop being in the Reset state, or the OCC (occupied) line on the Massbus being asserted. The MXF flip-flop is direct cleared by the CLR ERR L signal.

6.8.4 AC LO and DC LO

Power supply signals AC LO and DC LO are actively pulled up so that they may be used as inputs to the two M688 Power Fail Driver modules.

6.9 BCTK LOGIC DIAGRAM

The BCTK print provides the truth table for the register selection ROM shown on sheet BCTA.

6.10 LOGIC DIAGRAM CSRA

This logic diagram contains the data transfer command logic, the RUN flip-flop, the BUSY flip-flop, the PSEL (port select) flip-flop, the CS1 clocking logic, and the interrupt request logic.

6.10.1 Data Transfer Command Logic

The data transfer command logic consists of the Write, Read, and Write-Check flip-flops (E3 pin 6, E15 pin 6, and E15 pin 8, respectively). These flip-flops decode the Write, Read, or Write-check commands that are being passed through the controller into the drive. The commands are decoded in the RH11 to let the RH11 know what type of operation is to be implemented. In addition, these commands are also supplied to the drive where they are again decoded in the drive's function register. All other commands are not decoded in the RH11 but are merely decoded in the drive.

The D-input to the Write flip-flop represents the range of function codes that define the Write command. These codes range from 60 through 67. The D-input to the Read flip-flop represents the range of function codes that define a Read command. These codes range from 70 to 77. The D-input to the Write-check flip-flop represents the function codes that define a Write-check command. These codes range from 50 to 57. For example, the D-input to the Write flip-flop is enabled when D03 IN L is unasserted and D04 IN H and D05 IN H is asserted in gate E6 pin 12. This bit pattern corresponds to the digit 6, specifying function codes from 60 through 67. The other flip-flops are decoded in like manner.

The C-input to the flip-flop accepts the positive-going trailing edge of the GO CLR L signal to clock the flip-flop specified by the appropriate data bits which comprise the function code. Signal GO CLR L is used to initialize the Silo and NPR logic for a data transfer, and is also used to direct set the BUSY flip-flop in zone B-6, indicating a data transfer command is in progress. Signal GO CLR L is asserted at the output of NAND gate E17, pin 6 if CLK CS1 LO H, D00 IN H, and a data transfer command (Write, Read, or Write-check) has been decoded by NAND gates E6 pin 12, E14 pin 12, or E14 pin 6. Signal CLK CS1 LO H is asserted when the program is loading data into the low byte of the CS1 register, and D00 IN H is asserted when the GO bit is set by the program. As previously mentioned, the write block code is 60 through 67. Since D00 IN H is asserted to generate GO CLR L which, in turn, is used to clock the data transfer flip-flops, the function code for each data transfer command consists of only the odd function codes within the group. For example, the write function codes are 61, 63, 65 and 67. The even codes do not start a data transfer function since the GO bit (D00 IN H) must be asserted.

The outputs of the data transfer flip-flops are applied to various gates to generate signals for internal use. Gate E20, pin 4 generates the Ready signal when there is no Read, Write or Write-check command being processed, meaning that the RH11 is capable of accepting a data transfer command. This fact is reflected in bit 7 (RDY) of the CS1 register. NAND gate E1, pin 11 generates WRITE L after the function command has been loaded in the drive. This is done for the following reason: When the Write command is asserted, a DATA REQ signal is initiated, causing a memory access on the Unibus. To prevent this access from occurring when the RH11 is trying to access a non-existent drive, the WRITE flip-flop is ANDed with FCTN LOAD (1) L. Signal FCTN LOAD (1) L inhibits the Write command from initiating a memory access until the command has been loaded into the drive. In this way, the memory cycle is not performed for a non-existent drive. Should a non-existent drive be accessed, an NED (non-existent drive) error is raised which disables the DATA REQ signal from initiating an NPR cycle. Inverter E13, pin 10 merely provides a buffered output of the Read signal. Gate E5, pin 3 ORs the output of the Read and Write-check flip-flops to create the Read or Write-check signal. Inverter E13, pin 12 buffers the Write-check signal from the WR CHECK flip-flop. When the data transfer is complete for a particular operation, the appropriate data transfer flip-flop is cleared by gate E8, pin 3. This gate is asserted by BUSY (0) H and DEV SEL L not asserted or by CLR L being asserted. BUSY (0) H is asserted when the BUSY flip-flop is cleared, indicating that the RH11 is no longer busy. This flip-flop is described in subsequent paragraphs. The DEV SEL L signal is asserted when the program is reading or writing a register and prevents the program from looking at the ready bit during the time the bit might be changing. When the data transfer flip-flops are cleared, the RH11 goes to the RDY state.

6.10.2 RUN Flip-Flop

In a write operation, the RH11 transfers the Write command to the function register in the drive and then turns the drive on by setting the RUN flip-flop which asserts the RUN signal. The drive seeks the address specified by the program and starts accepting data words as a result of the SYNC CLK signals. Before the RUN signal is asserted, however, the RH11 prefills the Silo with data words so that data is available to the drive immediately. This logic is implemented by NAND gate E19, pin 6 which is enabled by WRITE H, START H, and OBUF FULL (1) H. The START H signal is asserted when the number of words specified by the start counter have been loaded in the Silo. If only one or just a few words are to be transferred, the RH11 ensures that a word is in OBUF as a result of OBUF FULL (1) H. In this case, the START H signal is asserted as a result of WC OFLO (1) H and not due to the start counter indication of words loaded in the Silo. Note that it takes from 0 to 32 μs for a word to propagate from the bottom cell of the Silo to the top cell with a typical time of 16 μs. Because of this time delay, the logic is designed to ensure that a word is in OBUF before the RH11 turns on the drive. The TRE (1) L input to gate E19, pin 8, if asserted, also sets the RUN flip-flop. This is necessary because the data transfer command has already been loaded for writes when errors occur before the signal START in the RH11 is asserted, and the only way to terminate the operation is to set the RUN flip-flop and wait for the end of the first block or sector (designated by EBL). At this time, the error condition clears the RUN signal. On the trailing-edge of the EBL (end-of-block) signal, the drive looks at the cleared RUN signal and terminates its operations.

In the case of a read or write-check operation, it is desired to set the RUN signal immediately in order that the drive can start filling up the Silo. This is accomplished by gate E19, pin 8.

The RUN line, when cleared, disconnects the RH11 from the drive. This line is cleared under the following conditions:

1. When drive word count overflow [DRWC OFLO (1) L] is asserted. This occurs when the desired number of words have been transferred.

2. If an error exists in the RH11 and the drive has asserted a SYNC CLOCK (SCLK). The logic is implemented by inverter gate E9, pin 6, which is enabled when an error occurs. In this situation, the RUN flip-flop is direct cleared and the drive looks at the RUN line on the trailing edge of EBL. If RUN is cleared or unasserted, the transfer is terminated. If RUN is asserted, the drive does the transfer for the next sector.

3. If an exception (EXCP L) occurs (see gate E27, pin 8). When the drive has an error, it raises the EXCP line which clears RUN upon receipt of the EBL signal. This indicates the end of the current sector. An exception is caused by any of the error conditions defined in the ER register.

4. If a data transfer command is to be loaded into a non-existent drive. This condition is implemented by FCTN LOAD (1) H and NED H via NAND gate E9, pin 3.

5. If a clear (CLR L) or missed transfer signal [MXF (1) L] occurs.

NOTE

The conditions described in 1, 2, 3 to clear the RUN flip-flop are synchronized to the drive. The conditions described in 4 and 5 are not synchronized to the drive since there is no guarantee that a valid drive has been accessed or that the drive will respond.

6.10.3 BUSY Flip-Flop

The BUSY flip-flop is set during a data transfer command and remains set until reset by one of the following situations:

1. When the RH11 is doing a data transfer command, the BUSY flip-flop cannot be cleared and the operation cannot be terminated until both the Unibus and Massbus cycles have been completed. This is indicated by DONE (1) and EOS (1) applied to NAND gate E1. When both signals are asserted, the BUSY flip-flop is cleared via gate E8, pin 8.

2. The CLR or MXF (1) signals which clear RUN are also used to clear BUSY.

3. The BUSY flip-flop can be clocked clear by a data transfer command being loaded into a non-existent drive. This is accomplished by NAND gate E9, pin 3, which is qualified by FCTN LOAD (1) H and NED H.

6.10.4 Port Select Flip-Flop

The Port Select (PSEL) flip-flop in zone B-6 is a programmable bit which selects Unibus A or Unibus B. If the flip-flop is set, Unibus B is selected; if the flip-flop is cleared, Unibus A is selected. The output of the PSEL flip-flop feeds driver E5, pin 6 which generates the SEL BUSA H signal used to control the data path for the Unibus.

A second input to E5, pin 6 is a jumper which overrides the PSEL bit. PSEL is set or cleared via CS1 IN H, REG STR H and HI BYTE H only when the RH11 is in the Ready state. This prevents changing of the data path during a data transfer. These signals are asserted when the program is loading the upper byte of the CS1 register. With these conditions asserted and the RH11 in the Ready state, AND gate E11, pin 3 is qualified and clocks the PSEL flip-flop set if D10 IN H is asserted.

6.10.5 CS1 Clocking Logic

The CLK CS1 HI H and CLK CS1 LO H signals are generated by AND gates E23, pin 6 and E23, pin 8, respectively. These signals are clocking signals for the high byte and the low byte of the CS1 register. Signals HI BYTE H, REG STR H, and CS1 H create CLK CS1 HI H. Signals LO BYTE H, REG STR H, and CS1 H create CLK CS1 LO H.

6.10.6 Interrupt Requests

Interrupt requests are allowed to occur if the interrupt facility is enabled. The facility is enabled by the program loading a 1 in bit position 6 (interrupt enable bit) of the CS1 register. This sets the IE (Interrupt Enable) flip-flop and generates IE (1) H. If an interrupt occurs (with the interrupt enable set), the IE bit is cleared by INTR DONE H which occurs when the processor has been interrupted, has acknowledged the interrupt, and is preparing to execute the interrupt service routine. Signal INTR DONE H is generated on sheet BCTF and clears the IE bit to prevent interrupts from occurring while the service routine is being executed. The IE bit can also be cleared by CLR L which may occur during a Unibus initialize sequence, a power fail assertion, or by setting program clear bit 5 on the CS2 register.

The interrupt facility is enabled by the IE bit. However, the interrupt occurs as a result of the INTR REQ signal being asserted. Interrupts can occur as a result of one of the following conditions:

1. If SC (special condition) and RDY H are asserted, the INTR REQ H signal is generated to initiate an interrupt. SC occurs as a result of TRE, an ATTN signal from the drive, or MCPE (Massbus Control Parity Error). The RDY H signal ensures that the RH11 is in the Ready state before it initiates an interrupt. For example, if a drive asserts ATTN while the RH11 is busy doing a data transfer with another drive, the interrupt would not be allowed to occur until the RH11 has completed the current data transfer and returned to the Ready state.

2. If the IE bit is set and the RH11 changes from the Busy to the Ready state, the INTR flip-flop sets and generates INTR REQ H, indicating completion of the data transfer and initiating the interrupt.

3. The program can force an interrupt by loading bits D06 H (IE) and D07 H (RDY) in the CS1 register which direct sets the INTR flip-flop.

6.11 LOGIC DIAGRAM CSRB

This diagram contains the logic associated with some of the error conditions and status indicators.

6.11.1 CS2 Clocking Signals

The program loads data into the CS2 register by the CLK CS2 HI H and CLK CS2 LO H signals. CLK CS2 HI H causes the program to load data into the high byte of the CS2 register, and CLK CS2 LO H causes the program to load data into the low byte of the register. REG STR H and CS2 IN H are enable signals to AND gates E27, pin 6 and E27, pin 12. Signal CLK CS2 HI H is qualified by the HI BYTE H signal, and CLK CS2 LO H is qualified by the LO BYTE H signal.

6.11.2 Program Clear Bit

The program clear bit (PG CLR L) is set when the program loads a 1 in bit 5 of the CS2 register and CLK CS2 LO H is asserted, indicating that the program is loading the low byte of the CS2 register. PG CLR L is an input which generates the CLR portion (see sheet BCTD) of the CLR + GO CLR L signal and also generates MB INIT (see BCTJ). The CLR signal initializes the RH11 and MB INIT initializes the drive.

6.11.3 Bus Address Increment Inhibit

The Bus Address Increment Inhibit (BAI) flip-flop, when set, prevents the Bus Address register on the BCT module from incrementing when doing NPR cycles. Consequently, all memory references are made to or from the same memory location. This feature is useful when refreshing a display from a disk, for example. The BAI bit can only be

changed if the RH11 is in the Ready state. The CLK CS2 LO H and RDY H are ANDed to clock the BAI flip-flop which represents bit 3 of the CS2 register.

6.11.4 Unit Select Number

The unit numbers are unit 0 through 2 of the CS2 register and are designated U00 through U02 H. These three bits are loaded by the program and used on the Massbus to select one of eight drives, and are generated by data bits D02 IN H through D00 IN H which are applied to three of four flip-flops contained on IC E21.

6.11.5 Parity Test Mode

A parity test mode is provided for maintenance purposes. This is implemented as PAT (bit 4 of the CS2 REG) and may be set or cleared by the program. When set, the parity logic associated with the Massbus in the RH11 is switched from odd parity to even parity generation.

6.11.6 Function Load

The use of the Function Load flip-flop is described on logic diagram CSRA. The flip-flop is set when a data transfer command (Read, Write or Write-check) is being loaded in the CS1 register. The C-input to the flip-flop is clocked by GO CLR L which is asserted when a data transfer command is specified, the clocking signal for the CS1 is asserted, and the GO bit is set. The flip-flop remains set until the bus cycle being used to load that command is completed. At this time, the master drops MSYN and the DEV SEL L signal goes unasserted to clear the Function Load flip-flop. The Function Load signal is used to delay the Write signal from being asserted until the function has been loaded in the drive (see sheet CSRA), and is also used to clear the RUN flip-flop when a function command is being loaded into a non-existent disk (see sheet CSRA).

6.11.7 Non-Existent Device

The Non-Existent Device (NED) error is generated at the output of a latch circuit consisting of gates E9, pin 8 and E9, pin 11. Signal NED H is asserted when SET NED L is asserted, and SET NED L is asserted 1.5 μs after DEMAND is asserted on the Massbus and no transfer response occurred. Thus, if no response was received from a drive 1.5 μs after the assertion of DEMAND and the register being addressed was not the Attention Summary register, then a non-existent device has been addressed. Signal NED H is cleared by CLR ERR L. This CLR ERR L signal clears all the error conditions, and is generated by CLR + GO CLR L. Signal CLR occurs as a result of power fail, Unibus initialize, or program clear. Signal GO CLR L is asserted by setting the GO bit during a data transfer command.

The errors are also cleared by loading a 1 in the TRE bit position in bit 14 of the CS1 register. This is accomplished by NAND gate E2, pin 3 in zone B-7. Consequently, loading a 1 in the TRE bit position clears out any error in the RH11. This is done so the error conditions in the RH11 can be cleared without having to clear the error conditions in the drive.

6.11.8 Transfer Error

The TRE (transfer error) flip-flop (zone B-6) is a summation of all the error conditions in the controller and the drive. These include Data Late Error (DLT), Massbus Data Parity Error (SYNC PE), Exception (summation of all error conditions in the ER register), Write-Check Error (WCE), Unibus Parity Error (UPE), Non-Existent Device (NED), Non-Existent Memory (NEM), Program Error (PGE), and Missed Transfer Error (MXF). Any one of these conditions enables gate E22, pin 8 and clocks the TRE flip-flop set. TRE is bit 14 of the CS1 register. TRE (0) H is ORed with ATTN and CNTL PE (MCPE) to create SC H, which is bit 15 of the CS1 register. Bits 14 and 15 are coded to inform the programmer of the type of error and where it occurred. Whenever the SC bit is set, this indicates that an error has occurred from some drive doing a data transfer command or that a drive has finished some movement command such as a Seek. By then examining the TRE bit, the programmer can determine additional information. If TRE is set, this indicates that a data transfer error has occurred. If TRE is not set, this indicates that:

1. an error has occurred in some drive not doing a data transfer command,
2. the drive has completed some operation which is not a data transfer command, or
3. a Massbus Control Parity Error was detected when the program read information from a drive register.

The programmer can then ascertain which drive has caused the SC H signal by referring to the Attention Summary register which shows the ATTN condition of each drive or if MCPE occurred (bit 13 of CS1). ATTN is raised by a drive when an error occurs or when it has finished some operation other than a data transfer command such as a Block Search. Completion of data transfer commands are indicated to the programmer by the condition of the RDY bit.

6.11.9 Program Error Flip-Flop

The Program Error (PGE) flip-flop in zone C-5 is set when the programmer tries to load a data transfer command while the RH11 is in process of doing a data transfer. Signal GO H is asserted indicating that a data transfer command is being loaded; if the RH11 is busy, RDY H is low which causes the PGE flip-flop to set creating PGE (1) H. This signal is applied to NAND gate E6, pin 6 and generates a STOP DEM L signal which is applied to the BCT module and prevents the DEMAND signal from going out on the Massbus and actually loading the data transfer command into a drive. The PGE (1) H signal also creates the TRE condition (zone B-6). The PGE flip-flop is direct cleared by CLR L or CLR TRE L.

6.11.10 End of Sector (EOS) Flip-Flop

An EBL pulse occurs at the end of every sector. The drive monitors the RUN line from the RH11 at the trailing edge of every EBL. If RUN is asserted, the drive continues to do another sector. If RUN is not asserted, this is the last sector and the drive stops since the data transfer is completed.

The RH11 also must monitor the RUN line in order to know when the drive has reached the end of the last sector. Otherwise, the RH11 might return to the Ready state before the drive has completed the operation. The EOS flip-flop in the RH11 monitors the RUN line at the trailing edge of EBL. Signal EOS (0) H prevents the BUSY flip-flop (sheet CSRA) from clearing. When the end of the last sector is reached at the trailing edge of EBL, the EOS flip-flop is set, thus allowing the BUSY flip-flop to clear and permitting the RH11 to return to the Ready state as long as the last word on the Unibus has been transferred (DONE is asserted). Remember that the Unibus transfer as well as the Massbus transfer must be complete to return the RH11 to the Ready state.

6.11.11 Unibus Parity Error (UPE) Flip-Flop

The Unibus Parity Error (UPE) flip-flop is direct set by a parity error on the Unibus as defined by the states of the PA (D16) and PB (D17) bits (see sheet DBCH). The UPE flip-flop can be set by the programmer by writing a 1 in bit position 13 of the CS2 and clocking the UPE flip-flop with CLK CS2 HI H which clocks the high byte of the CS2 register. Signal UPE (1) H causes TRE and the programmer can ensure proper operation of the UPE flip-flop by writing a 1 in bit 13 and checking to see if TRE occurs.

6.12 LOGIC DIAGRAM DBCA

This diagram contains the logic necessary to transfer data between the RH11 and memory over the PDP-11 Unibus. When the RH11 asserts a DATA REQ, the following events occur:

1. The RH11 asserts an NPR request (see sheet BCTH).
2. The processor arbitrates the NPR requests and issues NPG to the RH11. This indicates that the RH11 is the next device to become bus master.
3. The RH11 acknowledges receipt of the grant by issuing SACK (selection acknowledge), which drops the NPG signal.
4. The RH11 waits for BBSY and SSYN to clear, indicating that the device currently using the Unibus has finished its cycle.
5. When BBSY and SSYN clear, the RH11 asserts BBSY and NPC MASTER.
6. The RH11 places address and control information on the Unibus (and data if a Read command is specified).
7. After 200 ns, the RH11 issues MSYN since it is now bus master.
8. If a Read command is specified, the slave device returns SSYN upon receipt of the data. If a Write or Write-check command is specified, the data from the slave is deskewed 125 ns after SSYN is returned before it is used in the RH11.
9. MSYN is cleared which, in turn, causes the slave device to clear SSYN. If a single NPR cycle is being performed, BBSY is cleared 100 ns after MSYN is cleared. If a back-to-back NPR cycle is being performed, BBSY is cleared 75 ns after MSYN clears on the second cycle.
10. When BBSY is cleared, the NPR cycle is finished until a new DATA REQ is issued to initiate the next cycle.

The logic to accomplish the above events is contained on sheets BCTH (previously described) and DBCA. The following description covers sheet DBCA.

6.12.1 NPC MASTER Signal

When NPC MASTER is asserted, ADDR TO BUS H is asserted. In addition, the NPC MASTER signal enables gates E84 and E96 (zone D-6). When a Read command is specified, these gates are qualified to yield both polarities of the DATA TO BUS signal used to gate data onto the Unibus. The gates are connected in parallel to avoid the delay normally required in going through an inverter.

6.12.2 ADDR TO BUS Signal

The ADDR TO BUS signal, generated at the output of E89, pin 10, accomplishes the following functions:

1. ADDR TO BUS triggers one-shot multivibrator E92 (zone C-5). In the first memory cycle, END CYCLE (1) H is unasserted, thus enabling gate E89. The assertion of ADDR TO BUS triggers the one-shot (the function of the one-shot is described in subsequent paragraphs). At the end of the first memory cycle, END CYCLE (1) H is asserted disqualifying E89. When END CYCLE (1) H goes low, it produces a positive-going pulse at E89, pin 10 which triggers the one-shot for the second memory cycle. Consequently, the one-shot is triggered by NPC MASTER in the first memory cycle and by the assertion and subsequent unassertion of END CYCLE (1) H in the second memory cycle.

2. ADDR TO BUS H is the enable signal which gates the address onto the selected Unibus. The leading edge of END CYCLE (1) H causes the trailing edge of ADDR TO BUS H which increments the Bus Address register. During the width of the END CYCLE pulse, the address in the address register is stabilized. At the trailing edge of END CYCLE, one-shot E92 is again triggered.

3. ADDR TO BUS is also applied to gate E89 and gate E90 (zone D-2). The other input to those gates is SEL BUSA, which selects the appropriate Unibus. If SEL BUSA is asserted, Unibus A is selected; otherwise Unibus B is selected. E89 and E90 enable the drivers shown in zone C1 and D1 to generate MSYN and C1 signals for the appropriate Unibus (BUSA or BUSB). MSYN is asserted by ADDR TO BUS H when the MSYN flip-flop is set. The setting of this flip-flop is described in the paragraph entitled MSYN Deskew. C1 is asserted low by ADDR TO BUS H when a Read command is specified. This designates a DATO operation (data written into memory). If C1 is unasserted (no Read command specified), a DATI operation is performed.

NOTE

The C0 control line specifies a DATOB or DATIP operation. Since the RH11 does neither operation, the C0 line is not required and remains unasserted.

6.12.3 MSYN DESKEW

The ADDR TO BUS H signal triggers one-shot multivibrator E92 as previously mentioned. This one-shot provides a 200 ns deskew for MSYN to allow the address and control lines time to stabilize on the Unibus.

NOTE

Gate E90 (zone C-6) is used during a Read command to lock the Silo timing to the Unibus timing and ensures that data will be deskewed for the proper interval before MSYN is set on the second cycle of back-to-back NPR sequences.

The positive-going trailing edge of the 200 ns pulse from pin 4 of E92 clocks DESK COMPL flip-flop E93 (zone C-4), indicating that the deskew is completed. This enables one input to gate E69 (zone C-3). The other inputs to this gate represent inhibit conditions to prevent MSYN flip-flop E93 (zone C-3) from setting. These inhibit conditions are described in the paragraph entitled MSYN Inhibit Conditions. If none of the inhibit conditions are present, and the Silo and Unibus signals are in the proper state, MSYN is set, and is ANDed with the appropriate Unibus select signal (zone D-1) to generate BUSA MSYN L or BUSB MSYN L.

6.12.4 MSYN Inhibit Conditions

In the second cycle of back-to-back NPRs or in BUS HOG mode (described in subsequent paragraphs), there are several conditions used to inhibit MSYN. These conditions are ORed in gate E69 (zone C-3). The purpose of these inhibits is to lock the data transfer rate to the Silo data rate. The inhibit conditions are listed below:

1. The RH11 cannot assert MSYN for the current cycle until NPC SSYN from the previous cycle has been cleared.

2. In a write function, the RH11 does not assert MSYN until it is certain that IBUF is empty and available to receive the data from the Unibus. If IBUF is full, E69 gate is disabled and inhibits MSYN until IBUF is cleared.

3. In a write-check function, the RH11 does not fetch a word from memory until it is sure that the word from the drive is in OBUF. When OBUF is not full, OBUF FULL (0) H is asserted which disqualifies gate E69 and prevents MSYN from setting until OBUF is full.

4. The fourth inhibit condition occurs during a Read command when the RH11 is doing the second NPR cycle of back-to-back NPRs or is in BUS HOG mode. In this instance, the RH11 does not initiate MSYN deskew until it is assured that a data word is available in OBUF. At this time, then, the data and address can be deskewed from MSYN to allow time for the data and address to stabilize on the Unibus. This inhibit condition is implemented in AND gate E90 (zone C-6). If OBUF is full, OBUF FULL (0) H goes low and allows 200 ns one-shot E92 to be triggered. If OBUF is not full, this gate inhibits the one-shot from firing.

6.12.5 MSYN Timeout

The MSYN (1) H signal is applied to NEM flip-flop E85 (zone B-6) and to 10 μs one-shot multivibrator E83 (zone B-6). The 10 μs one-shot measures the time it takes for SSYN to respond. If SSYN does not respond within 10 μs, the positive-going trailing edge at pin 4 of E83 clocks the NEM flip-flop set, denoting a non-existent memory. This sets bit 11 in the CS2 register to flag the programmer and also raises the TRE bit in the CS1 register. If SSYN does respond within 10 μs after MSYN is issued, it direct clears the 10 μs one-shot and the NEM flip-flop via gate E80, pin 3. The CLR ERR signal is used by the programmer to clear the NEM flip-flop after it has been set by the timeout circuitry.

6.12.6 DATA WAIT and MSYN WAIT One-Shot Multivibrators

The DATA WAIT one-shot is shown in zone B-5, and the MSYN WAIT one-shot is shown in zone B-3. The DATA WAIT one-shot is used during a Write or Write-Check command (READ L unasserted) and provides a 125 ns pulse to deskew the data from SSYN. Of the 125 ns, 75 ns are in accordance with Unibus specifications and 50 ns is the propagation time for the data to be supplied to IBUF from the Unibus in a write cycle. In a write-check cycle, it provides the propagation time for this data to be compared with the device data in OBUF. The DATA WAIT one-shot is triggered by NPC SSYN, or in its absence, a non-existent memory error when the RH11 is bus master (NPC MASTER H asserted), MSYN has been issued, and a write or write-check operation has been designated. The negative-going trailing edge of the DATA WAIT one-shot triggers the MSYN WAIT one-shot which initiates a 75 ns pulse. At the end of 75 ns, the positive-going output from E95, pin 4 triggers 200 ns END CYCLE one-shot (zone B-2). END CYCLE (1) H inhibits the ADDR TO BUS signal and retriggers the NPR control logic if a second cycle is to be performed or clears BBSY if it is the last cycle of the NPR sequence. During the 75 ns interval between the firing of MSYN WAIT and the firing of the END CYCLE one-shot, the RH11 has cleared MSYN and must hold the address and BBSY asserted.

The MSYN WAIT one-shot accomplishes the following functions:

1. Clears the MSYN flip-flop via OR gate E80 (zone C-3).

2. Is fed to CYCLE COUNT flip-flop E85 (zone B-3) and NEXT CYCLE flip-flop E36 (zone B-2). The CYCLE COUNT flip-flop determines whether the cycle is the first or second cycle of back-to-back NPRs. The NEXT CYCLE flip-flop determines whether a second memory cycle is to be performed in the NPR sequence.

3. Generates DATA STR H which is used to clock data into IBUF or to change data in OBUF.

If a Read command is specified (writing a data word into memory), the data does not have to be deskewed when NPC SSYN is received. However, MSYN must be cleared. Prior to the receipt of NPC SSYN, all inputs to NAND gate E94 (zone B-4) are high, forcing the output low. Upon receipt of NPC SSYN, pin 9 of E94 is driven low, forcing the output high. The positive-going output triggers the MSYN WAIT one-shot which clears MSYN. Consequently, in the case of a Write or Write-check command, both the DATA WAIT and MSYN WAIT one-shots are fired. In the case of a Read command, the data does not need to be deskewed and the DATA WAIT one-shot is bypassed.

6.12.7 CYCLE COUNT and NEXT CYCLE Flip-Flops

The CYCLE COUNT flip-flop is shown in zone B-4 and determines whether the RH11 is doing the first or second cycle of back-to-back NPRs. Initially, NPC MASTER H is not asserted which causes CYCLE COUNT to direct set. Near the end of the first cycle, MSYN WAIT is triggered which toggles CYCLE COUNT. The low (0) output of the flip-flop is fed through gates E98 and E97. As a result of the double inversion, the D-input is low which causes the flip-flop to reset. Assume that the RH11 is not in BUS HOG mode (pin 10 of E98 asserted high), there is no TRE error (pin 5 of E97 asserted high), and word count overflow, exception stop, or non-existent memory is not holding the flip-flop direct set. The RH11 monitors the flip-flop at END CYCLE time. Since CYCLE COUNT is reset, it indicates the first NPR cycle is being performed. The second MSYN WAIT signal toggles the CYCLE COUNT flip-flop again. Since the flip-flop was reset, the high output from pin 6 is reflected as a high level at the D-input. This action causes the flip-flop to set, indicating the second NPR cycle is being performed.

Whenever the CYCLE COUNT flip-flop is set, gates E71 (zone A-1) and E97 (zone B-2) are enabled. At END CYCLE time, therefore, gate E96 (zone B-1) is enabled to assert CLR BBSY L. This indicates that the RH11 has completed the second cycle of back-to-back NPRs or desires to terminate after the first cycle.

If the RH11 is in BUS HOG mode or if a TRE (Transfer Error) occurs, the CYCLE COUNT is prevented from toggling because a high level is presented at the data input.

The NEXT CYCLE flip-flop determines whether a second memory cycle is to be performed in the NPR sequence. If the NEXT CYCLE signal is asserted, a second cycle is desired, and the reset output of the NEXT CYCLE flip-flop goes low which inhibits the clearing of BBSY. The NEXT signal indicates the availability of a data word in the Silo indicated by Input Ready or Output Ready (depending on the function performed). If the NEXT signal is not asserted, indicating a second cycle is not desired, the reset output of NEXT CYCLE goes high enabling gates E97 and E96 (zone B-2). At END CYCLE time, E96 is qualified and BBSY is cleared terminating the transfer.

6.12.8 ERROR Conditions

The error conditions in the RH11 can also cause a cycle to terminate. The UPE (Unibus Parity Error) and WCE (Write-Check Error), if asserted at END CYCLE time, cause BBSY to clear. NEM (Non-Existent Memory), if asserted, keeps the CYCLE COUNT flip-flop direct set so the flip-flop cannot toggle. A TRE error, if asserted, keeps the data input high to prevent the CYCLE COUNT flip-flop from toggling.

6.12.9 1-Cycle Jumper

If the RH11 is to do single NPR cycles, a jumper designated "1 CYCLE" and located in zone B-5 is inserted. This places a steady high level at the data input to the CYCLE COUNT flip-flop, causing single memory cycle NPR sequences to always be performed.

The SACK ENB H signal is always asserted at the output of gate E96, pin 8. This signal allows the SACK flip-flop to be cleared when the RH11 becomes bus master and allows NPR arbitration to occur on the Unibus.

6.12.10 BUS HOG Mode

In BUS HOG mode, the RH11 desires to hold onto the Unibus to transfer the total number of words indicated in the word counter. This feature is only employed on Unibus B if this bus is dedicated and no other devices are connected to it. Its purpose is to reduct the NPR latency time of the Unibus. The RH11 enters BUS HOG mode by doing the first NPR cycle and holding the Unibus by asserting BBSY until the required number of words have been transferred or an error condition occurs.

The MSYN inhibit conditions (Paragraph 6.12.4) locks the Unibus cycle timing with the Silo buffer word rate.

To implement BUS HOG mode, the jumper in zone D-2 is cut which enables gate E98. If Unibus B is selected, the gate is qualified, and BUS HOG L is asserted. This signal forces the NEXT CYCLE flip-flop set, indicating another cycle is to be performed. With this flip-flop set, CLR BBSY L is inhibited (except if a UPE or WCE error is raised at END CYCLE time). In addition, BUS HOG L is applied to gate E98, causing a low input to be applied to the D-input of the CYCLE COUNT flip-flop. This overrides the toggling action from pin 6 of the CYCLE COUNT flip-flop and prevents the flip-flop from counting cycles. However, it still allows errors (TRE) or word count overflow to terminate the cycle.

NOTE

The "1 CYCLE" jumper must not be inserted and BUSB must be selected to implement the BUS HOG mode of operation.

6.13 LOGIC DIAGRAM DBCB

This diagram contains the logic used to transfer data into IBUF and from IBUF into the Silo (Silo input logic). Also, the diagram contains the logic used to clock data out of the Silo and into OBUF (Silo output logic).

6.13.1 Silo Input Logic

Data is supplied to IBUF as a result of one of the following conditions:

a. During a Write command – In this case, WRITE H and MSYN WAIT (1) H are asserted which qualifies gate E72, and causes the output of E72, pin 11 to go high for 75 ns. The effect of this is described in subsequent paragraphs. Signal MSYN WAIT (1) H is a 75 ns pulse which occurs during every Unibus cycle. The positive-going leading edge of this pulse is used to clock data off the Unibus during a Write (WRITE H) command. The data is transferred to IBUF, bubbled through the Silo into OBUF, and is written on the drive.

b. During a read or write-check operation – In a read operation, the synchronous data from the Massbus is clocked into IBUF, bubbled through the Silo into OBUF, and then to the Unibus. In a write-check operation, the synchronous Massbus data is clocked into IBUF, bubbled through the Silo into OBUF, and then to a series of Exclusive-OR gates where it is compared to the corresponding memory location from which it was written. The READ + WR CHK H signal is asserted during a read or write-check operation and is ANDed with 150 ns pulse in gate E77 to initiate this action. The 150 ns pulse is produced by one-shot multivibrator E58 which is triggered by the positive-going trailing edge of DRIVE CLK H signal (zone D-7). Also, when an exception condition is detected (error condition in the device), a special stop word is inserted into the Silo to allow all previous data words in the buffer to be transferred before signaling the RDY state. The positive-going trailing edge of EXCP L, which is an exception condition at EBL time, will fire the 150 ns one-shot. Either of these two conditions mentioned above will cause E72, pin 11 to go high for 150 ns.

c. When the program is loading data in the Silo – This function is used during maintenance and allows the data buffer to be read from or written into by the program. To accomplish this, REG STR H and DB IN H are both asserted. When this occurs, both inputs to the lower AND gate of E77 are high which cause the output of gate E72, pin 11 to go high for 125 ns. The REG STR signal allows the RH11 or one of the device registers to be written into. In this case, the register specified is the data buffer as designated by the DB IN H signal.

Consequently, the three situations described above cause the output of E72, pin 11 to go high for 75 to 150 ns, depending on the condition causing the output. This pulse is designated CLK IBUF H and clocks the data from the data lines into IBUF. IBUF is shown on logic diagrams DBCC and DBCD. The output of E72, pin 11 also direct sets the IBUF FULL flip-flop via inverter E82, pin 10.

When the trailing edge from E82, pin 10 goes positive (75 to 150 ns after the negative-going leading edge), the BUBBLE IN flip-flop is set.

The width of the pulse at the output of E72 is sufficient to guarantee that the data is clocked into IBUF and has adequate time to be clocked into the Silo. In other words, the pulse width ensures that the data has time to be propagated through IBUF.

When the BUBBLE IN flip-flop sets and the Input Ready signals (IR5 through IR1) are asserted, a SHIFT IN H signal is generated which allows the data to be shifted into the Silo (see gate E78, pin 4). Signals IR5 through IR1 originate from the five parallel ICs which comprise the 18-bit data word. When IR5 through IR1 is asserted, it means that the Silo is ready to accept data from IBUF. The Input Ready signals are guaranteed to have a certain width to comply with the specification of the Silo.

When the Input Ready signals are no longer asserted, the output of E62, pin 8 goes high and clocks the IBUF FULL flip-flop clear since the data has been accepted by the Silo. The output of IBUF FULL, in turn, clears the BUBBLE IN flip-flop. The Input Ready signals, when not asserted,

indicate that the data need not be stored any longer in IBUF and sufficient time has ensued to strobe the data into the Silo. After the data has bubbled out of the first cell in the Silo, the Input Ready signals once again are asserted. Consequently, these signals are asserted when an empty data cell exists at the bottom of the Silo buffer. This timing sequence of INPUT RDY and the movement of data in the Silo is all accomplished in the 3341 Silo IC.

NOTE

The time required for a data word to propagate from the bottom cell to the top cell in the Silo is specified from 0 to 32 μs. For an empty Silo, the typical time is 16 μs but may vary between Silos due to internal characteristics.

DLT IN

When inputting data to the Silo, a DLT (data late) error can be raised in one of the following two instances:

a. If a word is stored in IBUF [IBUF FULL (1) H] and a second word is to be loaded from the Massbus into IBUF during a Read or Write-check command, the DLT IN flip-flop is set. The READ + WR CHK signal is ANDed with a 150 ns pulse derived from DRIVE CLK (or EXCP for the stop word case) and is applied to the clock input of DLT IN. The data input monitors the IBUF FULL flip-flop and, if IBUF is full, DLT IN is set. The 0 output of DLT IN causes DLT to be created at the output of E72, pin 8. This condition would occur if the Unibus latency time is increased to the point where the Unibus cannot accept data from the Silo at a fast enough rate.

b. A maintenance feature is provided in the DLT logic. The program can load 66 words in the DB register, thus filling IBUF, the Silo, and OBUF. The next word that is loaded in IBUF simulates a DLT error which is posted in bit 15 of CS2. This condition is implemented by DB IN H and REG STR H signals being asserted which cause the DLT IN flip-flop to be clocked to a 1 when IBUF FULL is asserted. As a result, a DLT error at E72, pin 8 is raised.

   A third condition causes the DLT IN flip-flop to set when performing any of the data transfer commands over BUSB. If NPR transfers are being done on Unibus B and the processor issues an initialize pulse or a power fail occurs on Unibus B, a CLRB H signal is asserted and is applied to gate E79. The other two inputs to NAND gate E79 are SEL BUS A L (which indicates BUS B is selected when unasserted) and RDY L (which indicates that the RH11 is busy when unasserted). If all three inputs are asserted, the DLT IN flip-flop is set, causing a DLT error to be asserted.

   The DLT error, in this case, does *not* mean that IBUF is full and cannot accept another word but *does* mean that additional transfers cannot be done due to the power fail or initialize condition.

6.13.2 Silo Output Logic

The Silo output logic clocks data words out of the Silo and loads them in OBUF, where they can be transferred to the Unibus (Read command), to the drive (Write command), or to the Exclusive-OR gates in the controller (Write-check).

The output ready signals from each of the five parallel Silo chips are asserted when a data word bubbles to the top cell in the Silo. The output of gate E59, pin 8 is driven low when the output ready signals are asserted. This action causes ORDY H to be asserted at the output of inverter E61, pin 8, indicating a word has bubbled to the top of the Silo. In addition, a SHIFT OUT H signal is asserted provided BUBBLE OUT flip-flop is set. When OBUF is empty, the OBUF FULL flip-flop is cleared which sets the BUBBLE OUT flip-flop which, in turn, qualifies gate E78, pin 1 to enable SHIFT OUT H to be developed. The SHIFT OUT H signal is applied to the Silo and causes the word in the top cell to be transferred out of the Silo. In addition, the SHIFT OUT signal fires one-shot multivibrator E58, pin 4 which creates a 45 ns negative-going pulse used to deskew the data at the output of the Silo before it is loaded into OBUF. The positive-going trailing edge of the SHIFT OUT signal fires one-shot multivibrator E70. The negative-going edge from E70, pin 4 creates a second 45 ns pulse which is used to generate CLK OBUF H. CLK OBUF H loads the data word from the Silo into OBUF. The positive-going pulse from the 1 side of E70 generates SET OFULL L if EXC STOP has not been asserted. The SET OFULL L signal direct sets the OBUF FULL flip-flop, indicating that OBUF is presently storing a valid data word.

NOTE

If OBUF is full, the OBUF FULL flip-flop is set and the BUBBLE OUT flip-flop is cleared. This condition inhibits the SHIFT OUT signal from clocking the top cell in the Silo.

When the Output Ready signal becomes unasserted due to one of the five parallel Silo chips responding to the SHIFT OUT signal, gate E59, pin 8 is driven high. As a result, the SHIFT OUT signal is terminated and the BUBBLE OUT signal is cleared because OBUF FULL has been set and has removed the direct set on the BUBBLE OUT flip-flop. The purpose of the BUBBLE OUT flip-flop is to enable the completion of the SHIFT OUT signal after data has been clocked into OBUF and OBUF FULL has been set. When the next word bubbles to the top of the Silo, the word will not be clocked into OBUF since the BUBBLE OUT flip-flop is clear which inhibits the SHIFT OUT signal from shifting the word out of the Silo.

Consequently, the OBUF FULL flip-flop must be cleared in order that the BUBBLE OUT flip-flop becomes set and allows SHIFT OUT pulses. When this occurs, the data in OBUF is automatically written over by the next data word bubbling out of the top of the Silo. The OBUF FULL flip-flop can be cleared under the following conditions:

a. When the program is reading the Data Buffer register. After the program reads the data buffer, the next data word is allowed to sequence to the top. This logic is shown in NAND gate E75, pin 6. The DB OUT H signal occurs when the data buffer is read, and the DB OCLK H signal occurs when the RH11 asserts SSYN for that register operation. When the master device removes MSYN and the RH11 is deselected, the DB OCLK signal is unasserted, causing a positive-going edge at the clock input to OBUF FULL. This indicates that the RH11 does not have to store the data any longer and OBUF FULL is clear.

b. When the RH11 is doing a write operation (memory-to-drive transfer). This condition is implemented by the WRITE H and DRIVE CLK H signals at the input to NAND gate E75, pin 3. Signal WRITE H denotes a write operation. Upon the assertion of DRIVE CLK H, NAND gate E74, pin 3 goes low and the drive clocks the data off the Massbus.

   On the trailing edge of DRIVE CLK, E75, pin 3 goes high to clock the OBUF FULL flip-flop clear, and allows the RH11 to change the data on the Massbus.

c. When the RH11 is doing a read (drive-to-memory transfer) or write-check operation where the output of OBUF is applied to the Exclusive-OR gates in the controller. In this instance, READ + WR CHK H and DATA STROBE are applied to gate E76. Signal READ + WR CHK H, when asserted, denotes a read or write-check operation; signal DATA STROBE H, when asserted, drives the output of E76, pin 6 low. When DATA STROBE H goes unasserted, E76, pin 6 is driven high, clocking the OBUF FULL flip-flop clear and allowing the RH11 to change the data on the Unibus. If WCE (Write-Check Error) is detected, the data word in OBUF is frozen by forcing gate E76, pin 6 low which keeps the clock input to OBUF FULL low.

DLT OUT Flip-Flop

DLT OUT flip-flop E73 is shown in zone D-2. This flip-flop is clocked by OUT CLK L which goes positive on the trailing edge of DRIVE CLK during a write operation (see gate E75, pin 3 in zone B-6). On the trailing edge of DRIVE CLK (SYNC CLK from the drive), the RH11 monitors the top cell in the Silo to determine if a word is there to output to OBUF. If a word is present, it is indicated on the trailing edge of DRIVE CLK by ORDY H being asserted, which inhibits DLT from being generated via gate E71. If ORDY is not asserted, indicating the absence of a word available for OBUF, and it is not the last word (LWRD asserted), the DLT OUT flip-flop is clocked to the Set state, thus enabling gate E72, pin 8 to post a DLT error.

The DLT OUT flip-flop can be direct set if DB OCLK H, DB OUT H, and OBUF FULL (0) H are asserted. Signal DB OCLK H is asserted at the time of MSYN; DB OUT H denotes a register select function is specified; and OBUF FULL (0) H indicates OBUF is empty. The setting of DLT OUT, in this manner, occurs when the program tries to read the Data Buffer register without a word available in it (OBUF). It allows the program to simulate the clocking of non-existent words out of OBUF in order to post DLT errors. This feature is used as a maintenance aid.

Generation of DRIVE CLK H

The DRIVE CLK H signal is asserted when the disk has rotated to the correct address and starts to transfer data to or from that address. At that time the drive issues SYNC CLK H, which is DRIVE CLK H if no error conditions are present (indicated by INH CLK L) and if the desired number of words have not been transferred as indicated by DRWC OFLO (0). As previously described, SYNC CLK signals originate at the drive. On the leading edge of SYNC CLK, the drive either accepts the data (Write) or prepares it for transfer to the RH11 Controller (Read or Write-Check).

On the trailing edge of SYNC CLK, the controller accepts the data (Read or Write-Check) or prepares the next word (Write). If word count overflow has not occurred (indicating more words are to be transferred) and if no error conditions are present, the SYNC CLK signal becomes DRIVE CLK in the RH11. This is accomplished through gate E68 in zone C-7.

6.13.3 Error Flip-Flop

If an error condition occurs in the controller or the drive, a TRE (Transfer Error) is posted. TRE (bit 14 of CS1) is applied to the data input of the ERROR flip-flop (zone B-7). The error condition sets the ERROR flip-flop when clocked by SYNC CLK which then causes an INH CLK assertion to prevent further DRIVE CLK signals. The purpose of synchronizing the TRE with SYNC CLK is to prevent spurious spikes from occurring on DRIVE CLK during detection of an error. The ERROR flip-flop is cleared by SILO CLR L which is derived from CLR + GO CLR.

6.13.4 Generation of INH CLK L

INH CLK L is asserted as a result of a TRE or DLT error. These error conditions are ORed in gate E71. INH CLK L prevents DRIVE CLK H from occurring and thus prevents the RH11 from accepting any more data words from the device.

6.13.5 SILO CLR Generation

The SILO CLR L signal is generated by CLR + GO CLR which triggers 400 ns one-shot multivibrator E92. The 400 ns provides the required pulse width to clear the Silo chip. The CLR signal occurs when the program sets the CLEAR bit (bit 5 in CS2) when a reset or Unibus initialize pulse is asserted, or when the power supply is failing which asserts the DC LO L signal on the Unibus. The GO CLR signal is asserted when a data transfer command is loaded with the GO bit asserted. There are two instances in which the pulse used to generate CLR + GO CLR L is too narrow (less than 400 ns) to clear the Silo: 1) when the program is loading the CLEAR bit and 2) when a data transfer command is loaded in CS1 with the GO bit asserted. In these cases, the CLR + GO CLR is applied to the one-shot which widens the pulse to 400 ns. The other conditions used to generate CLR + GO CLR L (reset, Unibus initialize, and DC LO) are applied to gate E98 to ensure full width of the clear condition. Signal SILO CLR is used to initialize the Silo and Silo control signals.

6.13.6 Write Clock

The WRITE CLK H signal at the output of AND gate E90, pin 6 is the SYNC CLK signal from the drive which is ANDed with the WRITE H signal. Signal WRITE CLK H is sent back to the drive over the Massbus and is used by the drive to clock data into its buffer during a write operation. The purpose of WRITE CLK is to ensure the proper deskew of data on the Massbus during write operations.

6.13.7 Gating Synchronous Data

The GATE SYNCD signal at the output of gate E63, pin 11 turns on the Massbus drivers, when asserted, and allows the data from OBUF to be gated on the Massbus synchronous data lines. This signal is asserted during a write operation if drive word count overflow has not occurred or an error condition has not been raised. If an error or drive word count overflow occurs before the end of a sector, GATE SYNCD H goes unasserted which disables the data drivers, causing 0s to be written in the remaining words in the sector by presenting all 0s on the synchronous Massbus data lines.

6.13.8 Data Requests (Write Command)

When requesting words from the Unibus during a write operation, the DATA REQ L signal must be asserted. This signal is transferred to the BCT module to initiate an NPR request on the Unibus. Signal DATA REQ L is asserted when IBUF is empty, provided there is no word count overflow or no TRE. This is shown in AND gate E68 (output pin 8) which feeds gate E67. The output of E82 is fed back to AND-OR gate E67 and serves to keep this circuit latched. The circuit will unlatch as a result of CLR BBSY L or RDY L. Signal CLR BBSY L occurs when the RH11 gives up the Unibus. After the first DATA REQ, subsequent DATA REQ signals are asserted by the SHIFT IN H signal fed to gate E67. The SHIFT IN signal anticipates the availability of IBUF to accept a data word from the Unibus.

6.13.9 Data Requests (Read or Write-Check)

The RH11 requests the Unibus by the DATA REQ signal which is used to initiate the NPR logic on diagram BCTH. The DATA REQ signal is asserted by the Silo output logic when OBUF FULL is set (indicating a word has bubbled up the Silo and into OBUF), there is no TRE (Transfer Error), and a READ + WR CHK command is specified. The logic is implemented in gate E68, pin 6. The output at pin 6 is applied to gate E67. The output of inverter E82, pin 6 latches gate E67 until unlatched by CLR BBSY L. Signal CLR BBSY L is generated at the end of the cycle in a single-cycle NPR or at the end of the second cycle when doing back-to-back NPR cycles.

6.13.10 NEXT SIGNAL (Write)

The NEXT signal shown in zone C-1, when asserted, causes back-to-back NPR cycles to occur. The DATA REQ L signal is keyed when the IBUF is empty or SHIFT IN

occurs. As soon as the RH11 gains control of the Unibus, it asserts BBSY, prepares to obtain the data word, and monitors Input Ready (IRDY). This is done at MSYN WAIT time. If IRDY is asserted, the NEXT signal is generated by AND-OR gate E76 (as a result of IRDY H and WRITE H both being asserted). This means that the bottom cell of the Silo is empty, and the RH11 will do a second NPR cycle before releasing the Unibus. If the NEXT signal is not asserted, it indicates that the bottom cell of the Silo is full. In this case, the single NPR cycle is completed, the bus is released, and the RH11 waits for SHIFT IN to be asserted to repeat the cycle.

6.13.11 NEXT SIGNAL (Read or Write-Check)

In order for the RH11 to initiate back-to-back NPR cycles, the NEXT L signal must be asserted. Signal NEXT L is asserted when OR5 through OR1 are asserted (indicating a data word in the top cell of the Silo) and READ + WR CHK H is asserted. Consequently, the RH11 monitors the leading edge of MSYN WAIT in the first memory cycle and determines whether there is a word in the top cell of the Silo (ORDY asserted). If there is, the NEXT CYCLE flip-flop is set on DBCA and back-to-back NPR cycles are done. If there is no word in the top cell of the Silo, NEXT L is unasserted to inhibit the next NPR cycle and CLR BBSY L is asserted which removes the latch keeping the DATA REQ signal asserted.

6.13.12 Word Count Increment (Write Command)

The INC WC gate below NEXT causes the word counter to be incremented if DESK MSYN is asserted. Consequently, each memory cycle causes the word counter to increment.

6.13.13 Word Count Increment (Read or Write-Check)

The INC WC L signal at the output of gate E77, pin 6 is asserted during a read or write-check operation when the SHIFT OUT signal is generated. This indicates a word is in OBUF ready to transfer and the word counter is thus incremented.

6.13.14 EXCEPTION ERROR (Write Command)

The EXCP ERR L signal indicates that an exception condition in the drive (any error set in the ER register) can be recognized and may cause TRE to set to end the operation. When performing a Write command, EXCP SAVE (1) H immediately causes EXCP ERR L to be asserted.

6.13.15 EXCEPTION ERROR (READ or WRITE-CHECK)

When performing a read or write-check operation and an exception condition is raised in the drive, it is desirable to finish transferring the data words which already exist in the Silo before returning to the Ready state. This is accomplished by inserting a stop word into the Silo upon detection of exception and waiting for the word to appear at the output of the Silo before raising the error condition as TRE and thus producing the return to RDY state.

The above operation is performed by causing a 150 ns pulse to be generated by one-shot E58 in zone D7 when the positive-going trailing edge of EXCP L occurs, which at the same time sets the EXCP SAVE flip-flop located on drawing DBCD. The 150 ns pulse creates an input clock to the Silo as previously described. The EXCP SAVE condition is then inserted in the 20th bit position of the Silo and begins to bubble to the top as does a normal data word. When this stop word reaches the top cell of the Silo, the EXCP STOP signal is asserted, indicating the last word in the Silo is or has been transferred on the Unibus. The Silo control then attempts to transfer this stop word into OBUF. However, the EXCP STOP signal diverts the 45 ns pulse from one-shot E70, pin 13 to cause EXCP ERR L and prevents the SET OFULL signal from setting OBUF FULL (an indication that means a valid data word exists in OBUF). If, however, the WC OFLO (1) condition is asserted when EXCP SAVE has been set, the EXCP ERR signal is immediately asserted, causing TRE to set as the RH11 returns to the Ready state.

NOTE

If another error occurs causing TRE to set, operations on the Unibus are halted and the RH11 will return to the Ready state with data words remaining in the Silo buffer.

6.14 LOGIC DIAGRAM DBCC

This diagram shows bits 11 through 0 of the DMX, IMX, IBUF, Silo and OBUF. For a Write command, the data is gated from the appropriate Unibus (DMX) to IMX, and then through IBUF, the Silo, and OBUF for transfer to the drive. For a Read command, the data from the drive is supplied to IMX from the Massbus and then to IBUF, the Silo, and OBUF for transfer onto the appropriate Unibus. For a Write-check command, the output of DMX (from the Unibus) is compared with the synchronous data at the output of OBUF (from the drive).

When the RH11 is bus master (NPC MASTER L asserted), the CSRA SEL BUSA signal is checked to determine which Unibus is selected. If CSRA SEL BUSA is asserted, Unibus A is selected; if the signal is not asserted, Unibus B is selected. If the RH11 is not master (NPC MASTER L unasserted), the DMX is selected to BUSA. If the RH11 is not performing a Read or Write-check command, IMX is selected to accept DMX rather than Massbus synchronous

data. In this case, the DMX and IMX are set up to only accept data from Unibus A regardless of the setting of the PORT SEL bit. Consequently, when the program is loading data into the Data Buffer register, the data originates from Unibus A. The clocking logic for the IBUF, Silo, and OBUF is shown on sheet DBCB.

6.15 LOGIC DIAGRAM DBCD

This diagram shows bits 17 through 12 of the DMX, IMX, IBUF, Silo, and OBUF. The description of these bits is similar to that described on sheet DBCC.

In addition to selecting the 18 data bits from the Unibus or Massbus, the IMX incorporates a parity bit. During a Write command, the parity bit is forced to 0 through the Silo and into OBUF. The parity bit generated by the drive during a Read or Write-check command is carried through the Silo, providing a parity check of the Silo logic as well as transmission over the Massbus. The parity logic associated with the Massbus is described in more detail on sheet PACA.

The EXCP SAVE flip-flop in zone A-5 stores the fact that an exception condition was received from the drive and is used as an input to the 20th bit position of the Silo. This input provides the stop word described previously on DBCA (EXCP ERR) which will appear as EXCP STOP when all data words in the Silo have been transmitted.

The top of sheet DBCD shows 18 Exclusive-OR gates used during a Write-check command. These gates compare the data in OBUF that was taken from the drive to the output of DMX which represents the corresponding memory word. The outputs of the Exclusive-OR gates are open-collector ORed such that if corresponding bits fail to compare, an error will be registered and is indicated by the setting of the WCE (Write-Check Error) flip-flop. This flip-flop checks the status of the open-collector Exclusive-OR gates at the time of the MSYN WAIT signal and is latched if an error is detected. The flip-flop remains in this state until the CLR ERR signal is asserted.

6.16 LOGIC DIAGRAM DBCE

This diagram contains the drivers and receivers (8838 transceivers) for the Unibus B data lines. The Unibus B drivers drive the data from OBUF onto the BUSB data lines. In order to enable the drivers, the RH11 must be bus master, Unibus B must be selected (SEL BUSA H not asserted), and a read function must be specified (DATA TO BUS L asserted).

The Unibus B receivers receive the data from the Unibus (BUSB D00 L through BUSB D17 L) and supply them to the RH11 where the signals are designated UNIB D00 H through UNIB D17 H.

Bits 16 and 17 of the Unibus B data which is normally the Unibus PA and PB lines are employed as data when the EN DATA BUSB L signal is asserted. This signal is asserted when Unibus B is selected (SEL BUSA H unasserted) and the 16 BIT BUSB jumper (W2) shown on sheet DBCH is cut.

6.17 LOGIC DIAGRAM DBCF

This logic diagram contains the drivers and receivers (8838 transceivers) for the Unibus A data lines. The pull-up resistors for the internal open-collector bus (BUSI) in the RH11 are also shown. This internal open-collector bus is used when the program is reading information from an RH11 register (or a drive register via the Massbus control lines) and is actually the output of the 8234 open-collector multiplexers which route information to the Unibus.

Data from BUSI (BUSI D00 OUT L through BUSI D15 OUT L) is supplied to the Unibus A drivers which drive these signals onto the Unibus where they are designated BUSA D00 L through BUSA D15 L.

Data from OBUF is applied to the Unibus via 8881 bus drivers. The 8881 drivers are enabled if the RH11 is bus master, if a read operation is specified (DATA TO BUS H asserted), and if Unibus A is selected (SEL BUSA H asserted).

Data from Unibus A (BUSA D00 L through BUSA D17 L) is supplied to the RH11 via the 8838 gates and is designated D00 IN H through D17 IN H in the RH11.

Bits 16 and 17 of Unibus A data which is normally the Unibus PA and PB lines are employed as data when EN DATA BUSA L is asserted. This signal is asserted when Unibus A is selected (SEL BUSA H asserted) and the 16 BIT BUSA jumper (W1) shown on sheet DBCH is cut.

6.18 LOGIC DIAGRAM DBCH

This diagram contains the parity jumpers for Unibus A and Unibus B multiplexer E21 to monitor parity, and four 8234 multiplexers to multiplex the Massbus control lines with the data buffer output.

6.18.1 Parity Jumpers

The lower portion of the diagram shows a parity jumper (16 BIT BUSA) for Unibus A and a parity jumper (16 BIT BUSB) for Unibus B. The operation of each is similar, so only the Unibus B parity jumper will be described. If the jumper is left in, gate E27, pin 8 is inhibited from generating EN DATA BUSB L, indicating that the upper two bits (D16 and D17) are to be used as parity bits (PA and PB). In addition, AND gate E28, pin 6 is qualified by the jumper for the selected bus being inserted which causes EN PAR H (enable parity) to be generated. When the 16 Bit BUSB jumper is cut, one input to E27, pin 9 is enabled. If Unibus B is selected, the output goes low, creates EN DATA BUSB L, and disables EN PAR which indicates that the upper two bits are used as data bits. The lower jumper and gate for Unibus A are the same except that the gate is qualified by selecting Unibus A and not Unibus B.

6.18.2 74157 Parity Multiplexer

Multiplexer E21 monitors the parity bits for Unibus A and Unibus B. The multiplexer is enabled by EN PAR H. A parity error is detected when parity bit PB is asserted and PA is unasserted. For example, if Unibus A is selected, D16 IN H (PA) is unasserted and D17 IN H (PB) is asserted, which causes pins 3 and 4 of gate E79 to be enabled. At DATA STR time, E79 is qualified generating SET UPE L (SET Unibus Parity Error).

6.18.3 8234 Control Line/Data Buffer Multiplexing

The 8234 multiplexers select the Massbus control lines or the outputs from OBUF for transfer to the RH11 internal open-collector bus (BUSI). When the program reads a remote register, the 8234 open-collector multiplexers gate the Massbus control lines (C00 IN H through C15 IN H) to the internal bus (BUSI). In this instance, the multiplexers are enabled by CNTL OUT L, which is the signal associated with reading a remote register. When the program is reading the data buffer for maintenance purposes, the data buffer outputs (OBUF 00 H through OBUF 15 H) are multiplexed onto the BUSI lines. The multiplexers are enabled by DB OUT L, in this case, which is the signal associated with reading the data buffer.

6.19 LOGIC DIAGRAM DBCJ

The logic diagram shows the START counter, two 8234 open-collector multiplexers which select the low byte of the CS1 or CS2 register onto BUSI, and a regulator circuit.

6.19.1 Start Counter

The Start Counter consists of two ICs (E64 and E65) connected in series. Each time a data transfer command is loaded in the RH11, the CLR + GO CLR signal resets the counter to 0. For a write operation, words are fetched from memory. Every word fetched is accompanied by DATA STR which clocks the counter and causes it to increment. A selectable count range may be selected to determine when the START signal is to be asserted which will cause the RUN assertion on the Massbus. This is done to prefill the Silo with data before requesting the drive to start to perform the write operation. A count of 64 is designated by the FULL jumper being connected. Other jumper configurations may be inserted. For example, if the HALF jumper is inserted, the START H signal will be asserted at a count of 32. If the QTR jumper is connected, the START H signal will be asserted at a count of 16. Only one jumper may be inserted at any given time and, with no jumper inserted, START will always be asserted allowing RUN to be asserted when the first word reaches OBUF (see CSRA). If a write operation is designated, the START signal generates RUN when the Silo is filled to the selected value. This connects the RH11 to the drive and signals the beginning of the data transfer on the synchronous Massbus.

6.19.2 CS1/CS2 Gating Onto BUSI

The two 8234 open-collector multiplexers select the low byte of the CS1 or CS2 register and gate the contents onto the internal bus (BUSI). Inputs from the CS1 register are gated onto BUSI when CS1 OUT is asserted and the inputs from the CS2 register are gated onto BUSI when CS2 OUT is asserted.

6.19.3 Voltage Regulator

This diagram shows a regulator circuit which converts -15 Vdc to -12 Vdc for use on the Silo chips. The 2N5639 FET is connected as a constant current generator to stabilize the bias current through Zener diode 1N759A. The 2N2409A transistor is used as the series pass element (regulator in series with the load current).

6.20 M7297 PARITY CONTROL MODULE (PACA)

The M7297 Parity Control module contains the parity logic for parity generation and checking both the synchronous and the asynchronous sections of the Massbus. Each drive contains associated parity generation and checking logic. Sheet PACA shows the Massbus parity logic, consisting of 74180 8-bit parity generator/checkers. The three 74180s on the left are used for parity on the synchronous Massbus and the remaining four 74180s are used for parity on the asynchronous Massbus. Parity on the Massbus is odd.

6.20.1 Synchronous Massbus Parity

The 74180 chips serve a dual function. During a write operation, the 74180 chips in the RH11 *generate* parity while the associated parity logic in the drive *check* parity. Conversely, during a read or write-check operation, the parity logic in the drive *generate* parity while the 74180s in

the RH11 *check* parity. This is possible with the same set of parity chips because in write, read or write-check operations the parity bit is rippled through the Silo along with the data word. This feature is useful because the parity bit also checks out the Silo logic as well as the Massbus.

The 18 data bits and the parity bit from OBUF are applied to the 3 74180 chips. This can be considered as a 19-bit data word. Each 74180 also has an ODD and EVEN input and a ΣEVEN and a ΣODD output. The EVEN input is normally low and the ODD input is normally high, selecting the 74180 for odd parity. The 19 data bits and the ODD input are summed to yield an asserted ΣEVEN or ΣODD output. For example, if all the data bits (18 data bits plus the parity bit) are asserted, the sum is odd. This is summed with the ODD input to yield an even number of 1s. Consequently, the ΣEVEN output is asserted and the disconnected ΣODD output is unasserted. As another example, if the 18 data bits are summed to yield an even number of 1s and the parity bit is unasserted, the result is even. This is summed with the ODD input to yield an odd number. In this case, the ΣEVEN output is unasserted.

6.20.2 Read or Write-Check Parity

Note that the ΣEVEN output is applied to the SYNC PE (Synchronous Parity Error) flip-flop and, if ΣEVEN is asserted, this disables the SYNC PE flip-flop from setting, indicating that there is no parity error. The SYNC PE flip-flop is used when checking parity during a read or write-check operation. The flip-flop is clocked during the trailing edge of DATA STR from the Unibus cycle if WRITE L is unasserted which occurs during a Read or Write-Check command. A third input to gate E5, which feeds the SYNC PE clock input, is the 0 output of the flip-flop which prevents the flip-flop from being clocked again. In this instance, the flip-flop is direct cleared by the CLR ERR L signal from sheet CSRB.

6.20.3 Write Parity

For a write operation, the 18 data bits and the parity bit are supplied to the drive to yield an odd number of 1s. To accomplish this, the 19th bit, designated OBUF PA H, is forced to a 0 so the 18 data bits (designated OBUF 00 through OBUF 17) determine whether the ΣEVEN output of the 74180 is asserted or unasserted. For example, assume that the sum of the 18 data bits is odd (the parity bit OBUF PA can be disregarded since it is a forced 0). These bits are summed with the ODD input to assert the ΣEVEN output. This inhibits gate E7, pin 8 from generating a sync parity bit (SYNC PA H), if the second input to this gate is temporarily disregarded. Since the data is an odd number of 1s, it is not necessary to generate a parity bit. If the data contains an even number of 1s, it yields an odd number when summed with the ODD input. As a result, the ΣEVEN output goes low generating a SYNC PA bit, which creates odd parity.

In the case where an error condition exists or word count overflow occurs prior to the end of a sector, the remaining words in the sector are filled with 0s. This is accomplished by disabling the data drivers on the Massbus with the signal GATE SYNCD (see sheet DBCB). As a result, the number of 1s is zero which is even. Consequently, a parity bit must be simulated to generate odd parity. This is accomplished by the GATE SYNCD input going unasserted. The situation just described only occurs for a write operation and, consequently, the driver that drives the SYNC PA signal on the Massbus is ANDed with the Write signal.

6.20.4 Asynchronous Massbus Parity

The two 74180 chips in the center of sheet PACA are employed for parity generation when writing into a register in the drive. The 16 data inputs to the chips are from the Unibus A data lines. Note that odd parity is normally selected.

Assume the data inputs contain an even number of 1s. This is summed with the ODD input to assert the ΣODD output which generates CNTL PA OUT H. This is the parity bit generation and is supplied to the Massbus driver for transfer to the drive. If the data inputs contain an odd number of 1s, the CNTL PA OUT H signal is not asserted and no parity bit is generated. When reading from a drive register, a different set of data lines is used and this necessitates two additional 74180 chips to check parity. The lines are the "C" IN lines which are the outputs of the receivers used to monitor the Massbus control information. The parity bit generated by the drive is supplied to the ODD input. The inverted polarity of the parity bit is applied to the EVEN input. The sum of the bits should be odd which means that ΣEVEN should be unasserted. For example, if the 16 data bits are all 1s and the parity bit generated in the drive is a 1, the sum of all bits is 17, which is odd. This causes ΣEVEN to go low, which inhibits NAND gate E5, pin 5 which, in turn, places a low at the D-input to the CNTL PE (control parity error) flip-flop. If the data inputs to the 74180 chips contain an odd number of 1s and the parity bit from the drive (CNTL PA IN H) is asserted (indicating a parity error), the ΣEVEN output is forced high which sets the CNTL PE flip-flop during the trailing edge of CNTL OUT L. This signal is the gating signal used to gate data from the Massbus control lines to the Unibus. When the CNTL PE flip-flop is set, it remains latched by the 0 output feeding the data input via gate E7, pin 3. The flip-flop is cleared in the same manner as the SYNC PE flip-flop by CLR ERR L.

NOTE

The second input to gate E5 is the AS REG signal. This signal inhibits checking parity when the Attention Summary (AS) register is being read. The reason that parity cannot be checked when reading the Attention Summary register is that the AS register in each drive provides only one bit of information and a parity check is meaningless.

The output of the SYNC PE flip-flop causes an MDPE (Massbus Data Parity Error) which appears in bit 8 of the CS2 register and also causes TRE (bit 15 of CS1) to be raised.

The output of the CNTL PE flip-flop causes an MCPE (Massbus Control Parity Error) which appears in bit 13 of the CS1 register and causes SC (bit 15 of CS1).

The PAT H signal can be asserted by the program (bit 4 in CS2) to generate even parity on the Massbus and to check for even parity on the synchronous data lines when performing Read or Write-check commands. This maintenance feature allows verification of the parity logic in the drive.

The M7297 Parity Control module contains two light-emitting diodes: one for control bus parity error and one for synchronous bus parity error. This allows the maintenance personnel to quickly detect whether the parity error occurred on the synchronous section of the Massbus or on the control (asynchronous) section of the Massbus.

6.21 M5904 MASSBUS TRANSCEIVER MBSA, MBSB, MBSC

The Massbus consists of three Massbus cables and associated Massbus transceiver modules. A 40-pin connector on each M5904 Massbus Transceiver module connects the Transceivers to the Massbus cables. The transceivers plug into slots C4-D4, C5-D5, and C6-D6 in the RH11 to connect the RH11 to the Massbus.

Each signal on the Massbus is applied to a differential circuit which transmits the true signal and an inversion of the signal along the bus. At the other end of the bus, the signals are received by differential receivers which output the true form of the signal. The differential circuitry serves to eliminate noise since any common mode noise will be cancelled at the differential receivers. For additional description, refer to M5904 Massbus Transceiver module in Appendix A.

The three Massbus cables are designated: Massbus Cable A (D-BS-RH11-0-02, MBSA) Massbus Cable B (D-BS-RH11-0-02, MBSB) Massbus Cable C (D-BS-RH11-0-02, MBSC).

The M5904 Massbus Transceiver is functionally shown within the dotted block on each drawing. The 40-pin connector is shown in the center of the dotted block. The differential transmitters which drive signals onto the Massbus from the RH11 are shown to the left of the connector. The differential receivers which receive signals from the Massbus are shown to the right of the connector. These signals originate at the drive and are routed to the RH11 via the differential receivers.

To minimize switching of signals on any transceiver module at a given time, the signals are grouped on different modules. For example, OBUF 00–05 H is contained on MBSA, OBUF 06–11 H is contained on MBSB and OBUF 12–17 H is contained on MBSC. The D00 IN H through D15 IN H signals from BUSA are also divided on the three modules in similar manner. The RSEL 0 H through RSEL 4 H signals are grouped on MBSA and MBSB.

The OBUF signals are gated by GATE SYNCD H which enables the output of OBUF to be gated onto the MASS 'D' lines of the Massbus. The D00 IN H through D15 IN H signals which form the MASS 'C' lines are enabled by GATE CNTL H which occurs when the RH11 is writing a remote register. GATE CNTL H is the assertion of DEV SEL and a DATO. The RSEL signals select a drive register and are enabled by the DEV SEL signal. Unit select signals U00 H through U02 H are also enabled by DEV SEL and specify one of eight possible drives. The remaining control signals which are supplied to the drive are also shown. These include WRITE CLK, RUN, DIR TRANS, MB INIT, DEMAND, CNTL PA OUT, SYNC PA, and SUPPLY AC LO.

The signals sent from the drive to the Massbus are SYNC D00 through SYNC D17 which represents synchronous data, and C00 H through C15 H which represents the contents of a drive register. Control signals which include EXCP, EBL, ATTN, SYNC CLK, CNTL PA IN, OCC and TRANS are also shown.

6.22 UNIBUS A CABLE DIAGRAM

The Unibus A cable diagram is shown on D-IC-RH11-0-03. Slots A1 and A9 are wired together as are slots B1 and B9. The slots are wired to provide UNIBUS A IN and UNIBUS A OUT signals, except for the GRANT signals. The GRANT signals are passed through the device before being supplied

to the Unibus out cable. The cable slots occupy slots A1, B1, and A9, B9 as shown in the Module Utilization Chart D-MU-RH11-0-01.

The three small peripheral controller devices are shown on the lower portion of the cable diagram. If the devices are inserted in the slots, the GRANT signals are passed from device to device. G727 Grant Continuity modules are inserted in any of these slots (D7, D8, or D9) not containing small peripheral controllers. The designated slots for the peripheral controllers are C7 through F7, C8 through F8, and C9 through F9 (see D-MU-RH11-0-01).

Also shown on the diagram is the M688 Power Fail driver which buffers the AC LO and DC LO signals and supplies them to Unibus A for power fail detection.

6.23 UNIBUS B CABLE DIAGRAM

The Unibus B cable diagram is shown in drawing D-IC-RH11-0-04. It is similar to the Unibus A cable diagram with the following exceptions:

1. The signals are prefixed by BUSB to denote Unibus B.

2. In Unibus A, the BUS GRANT signals are passed through the devices and are not directly wired from the UNIBUS A IN slot to the UNIBUS A OUT slot. In Unibus B, the BUS GRANT signals are directly wired from the UNIBUS B IN slot to the UNIBUS B OUT slot. The reason for this is that the RH11 cannot interrupt on Unibus B and, consequently, does not have to look at the BUS GRANT signals. Note that the NPG signal is not directly connected but is passed through the device on both Unibuses.

Unibus B has an M688 Power Fail driver similar to that on Unibus A. This is to assert BUSB AC LO or BUSB DC LO on Unibus B in the event of a power-fail condition.

6.24 M9300 UNIBUS B TERMINATOR

The M9300 Unibus B Terminator is shown in drawing D-CS-M9300-0-1. Three main functions performed by the M9300 are:

1. to properly terminate the Unibus cable
2. to arbitrate NPRs and issue NPGs
3. to prevent NO-SACK timeout.

6.24.1 NPR Arbitration and Issuance of NPG

In certain multiport memory configurations, Unibus B will be employed without a processor. In order for the RH11 to acquire bus mastership, it must issue an NPR and must receive an NPG signal. Since there is no processor to issue grants, the arbitration logic on the M9300 performs this function. The logic is shown on the left-hand side of the drawing. If the M9300 is connected at the beginning of the Unibus and no processor is connected to this Unibus, jumper W1 is cut. This enables the arbitration logic as described below.

The NPR requests are arbitrated by the M9300. If an NPR request is received (and BUS SACK is not present or has not been on the Unibus for 100 ns), the latch consisting of E2, pin 3 and E2, pin 6 is enabled. When the NPR request is received, pin 1 goes low forcing pin 3 high which, in turn, forces pin 6 low and enables signal BUS NPG H to be generated.

NOTE

If a BUS SACK signal and an NPR request are both received, pins 3 and 6 will both be high because the arbitration logic recognizes NPRs while SACK is asserted. In accordance with the Unibus specification, a GRANT signal cannot be issued until 100 ns after the SACK signal is removed. This logic is shown by gates E1, pin 14, E2 pin 11, E6 pin 3, 100 ns delay DL1, E5 pin 2, and E2 pin 6. When BUS SACK is asserted, E2 pin 6 is high and inhibits NPG H from occurring. After BUS SACK is unasserted for 100 ns, E2, pin 5 goes high to allow the grant to be asserted.

The NPR request, as previously described, generates the NPG H signal. In addition, however, it fires 10 μs one-shot multivibrator E4, pin 4 via gate E2, pin 6 If the BUS SACK signal is not returned within 10 μs, the one-shot times out and the positive-going trailing edge at E4, pin 4 clocks NO-SACK TIMEOUT flip-flop E3 set. The 0 output of this flip-flop goes low and simulates the BUS SACK signal since it is ORed with BUS SACK in gate E6, pin 3. The simulated BUS SACK signal performs two operations: 1) it clears the latch by causing E2, pin 5 to go low, and allows other NPRs to be arbitrated, and 2) after the 100 ns delay through DL1, it direct clears the 10 μs one-shot and the NO-SACK TIMEOUT flip-flop.

In addition to arbitrating NPRs, the M9300 must also simulate a processor when a power-fail condition is asserted. In this case, the device on the Unibus asserts BUS DC LO L. The M9300 receives this signal and returns BUS INIT L via gates E1, pin 2 and E8, pin 1. Note that BUS INIT L is only returned when jumper W1 is cut (no processor connected to Unibus). Consequently, the M9300 simulates the BUS INIT signal from the processor.

If the M9300 is connected at the beginning of the Unibus and there is a processor connected to the Unibus, jumper W1 is not cut. This places a low input at NOR gate E8, pin 5 which causes the output to go high. This output is open-collector ORed with the processor GRANT signal on the Unibus. In this instance, E8, pin 5 diables the arbitration logic in the M9300 from arbitrating NPRs. E8, pin 4 is effectively disconnected from the Unibus, and the processor does the necessary arbitration.

6.24.2 Prevention of NO-SACK TIMEOUT

The logic on the right-hand side of D-CS-M9300-0-01 is employed when the M9300 is connected at the end of the Unibus. The purpose of this logic is to monitor the BUS NPG and BUS GRANT signals and to issue BUS SACK which bypasses the 10 μs timeout logic used in the processor or in an M9300 module when employed as an arbitrator.

If a processor is connected to this Unibus, jumper W3 is cut. Since the M9300 is at the end of the Unibus, jumper W2 is also cut. With W3 cut, NAND gate E6, pin 8 is enabled to pass the BUS GRANT signals, and with jumper W2 cut, NAND gate E8, pin 13 is enabled to pass the BUS GRANT or the BUS NPG signal.

Consequently, any grant that reaches the end of the bus, and has bypassed the device requesting a grant, causes the BUS SACK L signal to be asserted. BUS SACK L is sent to the processor and causes the GRANT signal to drop which, in turn, causes BUS SACK to become unasserted.

The 10 μs timeout logic is overridden as follows. Assume a device issues a request and then suddenly clears it. The processor arbitrates the request and issues the grant, thinking it saw a valid request. The processor then times out for 10 μs waiting for BUS SACK. However, the logic just described causes BUS SACK to be asserted immediately, thus bypassing the timeout feature and improving interrupt response time of the Unibus.

If the M9300 is at the end of the Unibus and there is no processor connected to the bus, then only jumper W2 is cut. With jumper W3 in, the gate (E6, pin 8) which normally passes the BUS GRANT signals is inhibited. Since there is no processor to issue BUS GRANT signals, they have no meaning. These signals are open-collector signals asserted high and since there is nothing to assert them low, they appear as valid BUS GRANT signals on the Unibus. Therefore, jumper W3 is in which disconnects these signals from the Unibus by opening gate E6, pin 8. The BUS NPG signal can be asserted by a processor or another M9300 terminator at the beginning of the bus, thereby causing the SACK assertion. This is verified by the fact that NAND gate E8, pin 13 is enabled to allow the BUS NPG signal to assert BUS SACK.

If jumpers W1 and W2 are erroneously cut, the M9300 would function abnormally. To prevent this condition from occurring, both jumpers are applied to NAND gate E8, pin 10. If both jumpers are cut, E8, pin 10 is driven low causing a light-emitting diode to illuminate. This immediately indicates an illegal jumper configuration for maintenance purposes.

NOTE

If all three jumpers are in, the M9300 logic is bypassed and only the terminating resistors are utilized.

6.25 G727 GRANT CONTINUITY MODULE

If there are no small peripheral controllers installed in slots C7 through F7, C8 through F8, and C9 through F9, G727 Grant Continuity modules must be installed in slot D7, D8, or D9. These modules merely continue the BUS GRANT signals to the next device on the Unibus.

6.26 M688 POWER FAIL DRIVER

The M688 Power Fail driver is a single-height module which receives power fail signals from the power supply and asserts them on the Unibus. If Unibus B is utilized as a second bus, an additional M688 is required to assert power fail signals on this bus. Figure 6-5 is the M688 Power Fail module schematic. AND-NOR gates E1, pin 8 and E4, pin 8 and the associated inverters are not used in the RH11.

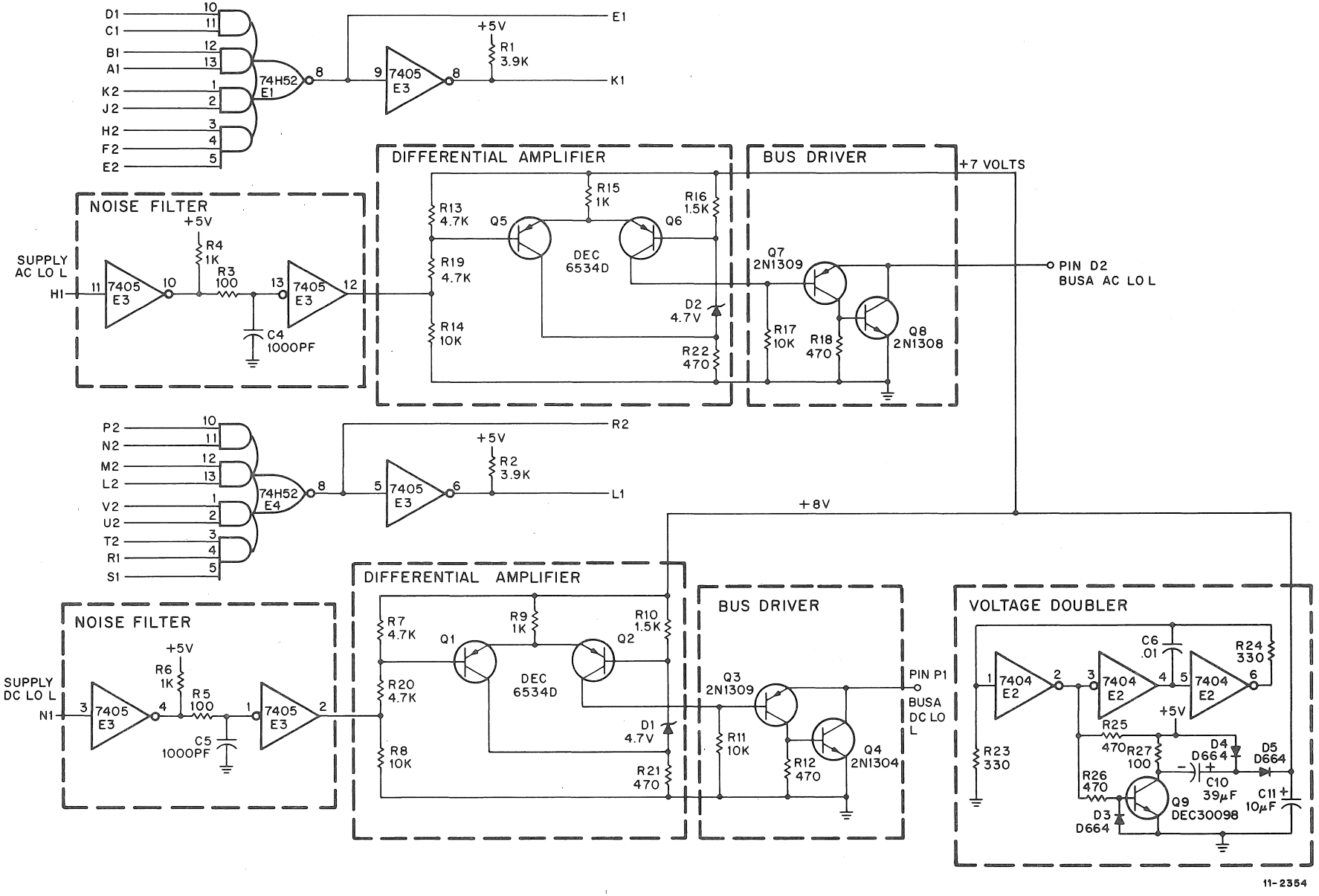


Figure 6-5 UNIBUS Power Fail Drivers Schematic

The schematic shows a noise filter, differential amplifier, and bus driver for two power fail input sources. Pin H1 is connected to the ac power fail line, and pin N1 is connected to the dc power line. When the input at pin H1 or N1 goes low, the output at pin D2 or P1, respectively, goes low. The input power fail signal is applied to a differential amplifier via the noise filter. The differential amplifier increases the voltage swing of 3 V (0 to 3 V) to 5 V (0 to 5 V), which is the voltage required to operate the bus driver. This circuit provides the drive necessary to supply the signal to the Unibus. The voltage doubler circuit increases the +5 V input to 8 V. This voltage is necessary to generate the +5 V required at the input to the bus driver circuit.

6.27 M5904 MASSBUS TRANSCEIVER MODULE

The M5904 Massbus Transceiver module contains nine differential driver chips (75113) and seven differential receiver chips (75107B). Each driver chip and each receiver chip is capable of carrying two signals. Thus, the chips can be designated dual drivers and dual differential receivers. The transmission line connected to the transceivers are bidirectional in that they can both receive and transmit information. This is illustrated for one signal line in Figure 6-6.

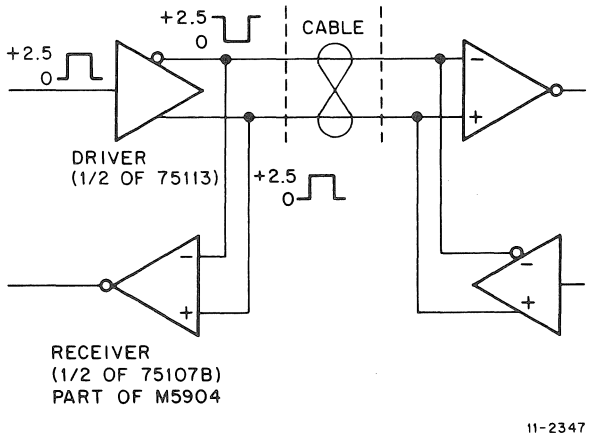


Figure 6-6 Typical Differential Driver/Receiver Connection

The advantage of differential circuitry is that any noise picked up is generally picked up on both the inverted and non-inverted signal lines. The differential receiver takes the difference between the signals regardless of the noise level, and the noise is effectively cancelled out.

Each driver on the M5904 must be terminated since the M5904 is used to drive transmission lines (Figure 6-7).

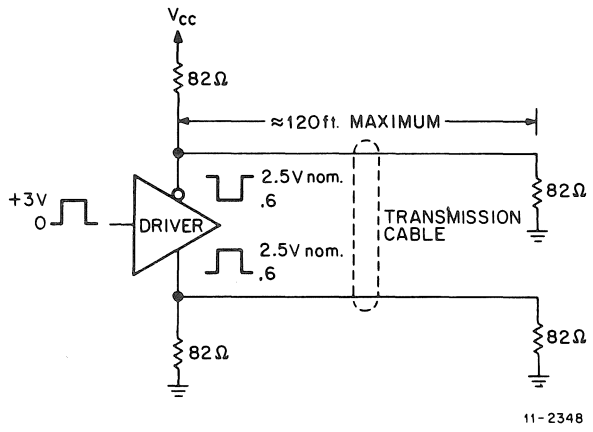


Figure 6-7 Driver Termination

The M5904 Massbus Transceiver requires input voltages of +5 Vdc and -15 Vdc. The dual drivers require +5 Vdc operating voltage while the dual differential receivers require +5 Vdc and -5 Vdc. The -5 Vdc is obtained from the -15 Vdc source via a resistor and Zener diode network.

6.27.1 75113 Dual Differential Driver Chip

The 75113 Tri-state Dual Differential Driver Chips provide differential outputs with high current capability in order to drive balanced lines. The chips feature a high output impedance making it possible to connect many drivers on the same transmission line. A simplified schematic of the 75113 is shown in Figure 6-8.

The inverting output of the driver chip is the transistor collector, while the non-inverting output is the transistor emitter shown at point B. When the input is low, neither transistor conducts and line A is biased to +2.5 V while line B is biased to 0 V by the terminator resistors (refer to diagram). When the input is high, the upper transistor collector is driven low (0 V) and the lower transistor emitter is driven high (+2.5 V). The pin connection diagram for the dual differential driver is shown in Figure 6-9.

6.27.2 75107B Dual Differential Line Receiver Chips

The 75107B Differential Receiver Chips feature dual independent channels with common voltage supply and ground terminals. The circuits operate as follows. If the voltage at pin 1 is positive with respect to the voltage at pin 2, the output at pin 4 goes positive (Figure 6-10).

If the voltage at pin 1 is negative with respect to pin 2, the output at pin 4 goes negative. The pin connection diagram for the receiver is shown in Figure 6-11.

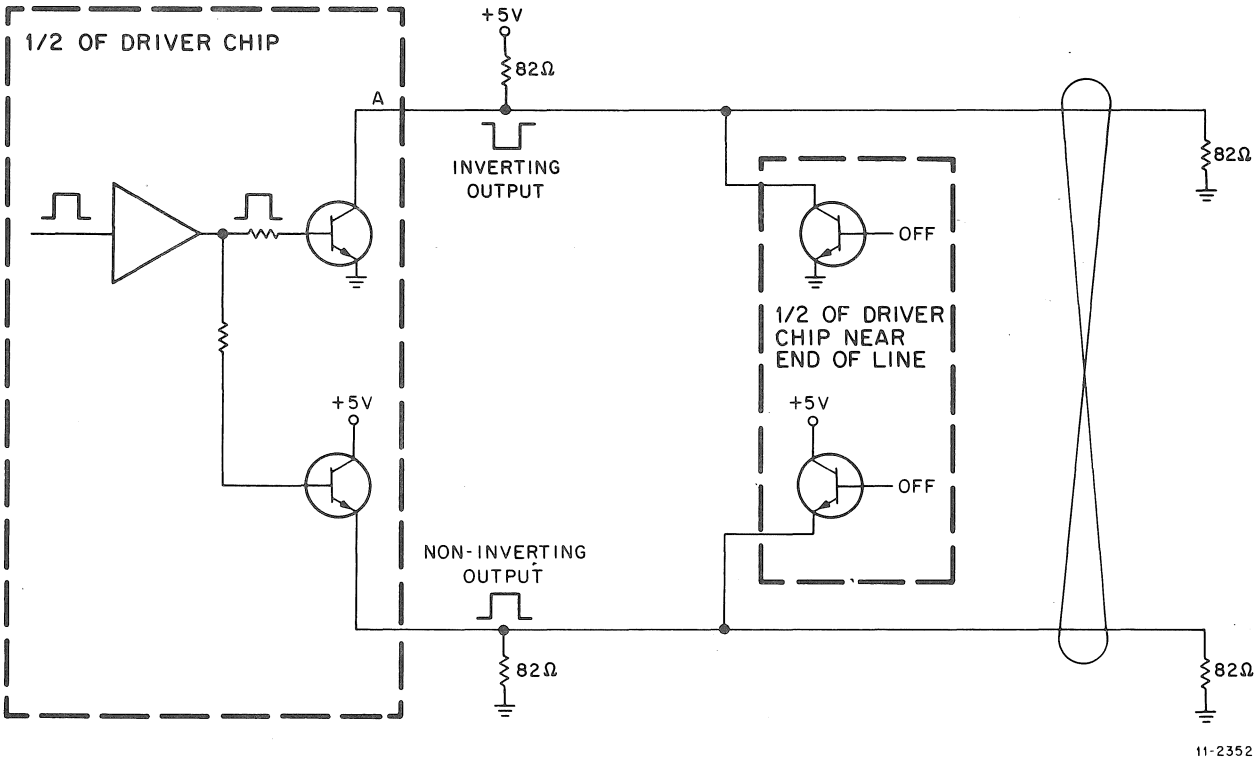


Figure 6-8 Driver Chip Simplified Schematic

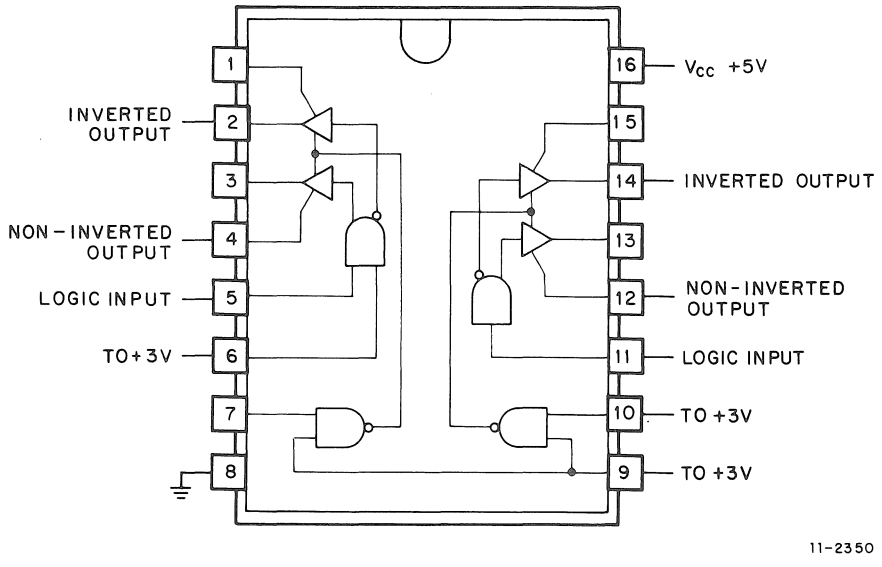


Figure 6-9 Dual Differential Driver Pin Connection Diagram

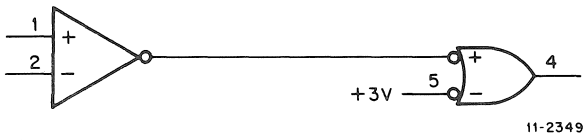


Figure 6-10 Simplified Line Receiver Logic Diagram

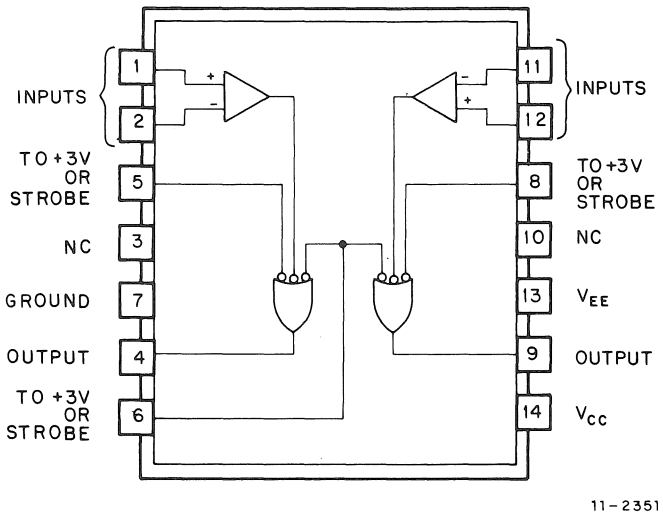


Figure 6-11 75107B Differential Receiver Pin Connection Diagram

6.28 7009938 TERMINATOR PACK ASSEMBLY

The 7009938 Terminator Pack Assembly provides a simple and reliable means of terminating the Massbus. This assembly is connected to the ZIF output connector of the last drive to terminate the three flat Massbus cables.

The Terminator Pack Assembly consists of three 14-pin dip packs containing 82 Ω terminating resistors.

6.29 M8838 UNIBUS TRANSCEIVER MODULE

The M8838 Unibus Transceiver module drives and receives signals on the Unibus. The module is a quad chip consisting of four Unibus drivers with common enables on pins 7 and 9 and four receivers which are always enabled. The pin connection diagram is shown in Figure 6-12.

6.30 UNIBUS TERMINATION

The terminating resistors for the Unibus comprise voltage divider networks necessary to properly terminate the Unibus. These resistors are similar to the terminating resistors on the M930 standard Unibus Terminator module.

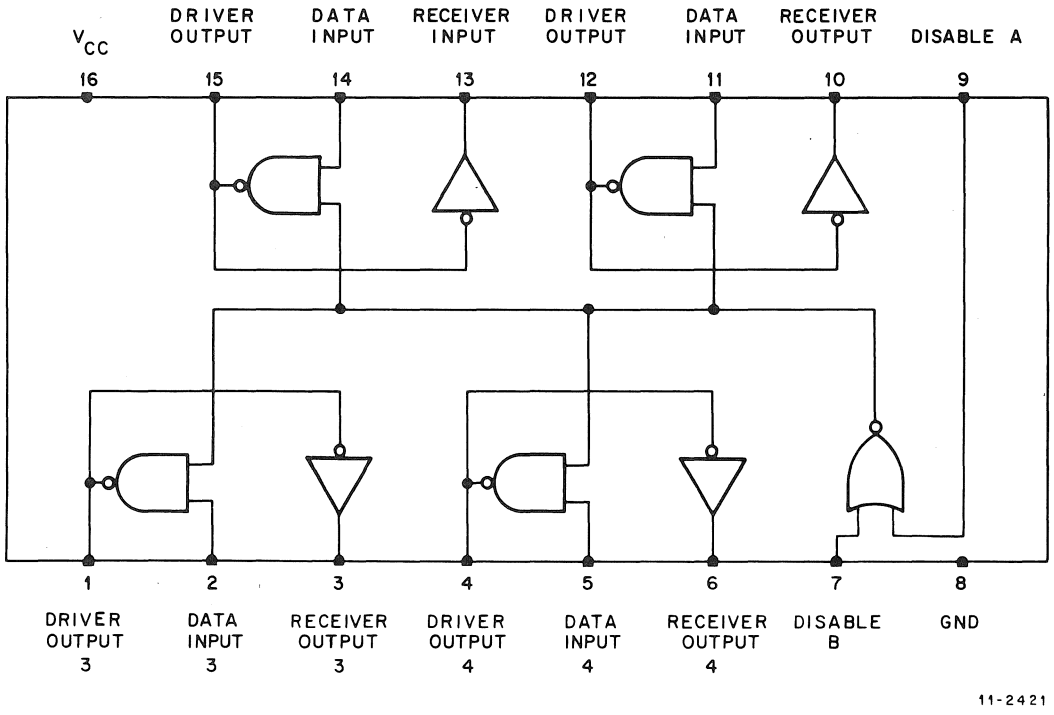


Figure 6-12 M8838 UNIBUS Transceiver Pin Connection Diagram

CHAPTER 7
INSTALLATION & MAINTENANCE

7.1 INTRODUCTION

This chapter describes the installation information required to install the RH11 as a Unibus device. The chapter also describes the preventive and corrective maintenance procedures that apply to the RH11 when connected to an RP04 Disk Drive.

A major point in the maintenance philosophy of this manual is that the user understand the normal operation of the RH11. This knowledge, plus the maintenance information contained in the *RP04 Device Control Logic Maintenance Manual,* will assist the maintenance personnel in isolating system malfunctions.

7.2 INSTALLATION

The following paragraphs describe the mechanical and electrical installation, power checks, jumper configurations, visual inspection, and diagnostics associated with the RH11. Refer to System Diagram E-SD-RP04-0-1 for system interconnection, module locations, power wiring, and single- and dual-port options.

7.2.1 Mechanical

The RH11 uses two hex-height modules and must be installed in a mounting box that accommodates hex-height modules. The modules are inserted in a double-system unit backplane which is installed in the mounting box with four thumbscrews. The double-system unit is oriented with the bus cable slots in line with the other options.

7.2.2 Electrical

The power cable connections, Unibus cable connections, and Massbus cable connections are described in the following paragraphs.

7.2.2.1 Power Cable Connections – Power is distributed to the RH11 modules via two power cables which attach to the printed circuit backplane assembly by quick-disconnect tabs. (Refer to RH11 Wired Assembly Drawing D-AD-7009397-0-0.) The power cables have Mate-N-Lok connectors on one end, which connect to the power distribution panel located above the backplane, and quick-disconnect tabs on the other end, which connect to the printed circuit backplane. The following chart shows the color codes associated with the power harness connections.

Red	+5 Vdc
Black	Gnd
Blue	-15 Vdc
Gray	+15 Vdc
Violet	DC LO (+3 V to +5 V)
Yellow	AC LO (+3 V to +5 V)
Brown	LTC 8 V peak-to-peak ac

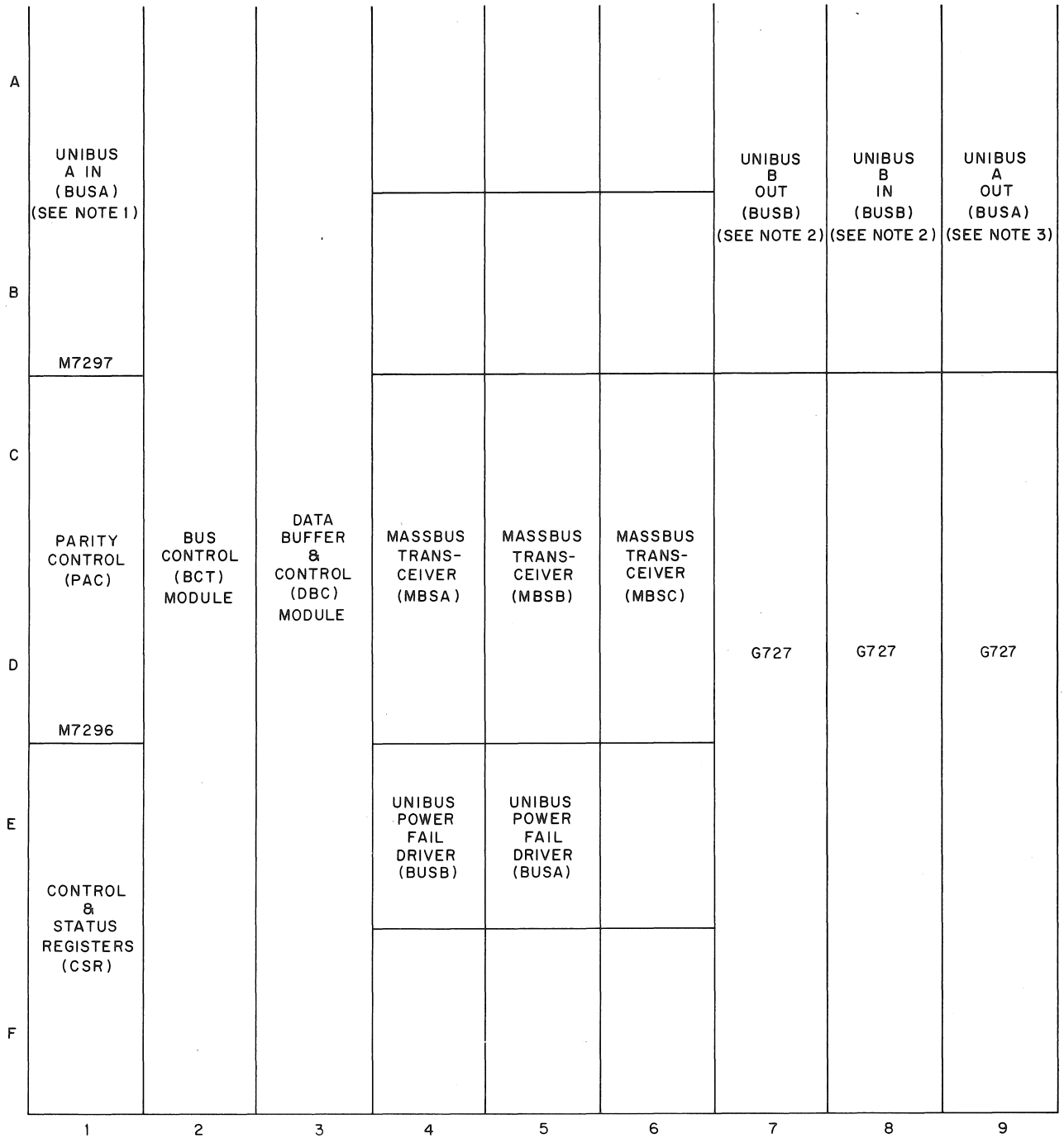
CAUTION

When connecting the power cables to the backplane, ensure that backplane wires are not damaged. Also, *do not cut* AC LO and DC LO wires out of the power harness as they are used for power fail conditions on the Massbus and on both Unibus A and Unibus B ports.

After power connections have been made, check for power shorts with an ohmmeter. Ensure that all modules are firmly seated in the proper slots (Figure 7-1). Power up the cabinet and measure voltages in accordance with values listed in the color code chart for power connections. After this is done, turn power off.

7.2.2.2 Unibus Cable Connections – The RH11 is a two-port Unibus device capable of accepting two Unibus cable systems, designated Unibus A and Unibus B.

Unibus A Connections – The Unibus A cable slots connect the RH11 to the processor controlling it. The Unibus A cable enters the RH11 via slot A1, B1 and connects to the next device via slot A9, B9. (Refer to Module Utilization Drawing D-MU-RH11-0-01.)



NOTES:

1. MAY BE EITHER M920 (CONNECTION FROM ADJACENT DEVICE) OR BC11A CABLE (CONNECTION FROM ANOTHER BOX OR NON-ADJACENT DEVICE).
2. MAY BE M9300 (TERMINATION AT BEGINNING OR END OF UNIBUS B) OR BC11A CABLE (CONNECTION TO OTHER BUS B DEVICES).
3. MAY BE M920 (CONNECTION TO ADJACENT DEVICE), M930 (TERMINATION AT END OF UNIBUS A), OR BC11A CABLE (CONNECTION TO NEXT BOX OR NON-ADJACENT DEVICE).
4. G727 GRANT CONTINUITY MODULE(S) MUST BE INSERTED IN SLOTS D.

11-2384

Figure 7-1 RH11 Module Utilization

Connections to slot A1, B1 are made via the BC11A Unibus cable if the RH11 is the first Unibus A device in the mounting box. Otherwise, connection to A1, B1 from the preceding device is made by an M920 Unibus Jumper module. Connection to the next adjacent device on the Unibus is made via the M920 Unibus Jumper module; it is made by a BC11A cable if the device is not adjacent.

NOTE

If the RH11 is the last device on Unibus A, an M930 Terminator module is installed in slot A9, B9.

Unibus B Connections – Unibus B connections are generally made in systems with multiport memories. When the Unibus B port of the RH11 is not used, an M9300 Terminator module (with jumper W1 cut) should be installed in slot A8, B8 to terminate Unibus B signals into the RH11. The second M9300 Terminator module should *not* be used in order to conserve power. If the Unibus B port of the RH11 is used, connections are determined on the basis of whether a processor is connected to Unibus B. These connections are described below.

a. Processor on Unibus B – If a processor is connected to Unibus B, it is electrically connected at the beginning of the bus. In this case, the M930 Terminator modules supplied with the processor are used for bus termination, and the two M9300 Unibus B Terminator modules supplied with the RH11 are not used.

NOTE

The M9300 Terminator may be used as a substitute for the M930 Terminator if the jumpers are selected correctly.

The Unibus B cable connection to the RH11 is made via slot A8, B8 with a BC11A cable. Connection from the RH11 to the next device is made via a BC11A cable connected to slot A7, B7. If the RH11 is the last device on the bus, the M930 or M9300 Terminator is installed in slot A7, B7 instead of the BC11A cable.

b. No Processor on Unibus B – If no processor is connected to Unibus B, a M9300 Unibus B Terminator module must be selected as an NPR arbitrator. If one RH11 is connected to Unibus B, the RH11 is electrically connected at the beginning of the bus with the M9300 selected to act as an NPR arbitrator. One M9300 Unibus B Terminator module is placed in slot A8, B8 of the RH11. Jumper W1 on this module must be cut to enable the arbitration logic. Connection to other devices on Unibus B, such as memory, is made via a BC11A cable connected to slot A7, B7. The second M9300 Unibus B Terminator module is installed in the last device on Unibus B. Jumper W2 is removed for terminating the Unibus with no processor connected.

NOTE

In this case, an M930 Terminator module can be substituted for the M9300 Unibus B Terminator in the last device slot. If more than one RH11 is installed, the user may have extra M9300 modules as a result of a particular configuration. Figures 7-2, 7-3, and 7-4 show typical Unibus configurations.

7.2.2.3 **Massbus Cables** – Massbus connections to the RH11 are made via three 40-conductor ribbon cables. These cables plug into three M5904 Transceivers in the RH11 and are designated Massbus Cable A, Massbus Cable B, and Massbus Cable C. The connections are made as shown below:

Massbus Cable A	Install in M5904 module in slot C4, D4.
Massbus Cable B	Install in M5904 module in slot C5, D5.
Massbus Cable C	Install in M5904 module in slot C6, D6.

The Massbus cables are marked and should be inserted per the individual cable markings. (Refer to Paragraph 2.7.) To terminate the Massbus, a 7009938 Terminator Pack assembly should be plugged into the output connector(s) of the last drive (Figure 7-5). The Massbus cable connections to the RH11 are as shown in Figure 2-2 (single-port systems) and Figure 2-3 (dual-port systems).

7.2.2.4 AC LO, DC LO – AC LO and DC LO signals from the RH11's power supply must be connected to the RH11.

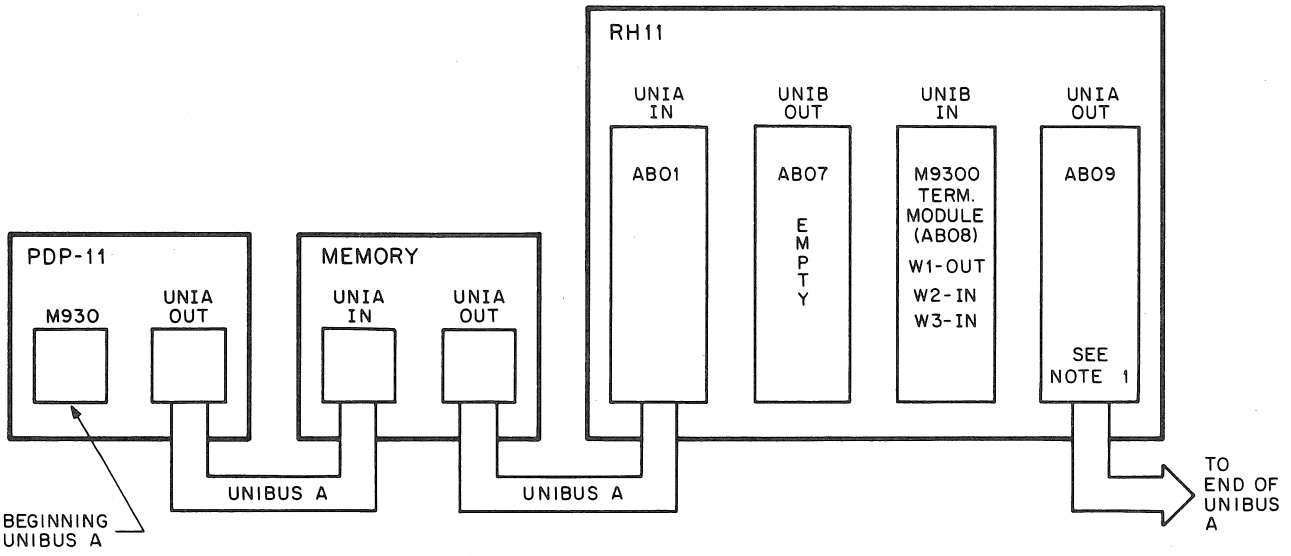


Figure 7-2 Single-Port Unibus Configuration

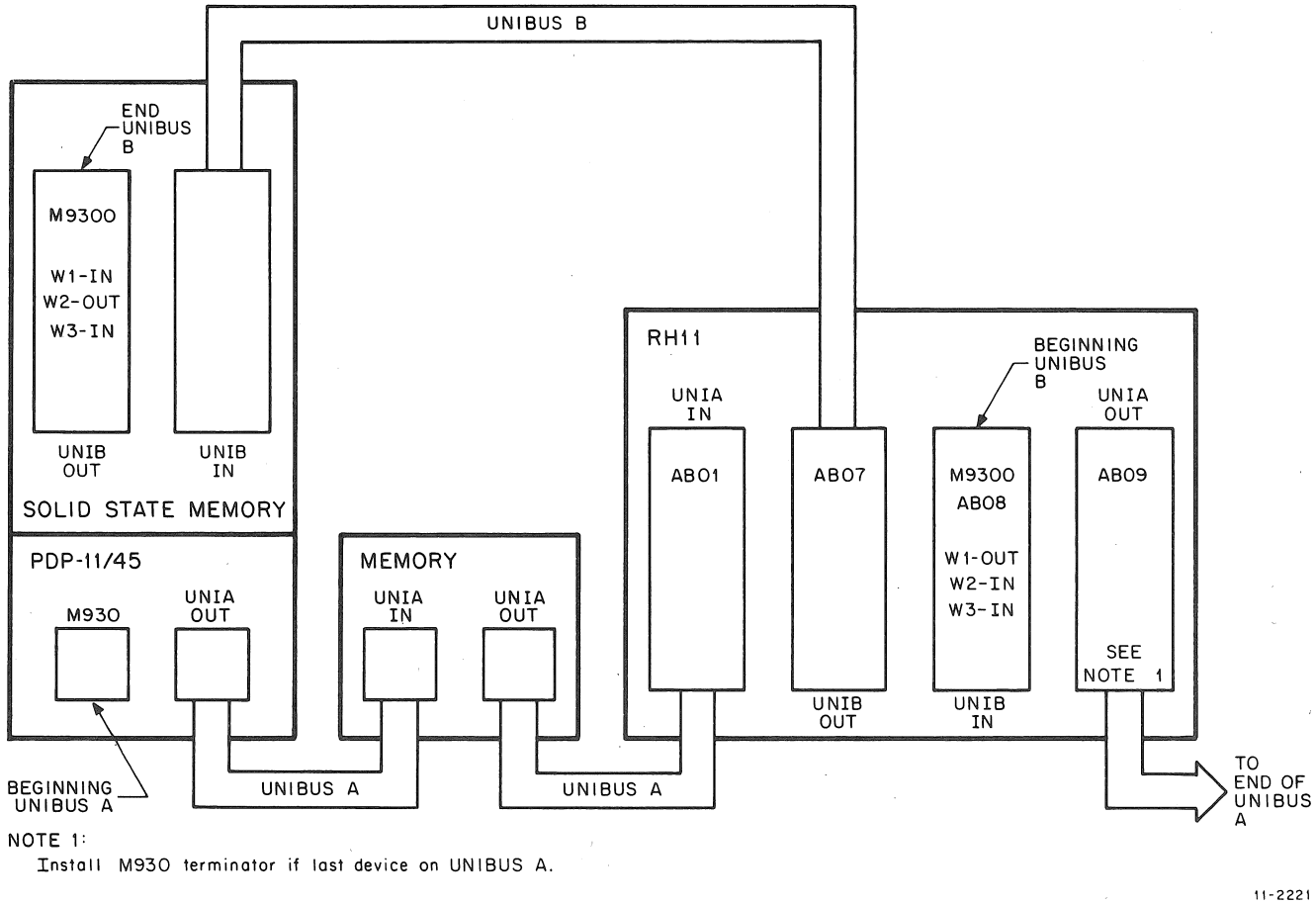
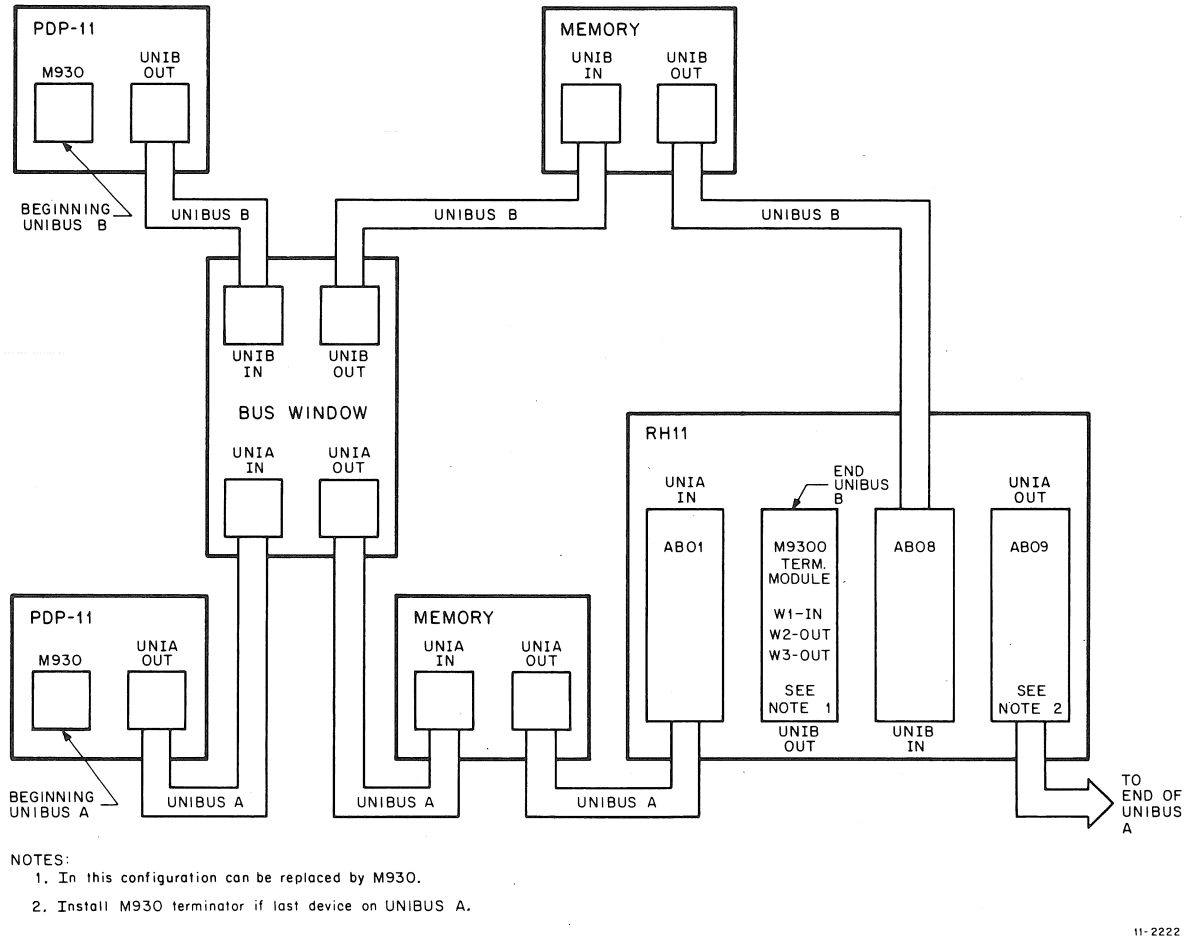


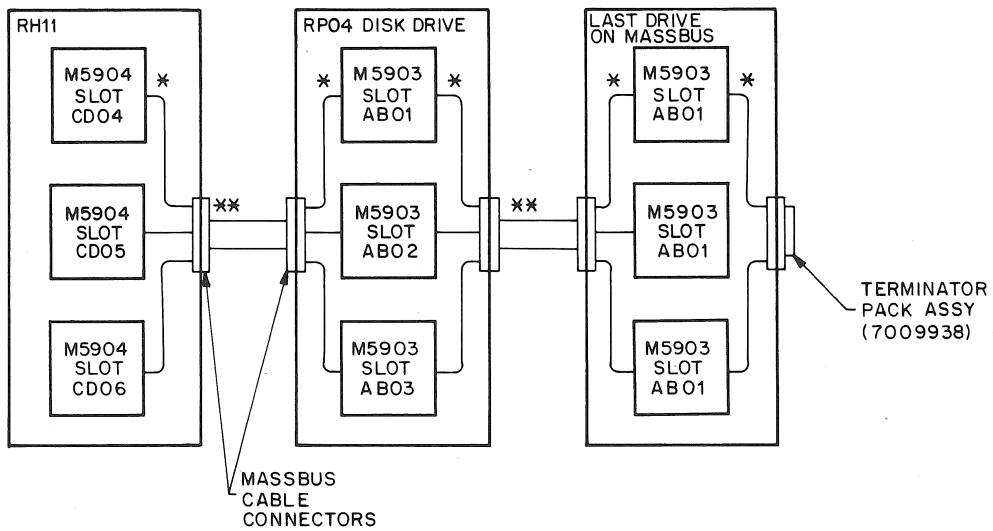
Figure 7-3 Dual-Port Configuration – Memory on Unibus B



NOTES:
1. In this configuration can be replaced by M930.
2. Install M930 terminator if last device on UNIBUS A.

11-2222

Figure 7-4 Dual-Port Configuration – Memory and Processor on Unibus B



NOTES:
* Flat massbus cable (3) internal to RP04 cabinet and to cabinet containing RH11.
** Round massbus cable external to cabinets.
1. Last drive terminated with 7009938 terminator pack assy.

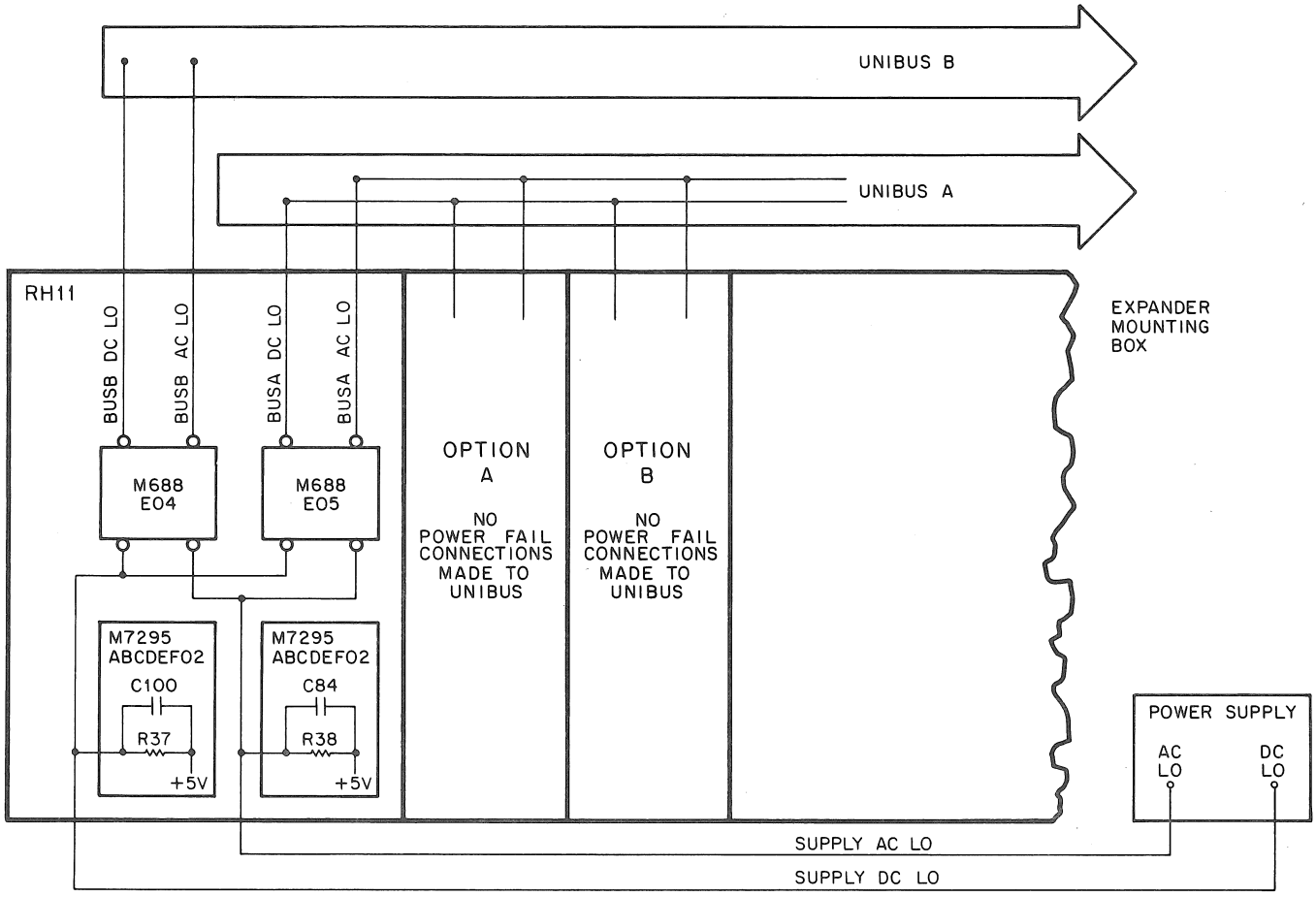
11-2561

Figure 7-5 Massbus Cable System Configuration

The wires supplying these signals *will not be cut* from the power harness. *There will be only one AC LO and one DC LO power fail connection to each Unibus for devices mounted in the same mounting box and sharing the same power supply.* Otherwise, power fail conditions would latch up due to positive feedback to the power fail logic. If a power fail connection for AC LO and DC LO is already made to a Unibus from a device in the same mounting box, the M688 Power Fail module in the RH11 for that Unibus is removed. The M688 module for Unibus A is located in slot E5 and the M688 module for Unibus B is located in slot E4. The following is a summary of power fail configuration rules.

1. For each mounting box, there is only one AC LO and DC LO power fail connection to a Unibus from the power supply.
2. Power supply AC LO and DC LO must always be wired to each RH11 via the power harness.
3. Power fail signals may only be disconnected from a Unibus in an RH11 by removing the appropriate M688 Power Fail Driver module.
4. Power supply AC LO and DC LO should be disconnected from all other options mounted in the same box as the RH11 if they do not need those signals for internal operation.

Figures 7-6, 7-7, and 7-8 show three typical power fail configurations which are configured in accordance with the above mentioned rules.



NOTE:
One RH11 mounted with other options in an expander mounting box.

11-2218

Figure 7-6 Typical Power Fail Configuration for RH11 and Options Mounted in Same Expander Box

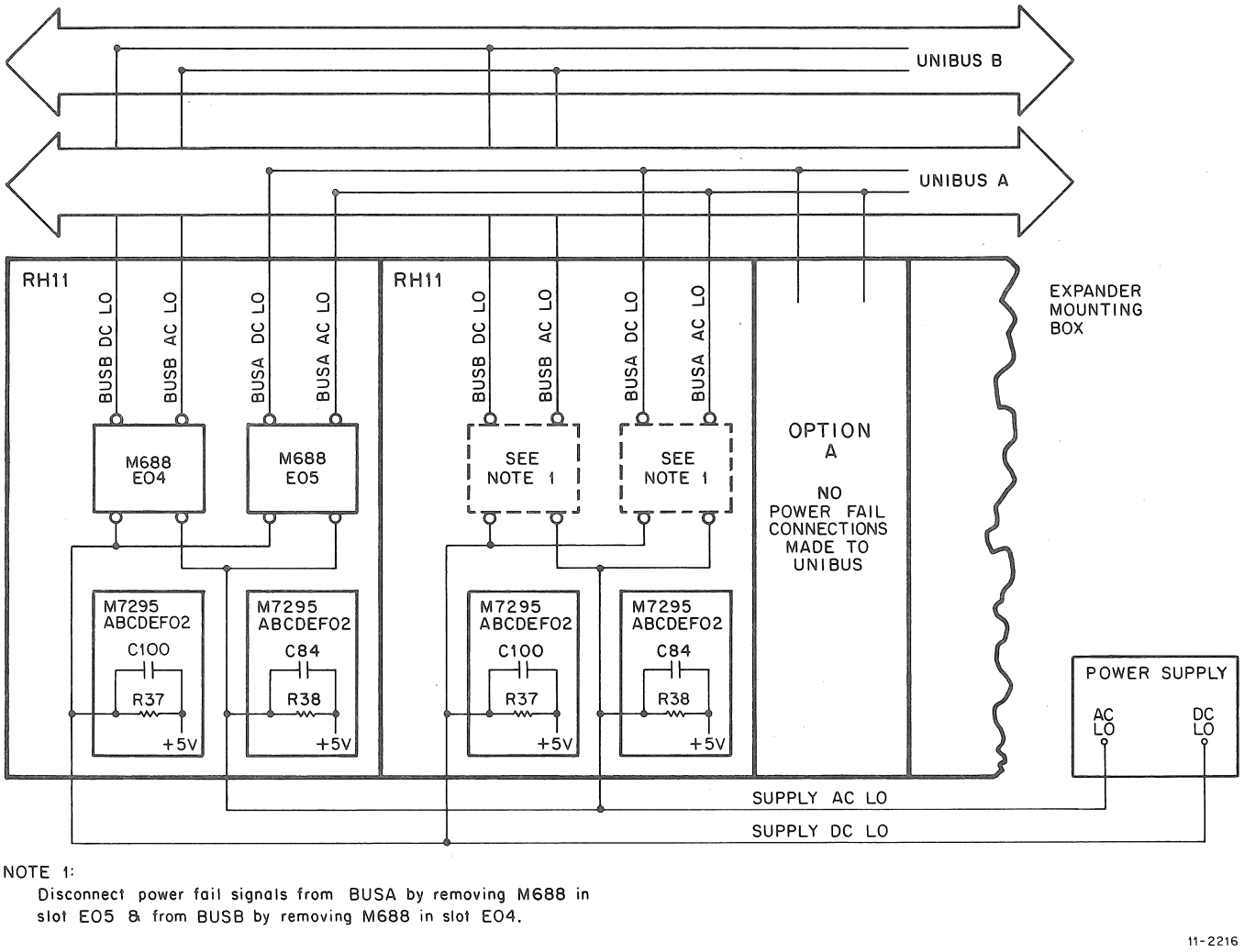


Figure 7-7 Typical Power Fail Configuration for Two RH11s Mounted in Same Expander Box

7.2.3 Jumper Configurations

The following paragraphs describe the various jumper configurations on the BCT (M7295), DBC (M7294), and the CSR (M7296) modules.

7.2.3.1 BCT Module – The BCT module contains jumpers for register selection, BR level interrupt, NPR latency, vector address, and missed transfer error.

Register Selection – The RH11 is capable of responding to 30 possible Unibus addresses. The number of addresses, however, is dependent on the Massbus device. For the RP04 Drive, the following jumper configuration should be used (D-CS-M7295-0-1, sheet 2).

Jumper in = binary 0

Jumper	Address Bit	Jumper In/Jumper Out
W1	12	OUT
W2	11	OUT
W3	10	OUT
W4	9	IN
W5	8	OUT
W6	7	OUT
W7	6	OUT
W8	5	IN

Jumpers W1 through W8 select the block of Unibus addresses to which the RH11/RP04 responds. The standard addressing block assigned is 776700 through 776746. If the jumper is left in, a binary 0 is encoded.

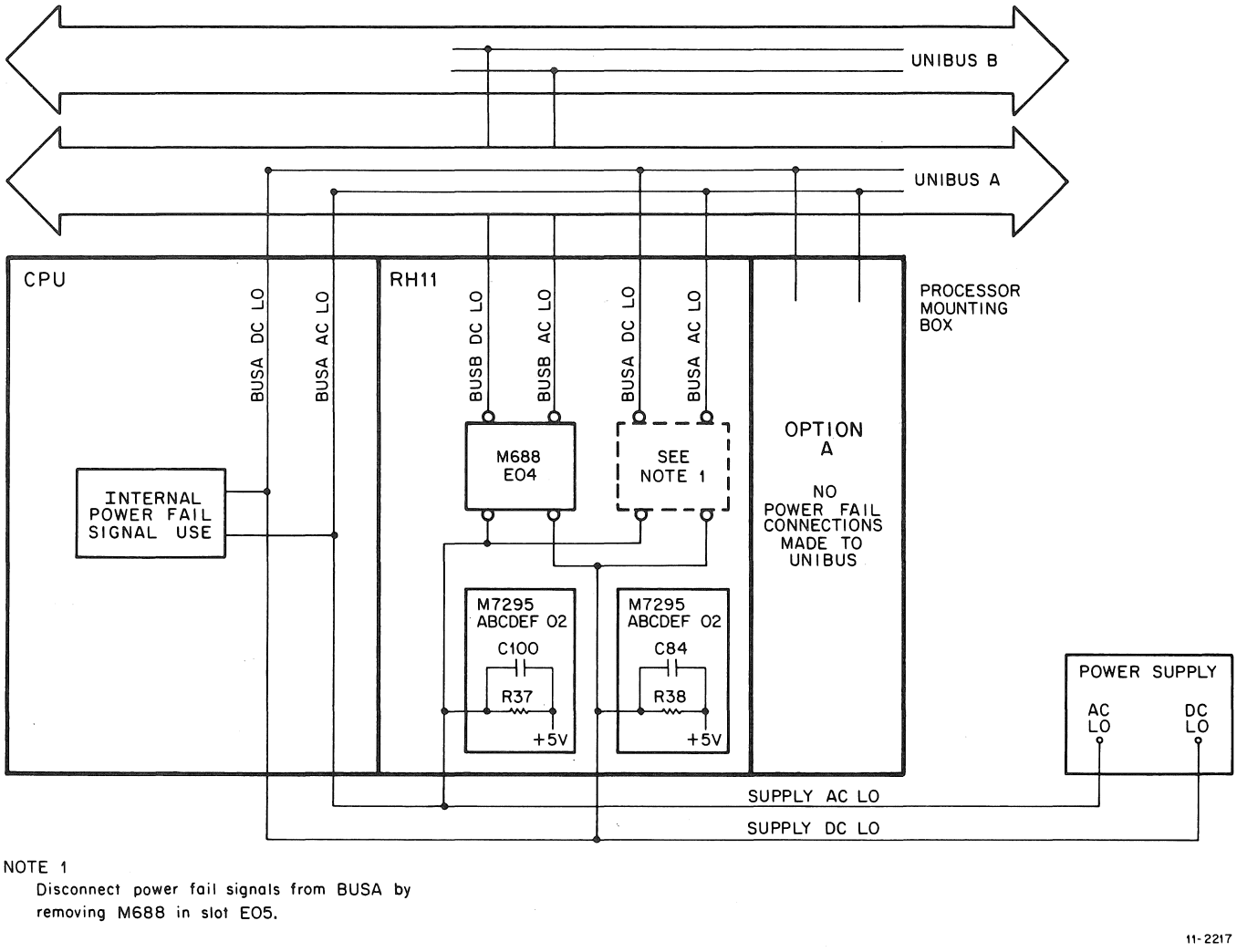


Figure 7-8 Typical Power Fail Configuration for RH11 and CPU Mounted in Processor Box

The jumpers in E3 (D-CS-M7295-0-1, sheet 2) are selected for the appropriate number of registers (20) in the RJP04 subsystem.

Slot	Jumper	Jumper In/Jumper Out
E3	1–16	OUT
	2–15	OUT
	3–14	IN
	4–13	IN
	5–12(2)	IN
	6–11(4)	OUT
	7–10(8)	IN
	8–9(16)	OUT

BR Level Interrupt – The priority jumper plug for the RH11 is normally set for the BR5 level. This plug is located in E57 (D-CS-M7295-0-1, sheet 7).

NPR Latency – Special circuitry is incorporated on the BCT module to improve NPR latency time for devices connected to the Unibus. This circuitry is enabled via jumper W18 (D-CS-M7295-0-1, sheet 7). When the jumper is left in, the NPR latency feature is enabled. Not all PDP-11 processors will work with this special feature.

Bus Grant – If there are no small peripheral controllers installed in slots C7 through F7, C8 through F8, and C9 through F9, G727 Grant Continuity modules must be

installed in slot D7, D8, or D9. These modules merely continue the Bus Grant signals to the next device on the Unibus.

Vector Address Jumpers – The interrupt vector transferred to the processor is jumper selectable via jumpers W11 through W17, representing vector bits 2 through 8, respectively. When a jumper is left in, a binary 1 is encoded. The RJP04 subsystems have been assigned a vector address of 000254. The jumper configuration for this address follows.

Jumper	Vector Bits	Jumper In/Jumper Out
W11	V2	IN
W12	V3	IN
W13	V4	OUT
W14	V5	IN
W15	V6	OUT
W16	V7	IN
W17	V8	OUT

MXF Jumper – Jumper W19 (D-CS-M7295-0-1, sheet 9) is used to disable detection of MXF errors and is used during special maintenance procedures. Normal operation requires that jumper W19 be left in.

7.2.3.2 **DBC Module** – The DBC module contains jumpers for NPR cycle selection, Unibus parity, and start counter capacities.

NPR Cycle Selection Jumpers – There are two jumpers used to select the type of cycle implemented when doing NPRs. Jumper E66 (3–14) (D-CS-M7294-0-1, sheet 2) selects the RH11 to perform one memory reference for each NPR request. In RJP04 subsystems, this jumper is removed to allow back-to-back memory cycles to occur.

Jumper E66 (2–15) (D-CS-M7294-0-1, sheet 2) takes advantage of dedicated Unibus B systems by allowing the RH11 to transfer complete consecutive blocks of data without giving up the Unibus. A dedicated Unibus B system is one in which the RH11 is used exclusively as a Unibus B master. To implement this feature (called BUS HOG mode), the one-cycle jumper and E66 (2–15) must be cut.

Unibus Parity Jumpers – The RH11 option can be selected for 16 data bit (plus two parity bits) transfers or 18 data bit transfers. Unibus A and Unibus B can each be selected individually via jumpers W1 and W2 (D-CS-M7294-0-1, sheet 8). Jumper W1, if left in, allows parity error code detection on Unibus A when the RH11 is doing DATI operations. If jumper W1 is removed, the Unibus A PA and PB parity lines are used as data bits 16 and 17, respectively. Jumper W2 serves the same function for Unibus B as jumper W1 does for Unibus A. The jumpers are normally left in.

Start Counter Jumpers – Different Silo fill capacities are jumper selectable before starting a write operation onto the disk drive. The jumper selections are listed below (D-CS-M7294-0-1, sheet 9).

Jumper E66, Pins 1–16	Selects full capacity of 64 words
Jumper E66, Pins 5–12	Selects 32 words
Jumper E66, Pins 7–10	Selects 16 words
No Jumper	Selects 1 word

NOTE

Only the jumper representing the desired Silo capacity should be connected. The other jumpers should be removed. For RJP04 subsystems, the 64-word jumper (E66, pins 1–16) should be connected.

7.2.3.3 **CSR Module** – The CSR module contains a jumper to allow for Unibus A selection only. The jumper is designated W1 and is shown on D-CS-M7296-0-1, sheet 2. The purpose of W1 is to override the ability of the program to select Unibus B data transfers; with jumper W1 connected, only Unibus A operations are allowed. The jumper is normally removed.

7.3 VISUAL INSPECTION

Before the diagnostics are run, the following visual inspections should be made.

1. Verify that all modules have been configured correctly in accordance with RH11 Module Utilization List D-MU-RH11-0-01.

2. Ensure that all modules are firmly seated in the system backplane assembly.

3. Inspect backplane wiring for broken wires or damaged pins. Repair or replace as required.

4. Ensure that the power cable is firmly attached to the Faston tabs on the system backplane assembly and that the Mate-N-Lok connector is seated firmly in the power distribution panel on the chassis.

5. Clean air filters at the top of the cabinet.

6. Ensure that all Unibus and Massbus cables are properly terminated and are firmly seated.

7. Check cabinet fans for proper operation.

7.4 DIAGNOSTIC MAINTENANCE

The diagnostic programs described herein are employed with the RJP04 subsystem. The following diagnostics are briefly described. Refer to the applicable diagnostic operating procedures for detailed information.

Test Programs

MAINDEC-11-DZRPI	RP04 Diskless Controller Test
MAINDEC-11-DZRPJ	RP04 Functional Controller Test
MAINDEC-11-DZRPK	Mechanical Read/ Write Test
MAINDEC-11-DZRPK	Mechanical Read/ Write Test
MAINDEC-11-DZRPP MAINDEC-11-DZRPQ	Dual-Port Logic Test (Parts 1 and 2)
MAINDEC-11-DZRPR	20-Sector Mode Logic Test (Diskless)

System Exerciser Programs

MAINDEC-11-DZRPN	Multidrive Exerciser

Utility Programs

MAINDEC-11-DZRPL	Formatter Program
MAINDEC-11-DZRPM	Head Alignment Verification Program
MAINDEC-11-DZRPO	Peripheral Test Generator Program

7.4.1 MAINDEC-11-DZRPI RP04 Diskless Controller Test

This program tests the RH11 and the DCL portion of the RP04 Drive. The DCL is the device control logic used to make the RP04 Massbus compatible and must be plugged into the MDLI or appropriately terminated. The program does not use the disk surface or any signals from the MDLI. The MDLI is the mass device level interface which connects the DCL to the drive assembly.

If the disk is powered up, it must be in the Heads Unloaded position. After a successful run (with no errors) of this diagnostic, it can be ascertained that the DCL logic which processes the data is working properly. The logic which handles the mechanical commands is not tested in this diagnostic. All data commands use the Maintenance register in the wraparound mode.

7.4.2 MAINDEC-11-DZRPJ RP04 Functional Controller Test

This diagnostic tests the DCL portion of the RP04 Drive. It exercises the disk surface and the mechanics of the drive to prove proper operation of the subsystem. To run the diagnostic, a disk pack with no vital information written on it is essential. The disk pack need not be formatted.

After a successful run of this diagnostic (with no errors), it can be concluded that the DCL circuitry in the RP04 works successfully while not connected to the rest of the subsystem. System interaction and drive timing is left to other diagnostics. It is assumed that the MAINDEC-11-DZRPI RP04 Diskless Controller Test has been run successfully.

7.4.3 MAINDEC-11-DZRPK Mechanical Read/Write Test

This program contains 15 tests numbered 0 through 16_8. Tests 0 through 6 use a Read Header and Data command to read the cylinder, track, and sector information from the header; the tests then check the information for validity, ensuring that the seek operation functions properly. Tests 7 through 12 measure the rotational speed, the one-cylinder seek, the average seek, and the maximum seek times to ensure that they are all within the specified tolerances. Tests 13 and 14 ensure that the sector and track addressing circuitry is working properly. Test 15 ensures that the data storage and retrieval capabilities are operative. Test 16 is used to stress and check the read/write and servo systems.

The program starts by identifying itself and determining that all drives are available for testing. All drives are then tested beginning with the lowest numerical drive and proceeding in sequential order. One pass (tests 0 through 15) is performed on each drive before moving to the next drive in sequence. The drive to be tested will be typed at the beginning of each pass. At the completion of each pass, an End of Pass message will be typed. After testing all drives, an End of Test message will be typed.

7.4.4 MAINDEC-11-DZRPP and -DZRRQ Dual-Port Logic Test (Parts 1 and 2)

This porgram checks the dual-port logic in the DCL portion of the RP04 and requires a special adapter cable.

7.4.5 MAINDEC-11-DZRPR 20-Sector Mode Logic Test

This program tests the operation of the 20-sector mode logic.

7.4.6 MAINDEC-11-DZRPN Multidrive Exerciser

The RP04 Multidrive Exerciser Program exercises one to eight RP04 Disk Drives attached to the same RH11. If two or more RP04 Disk Drives are being exercised, operations on the drives are overlapped. (Other drives are performing seek/search operations while one RP04 is performing a data transfer or write-check operation.) Operations among the RP04s are optimized so that a high subsystem data transfer rate or a high positioning operation rate is maintained.

The performance of each drive is monitored by the program. If a drive exceeds a preset number of errors in any of several categories, that drive is automatically deassigned. (The operator may override the automatic deassignment feature.) The program reports performance statistics for each drive being exercised on request from the operator or automatically at an interval determined by the operator.

All data transfer commands are used (i.e., Write Data, Write Header and Data, Read Data, and Read Header and Data) as well as Write-Check Data and Write-Check Header and Data commands. Recalibrate and Read-In Preset commands are used at startup and drive initialization. Recalibrate, Offset, and Return to Centerline commands are used during error processing.

Program/operator communications are through the Teletype®; program options are selected by Switch register settings and errors are normally reported on the Teletype. However, if a line printer is available, the program will use the printer for error message display.

All commands, data patterns, and data buffer sizes are selected randomly by the program. The addresses (e.g., cylinder, track, and sector) for each operation are also selected randomly.

At the completion of each operation, the program checks the RH11. The program requires data packs created by the Formatter Program (MAINDEC-11-DZRPL), by the Read/Write Mechanical Test (MAINDEC-11-DZRPK), or by the Data Pack Generation command of the Exerciser Program.

7.4.7 MAINDEC-11-DZRPL Formatter Program

The RP04 Formatter Program is designed to write and verify header and data information on all possible disk pack addresses with the intention of testing the retention of the recording surfaces. The format is maintained on a basis of 411 cylinders, 19 tracks per cylinder, and 22 sectors per track.

This program formats the disk pack on the assigned drive one track at a time. The data fields are written with the selected pattern. Key words are written with 0s. Each track is verified with a Write-Check command immediately after it is written.

The portion of the pack to be formatted is determined by the first and last cylinder and track addresses, inclusively. A single track is the smallest element that may be formatted.

Write-check errors are reported when they are detected. If an error is detected, the sector must be rewritten and verified correctly two successive times to be considered usable. Sectors which cannot be written correctly twice after an error will be declared unacceptable by the program.

After the last track has been formatted and verified, an additional check is performed. The header of track 0 and sector 0 of each cylinder is read and compared by the software. This check is performed to isolate a possible positioner error that may have occurred during the format operation. Two such cases of positioner malfunction are: failure of the positioner to advance to the next cylinder, and advancement of the positioner past the cylinder desired.

7.4.8 MAINDEC-11-DZRPM Head Alignment Verification Program

This program checks head alignment at cylinder 245, heads 0 through 18, and at cylinders 400 and 4, heads 0 and 18, and reverifies alignment of cylinder 245, heads 0 through 18. The operator will be notified if any head is out of alignment by more than the specified amount.

Head alignment is checked in the following manner:

1. Offset the positioner to +1200 microinches.
2. Store the sign change bit.

® Teletype is a registered trademark of Teletype Corporation.

3. Move the positioner in the opposite direction in 25-microinch increments until the sign change bit changes value. Store the offset value.

4. Offset the positioner to -1200 microinches and repeat steps 2 and 3.

5. Average the two sign change offset values and report if the selected head is misaligned by more than ±150 microinches for cylinder 245 or ±350 microinches for cylinders 4 and 400.

Repeat the above sequence for all heads at cylinder 245 and for heads 0 and 18 at cylinders 4 and 400.

7.4.9 MAINDEC-11-DZRPO Peripheral Test Generator Program

This program is a modified form of FOCAL-11 and allows the user to write RP04 programs in the FOCAL-11 language.

APPENDIX A
INTEGRATED CIRCUIT DESCRIPTION

A.1 INTRODUCTION

This appendix contains descriptions of some of the integrated circuits used in the RH11. Where applicable, logic diagrams, schematics, and pin connection diagrams are shown.

A.2 3341 64-WORD × 4-BIT SERIAL MEMORY (SILO)

The 3341 Silo Memory operates in a first in/first out mode (FIFO). The output rate is independent of the input rate and asynchronous or synchronous operation can be achieved.

The four data inputs (D0 through D3) are transferred to the first memory location if both the Input Ready (IR) and Shift In (SI) signals are asserted high (see Silo Memory Block Diagram). After 250 ns to allow the data to stabilize, IR goes low. However, data remains in the first memory location until both IR and SI are brought low. At this point, the data propagates to the next memory location, if the location is empty. When the data is transferred, IR goes high, indicating that the device is ready to accept new data. If the memory is full, the IR signal remains unasserted (low).

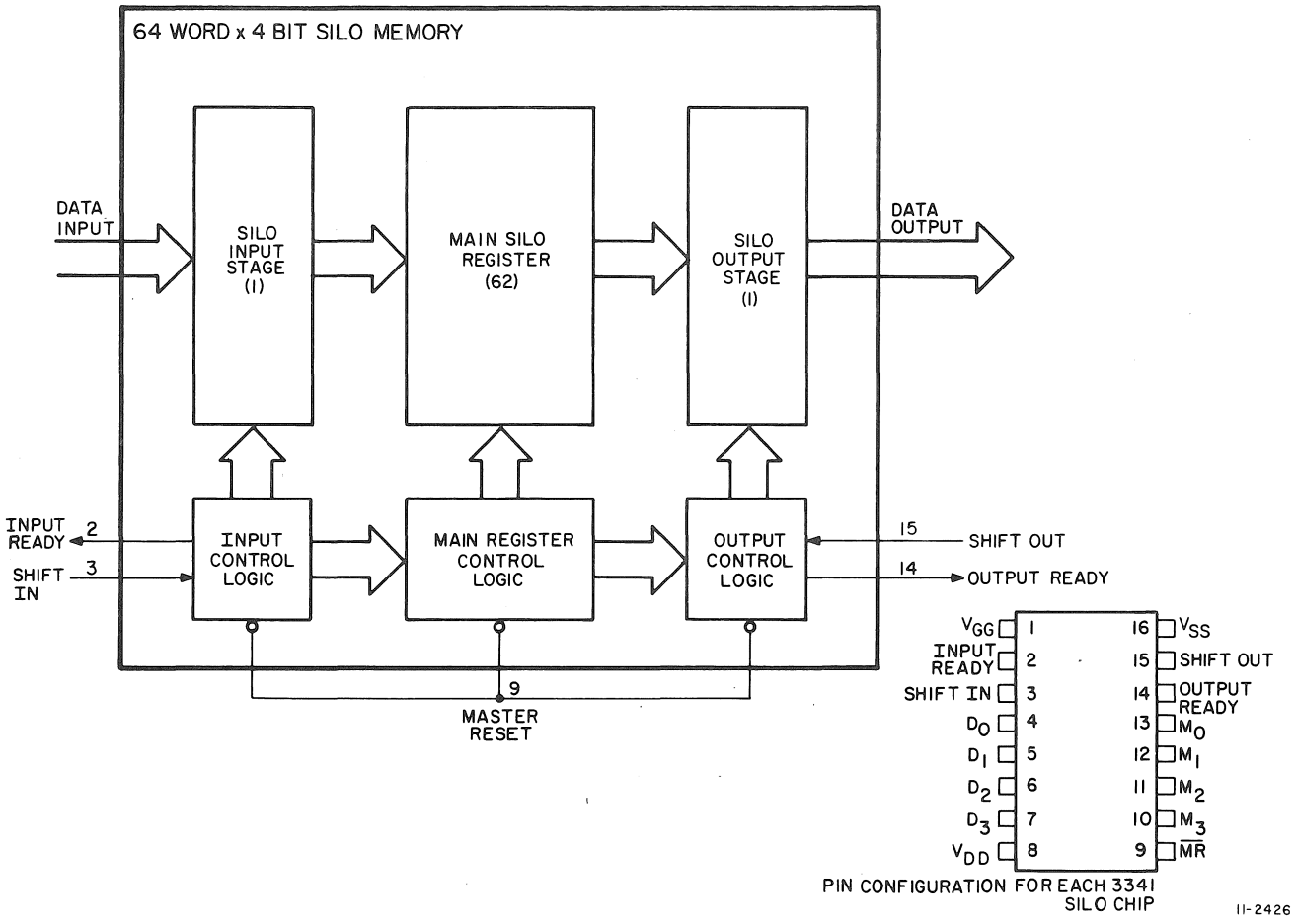
When data enters the second cell, the transfer of any data word from a full cell to the next empty cell is automatic and is activated by an on-chip control. Consequently, data stacks up at the output to the memory while empty locations "bubble" to the input of the memory. The throughput time from input to output of the Silo is from 0 to 32 μs (16 μs typical).

When data has transferred to the last cell in the Silo, OUTPUT READY (OR) is asserted high, indicating that valid data is present at the output pins (M0 through M3 on each chip). Data is not shifted out of the Silo, however, until the OUTPUT READY and SHIFT OUT signals to the Silo are both asserted high. When the data is shifted out, OUTPUT READY goes low. The output data is maintained until both OUTPUT READY and SHIFT OUT go low. At this point, the contents of the previous memory cell (if it is full) are transferred to the output cell, causing OUTPUT READY to be asserted high again. When the Silo memory is emptied, OUTPUT READY stays low.

Table A-1 lists the minimum, typical, and maximum times for the above mentioned signals at 0° C and at 70° C.

Table A-1
Control Signal Timing Specifications

Signal	0°			70°		
	MIN	TYP	MAX	MIN	TYP	MAX
Input Ready High Time	90	300	–	155	300	450
Input Ready Low Time	138	400	–	–	400	520
Data Input Stabilizing Time	–	250	–	–	250	400
Data Output Stabilizing Time	–	250	–	–	250	400
Output Ready High Time	90	250	–	155	250	350
Output Ready Low Time	170	450	–	–	450	650


64 WORD x 4 BIT SILO MEMORY
DATA INPUT
SILO INPUT STAGE (1)
MAIN SILO REGISTER (62)
SILO OUTPUT STAGE (1)
DATA OUTPUT
INPUT READY
2
SHIFT IN
3
INPUT CONTROL LOGIC
MAIN REGISTER CONTROL LOGIC
OUTPUT CONTROL LOGIC
15
SHIFT OUT
14
OUTPUT READY
9
MASTER RESET
VGG 1
INPUT READY 2
SHIFT IN 3
DO 4
D1 5
D2 6
D3 7
VDD 8
16 VSS
15 SHIFT OUT
14 OUTPUT READY
13 MO
12 M1
11 M2
10 M3
9 MR
PIN CONFIGURATION FOR EACH 3341 SILO CHIP
11-2426

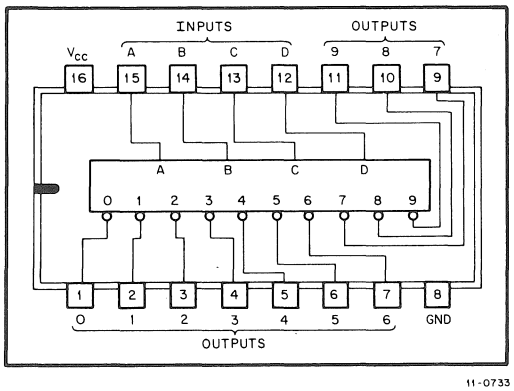
A.3 7442 4-LINE-TO-10-LINE DECODERS (1-of-10)

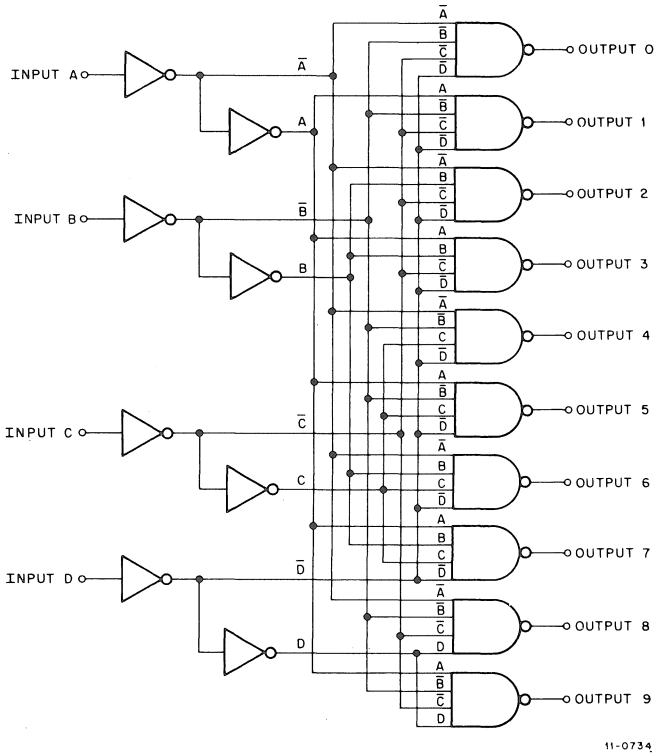
These monolithic decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The 7442 BCD-to-decimal decoder features familiar transistor-transistor-logic (TTL) circuits with inputs and outputs that are compatible for use with other TTL and DTL circuits.

TRUTH TABLES

BCD Input				Decimal Output									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1





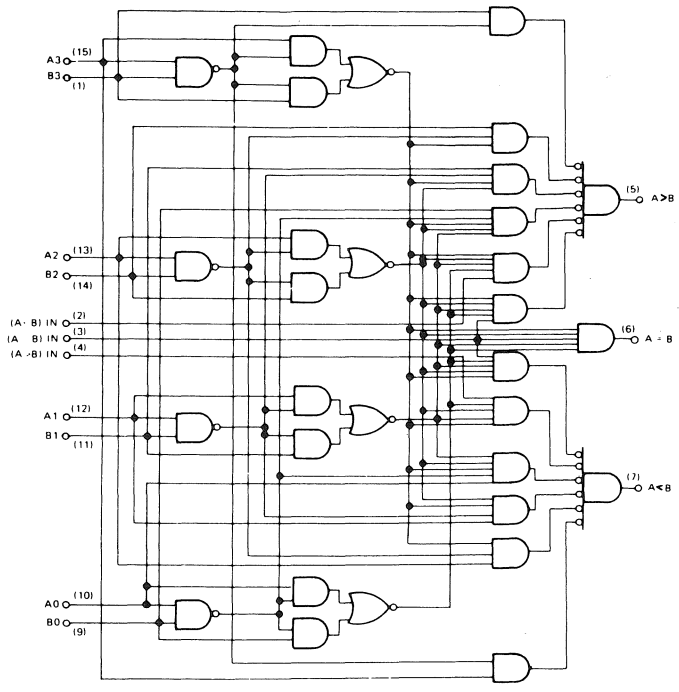
A.4 7485 4-BIT MAGNITUDE COMPARATORS

The 7485 performs magnitude comparison of straight binary and straight BCD (8421) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs.

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

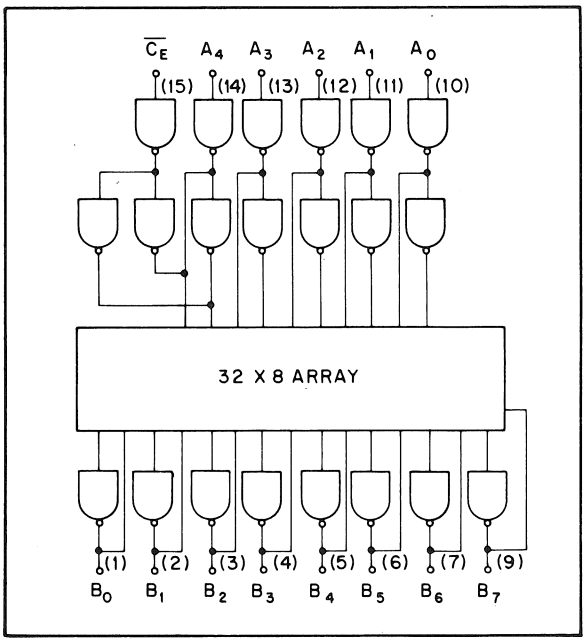
NOTE: H = high level, L = low level, X = irrelevant



Pin (16) = V_{CC}, Pin (8) = GND

A.5 8223 256-BIT BIPOLAR FIELD-PROGRAMMABLE ROM (32 X 8 PROM)

The 8223 is a TTL 256-bit read only memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to the high state when the chip enable input is high.

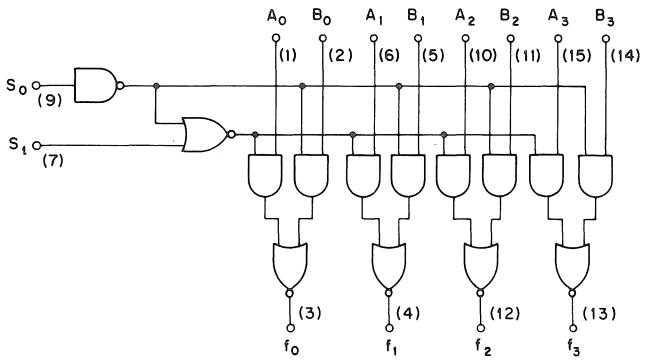


V_{CC} = (16)
GND=(8)
( ) = DENOTES PIN NUMBERS

11-2382

A.6 8234 2-INPUT 4-BIT DIGITAL MULTIPLEXER

This device is a 2-input, 4-bit digital multiplexer designed for general purpose, data selection applications. The 8234 features inverting data paths. The 8234 design has open-collector outputs which permit direct wiring to other open-collector outputs (collector logic).



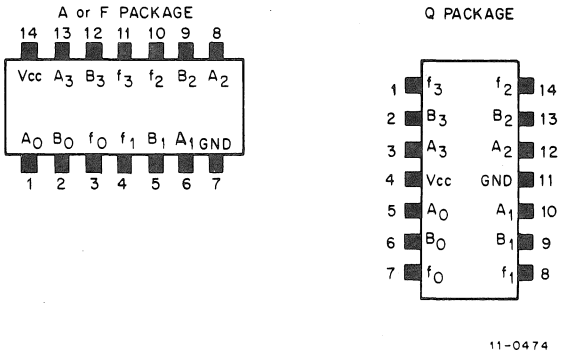
S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

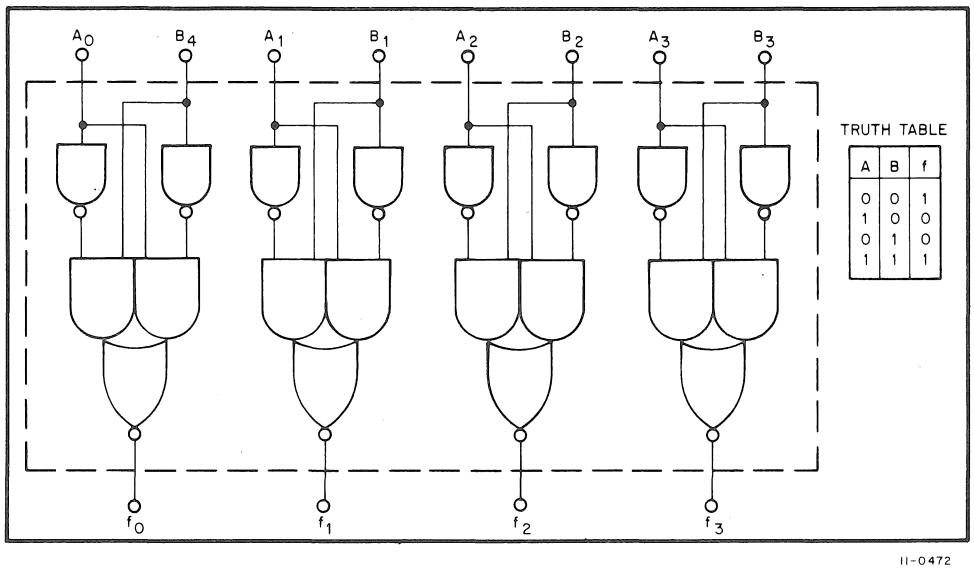
V_{CC} = (16)
GND = (8)
( ) = DENOTES PIN NUMBERS

11-2383

A.7 8242 EXCLUSIVE-NOR 4-BIT DIGITAL COMPARATOR

The 8242 digital comparator circuit consists of four independent Exclusive-NOR gates with each gate structure having an open-collector output to permit multiple bit comparisons. A 4-bit comparator network is formed by connecting the independent outputs; such a network is easily expanded by cascading the outputs.



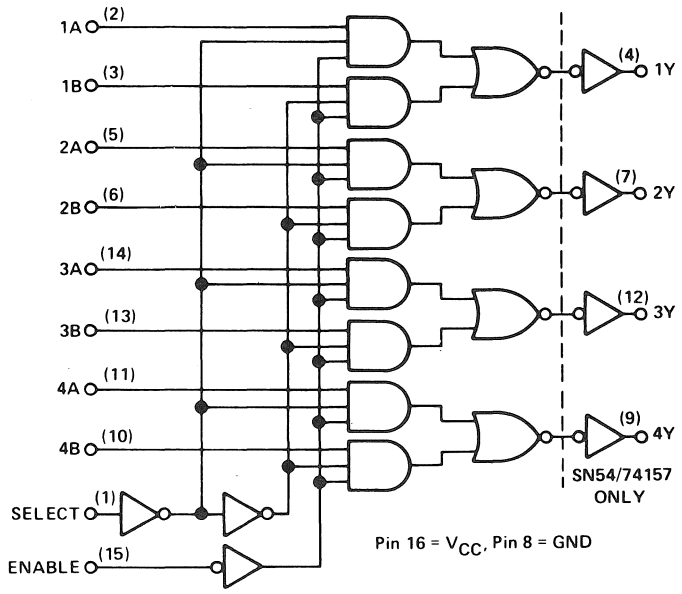


A.8 74157 QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXER

The 74157 quadruple 2-line to 1-line multiplexer features buffered inputs and outputs. All outputs are low when disabled (enable high). The truth table and logic diagram are shown below.

INPUTS			OUTPUT Y	OUTPUT W
ENABLE	SELECT	A B	SN54/74157, SN54S/74S157	SN54S/74S158
H	X	X X	L	H
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

H = high level, L = low level, X = irrelevant



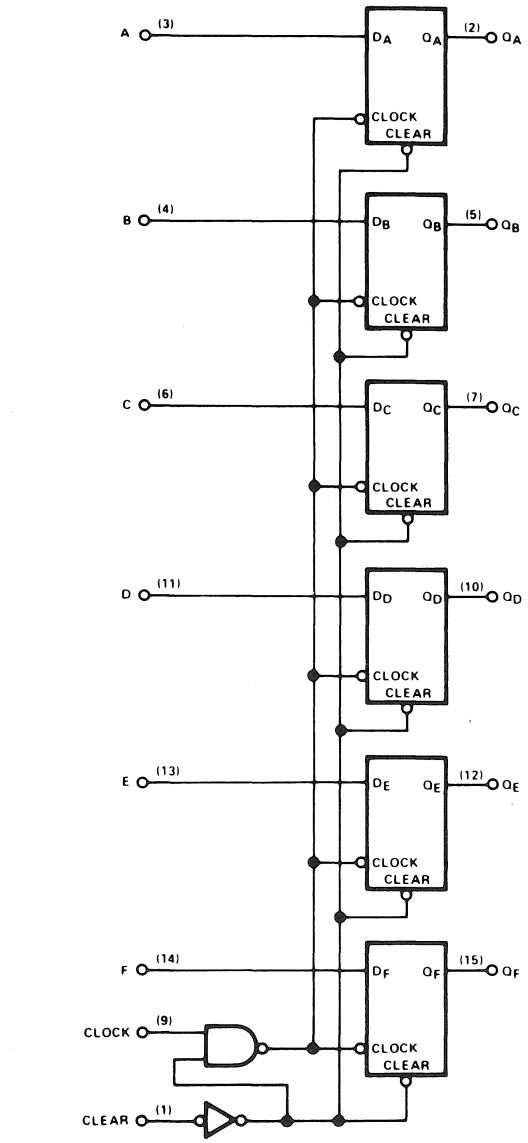
Pin (16) = V_{CC}, Pin (8) = GND

A.9 74174 HEX D-TYPE FLIP-FLOPS

The 74174 contains six flip-flops with single outputs. The flip-flops contain direct clear inputs and buffered clock inputs.

INPUT t_n	OUTPUTS t_n+1	
D	Q	Q
H	H	L
L	L	H

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.



Pin (16) = V_{CC}, Pin (8) = GND

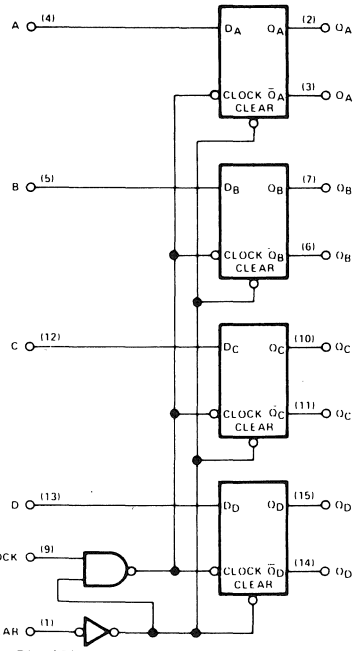
A.10 74175 QUAD D-TYPE FLIP-FLOPS

The 74175 contains four D-type flip-flops with dual outputs. Each flip-flop has direct clear and buffered clock inputs.

INPUT t_n	OUTPUTS t_n+1	
D	Q	$\bar{Q}$
H	H	L
L	L	H

t_n = Bit time before clock pulse.

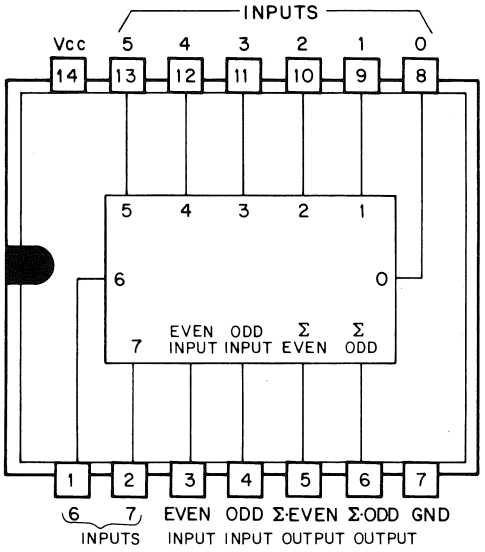
t_{n+1} = Bit time after clock pulse.



Pin (16) = V_{CC}, Pin (8) = GND

A.11 74180 PARITY CONTROL GENERATOR/ CHECKER

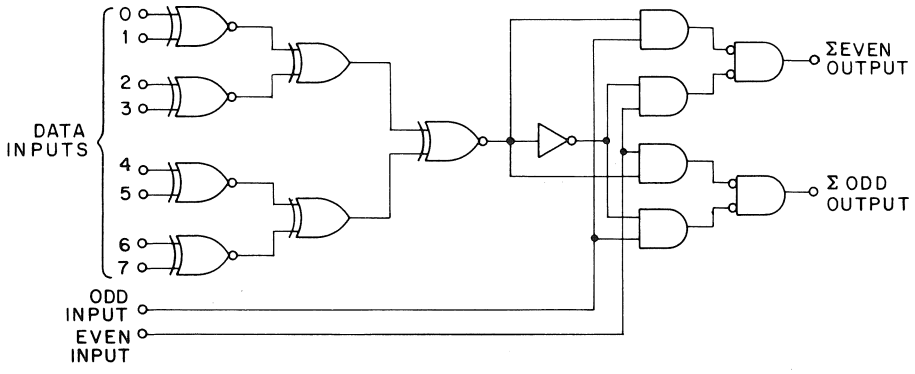
The 74180 is an 8-bit parity generator/checker featuring odd and even outputs and control inputs to provide odd or even parity operation. Word length is expandable by cascading. The truth table, pin connection diagram, and functional block diagram are shown below.



TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X= IRRELEVANT



11-2384

A.12 74193 4-BIT BINARY COUNTER

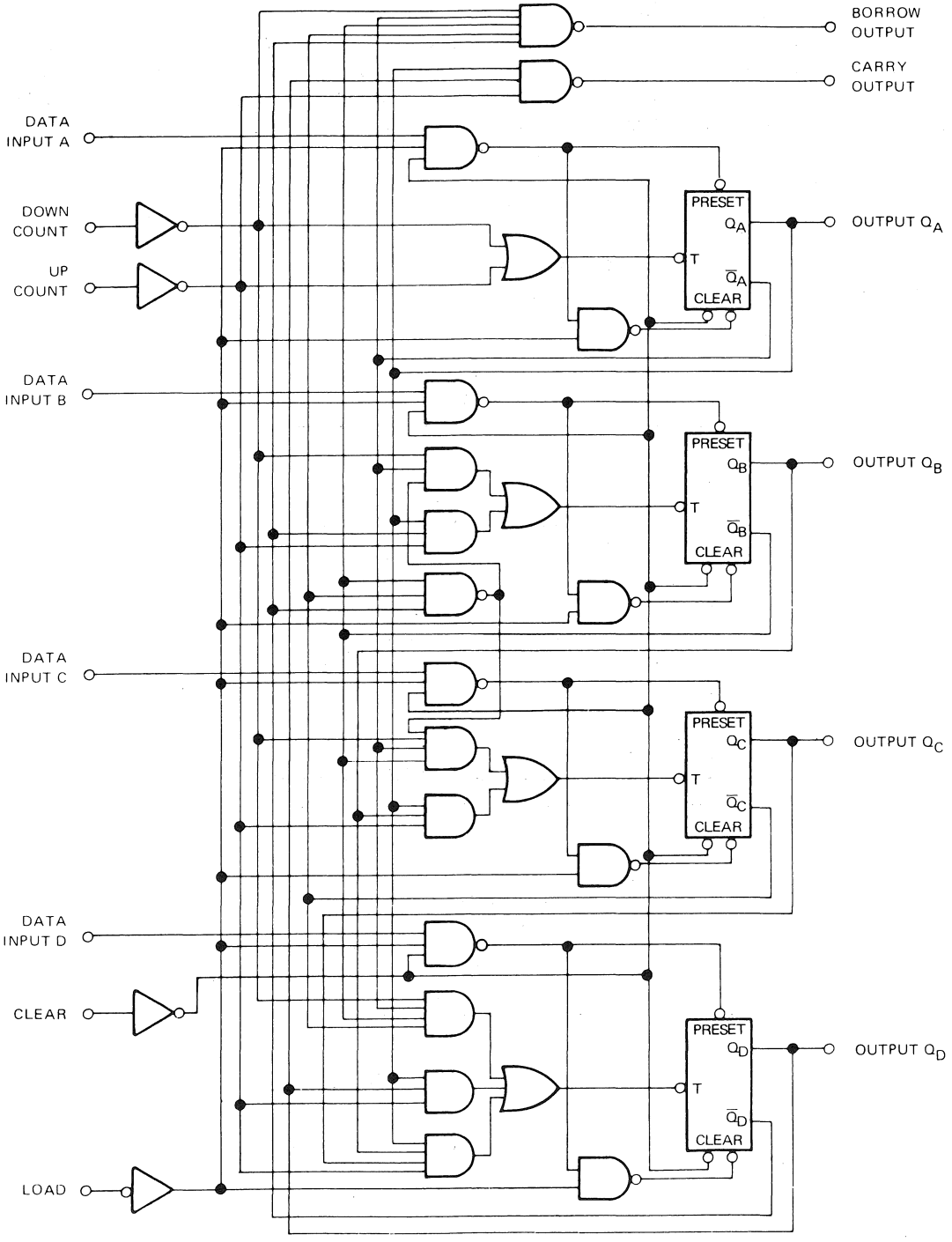
The 74193 binary counter has an individual asynchronous preset to each flip-flop, a fully independent clear input, internal cascading circuitry, and provides synchronous counting operations.

COUNT UP	COUNT DOWN	LOAD	MODE
X	X	L	Parallel Load
CLOCK	H	H	Count Up
H	CLOCK	H	Count Down

H = high level, L = low level, X = irrelevant

Signal/Pin Designation

Signal Name	Pin Designation
DATA INPUT A	15
DATA INPUT B	1
DATA INPUT C	10
DATA INPUT D	9
CLEAR	14
LOAD	11
DOWN COUNT	4
BORROW OUTPUT	13
CARRY OUTPUT	12
UP COUNT	5
OUTPUT Q_A	3
OUTPUT Q_B	2
OUTPUT Q_C	6
OUTPUT Q_D	7

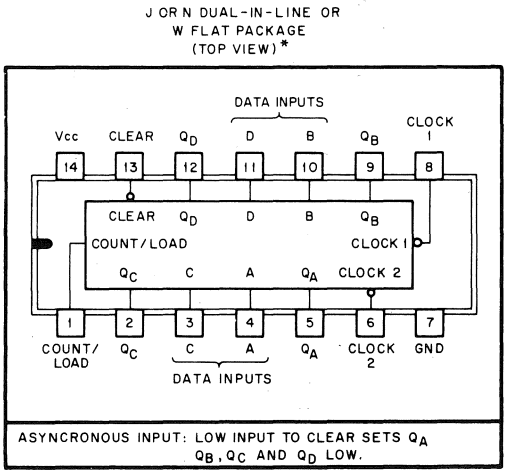

BORROW OUTPUT
CARRY OUTPUT
DATA INPUT A
DOWN COUNT
UP COUNT
DATA INPUT B
DATA INPUT C
DATA INPUT D
CLEAR
LOAD
PRESET
CLEAR
T
Q_A
$\overline{Q}_A$
Q_B
$\overline{Q}_B$
Q_C
$\overline{Q}_C$
Q_D
$\overline{Q}_D$
OUTPUT Q_A
OUTPUT Q_B
OUTPUT Q_C
OUTPUT Q_D

A.13 74197 50 MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

This high-speed monolithic counter consists of four dc coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-eight counter. The counter is fully programmable; i.e., the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

This counter may also be used as a 4-bit latch by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. It features a direct clear which, when taken low, sets all outputs low regardless of the states of the clocks.



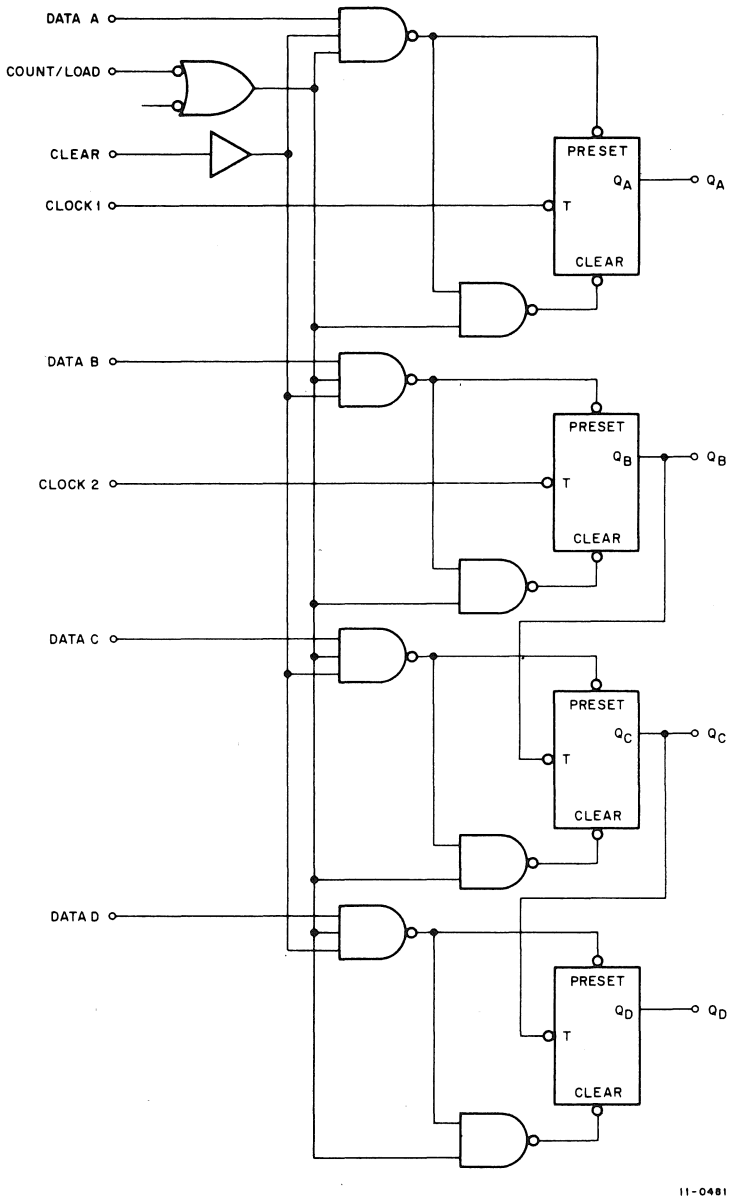
*Pin assignments for these circuits are the same for all packages.

11-0482

SN74197 TRUTH TABLE
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE A: Output Q_A connected to clock-2 input.


DATA A
COUNT/LOAD
CLEAR
CLOCK 1
PRESET
Q_A
T
CLEAR
Q_A
DATA B
CLOCK 2
PRESET
Q_B
T
CLEAR
Q_B
DATA C
PRESET
Q_C
T
CLEAR
Q_C
DATA D
PRESET
Q_D
T
CLEAR
Q_D
11-0481

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