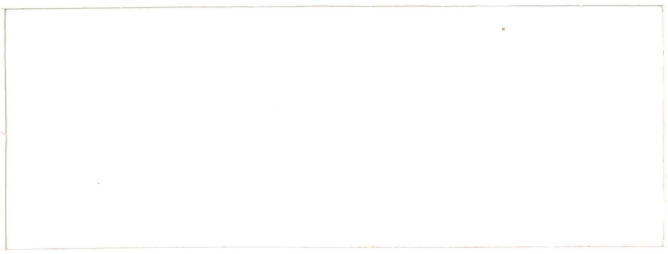
# RK11-D and RK11-E moving head disk drive controller manual

pdp11

digital



DEC-11-HRKDA-B-D

# RK11-D and RK11-E moving head disk drive controller manual

digital equipment corporation · maynard, massachusetts

1st Edition, August 1973

CONTENTS

CONTENTS (Cont)



ILLUSTRATIONS

## ILLUSTRATIONS (Cont)



## TABLES

# INTRODUCTION

This manual provides the user with the theory of operation of the RK11 Moving Head Disk Drive Controller, and with the logic descriptions necessary to understand and maintain it effectively. Discussions in the manual deal with general and detailed descriptions of the RK11-D and RK11-E Controllers. For detailed coverage of the RK05 itself, refer to the *RK05 Disk Drive Maintenance Manual,* DEC-00-RK05-DA.

Although control signals and data are transferred between the RK11 Controller and the Unibus, it is beyond the scope of this manual to cover the operation of the bus itself. Detailed information regarding the Unibus may be found in the *PDP-11 Peripherals and Interfacing Handbook.*

Reference is occasionally made within this manual to engineering drawings, not contained herein. These drawings are in the *RK11 Moving Head Disk Drive Controller Engineering Drawings Manual,* a copy of which is supplied with each RK11 Controller. That manual contains current RK11 prints, updated to the time when the equipment is shipped.

# CHAPTER 1
# GENERAL DESCRIPTION

## 1.1 INTRODUCTION

The RK11-D and RK11-E are controllers for rotating mass memories capable of communicating with up to eight daisy-chained disk drives (Figure 1-1). The system is block-oriented, but is capable of transferring from 1 to $2^{16}$ consecutive data words without reinitiation or processor intervention. These data transfers occur on the Unibus at the Non-Processor Request (NPR) level of communication.

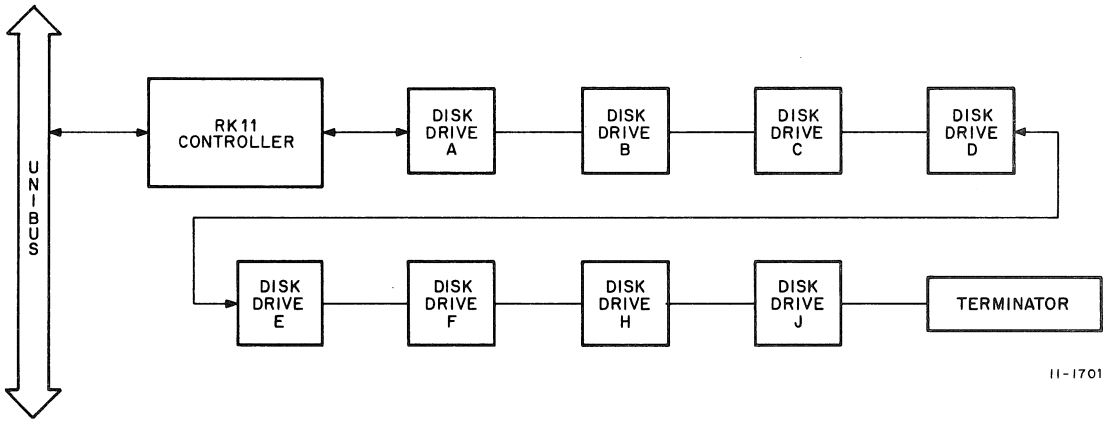



Figure 1-1 RK11-D and RK11-E Disk Drive System

## 1.2 OPTIONS

The RK11 Controller has two options, RK11-D and RK11-E, both of which are used with the RK05 Disk Drive. The RK11-D transfers 16-bit data, and the RK11-E transfers 18-bit data. Option selection is made by adjusting the jumper configuration as described in Paragraph 2.4.

## 1.3 FUNCTIONAL DESCRIPTION

The RK11 Controller and the RK05 Disk Drive form the disk drive system, which interfaces with a PDP-11 processor via the Unibus. The RK11 is implemented on four functional modules (M7254, M7255, M7256, and M7257), and interfaces with the RK05 Disk Drive via a drive bus (DR BUS) as shown in Figure 1-2.

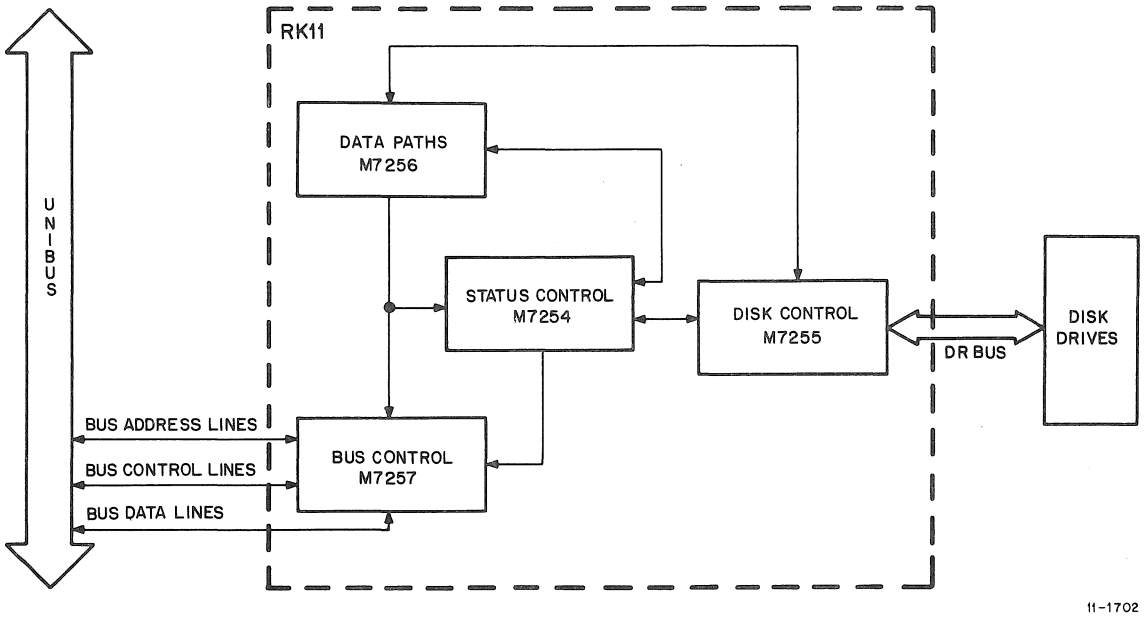



Figure 1-2 RK11 Controller, Functional Block Diagram

### 1.3.1 Disk Drives

The RK05 is a moving-head disk drive that uses RK03-KA disk cartridges for data storage. Data is stored on both sides of the disk by a pair of movable heads, which are always positioned over opposing surfaces of the same cylinder simultaneously. Each side of the disk contains $203_{10}$ tracks, each of which contains $12_{10}$ sectors capable of storing $400_8$ or $256_{10}$ data words.

The sector format consists of $15_8$ words of preamble terminating in a sync bit, followed by a one-word header, $400_8$ data words, a one-word checksum, and one word of postamble. Sector pulses signal the beginning of each sector, and an index pulse indicates the last sector, signifying that the sector following is Sector 0.

The DR BUS consists of eight disk drives connected in daisy-chain fashion, each of which can be write protected either by an RK11 Controller Write Lock function or by manual intervention.

On a disk cartridge, the upper surface is defined as surface 0, and is active when RKDA 04 (SUR) is clear. If a data transfer requires an overflow from surface 0, SUR is set automatically, and surface 1 (the lower surface of the cartridge) is activated at sector 0. If a data transfer requires an overflow from surface 1, the RK11 automatically moves the disk drive heads to the next cylinder, checks the header word to verify head positioning, and resumes the data transfer at sector 0 of surface 0 again, but this time on a new cylinder. Attempting this cross-cylinder operation from surface 1 of the last cylinder will result in an error condition (RKER 14 – OVR).

For more detailed information on the disk drive operation and the related power supply, refer to the *RK05 Disk Drive Maintenance Manual* (DEC-00-RK05-DA), which is shipped with the disk drives. That manual also contains a complete description of the DR BUS lines.

### 1.3.2 RK11 Controller

The RK11 is divided into four major functional units, as shown in Figure 1-2. The Status Control initiates the programmable RK11 functions and monitors logic status conditions. The Disk Control monitors disk drive status conditions and controls all disk drive functions. The Data Paths transfer parallel data to and from the Unibus, and serial data to and from the disk drives. The Bus Control interfaces the RK11 with the Unibus for address selection, NPR data transfers, and interrupt sequences.

The RK11 contains seven 16-bit programmable hardware registers, addressed from the Unibus, that provide the software interface between the RK11 and the Unibus. Table 1-1 lists these registers and their addresses.

**Table 1-1**
**RK11 Registers**

| Name | Abbreviation | Address |
|---|---|---|
| RK11 Drive Status Register | RKDS | 777400 |
| RK11 Error Register | RKER | 777402 |
| RK11 Control Status Register | RKCS | 777404 |
| RK11 Word Count Register | RKWC | 777406 |
| RK11 Bus Address Register (Current Memory Address) | RKBA | 777410 |
| RK11 Disk Address Register | RKDA | 777412 |
| RK11 Data Buffer Register | RKDB | 777416 |

Through software control, the RK11 can perform four control functions (Control Reset, Seek, Drive Reset, and Write Lock) and four data transfer functions (Write, Read, Write Check, and Read Check). The hardware poll feature enables more than one disk drive to perform multiple Seek or Drive Reset functions simultaneously. The RK11 also initiates an interrupt sequence on the Unibus in response to any of six interrupt conditions described in Paragraph 3.4.

**1.3.2.1 Control Reset** – The Control Reset function initializes all internal registers and flip-flops, and clears all of the bits of the seven programmable registers except RKCS 07 (READY), which it sets, and RKDS 01 through 11, which are not affected. Disk drive operation is only affected indirectly, as a result of RK11 logic being cleared.

Control Reset serves as an effective "abort," because it terminates all controller action; however, care should be taken during a Write operation as the abort does not occur until completion of the current sector. If a Control Reset function is used to abort a function in process to allow a high-priority user access to a disk drive, that drive must first be checked for head motion (indicated by RKDS 06 – Read/Write/Seek Ready). If the function is initiated before the heads have stopped, a hard error results, after which a Drive Reset function must be performed on that drive before it can be used again.

**1.3.2.2 Seek Function** – For a Seek function, the RK11 directs the selected disk drive to move its head mechanism to the cylinder address specified by RKDA 05 through 12. When this portion of a Seek has been initiated, the controller returns to the Ready state (RKCS 07). But if the specified cylinder address is greater than $312_8$, the function is aborted and bit 06 (nonexistent Cylinder) of the RKER is set. RKCS 06 (Interrupt Done Enable) then determines the program reaction.

The selected disk drive completes the Seek function by moving its head mechanism to the desired cylinder, whereupon RKDS 06 (R/W/S RDY) is set. The time required to initiate a Seek function is normally 1 $\mu$s, but may range up to 3.3 ms if an attempt is made to abort a Write function. Head movement may take up to a maximum of 80 ms.

**1.3.2.3 Drive Reset Function** – For a Drive Reset function, the controller directs the selected disk drive to move its head mechanism to cylinder address 000 and reset all active error status lines. To the controller, the Drive Reset function is the same as a Seek function, even to the manner in which the hardware poll logic is used; however, a Drive Reset function can take much longer than a Seek function to execute. The time required to complete a Drive Reset function depends on the physical position of the head mechanism at the time the function is initiated, and therefore may take up to a maximum of two seconds.

1.3.2.4 **Write Lock Function** – The Write Lock function write-protects a selected disk drive until the condition is overridden by operation of the corresponding WT PROT (Write Protect) switch on the disk drive (refer to *RK05 Disk Drive Maintenance Manual,* DEC-00-RK05-DA). The disk drive is automatically write-enabled when power is first applied, or when the disk drive RUN/LOAD switch is set to RUN.

1.3.2.5 **Write Function** – For a Write function, the controller first performs a normal Seek function. When that is completed, the next Header word is read and checked for correct cylinder identification (cylinder address). If the header is correct, the controller begins the Write operation when the Sector Counter (RKDA 00 through 03) equals the sector address (RKDS 00 through 03), hereafter referred to as SC = SA.

A preamble consisting of 15 words of zeroes is written, followed by a sync pulse. Then the header word is rewritten automatically, followed immediately by the data words for the sector. As the data words pass through the controller, a one-word checksum word is calculated and automatically written after the last sector data word, followed by one word of zeroes for the postamble. If the cylinder address is incorrect, the controller makes 16 attempts to establish the correct cylinder address before the function is aborted, setting RKER 12 (Seek Error). (Compatibility with the RK11-C, which makes only one attempt, may be achieved by cutting a jumper on the Status Control module.)

An RKWC overflow at any time from the start of the Write function stops the NPR data transfers and sets RKCS 07 (Ready, RDY) at the end of the current sector. If the RKWC has not overflowed at the end of a given sector, the function is continued at the next contiguous sector; however, if the last sector of the disk cartridge is transferred without RKWC having overflowed, then RKER 14 (OVR, Overrun) is set.

1.3.2.6 **Read Function** – For a Read function, the controller first performs a normal Seek function. When that is completed, the controller waits for SC = SA, then reads and checks the header word. If the cylinder address is correct, the controller continues reading the sector and NPR-transfers the data words onto the Unibus. If the cylinder address is initially incorrect, the controller makes 16 attempts (jumper selectable to one, as previously noted) to establish the correct cylinder address before the function is aborted, setting RKER 12. As the data words of a sector pass through the controller, a one-word checksum word is calculated and compared with the checksum read from the disk drive. If there is a discrepancy between the two checksums, RKER 01 (Checksum Error) is set, and the controller reaction is determined by RKCS 06 (IDE) and RKCS 08 (SSE, Stop on Soft Error). An RKWC overflow at any time from the start of the Read function stops the NPR data transfers and sets RKCS 07 (RDY) at the end of the current sector. If the RKWC has not overflowed at the end of a given sector, the function is continued at the next contiguous sector.

1.3.2.7 **Write Check Function** – The Write Check function is used to compare the contents of memory to the contents of a continuous block of data on a disk cartridge. The controller first performs a Seek function, just as for a Write function, and then reads and checks the next header word. If the cylinder address is correct, the controller waits for SC = SA, then begins reading the rest of the sector (Data and Checksum) while performing BUS NPR transfers for each data word. Each data word from the disk drive is compared, bit by bit, with memory data from the Unibus. The disk drive checksum, in turn, is compared with the checksum calculated by the controller. If any bit is found to be in error, RKER 00 (Write Check Error) is set. Controller reaction is then determined by RKCS 06 (IDE) and RKCS 08 (SSE). The Write Check function may be performed on a short sector (less than 256 data words) as long as the number of words write checked is equal to the number of words previously written into the sector.

1.3.2.8 **Read Check Function** – The Read Check function is identical to a normal Read function, except that no NPRs occur. Only the checksum is calculated and compared with the checksum read from the disk drive. This function enables the program to know beforehand if a given block of data is readable and error free. Because the Read Check is essentially a parity check, it must be performed on a whole-sector basis only.

1.3.2.9 **Hardware Poll** – The controller is capable of permitting any or all disk drives to perform a Seek or Drive Reset function simultaneously. The hardware poll feature in the Disk Control identifies the logical disk drive in RKDS 13–15 (DRIVE IDENT) for any disk drive that has completed a Seek or Drive Reset function. This poll causes an interrupt if RKCS 06 (IDE) is set, the controller is in the Ready state (RKCS 07 set), and the controller is not already attempting to initiate an interrupt from some other function. If two or more disk drives complete a Seek or Drive Reset function simultaneously, the controller interrupts once for each disk drive and identifies each in turn to the RKDS. In this situation, the processor interrupt status must be raised to a level equal to or greater than that of the RK11, or else a second interrupt will occur immediately after the first, causing the interrupt service routine to be interrupted. Similarly, back-to-back interrupts will also result from directing the heads to a cylinder at which they are already positioned, with the first interrupt coming from the initiation of a Seek function and the second coming from notification from the hardware poll that the heads are already at the desired address. In this case, also, care should be taken in the assigning of processor priorities to handle this situation.

## 1.4 PHYSICAL DESCRIPTION

The RK11 Controller consists of the four RK11 modules (M7254, M7255, M7256, and M7257) and one system unit. The system unit containing the modules can be mounted in any PDP-11/15, 11/20, 11/35, 11/40, or 11/45 mounting box when used in conjunction with the proper power harness. The modules utilize many MSI integrated circuits (ICs). (Refer to Appendix A.)

The RK11 Disk Drive System consists of the Controller, disk drives, and the necessary cabling. Disk drives A through D (Figure 1-1) are contained in a standard 19-in. PDP-11 cabinet, which can be configured as part of a system or made to stand alone. Disk drives E through J are mounted in a second 19-in. cabinet, which is always bolted to the left side of the first cabinet. An 860 C/D Power Control Unit located at the top of the first cabinet supplies ac power for disk drives A through D. Power for disk drives E through J is supplied in a similar manner in the second cabinet. Drives A through D make up a daisy-chained bus of four disk drives connected directly to the controller. Drives E through J make up a second daisy-chained bus of four disk drives connected directly to disk drive D in the first cabinet. The M7700 card of each disk drive contains a rotary switch that defines the physical disk drive bus (DR BUS) position. The first disk drive on the DR BUS is switched to position 1 and is designated disk drive A, and so on through disk drive J. This configuration may be varied as DR BUS length allows. The maximum length of DR BUS is 50 ft. The disk drives on the DR BUS terminate in an M930 Terminator module connected to the last drive on the bus. For more disk drive system and disk drive information, refer to the *RK05 Disk Drive Maintenance Manual,* DEC-00-RK05-DA.

Both the RK11-D and the RK11-E require an M7700, Rev J or later. The RK11-E also requires a G180, Rev K or later, but the RK11-D is capable of operating with any revision of the G180.

## 1.5 SPECIFICATIONS

Table 1-2 specifies the RK11 parameters in the areas of environmental limits, logic format, timing format, and power requirements, and sets forth model designations.

## 1.6 RELATED DOCUMENTS

Table 1-3 lists software and hardware documents that pertain to the RK11 Controller.

Table 1-2
Specifications

| Category | Parameters |
|---|---|
| **Environmental Limits** | |
| Temperature: | 60° to 110° F ambient (Operating) |
| Relative Humidity: | 20 to 80% without condensation (Operating) |
| Vibration/Shock: | To prevent data errors, extreme vibrations should be avoided while the disk drives are transferring data. (Operating) |
| **Format** | |
| Drive Format: | 1 Disk Cartridge/Disk Drive<br>203 Cylinders/Disk Drive<br>2 Disk Surfaces/Disk Drive<br>2 Tracks/Cylinder<br>12 Sectors/Track |
| Data Word Format: | 16-bit (RK11-D) or 18-bit (RK11-E) data word<br>$256_{10} = 400_8$ Data Words/Sector<br>$3072_{10} = 6000_8$ Data Words/Track<br>$614{,}400_{10}$ Data Words/Surface<br>$1{,}247{,}232_{10}$ Data Words/Disk Drive<br>Bit Density – Approximately 2200 bpi |
| Recording Method: | Double Frequency |
| Data Transfer Path: | Unibus NPR |

Table 1-3
Related Documents

| Title | Number |
|---|---|
| **Software:** | |
| Disk Operating System Monitor Programmer's Handbook | DEC-11-SERA-D |
| **Hardware:** | |
| PDP-11 Peripherals and Interfacing Handbook | None |
| RK05 Disk Drive Maintenance Manual | DEC-00-RK05-DA |

(Also the related PDP-11 System and Processor manuals used with the RK11 Controller.)

# CHAPTER 2
# INSTALLATION

## 2.1 INTRODUCTION

The RK11 Controller system configuration depends on the number of disk drives used in a particular disk drive system. Each RK11 can interface up to eight disk drives. The first four disk drives are housed in one cabinet; the additional disk drives are housed in a second cabinet. Each cabinet contains the power controls for the associated disk drives and all necessary cabling. The RK11 Controller options (RK11-D and RK11-E) are jumper selectable on the RK11 modules (Paragraph 2.4). For details regarding disk drive installation, refer to the *RK05 Disk Drive Maintenance Manual*, DEC-00-RK05-DA.

## 2.2 POWER REQUIREMENTS

Power is supplied to the RK11 Controller by the +5 V power supply for the mounting box in which it is positioned. For an RK11 mounted in a BA11 Mounting Box (PDP-11/20), power is supplied via a PDP-11 system power cable, which plugs into slot A3 of the system unit. For PDP-11/35, PDP-11/40, and PDP-11/45 use, a special power cable is supplied with the equipment.

## 2.3 CABLING REQUIREMENTS

Cabling requirements for the RK11 Controller include the Unibus cable connections and the disk drive cable (DR BUS) connections (Figure 2-1), as well as power cabling in certain systems. Both the Unibus and the DR BUS use BC11A cables.

The Unibus In cable plugs into slots A1 and B1 of the system unit, and the Unibus Out cable plugs into slots A4 and B4. If the system unit is mounted in a mounting box adjacent to other operating units utilizing the Unibus, Unibus In and Out connections between the units are made with an M920 Unibus Connector module. If the RK11 is the last unit on the Unibus, an M930 Unibus Terminator module is plugged into slots A4 and B4. The DR BUS cable plugs into system unit slots A2 and B2.

## 2.4 RK11-D AND RK11-E OPTION CONFIGURATIONS

The RK11 Controller is normally configured as the RK11-D option, but may be configured to the RK11-E option by altering the jumpers. Details concerning these optional jumper configurations are available on the cover sheets for circuit schematics of modules M7254, M7255, M7256, and M7257. The jumpered connections are also shown in the module engineering drawings, which show the jumper function in the logic (refer to Chapter 4). The crystal on the M7255 module must also be changed for the RK11-E option. The 2.88 MHz crystal should be replaced with a 3.09 MHz crystal (see DISK 4).

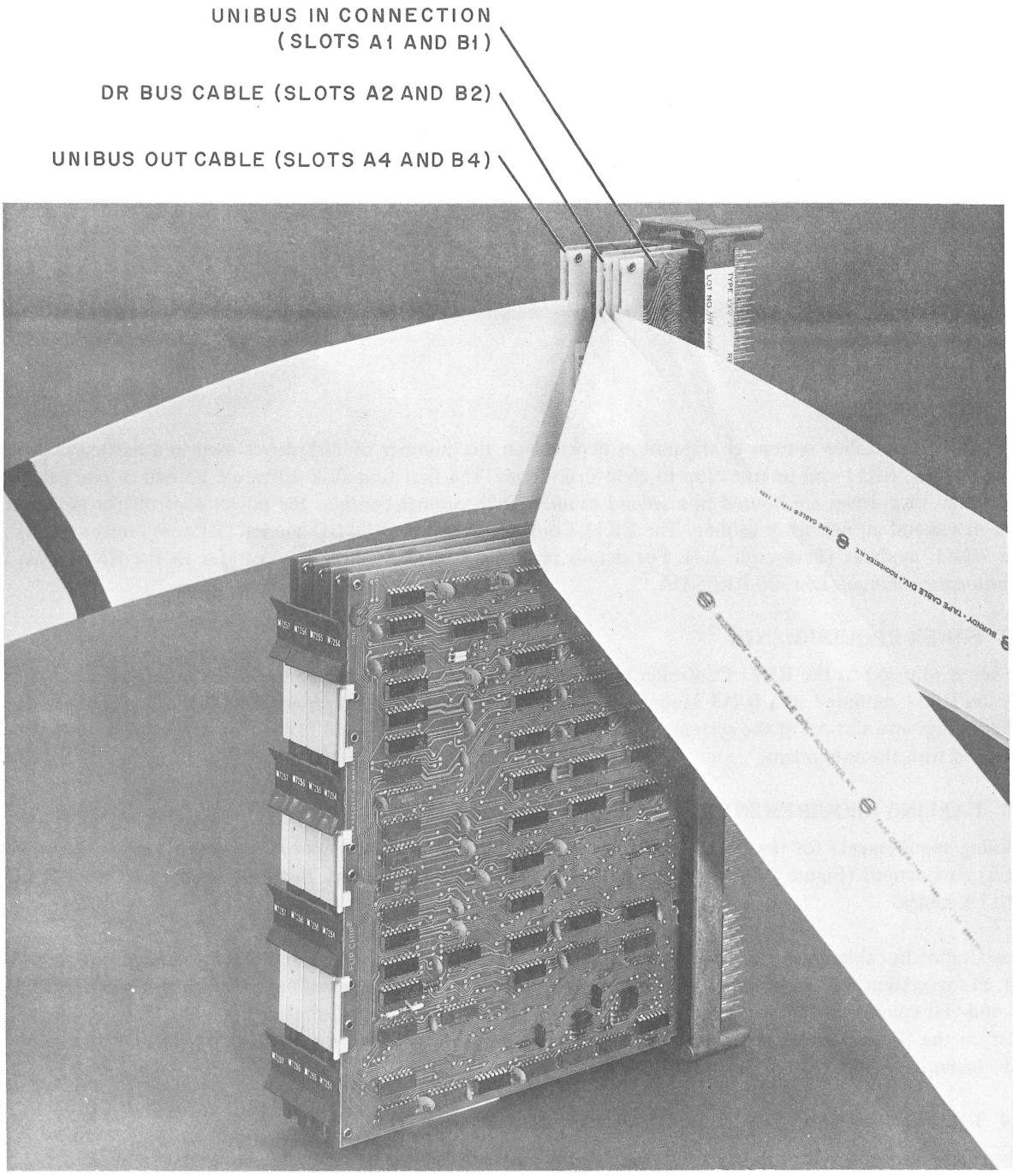



Figure 2-1 RK11 Cable Connections

## 2.5 INSTALLATION PROCEDURE

The jumpers on the modules should be in the desired configuration before the RK11 is installed. After the jumpers for option selection have been configured, the seven interrupt vector address jumpers and eight address selection jumpers of the M7257 should be configured to the proper values. Those values are, typically, 220 for the vector address and 777400 through 777416 for the address selection (refer to engineering drawing D-CS-M7257-0-1). There are also seven inhibit strobe jumpers on the M7257 module which, when cut, inhibit the loading of a particular programmable register (Paragraph 4.5.1).

When the jumpers have been properly configured, the desired interrupt level jumper, typically BR5, should be installed on the M7254 Status Control module (see the cover sheet for that module). The RK11 crystal clock switch on the M7255 Disk Control module (see cover sheet) should be positioned to AUTO for the RK11 internal crystal clock.

The RK11 Controller unit is installed in the following manner:

1. Check that wiring is not damaged, that module holddown clips are in place, and that no modules are loose.

2. Install the Unibus cabling or modules according to the RK11 configuration in the PDP-11 system (Paragraph 3.3).

3. Install the disk drive cable (DR BUS) in slots A2 and B2.

4. Connect the power wiring from the system.

Power is applied to the RK11 as the system power is turned on. The disk drives are powered independently, as described in the *RK05 Disk Drive Maintenance Manual*. When power is applied to the RK11, a processor initialize (BUS INIT) signal from the Unibus initializes the logic.

## 2.6 INSTALLATION TESTING

To ensure that the RK11 system is properly installed and operational, installation testing is performed by running RK11 diagnostic programs, including one pass of the RK11 disk data test (MAINDEC-11-D5HA-PB2), 15 minutes of the RK11 static test (MAINDEC-11-D5HA-PB1), and random exerciser (MAINDEC-11-DZRKG-A-PB). If performance of these tests fails to reveal any errors, it may be assumed that the RK11 is operational, and that it has been correctly installed. These diagnostics are supplied with the RK11, together with instructions and descriptions regarding their use.

# CHAPTER 3
# PROGRAMMING CONSIDERATIONS

## 3.1 INTRODUCTION

This chapter discusses the software interface for the RK11 Controller, including device registers and their addresses, the interrupt process, timing considerations, and data format.

## 3.2 DEVICE REGISTERS AND ADDRESSES

All RK11 software control is accomplished by seven device registers. These registers are assigned memory addresses and can be read or written into (except as noted) using instructions that refer to the respective register addresses. The seven device registers, their bit assignments, and their memory addresses are listed below. Unassigned and write-only bits are always read as zeroes. Any attempt to manipulate unassigned or read-only bits has no effect on the bit. The INIT signal refers to the initialization signal issued by the processor.

**DRIVE STATUS REGISTER (RKDS)**
**Address = 777400**

**NOTE**
**This register is a read-only register, and contains the selected drive status and current sector address.**

| DRIVE IDENT 2 1 0 | DPL | RK05 | DRU | SIN | SOK | DRY | R/W/S RDY | WPS | SC= SA | SECTOR COUNTER 3 2 1 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 15 14 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 2 1 0 |

| Bit | Designation | Description and Operation |
|---|---|---|
| 00–03 | Sector Counter (SC) | These 4 bits are the current sector address of the selected drive. Sector address 00 is defined as the sector following the sector that contains the index pulse. |
| 04 | Sector Counter Equals Sector Address (SC = SA) | Indicates that the disk heads are positioned over the disk address currently held in the sector address. |
| 05 | Write Protect Status (WPS) | Sets when the selected disk is in the write-protected mode. |

| Bit | Designation | Description and Operation |
|---|---|---|
| 06 | Read/Write/Seek Ready (R/W/S RDY) | Indicates that the selected drive head mechanism is not in motion, and that the drive is ready to accept a new function. |
| 07 | Drive Ready (DRY) | Indicates that the selected disk drive complies with the following conditions:<br>a. The drive is properly supplied with power.<br>b. The drive is loaded with a disk cartridge.<br>c. The disk drive door is closed.<br>d. The LOAD/RUN switch is set to RUN.<br>e. The disk is rotating at a proper speed.<br>f. The heads are properly loaded.<br>g. The disk is not in a DRU (bit 10 of RKDS) condition. |
| 08 | Sector Counter OK (SOK) | Indicates that the Sector Counter operating on the selected drive is not in the process of changing, and is ready for examination. If this bit is not set, the Sector Counter is not ready for examination, and a second attempt should be made. |
| 09 | Seek Incomplete (SIN) | Indicates that due to some unusual condition a Seek function cannot be completed. Can be accompanied by RKER 15 (Drive Error). Cleared by a Drive Reset function. |
| 10 | Drive Unsafe (DRU) | Indicates that an unusual condition has occurred in the disk drive, and it is unable to properly perform any operations. Reset by setting the RUN/LOAD switch to LOAD. If, when the switch is returned to RUN, the condition recurs, an inoperative drive can be assumed, and corrective maintenance procedures should be begun. Can be accompanied by RKER 15 (Drive Error). |
| 11 | RK05 Disk on Line (RK05) | Always set, to identify the selected disk drive as RK05. |
| 12 | Drive Power Low (DPL) | Sets when an attempt is made to initiate a new function, or if a function is actively in process when the control senses a loss of power to one of the disk drives. Can be accompanied by RKER 15 (Drive Error). Reset by a BUS INIT or a Control Reset function. |
| 13–15 | Identification of Drive (ID) | If an interrupt occurs, these bits will contain the binary representation of the logical drive number that caused the interrupt. |

**ERROR REGISTER (RKER)**
**Address = 777402**

**NOTE**
**This is a read-only register.**

| DRE | OVR | WLO | SKE | PGE | NXM | DLT | TE | NXD | NXC | NXS | UNUSED | CSE | WCE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 3 2 | 1 | 0 |

| Bit | Designation | Description and Operation |
|---|---|---|
| | Write Check Error (WCE) | Indicates that an error was encountered during a Write Check function as a result of a faulty bit comparison between disk data and memory data. Clears upon the initiation of a new function. This is a soft error condition. |
| 01 | Checksum Error (CSE) | Sets while performing a Read Check or a Read function as a result of a faulty recalculation of the checksum. Cleared upon the initiation of any new function. This is a soft error condition. |
| 02–04 | Unused | |

The remaining bits of the RKER are all hard errors, and are cleared only by a BUS INIT or a Control Reset function.

| | | |
|---|---|---|
| 05 | Nonexistent Sector (NXS) | Indicates that an attempt was made to initiate a transfer to a sector larger than $13_8$. |
| 06 | Nonexistent Cylinder (NXC) | Indicates that an attempt was made to initiate a transfer to a cylinder larger than $312_8$. |
| 07 | Nonexistent Disk (NXD) | Indicates that an attempt was made to initiate a function on a nonexistent drive. |
| 08 | Timing Error (TE) | Indicates that a loss of timing pulses for at least 5 $\mu$s has been detected. |
| 09 | Data Late (DLT) | Sets during a Write or Write Check function when the multibuffer file is empty and the operation is not yet complete. Sets during a Read function when the multibuffer file is filled and the operation is not yet complete. |
| 10 | Nonexistent Memory (NXM) | Sets if memory does not respond with a SSYN within 20 $\mu$s of the time when the RK11 becomes bus master during an NPR sequence. Because of the speed of the RK05 Disk Drive, it is possible that NXM will be accompanied by RKER 09 (Data Late). |

| Bit | Designation | Description and Operation |
|---|---|---|
| 11 | Programming Error (PGE) | Indicates that RKCS 10 (Format) was set while initiating a function other than Read or Write. |
| 12 | Seek Error (SKE) | Sets if the disk head mechanism is not properly positioned while executing a normal Read, Write, Read Check, or Write Check function. The control checks 16 times before flagging this error. A simple jumper change will force the control to check just once. |
| 13 | Write Lockout Violation (WLO) | Sets if an attempt is made to write on a disk that is currently write-protected. |
| 14 | Overrun (OVR) | Indicates that, during a Read, Write, Read Check, or Write Check function, operations on sector $13_8$, surface 1 of cylinder address $312_8$ were finished, and the RKWC has not yet overflowed. This is essentially an attempt to overflow out of a disk drive. |
| 15 | Drive Error (DRE) | Sets if one of the drives in the system senses a loss of either ac or dc power and a function is either initiated or in process while the selected drive is not ready or in some error condition. |

**CONTROL STATUS REGISTER (RKCS)**
**Address = 777404**

| ERR | HE | SCP | X | IBA | FMT | EXB | SSE | RDY | IDE | EX. MEM. | | FUNCTION | | | GO |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | 1 | 0 | 2 | 1 | 0 | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Bit | Designation | Description and Operation |
|---|---|---|
| 00 | GO (Write Only) | Loaded by the operator. Causes the control to carry out the function contained in bits 01 through 03 of the RKCS (Function). Remains set until the control actually begins to respond to GO, which may take from 1 $\mu$s to 3.3 ms, depending on the current operation of the selected disk drive (to protect the format structure of the sector). |

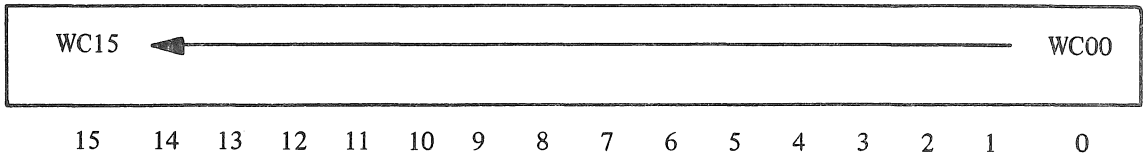
| Bit | Designation | Description and Operation |
|---|---|---|
| 01–03 | Function (Read/Write) | The Function register, or function bits, are loaded with the binary representation of the function to be performed by the control when a GO command is initiated. These bits are loaded by the program and cleared by BUS INIT. They retain the function until altered by the program or cleared, enabling the user to continue from a soft error condition with GO. A description of each of the eight functions is given in Paragraph 1.3.2. The binary codings are as follows: |

| Bit 2 | Bit 1 | Bit 0 | Operation |
|---|---|---|---|
| 0 | 0 | 0 | Control Reset |
| 0 | 0 | 1 | Write |
| 0 | 1 | 0 | Read |
| 0 | 1 | 1 | Write Check |
| 1 | 0 | 0 | Seek |
| 1 | 0 | 1 | Read Check |
| 1 | 1 | 0 | Drive Reset |
| 1 | 1 | 1 | Write Lock |

| | | |
|---|---|---|
| 04, 05 | Memory Extension (MEX) (Read/Write) | Reserved for extended bus addresses used in conjunction with the RKBA. This 2-bit counter increments each time the RKBA overflows. A bus DATO to these bits overrides any RKBA overflow. Loaded by the program and cleared by BUS INIT. Use of these bits is intended for systems equipped with a memory larger than 32K words. |
| 06 | Interrupt on Done Enable (IDE) (Read/Write) | When set causes the control to issue a bus request and interrupt to vector address 220 if:<br>a. A function has completed activity.<br>b. A hard error is encountered.<br>c. A soft error is encountered and bit 08 of the RKCS (SSE) is set.<br>d. RKCS 07 (RDY) is set and GO is not set. |

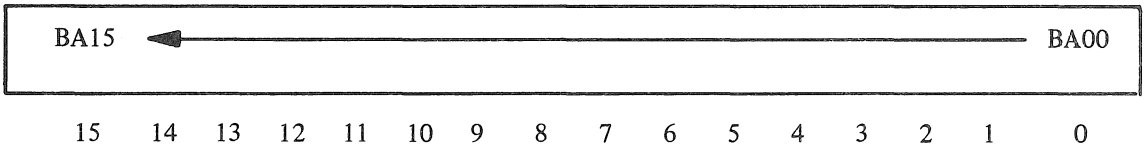
| Bit | Designation | Description and Operation |
|---|---|---|
| 07 | Control Ready (RDY) (Read Only) | Indicates that the control is ready to perform a function. Set by INIT, a hard error condition, or by the termination of a function. Cleared by GO being set. |
| 08 | Stop on Soft Error (SSE) (Read/Write) | If a soft error is encountered when this bit is set:<br>a. All control action will stop at the end of the current sector if RKCS 06 (IDE) is reset, or<br>b. All control action will stop and a bus request will occur at the end of the current sector if RKCS 06 (IDE) is set. |
| 09 | Extra Bit (EXB) | For the RK11-D and RK11-E, EXB is unused. |
| 10 | Format (FMT) (Read/Write) | FMT is under program control, and must be used only in conjunction with normal Read and Write functions. Used to format a new disk pack or to reformat any sector erased due to control or drive failure. Alters the normal Write operation, under which the header is rewritten each time the associated sector is rewritten, in that the head positioner is not checked for proper positioning before the Write. Alters the normal Read operation in that only one word, the header word, is transferred to memory per sector. For example, a 3-word Read function in Format mode will transfer header words from three consecutive sectors to three consecutive memory locations for software checking. |
| 11 | Inhibit Incrementing the RKBA (IBA) (Read/Write) | Inhibits the RKBA from incrementing during a normal transfer function. This allows data transfers to occur to or from the same memory location throughout the entire transfer operation. |
| 12 | Unused | |
| 13 | Search Complete (SCP) (Read Only) | Indicates that the previous interrupt was the result of some previous Seek or Drive Reset function. Cleared at the initiation of any new function. |
| 14 | Hard Error (HE) (Read Only) | Sets when any of RKER 05 – 15 are set. Stops all control action, and processor reaction is dictated by RKCS 06 (IDE), until cleared, along with RKER 05 – 15, by INIT or a Control Reset function. |
| 15 | Error (ERR) (Read Only) | Sets when any bit of the RKER sets. Processor reaction is dictated by RKCS 06 and RKCS 08 (IDE and SSE). Cleared if all bits in the RKER are cleared. |

**WORD COUNT REGISTER (RKWC)**
**Address = 777406**




| Bit | Designation | Description and Operation |
|---|---|---|
| 00-15 | WC00-WC15 (Read/Write) | The bits in this register contain the 2's complement of the total number of words to be affected or transferred by a given function. The register increments by one after each word transfer. When the register overflows (all WC bits go to zero), the transfer is complete and RK11 operation is terminated at the end of the present disk sector. However, only the number of words specified in the RKWC are transferred. |

**CURRENT BUS ADDRESS REGISTER (RKBA)**
**Address = 777410**




| Bit | Designation | Description and Operation |
|---|---|---|
| 00–15 | BA00–BA15 (Read/Write) | The bits in this register contain the bus address to or from which data will be transferred. The register is incremented by two at the end of each transfer. If the system has extended memory, the RKBA will overflow to the EX MEM (bits 04 and 05 of the RKCS) to reflect the extended bus addresses. |

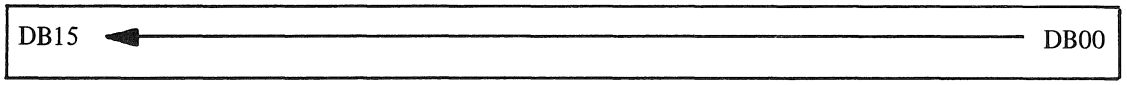
**DISK ADDRESS REGISTER (RKDA)**
**Address = 777412**

| DRIVE SELECT | | | CYLINDER ADDRESS | | | | | | | | SUR | SECTOR ADDRESS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | 3 | 2 | 1 | 0 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**NOTE**
**This register will not respond to commands while the controller is busy. Therefore, RKDA bits are loaded from the bus data lines only in the Control Ready (RDY – bit 07 of the RKCS) state, and are cleared by BUS INIT and Control Reset. The RKDA is incremented automatically at the end of each disk sector.**

| Bit | Designation | Description and Operation |
|---|---|---|
| 00–03 | Sector Address (SA) | Binary representation of the disk sector to be addressed for the next function. |
| 04 | Surface (SUR) | When active, enables the lower disk head so that operation is performed on the lower surface; when inactive, enables the upper disk head. |
| 05–12 | Cylinder Address (CYL ADDR) | Binary representation of the cylinder address currently being selected. The largest valid address or number for the cylinder address is $312_8$. |
| 13–15 | Drive Select (DR SEL) | Binary representation of the logical drive number currently being selected. |

**DATA BUFFER REGISTER (RKDB)**
**Address = 777416**




| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| Bit | Designation | Description and Operation |
|---|---|---|
| 00–15 | DB00–DB15 (Read Only) | The bits of this register work as a general data handler in that all information transferred between the control and the disk drive must pass through this register. Loaded from the bus only while the RK11 is bus master during an NPR sequence. |

**NOTE**
**Address 777414 is unused.**

## 3.3 DATA FORMAT

Data is stored on the disk cartridge in groups of 12 sectors per track for both 16-bit (RK11-D) and 18-bit (RK11-E) options. Each of the twelve disk sectors contains 256 words and is defined by physical sector marks. These sector marks generate a sector pulse from the disk drive to the controller. Another similar physical disk mark, called an index mark, defines the starting point for the sequence of sectors. All of the sectors are formatted identically in five parts; preamble (terminated with a sync bit), header, data, checksum, and postamble (Figure 3-1).

SYNC BIT

| PREAMBLE | | HEADER | DATA | CHECKSUM | POSTAMBLE |
|---|---|---|---|---|---|
| $15_8$ Words of Zeroes | | Cylinder Address (1 Word) | $256_{10}$ ($400_8$) Words (16-Bit or 18-Bit) | Sector Checksum (1 Word) | 1 Word of Zeroes |

The preamble and postamble areas of a sector serve as boundaries before and after the information major states (header, data, and checksum) to ensure compatibility between disk drives at the cartridge level despite variations in sector pulse positioning (refer to the *RK05 Disk Drive Maintenance Manual,* DEC-00-RK05-DA).

The preamble consists of $15_8$ words of zeroes, adequate to guarantee that RD GATE will turn on during a known zero data field. The disk drive head then waits for the first one to occur (sync bit), and begins to read with the header word. For a Write function, the sync bit is automatically written by hardware following $15_8$ words of zeroes.

The header area of a sector consists of a single word containing the cylinder address from RKDA 05 – 12. Before a data transfer function is performed, the header word is read and checked against the cylinder address portion of the RKDA to ensure that the disk drive heads are positioned above the proper cylinder. The Write function always rewrites the header on the disk, using the cylinder address portion of the RKDA. The sector format for a raw (unformatted) cartridge is written under program control in conjunction with RKCS 10 (Format, FMT) (Paragraph 3.2).

The data area consists of $256_{10}$ data words. These words, like all of the words in each area of the sector, are 16 bits long in the RK11-D and 18 bits long in the RK11-E.

The checksum area of a sector consists of a single word that is the checksum of all 256 data words. This checksum is compared by the controller to the checksum that it calculates itself whenever a Write Check, Read, or Read Check function is performed within a given sector. For a Write function, the controller calculates a checksum and writes it on the disk cartridge following the last data word.

Short portions (less than 256 data words) of a sector may be read or written as long as this short sector is the last sector of the data transfer. When a short sector is written, the remainder of the sector is automatically written with zeroes. The Write Check function may be performed on a short sector as long as the number of words write checked is equal to the number of words previously written into the sector. Because the Read Check function is essentially a parity check, it must be performed on a whole-sector basis only.

## 3.4 PROGRAM INTERRUPTS

A program interrupt is initiated by an interrupt request, which can only occur if RKCS 06 (IDE, Interrupt Done Enable) is set. Six hardware conditions can generate an interrupt request to the processor:

a. The occurrence of a hard error condition (RKCS 14 – HE).

b. The presence of a soft error condition (RKER 00 – WCE) or RKER 01 (CSE) if RKCS 08 (SSE) is set.

c. Completion of transfer of the designated number of words.

d. The acceptance (Address Acknowledge) of a Seek or Drive Reset function by the selected disk drive, freeing the controller for hardware polling or a new function.

e. The initiation of a Write Lock function on a disk drive, indicating that the controller is free to perform a new function.

f. The completion of hardware polling (RKCS 13 – SCP), indicating that the disk drive in the DR SEL bits of the RKDA has completed a Seek or Drive Reset function (RKDS 06 – R/W/S RDY).

The interrupt request of the RK11 Controller can be configured at BR levels 4, 5, 6, or 7. The RK11 is typically set at level BR5.

Because of the format structure of the RK11, any interruption of the Write function cannot be tolerated until the end of the current sector, as it would result in what would be essentially an unformatted disk cartridge. As a result, outside intervention is inhibited until the current sector is completed, including Control Reset functions and processor initialize (BUS INIT) signals. This means that such functions as Control Reset, Seek, and Write Lock, which take only a few microseconds to initiate, can take as long as 3.3 ms if initiated during a Write function. For this reason, Seek, Drive Reset, and Write Lock functions cause an interrupt as soon as the function is initiated, provided that RKCS 06 (IDE) is set.

### 3.5 TIMING CONSIDERATIONS

RK11 timing is a consideration in the performance of overlapping Seek or Drive Reset functions, because these functions can be initiated on free disk drives while previous Seek or Drive Reset functions are in process on other disk drives. Thus, up to eight disk drives can be performing a Seek or Drive Reset function simultaneously. The hardware poll logic of the Disk Control generates an interrupt when a disk drive has completed the Seek or Drive Reset function (RKDS 06 – R/W/S RDY set). When a Seek or Drive Reset function has been initiated on the disk drive (Address Acknowledge), an interrupt request occurs if RKCS 06 (IDE) is set. This process normally requires 1 μs, but may range up to 3.3 ms if an attempt is made to abort a Write function. Head movement, however, may take as long as 80 ms, after which a second interrupt (RKCS 13 – Search Complete) occurs (if Interrupt Done Enable is set). In the interval between these two events, the selected disk drive is busy moving its heads, but the controller is free to perform any RK11 function on any other available disk drive. Once a disk drive has begun moving its head mechanism, only a Drive Reset function can stop it. An attempt to perform any other function on a disk drive whose heads are in motion results in a hard error condition.

The data transfer (Read, Write, Read Check, and Write Check) functions all begin with an automatic Seek function. This allows the user of a single disk drive system to forget about the Seek function completely and initiate data transfer functions directly. The hardware poll logic is initiated only for Seek and Drive Reset functions and not for the Seek portion of data transfer functions.

### 3.6 POWER FAIL

If any of the disk drive power supplies senses a loss of either ac or dc power, no new functions can be initiated. If only an ac power loss is sensed and a function is in process, the current disk sector is completed. If, at the beginning of the next sector, an ac power loss is still sensed but dc power is satisfactory (e.g., momentary line power fluctuations), the controller waits for ac power to return before starting operation on the next sector, as long as the next sector is in the same cylinder. However, if the heads must be moved to reach the next sector, an error condition is generated (RKER 155 – Drive Error, and RKDS 12 – Drive Power Low) and the function is aborted. If, at the beginning of the next sector, a loss of dc power is sensed, the same error condition is generated. That condition (DRE and DPL) is also set if a dc power loss occurs while the controller is actively transferring data to or from a disk drive.

# CHAPTER 4
# DETAILED DESCRIPTION

## 4.1 INTRODUCTION

This chapter provides a detailed logic level description of each of the four RK11 modules (Figure 1-2): Status Control, Disk Control, Data Paths, and Bus Control. Much of the logic is implemented by means of MSI integrated circuits (ICs). Appendix A to this manual provides logic diagrams containing pin designations for such ICs.

## 4.2 STATUS CONTROL

The Status Control logic of the M7254 module initiates the programmable functions of the RK11 Controller and monitors logic status conditions by means of the programmable Control Status register (RKCS) and Word Count register (RKWC) and the Error register (RKER).

The RKCS receives function and control information from the Unibus and implements it by initiating and directing RK11 functions, generating interrupt requests, and monitoring RK11 status information, which it transmits to the Data Paths via the Internal Bus A Multiplexers.

The RKWC receives data transfer word count information from the Unibus, is incremented for each word of data that is transferred, and overflows (WC OVF) to indicate the end of NPR transfers.

The RKER provides error status information to the RKCS control logic and to the programmer via the Internal Bus A Multiplexers.

The Status Control also contains the bus request level selection jumper for the Unibus interrupt level lines. The RK11 Controller is normally set at bus request level 5 (BR5). Status Control logic is contained in engineering drawing D-CS-M7254-0-1, sheets 1 through 6.

### 4.2.1 RKCS, Function, and Control Logic

The function logic of the RKCS determines the function to be performed and provides control signals for each function. The control logic directs RK11 logic operations, supplies status information to the RKCS, and generates interrupt requests to the Bus Control.

The function bits (RKCS 01-03 – FUN) from the D-type flip-flop ICs (see ST 4) are loaded into the latch IC on the trailing edge of GEN CLR. Buffered Function (B FUN) 00 – 02 from the Buffered Function register feed a decoder IC (see ST 3), which decodes the function bits for one of eight RK11 functions and asserts the appropriate signal in the RK11 logic to indicate which function has been selected. The memory extension bits (RKCS 04 and 05) are loaded into a counter IC (see ST 4) when the Bus Control asserts LOAD RKCS, and extend the RKBA for added memory addresses above 177777. The counter is cleared by INIT and counts when RKBA OVF is asserted by the data paths. EX MEM 0 and EX MEM 1 are driven onto the Unibus address (A) lines 16 and 17, respectively, when RK NPR MASTER is asserted by the Bus Control.

The RK11 control logic is initiated by GO (RKCS 00). The GO flip-flop (see ST 2) is loaded from BUS D00 on the trailing edge of LOAD RKCS LO. WT GATE unasserted and GO set triggers a 500 ns one-shot which generates T1, clearing the GO flip-flop, generating a GEN CLR pulse, and triggering a 250 ns one-shot (NEW FUN) with its trailing edge if no hard error exists and the RK11 function currently being performed is not a Control Reset. GEN CLR is also generated when an INIT pulse occurs.

When GO initiates a function, CNTRL RDY is unasserted to indicate that a function is in process. CNTRL RDY is asserted when HE (hard error), INIT, POLL DONE, or 1 → XFC is asserted. All of the RK11 interrupt request conditions (e.g., RKWC overflow) except hard errors are indicated by either POLL DONE from the Disk Control or 1 → XFC. With RDY set, a POLL DONE pulse momentarily unasserts B CNTRL RDY (Buffered Control Ready), after which a Unibus interrupt request (BR) is generated from the Bus Control (BUS 3) if Interrupt Done Enable (RKCS 06 – IDE) is set. When RDY is clear, indicating that a function is in process, a hard error or a 1 → XFC pulse sets RDY and generates an interrupt request from the Bus Control if IDE is set. When B CNTRL RDY goes unasserted, IDE is unasserted (interrupts not enabled) or HE is asserted (hard error), STOP POLL is generated (see ST 2), disabling any hardware poll in the Disk Control.

The HE (RKCS 14) and ERROR (RKCS 15) bits maintain RK11 error status from the RKER (see ST 2). Assertion of any of the error conditions in the RKER except Write Check Error (RKER 00 – WCE) and Checksum Error (RKER 01 – CSE) sets HE. Data Late (RKER 09 – DLT) or Nonexistent Memory (RKER 10 – NXM) asserted sets HE when WT GATE is unasserted by the Disk Control. DLT, HE, or NXM asserted when a 0 → NPR pulse is generated in the Bus Control asserts STOP NPRS at the end of the NPR sequence, clearing the NPR EN flip-flop in the Data Paths. GEN CLR or INIT SENSE (i) (from BUS INIT L) also generates STOP NPRS. ERROR is generated for all RKER error conditions. WCE or CSE asserted generates SOFT ERR.

### 4.2.2 RKWC Logic

The programmable RKWC consists of four 4-bit binary counter ICs that are parallel loaded from the Unibus D lines (BUS D00 through D15) with the 2's complement of the number of data words to be transferred when LOAD RKWC LO and LOAD RKWC HI are asserted by the Bus Control. The RKWC is incremented by a 0 → NPR pulse from the Bus Control, or for a Read Check during the data major state when LAST BIT · CLK is asserted. LAST BIT · CLK is asserted when the last bit (LAST BIT asserted) of a data word is transferred to or from the RK11. When RKWC overflows, indicating that the stipulated number of data words have been transferred, the WC OVF flip-flop is set. When COUNT SA from the Data Paths increments the RKDA and FILE DONE is asserted, 1 → XFC is generated, setting RDY (RKCS 07) and initiating an interrupt request if IDE is set. Pulse 1 → XFC is also generated for Seek or Drive Reset functions when ADDRESS ACKNOWLEDGE (ADD ACK) is asserted by Disk Control, indicating that the selected disk drive has accepted the cylinder address from the RKDA.

For an error condition with SSE (RKCS 08) set, 1 → XFC is generated when COUNT SA occurs to stop the RK11 as a result of any soft error condition. For a Write Lock function (WT LOCK asserted), 1 → XFC is generated when NEW FUN occurs.

### 4.2.3 Internal Word Count Logic

The Internal Word count Logic (see ST 3) consists of three synchronous 4-bit counter ICs, which are controlled in the RK11 Status Control by the Major State register. One of the counters maintains the bit count of the current data word (BC00 – BC03). The other two counters maintain the internal word count (IWC00 – IWC07) of the major state. The shift register determines the major state (idle, preamble, header, data, checksum, or postamble) in which a function is being performed.

A shift in the Major State register occurs at the end of any of the major states (COUNT MSR). During a Read, Read Check, Write Check, or the Read Header portion of a Write function, when RD GATE is asserted while the selected head is positioned over the $15_8$ words of zeroes that make up the preamble portion of a sector, the first clock pulse thereafter shifts the Major State register to header. During a Write function, when WT GATE is asserted while the head is positioned over an interrecord gap, the first clock pulse from the crystal oscillator shifts the Major State register from idle to preamble, after which the $15_8$ words of zeroes are written and END OF SYNC is generated, shifting the Major State register to the header major state.

In the header major state, the last bit of the word generates the shift pulse. RD HEADER indicates when the header is being read for a Write or Write Check function. At the end of the data major state, COUNT MSR is generated when DATA OVF is asserted, indicating that $256_{10}$ words have been transferred and have caused the IWC to overflow. This shifts the Major State register to checksum, until the last bit of the checksum word again generates COUNT MSR. At the end of the postamble major state, CLR MSR clears the Major State register.

CLR MSR is asserted when a hard error occurs, when GEN CLR or SECTOR PULSE is generated, or when 0 → MSR is asserted. GEN CLR or SECTOR PULSE (see ST 4) indicates that GO has been set or that a SECTOR PULSE has occurred. Pulse 0 → MSR (see ST 4) is generated by a 250 ns one-shot on the trailing edge of LAST WORD DONE, which is asserted for a Read, Read Check, or Write Check function during the first bit of postamble, and for a Write function at the end of postamble during LAST BIT · CLOCK.

CLR MSR clears the shift register and the BC and IWC and sets IDLE. This enables COUNT MSR, which, at the next CLK, clears BC, IWC, and IDLE and asserts PREAMBLE in the Major State register. For a Read, Read Check, or Write Check function, COUNT MSR shifts the shift register to generate HEADER when SER RD DATA is asserted. For a Write function, END OF SYNC is generated during preamble when the word count reaches 15, generating COUNT MSR and shifting the shift register to HEADER.

In the data major state, the IWC counts $256_{10}$ data words, then DATA OVF causes another COUNT MSR, which clears the BC and IWC and shifts the Major State register to CHECKSUM. LAST BIT asserted at the end of the checksum major state generates another COUNT MSR, again clearing the BC and IWC and shifting the shift register to POSTAMBLE. At the end of the postamble major state, the Major State register is cleared by CLR MSR from 0 → MSR, which also clears BC and IWC.

### 4.2.4 RKER and Error Detection Logic

RKER 00 and 01 are cleared by GEN CLR, and RKER 05 through 15 are cleared by INIT, which can be generated in one of three ways:

a. When BUS DC LO L and BUS AC LO L are asserted by the Unibus.

b. For the Unibus to assert BUS INIT for system initialization, setting the INIT SENSE flip-flop, which, with WT GATE unasserted, generates a low to the RC circuit of a one-shot, triggering it and generating an INIT pulse in the control.

c. For the one-shot to be triggered by a Control Reset function (CONTROL RESET asserted by the RKCS function logic) when a T1 pulse is generated by the RKCS control logic, indicating that GO has been set.

*RKER 00 (Write Check Error – WCE)* is set during a Write Check function in the checksum major state when BAD BIT is asserted. BAD BIT is asserted by the error detection logic when a header, data, or checksum bit read from the disk does not match the corresponding bit of the data from memory or the checksum calculated in the Disk Control (RD DATA = WT DATA unasserted). Once BAD BIT is set, a feedback circuit ensures that it will not be cleared by the next clock pulse, even if subsequent bit comparisons are favorable.

*RKER 01 (Checksum Error – CSE)* is set during a Read or Read Check function when a BAD BIT is asserted during the checksum major state. BAD BIT in this case is set when RD DATA = WT DATA is unasserted at the next CLK pulse, indicating a discrepancy between the checksum taken from the disk and the checksum calculated in the Disk Control.

*RKER 05 (Nonexistent Sector – NXS)* is set for a data transfer (XFER FUNCTION) with a sector address larger than $13_8$ when NEW FUN is generated by the RKCS control logic. NEW FUN is generated 500 ns after GO (RKCS 00).

*RKER 06 (Nonexistent Cylinder – NXC)* is set if the disk drive has received a cylinder address greater than $202_{10}$ and FIRST SEEK DONE is unasserted. (ILLEGAL ADDRESS is asserted by the disk drive.) FIRST SEEK DONE is asserted if ADDRESS ACKNOWLEDGE (ADD ACK) has been asserted by the disk drive. ADD ACK indicates that the disk drive has accepted the cylinder address.

*RKER 07 (Nonexistent Disk – NXD)* is set if DRIVE OK is unasserted by the Disk Control when a NEW FUN pulse is generated. DRIVE OK unasserted indicates that the selected disk drive does not exist in the RK11 system.

*RKER 08 (Timing Error – TE)* is set during header, data, or checksum (GEN DATA asserted) if the CLK pulse train is broken for 5 $\mu$s. This timing error indicates that a break in the DSK CLK pulse train exists on the disk, or that the RK11 WT CLK in the Disk Control has failed.

*RKER 09 and 10* are generated on other modules.

*RKER 11 (Programming Error – PGE)* is set when a NEW FUN pulse occurs in the Format mode (FMT asserted) and the function is not a Read or Write. Only Read or Write functions can be performed in the Format mode.

*RKER 12 (Seek Error – SKE)* is set if 16 bit-by-bit checks of the disk drive header and the RKDA cylinder address have been completed and the selected disk drive is still not positioned over the correct cylinder. A bit discrepancy in the header word unasserts RD DATA = WT DATA from the Disk Control, which sets BAD BIT on the next CLK pulse for a Read or Read Check function. During a Write or Write Check function, in the header major state, RD DATA = WT DATA unasserted sets BAD BIT if RD HEADER is asserted by the Disk Control. When BAD BIT is clear, indicating no header error, CHECK HEADER sets the HEAD OK flip-flop. CHECK HEADER is asserted at the end of the header major state on the trailing edge of LAST BIT · CLK when WT GATE is unasserted by the Disk Control and if the RK11 is not in the Format mode. When BAD BIT is set, CHECK HEADER clocks BAD BIT into a 4-bit binary counter IC. If the correct header is not indicated (HEAD OK set) after 15 more CHECK HEADER signals, then SKE is set. If, however, the correct header is found, HEAD OK loads all zeroes into the Bad Header Counter on the trailing edge of the next CHECK HEADER pulse. The counter is also cleared by ADD ACK from the Disk Control or GEN CLR from the control logic.

*RKER 13 (Write Lock Out – WLO)* is set when WT GATE and WT PRCT STATUS are generated by the Disk Control. WT GATE asserted initiates a Write function to a disk drive, and WT PRCT STATUS (RKDS 05, WPS) indicates that the selected disk drive is currently write-protected.

*RKER 14 (Overrun – OVR)* is set if ILLEGAL ADD is asserted by the Disk Control from the DR BUS and FIRST SEEK DONE is asserted. This indicates an attempt to overflow out of the disk drive.

*RKER 15* is generated on another module.

### 4.2.5 Internal Bus A Multiplexers

The Internal Bus A Multiplexers consist of eight 4-to-1 Line Data Multiplexer ICs. The RKA 02 and RKA 01 signals from the Bus Control select either the RKCS, RKWC, RKER, or RKDS to be multiplexed to the Internal Bus D Multiplexers in the Data Paths (INT BUS A 00 – 15). These registers are selected in the multiplexers according to Table 4-1 of Paragraph 4.4.7.

## 4.3 DISK CONTROL

The Disk Control logic of the M7255 module controls the functions of the disk drives according to commands received from the Status Control and acts as an intermediary, organizing information from and feeding information to other logic areas.

The DR BUS conveys disk drive status information for RKDS 00 – 11 and includes control signals DR AC LO, DR DC LO, ADDress ACKnowledge, ILLEGAL ADDress, LAST SECTOR (Index Pulse), DR BUS RD CLK, and DR BUS RD DATA. CLK from the Disk Control is the RK11 WT CLK for a Write function, or the DSK RD CLK from the selected disk drive for Read, Read Check, or Write Check functions.

Disk Control logic is contained in engineering drawing D-CS-M7255-0-1, sheets 1 through 7. In the engineering drawings, the boxes labeled 13-11003-01 represent IC packages of pullup/pulldown resistors, with each box containing 28 resistors.

### 4.3.1 Head Movement

Head movement of a selected disk drive is controlled in the RK11 by the MOVE HEADS flip-flop. MOVE HEADS is cleared by INIT, ADD ACK, ILLEGAL ADD, or HE (Hard Error). ADD ACK from the disk drive indicates that the drive has accepted a cylinder address and will control its own head movement. ILLEGAL ADD indicates that the cylinder address sent to the disk drive is nonexistent and results in no head movement.

MOVE HEADS is set for all functions except Control Reset and Write Lock on the trailing edge of 1 → MOVE HEADS. DRIVE OK indicates that RKDS 07 (DRY) is set and either RKDS 06 (R/W/S RDY) is set or the function is a Drive Reset. DR PWR LO indicates that DR AC LO or DR DC LO is asserted from the disk drive. 1 → MOVE HEADS is asserted by NEW FUN or CYL OVF to direct head movement to a new cylinder. For a normal Write or Write Check function (FMT unasserted), 1 → MOVE HEADS generates RD HEADER, indicating that the header word on the disk is to be read and checked before a function begins. RD HEADER is cleared by HEAD OK from the Status Control, which indicates a correct header word, and by GEN CLR.

To check the header or checksum for a Write Check function, ADD 00 is compared bit-by-bit to SER RD DATA via an Exclusive-OR gate. For a Write Check, Read, or Read Check function, the calculated checksum is compared bit-by-bit to the checksum from the disk. Each favorable bit comparison for any function generates RD DATA = WT DATA. The negation of RD DATA = WT DATA indicates a bit discrepancy, which sets the BAD BIT flip-flop in the Status Control error detection logic.

A 4-bit Exclusive-OR comparator (DISK 2) compares the desired sector address (RKDA 00 – 03) with the Sector Counter (RKDS 00 – 03) derived from DR BUS SEC CNTR 0 – 3. If they are the same, SC = SA (RKDA 04) is generated, indicating that the disk drive has reached the desired sector.

### 4.3.2 RD GATE and WT GATE

The WT GATE and RD GATE flip-flops control all disk drive Write and Read operations. Either RD GATE or WT GATE is set if SECTOR END is unasserted by the Data Paths and R/W gate EN is asserted. (B CNTRL RDY is unasserted by the Status Control, POLL is unasserted, DR PWR LO is unasserted, and R/W/S RDY (RKDS 06) is asserted). The data input of the WT GATE flip-flop is asserted only for a Write function when SC = SA is asserted and RD HEADER is unasserted (header has successfully been checked). WT GATE sets approximately 10 $\mu$s after the assertion of SECTOR PULSE. SECTOR PULSE is generated by the disk (DR BUS SEC PULSE) to indicate a new sector.

The data input of the RD GATE flip-flop is asserted when reading a header word for a Write or Write Check function, or when RD GATE EN is asserted by the Status Control (Read, Read Check, or Write Check function) and SC = SA is asserted. RD GATE sets approximately 85 $\mu$s after the assertion of SECTOR PULSE. Both RD GATE and WT GATE are cleared by CLR MSR from the Status Control.

For a Read function, serial read data from the disk drive (DR BUS RD DATA) sets the SER RD DATA flip-flop, which is sampled by the leading edge of CLK and cleared by the trailing edge of CLK when RD GATE is asserted. A 1 bit (DR BUS RD DATA L asserted) sets SER RD DATA.

For Write functions, WT GATE controls the use of the WT CLK pulse train for clocking the WT DATA flip-flop and driving the serial write data onto the DR BUS (DR BUS WT DATA + CLK L). The oscillator pulses complement a flip-flop, which, when set, generates CLK pulses, gating serial WT Data to the DR BUS driver. This serial data and WT CLK pulses supply DR BUS WT DATA + CLK L to the selected disk drive.

The WT DATA flip-flop supplies either data, header, or checksum information to the disk. Header or checksum information is provided serially from the Adder Shift register. Serial data is provided by RKDB 00 of the Data Paths, the output of the Data Buffer register. END OF SYNC asserted from the Status Control indicates the end of the preamble, setting WT DATA on the next clock pulse (SYNC BIT).

### 4.3.3 Adder Register

For a Write, Write Check, Read, or Read Check function, the cylinder address is serially compared to the disk drive header word in the Status Control. Bits 05 – 12 of the Adder Shift register (16 bits for the RK11-D, 18 bits for the RK11-E) are contained on a pair of parallel-loaded (from RKDA) flip-flop shift registers. Because these are parallel-loaded, individual bits may be preset before the contents are shifted. RKDA 05 – 12, containing the desired cylinder address, are applied to the data inputs of ADD 05 – 12, which have been cleared by a CLR pulse at the onset of a new function. The initiation of PREAMBLE, asserted by the Status Control with the hardware poll off, generates LOAD CYL ADD, which places RKDA 05 – 12 into ADD 05 – 12.

For a Write function, the cylinder address is written serially on the disk drive as the header word. To check the header for any function, SER RD DATA is compared bit-by-bit to the cylinder address held in the Adder register.

The checksum is calculated by serially adding each bit of a sector as it is transferred. During a Write, the accumulated checksum is then written onto the disk at the end of the sector. For a Read, Read Check, or Write Check, the accumulated checksum word is compared by the Status Control to the checksum word that is written on the disk.

### 4.3.4 Drive Selection and Hardware Poll

The drive selection logic selects one of eight possible disk drives on DR BUS from either the programmable RKDA 13 – 15 or the hardware poll logic (DISK 1). A multiplexer IC selects RKDA 13 – 15 or DR CNT 00 – 02 as controlled by the hardware poll logic. If a search complete interrupt occurs, DR CNT 00 – 02 are loaded into ID 00 – 02 (RKDS 13 – 15) identifying the disk drive that caused the interrupt.

The hardware poll logic monitors the disk drives for completion of a Seek or Drive Reset function, generates an interrupt if Interrupt Done Enable (RKCS 06, IDE) is set, identifies the polled disk drive in RKDS 13 – 15, and asserts Search Complete (RKCS 13, SCP). Polling of the disk drives is initiated through the generation of POLL, which is generated when RK INT REQ and Gate DATA → BUS D are unasserted by the Bus Control, and STOP POLL is unasserted from the Status Control. STOP POLL asserted indicates that IDE is clear, the control is busy, or a Hard Error (HE) exists. Search Complete (RKCS 13, SCP) indicates that the last interrupt to occur was a result of a hardware poll operation after a Seek or Reset function has been completed.

TEST POLL monitors the MASK flip-flops. Each MASK flip-flop (0 – 7) represents one of eight possible disk drives, and is set when SEEK STARTED is asserted. SEEK STARTED is generated for a Seek or Drive Reset function when ADD ACK is asserted from the selected disk drive and sets the appropriate MASK flip-flop to identify the drive performing the Seek or Drive Reset function. When TEST POLL is asserted, if the selected MASK flip-flop is set and if the selected disk drive has asserted R/W/S RDY, indicating that the disk drive is ready for another function, then INT SCH CMP is set. INT SCH CMP set, in turn, generates POLL DONE, which initiates an interrupt in the Bus Control by momentarily unasserting B CNTRL RDY if IDE (RKCS 06) is set. When the RK11 becomes bus master (RK INT MASTER asserted by the Bus Control), then SCH CMP is generated (RKCS 13, SCP) and POLL INTR DONE is generated, clearing INT SCH CMP and whichever MASK flip-flop is set.

### 4.3.5 Drive Error and Drive Power Low

Drive Error (RKER 15, DRE) sets Drive Power Low (RKDS 12, DPL) when DR PWR LO is asserted by DR AC LO or DR DC LO. When 1 → MOVE HEADS is asserted, DR PWR LO, DR UNSAFE (RKDS 10, DRU), or SIN (RKDS 09) sets DRE. SIN FLAG from the hardware poll logic sets DRE when SIN (RKDS 09) is asserted (except during a drive reset) by the currently selected disk drive during hardware poll. Also, DR UNSAFE, DR DC LO, or SIN (except during a drive reset) asserted or DRY unasserted sets DRE when XFER FUNCTION and FIRST SEEK DONE (ADD ACK previously asserted) are asserted by the Status Control.

### 4.3.6 Drivers and Receivers

All bus signals are received with Unibus-type receivers with built-in noise immunity, either 380s or 7384s, depending upon the individual function involved and its requirements.

All bus signals are driven with 8881 Unibus-type drivers, which are open-collector NAND gates, each capable of sinking 50 mA.

### 4.3.7 Crystal Oscillator

The WT CLK pulse train (DISK 4) is generated by a crystal oscillator with an AUTO/MANUAL switch. When the switch is in the AUTO position, BD2 is grounded and the crystal oscillator runs its normal pattern. For maintenance purposes, the switch may also be placed in the MANUAL position, shutting off the feedback path and making it possible to introduce a separate train of clock pulses into WT CLK via pin BD2, bypassing the oscillator completely.

## 4.4 DATA PATHS

The Data Paths logic of the M7256 module (see engineering drawing D-CS-M7256-0-1, sheets 1–7) controls bidirectional data flow (Read or Write) between a selected disk drive and the Unibus. The Data Paths logic also controls the data flow in the RK11, and contains the programmable RKDA and RKBA registers.

For a Read function, the Disk Control supplies serial data from a selected disk drive to the In Buffer Shift register of the Data Paths. When a data word is complete, it is parallel loaded into one of the four word locations in the 4-Word File, from where it is loaded into the Out Buffer (RKDB). The data word is then multiplexed to the Bus Control and from there to the Unibus data lines via an NPR. Meanwhile, subsequent data words are transferred from the In Buffer to other locations in the 4-Word File. For a Read Check function, the file is not used.

For a Write or Write Check function, a data word is parallel loaded into the In Buffer from the Unibus D lines. Each data word, in turn, passes through the 4-Word File to the Out Buffer, which shifts serial data from RKDB 00 to the Disk Control. The Disk Control then transfers the data to the selected disk drive for a Write function, or checks data for a Write Check function.

### 4.4.1 In Buffer

The In Buffer consists of five shift register ICs that handle data transfers between the selected disk drive, the Unibus, and the 4-Word File. These ICs may be configured to handle either a 16-bit or an 18-bit data word, depending on whether the RK11 option implemented is the RK11-D or the RK11-E.

For a Write or Write Check function, the In Buffer is parallel loaded with a data word from the Unibus data lines (BUS D). The Status Control negates READ during a WT + WT CHK to enable the ICs to load, and a DATA STROBE 2 pulse from the Bus Control module clocks in the data word from the Unibus D lines to the In Buffer, from where it is parallel loaded to the 4-Word File.

For a Read function, READ is asserted, enabling shifting of the In Buffer. Each CLK IN BUFF pulse then shifts the In Buffer one bit position toward bit 00. CLK IN BUFF also loads serial data from the Disk Control (SER RD DATA (1) ) to either bit position 15 (for the RK11-D) or bit 17 (for the RK11-E). When the entire word has been assembled in the In Buffer, it is then loaded into the 4-Word File.

The In Buffer is cleared by GEN CLR from the Status Control.

### 4.4.2 4-Word File

The 4-Word File consists of five register file ICs intended to provide four 16-bit (RK11-D) or 18-bit (RK11-E) word locations of storage area (see DATA 5). It is possible to read a word from one location while simultaneously writing another word into a different location.

To write into the 4-Word File, the In Counter selects the word location into which a data word is to be written. The Data Paths control logic then asserts WT FILE, which loads the In Buffer into the selected location.

To read from the 4-Word File, the Out Counter selects the word location from which a data word is to be transferred to the Out Buffer (RKDB).

### 4.4.3 Out Buffer

The Out Buffer consists of five shift register ICs that serve to handle data between the 4-Word File and either the Disk Control or the Bus Control (via multiplexer).

During a read function, the Out Buffer transfers its contents to the Internal Bus Multiplexer. During a Write function, the Out Buffer transfers the contents of the 4-Word File to the Disk Control, which passes the data to the selected disk drive. In the case of a Write Check function, the Disk Control checks the data, instead of transferring it to a disk drive as would occur in a Write function.

### 4.4.4 RKDA

The programmable RKDA register consists of four counter ICs configured to select that portion of a given disk on which a function is about to be or is currently being performed (see DATA 1). The RKDA is loaded with disk address information from the Unibus D lines by Bus Control asserting LOAD RKDA LO or LOAD RKDA HI. Bits 00 – 03 select the sector address, up to a maximum of $13_8$. The Data Paths control logic asserts COUNT SA when the selected disk drive reaches the end of a sector, incrementing the RKDA to successive sector locations. At the end of the last sector ($13_8$) of the upper surface, the Data Paths control logic asserts CHANGE HEADS, enabling the lower disk head so that the succeeding operation is performed on the lower surface of the disk. This requires a change in the status of bit 04 (SUR), which, when cleared, selects the lower surface. At the end of the last sector of the lower surface, SUR overflows to 0, and CYL ADDR is incremented, directing the disk drive head to move to the next succeeding cylinder.

Bits 05 – 12 of the RKDA select the cylinder address, up to a maximum of $312_8$. Bits 13 – 15 select the disk drive, up to a maximum of 8.

RKDA bits 04 – 15 are cleared by INIT from the Status Control, and RKDA bits 00 – 03 are cleared by CLR 0 → 3 from the Data Paths control logic. CLR 0 → 3 is asserted when INIT is asserted or when CHANGE HEADS is asserted.

### 4.4.5 RKBA

The programmable RKBA consists of four counter ICs (seee DATA 1) configured to count up sequentially by 2 through 16 bits. The RKBA is parallel loaded from the Unibus D lines with bus address information when LOAD RKBA LO and LOAD RKBA HI are asserted by the Bus Control.

When the Bus Control asserts 0 → NPR and the Status Control asserts IBA (0), the RKBA register is incremented by 2. Pulse 0 → NPR indicates completion of an NPR transfer, and IBA is bit 11 of the RKCS, which inhibits the RKBA from incrementing during a normal transfer function when set. Thus, the RKBA is incremented by 2 for each transfer to the next sequential bus address (which will always be an even number).

The RKBA is cleared by INIT from the Status Control.

### 4.4.6 Data Paths Control Logic

The Data Paths control logic (see DATA 3 and 4) controls the In Buffer, 4-Word File, and RKDA, controls the programmable RKER bit 09 (DLT), and generates requests to the Bus Control.

**4.4.6.1 In Buffer Control** – In Buffer control is achieved by the CLK IN BUFF pulse, which may be asserted for any of three conditions:

a. The assertion of a DATA STR 2 pulse from the Bus Control asserts CLK IN BUFF to load the In Buffer. DATA STR 2 indicates that the function is a Write or Write Check function, and that data is on the Unibus D lines.

b. For a normal Read function (FMT clear) in the data major state of a sector, a CLK pulse asserts CLK IN BUFF, which shifts the In Buffer for each bit during the data major state.

c. During a Read function in the Format mode (RKCS 10, FMT, set), only the header major state is read. Thus, a CLK pulse from Status Control asserts CLK IN BUFF to shift the In Buffer for each bit. CLK is generated by DR BUS RD CLK L, which is the disk drive read clock signal.

The occurrence of either b. or c. during a Read function when the last bit of a word is shifted out (LAST DATA BIT asserted) sets the IN BUFF FULL flip-flop. IN BUFF FULL is also set during a Write or Write Check function when 0 → NPR is asserted by Bus Control, indicating the completion of an NPR data transfer. IN BUFF FULL is cleared when the File Write sequence is completed.

LAST DATA BIT is generated by the overflow of a 4-bit binary counter IC (jumper selectable for the RK11-D and RK11-E). Each bit shift (Read or Write) asserts +1 → SHIFT CNTR, which increments the counter. When this counter overflows, LAST DATA BIT asserted clears the counter on the next +1 → SHIFT CNTR pulse. For the jumper selectable RK11-E 18-bit option, two flip-flops provide the 17th and 18th bit counts.

The NPR EN flip-flop is set when NEW FUN is asserted by the Status Control, indicating the initiation of a new RK11 function (RKCS 00, GO, is set under program control). NPR EN is cleared when WC OVF is asserted by the Status Control, indicating that the designated number of data transfers (RKWC) has been performed. NPR EN is also cleared by STOP NPRs, asserted by the Status Control.

**4.4.6.2 Out Buffer Control** – Control of the Out Buffer is achieved by the CLK OUT BUFF pulse and the OUT BUFF FULL flip-flop. A CLK OUT BUFF pulse is generated for one of two conditions:

a. For Write or Write Check functions in the data major state of a sector, a CLK pulse asserts CLK OUT BUFF. CLK pulses for a Write or Write Check function are generated by the RK11 crystal-controlled WT CLK pulses in the Disk Control.

b. For Read, Write, and Write Check functions, the assertion of RD FILE asserts CLK OUT BUFF. RD FILE transfers the contents of the file to the Out Buffer.

The OUT BUFF FULL flip-flop is set when RD DONE is asserted. The RD DONE signal occurs just after RD FILE, indicating that the Out Buffer has been loaded and is full. For a Write or Write Check function, OUT BUFF FULL is cleared when the last data bit is shifted out of RKDB 00. For a Read function, OUT BUFF FULL is cleared when 0 → NPR goes unasserted. The GEN CLR signal from the Status Control also clears OUT BUFF FULL.

**4.4.6.3 RKER 09 (DLT) Control** – DLT (Data Late) can be set for either Read, Write, or Write Check functions. For a Read function, DLT sets if the In Buffer is full and an attempt is made to shift more data into it. For a Write or Write Check function, DLT sets when the Out Buffer is empty when an attempt is made to withdraw data from it. RKER 09 is cleared by INIT from the Status Control.

4.4.6.4 **4-Word File Control** – The 4-Word File responds to the condition of the In Buffer and Out Buffer flip-flops. When the File is not empty and the Out Buffer becomes empty, the RD FILE one-shot generates CLK OUT BUFF, followed by RD DONE. A RD DONE pulse indicates the completion of reading from a File location and loading it into the Out Buffer.

When the File is not full and the In Buffer is full, WT FILE loads the contents of the In Buffer into the selected File location. The WT FILE pulse, in turn, generates the WT DONE pulse. The generation of a WT DONE pulse indicates that the data has been written into the File location and the In Buffer has been emptied.

WT DONE controls the 2-bit In Counter, and RD DONE controls the 2-bit Out Counter (see DATA 4). Each WT DONE and RD DONE pulse increments the corresponding counter sequentially. Both counters are cleared by GEN CLR.

FILE FULL and FILE EMPTY are generated by monitoring four flip-flops that represent the four File locations. The WT DONE decoder outputs are connected to the direct set inputs of File location flip-flops; the RD DONE decoder outputs are connected to the clock inputs of the File location flip-flops and clear those flip-flops. Each time a File location is written into, the corresponding flip-flop for that File location is set; each time a File location is read from, the corresponding flip-flop is cleared. When all four flip-flops are set, FILE FULL is asserted; when all four flip-flops are clear, FILE EMPTY is asserted.

4.4.6.5 **NPR Initiation** – The generation of NPR REQ (see DATA 3) initiates NPR Bus Control operations for performing data transfers on the Unibus if the NPR EN flip-flop is set. For a Write or Write Check function, NPR REQ is generated when IN BUFF FULL is clear. For a Read function, NPR REQ is generated when OUT BUFF FULL is set. NPR REQ is not generated for a Read Check function.

4.4.6.6 **RKDA Control** – The RKDA is controlled by generation of the COUNT SA pulse and CLR 0 → 3. (The RKDA loading signals are generated by the Bus Control.) The COUNT SA pulse comes from a one-shot that is triggered when SECTOR END becomes unasserted, which occurs for a Read or Read Check when FILE EMPTY is asserted and OUT BUFF FULL is unasserted. For a Write or Write Check function, SECTOR END goes unasserted when FILE FULL and IN BUFF FULL are asserted. SECTOR END also goes unasserted when NPR EN goes unasserted. LAST WORD DONE from the Status Control asserts SECTOR END, which occurs during the postamble major state in the Status Control to indicate the end of the sector.

CLR 0 → 3, which clears RKDA 00 through 03, is generated when INIT from the Status Control or CHANGE HEADS is asserted. CHANGE HEADS increments RKDA 04 (SUR), which selects the disk surface, when the LAST SECTOR flip-flop is set and a COUNT SA pulse is generated. LAST SECTOR is asserted by the Disk Control at index pulse time.

CYL OVF is generated when CHANGE HEADS is asserted, RKDA 04 (SUR) is set, and FILE DONE is unasserted. CYL OVF causes the disk drive heads to move to the next sequential cylinder.

### 4.4.7 Internal Bus D Multiplexers

Internal Bus D Multiplexers include two sets of multiplexers; eight 74153 ICs and four 74157 ICs. The eight 74153s select one of three programmable registers (RKBA, RDKA, or RKDB) from the Data Paths according to RKA 01 and RKA 02 from the Bus Control. The four 74157s select, according to RKA 03, either the selected RKBA, RKDA, or RKDB register or the INT BUS A 00 – 15 inputs from the Internal Bus A Multiplexers of the Status Control. INT BUS A 00 – 15 provide the other programmable registers (RKDS, RKER, RKCS, or RKWC) to the Internal Bus D Multiplexers.

The RKA 01, RKA 02, and RKA 03 select signals from the Bus Control represent Unibus Address lines 1, 2, and 3, respectively. These lines select the programmable registers according to the code in Table 4-1.

**Table 4-1**
**Multiplexer Register Selection**

| Select Signals | | | Register | Address |
|---|---|---|---|---|
| RKA 03 | RKA 02 | RKA 01 | | |
| 0 | 0 | 0 | RKDS | 777400 |
| 0 | 0 | 1 | RKER | 777402 |
| 0 | 1 | 0 | RKCS | 777404 |
| 0 | 1 | 1 | RKWC | 777406 |
| 1 | 0 | 0 | RKBA | 777410 |
| 1 | 0 | 1 | RKDA | 777412 |
| 1 | 1 | 1 | RKDB | 777416 |

## 4.5 BUS CONTROL

The Bus Control logic of the M7257 module serves as an interface between the Unibus and the RK11 Controller, and generates all Unibus control signals. The Bus Control consists of the address selection, Non-Processor Request (NPR) control, interrupt control, and Unibus driver and receiver logic. Bus Control logic is contained in engineering drawing D-CS-M7257-0-1, sheets 1 – 6.

The address selection logic determines if an RK11 addressable register has been selected for a Unibus data transfer (BUS A 04 – BUS A 17), and which Unibus data transfer (DATI, DATO) is to be performed (BUS C0 and BUS C1). The address selection logic also generates low-order and high-order byte control signals for the individual write-programmable registers (RKCS, RKWC, RKBA, and RKDA), and gates data to the Unibus D lines for DATI operations.

All NPR requests are handled within this module without requiring outside intervention or control.

### 4.5.1 Address Selection Logic

The address selection logic (see BUS 1) detects addressing of the RK11 programmable registers from the Unibus. This occurs when the processor as bus master asserts BUS MSYN L (Master Sync) to read or write the RK11 (Bus Slave) register, designated by the Unibus address lines (BUS A 00 – BUS A 17). In the RK11, only the RKCS, RKWC, RKBA, and RKDA are written from the Unibus. All other registers are read-only.

The Exclusive-OR gate (jumper selectable) network (BUS A 04 – 10 and BUS A 12) together with BUS A 11 and BUS A 13 – 17 with BUS MSYN L asserted trigger a 600 ns one-shot for any valid RK11 register address (777400 – 777416). The one-shot generates BUS SSYN (Slave Sync) to acknowledge the processor MSYN signal. If the operation called for by the processor is a DATI (BUS C1 L unasserted), GATE DATA → BUS D is asserted. For a valid address, the Slave Sync one-shot output also enables STROBE LOW and STROBE HI if the bus operation to be performed is a word DATO (BUS C1 L and BUS C0 L asserted).

RKA 01 – RKA 03 specify which of the RK11 registers (addresses 777400 – 777416) is addressed by the Unibus (BUS A 01 – BUS A 03). For NPR operations, RKA 01 – RKA 03 are automatically asserted to specify the RKDB (777416). For reading RK11 registers, RKA 01 – RKA 03 enable the designated register to the Unibus drivers via the Internal Bus A Multiplexers (RKDS, RKER, RKCS, and RKWC) in the Status Control and the Internal Bus D Multiplexers (RKBA, RKDA, and RKDB) in the Data Paths.

RKA 01 – RKA 03 also select one of the seven input lines of a multiplexer IC (corresponding to the seven addressable registers) when the Status Control unasserts B CNTRL RDY to indicate that the control is busy. These jumper selectable inputs can be cut to disable any register addressed. When a jumper is cut, STROBE LO and STROBE HI are inhibited, preventing the register addressed from loading Unibus data while the Bus Control is busy.

### 4.5.2 NPR Logic

The NPR logic (BUS 3 and 4) requests control of the Unibus by generating BUS NPR L for RK11 data transfer functions. With NPR EN set, NPR REQ asserted by the Data Paths indicates that the Out Buffer (RKDB) is full for a Read function, or that the In Buffer is empty for a Write or Write Check function. NPR REQ generates BUS NPR L. Figure 4-1 shows the NPR timing for a Write or Write Check function; Figure 4-2 shows the NPR timing for a Read function.

The processor grants the NPR by asserting BUS NPG IN H, which is inhibited from setting the GRANT 1 flip-flop by NPR REQ. If the RK11 is not the device asserting the NPR (NPR REQ unasserted), then BUS NPG IN H sets GRANT 1 and asserts BUS NPG OUT H onto the Unibus. If the RK11 is the device asserting the NPR, BUS NPG IN H triggers a 75 ns one-shot that sets SACK 1 on its trailing edge if GRANT 1 is clear. SACK 1 set asserts BUS SACK L onto the Uniubs to acknowledge the processor grant (NPG).

When the present bus master finishes operating on the Unibus, BUS BBSY L and BUS SSYN L are unasserted, SACK 1 is set, and BUS NPG IN H is unasserted, the RK NPR MASTER flip-flop is set. RK NPR MASTER gates the RKBA onto the BUS A lines, clears SACK 1, reasserts BUS BBSY L onto the Unibus, and sets the RK MSYN flip-flop after a 150 ns delay. RK MSYN set asserts BUS MSYN L on the Unibus and triggers a 20 μs one-shot. If RK MSYN is still set at the trailing edge of that one-shot, the Nonexistent Memory (RKER 10 – NXM) flip-flop is set to indicate that BUS SSYN L has not returned from the NPR slave device.

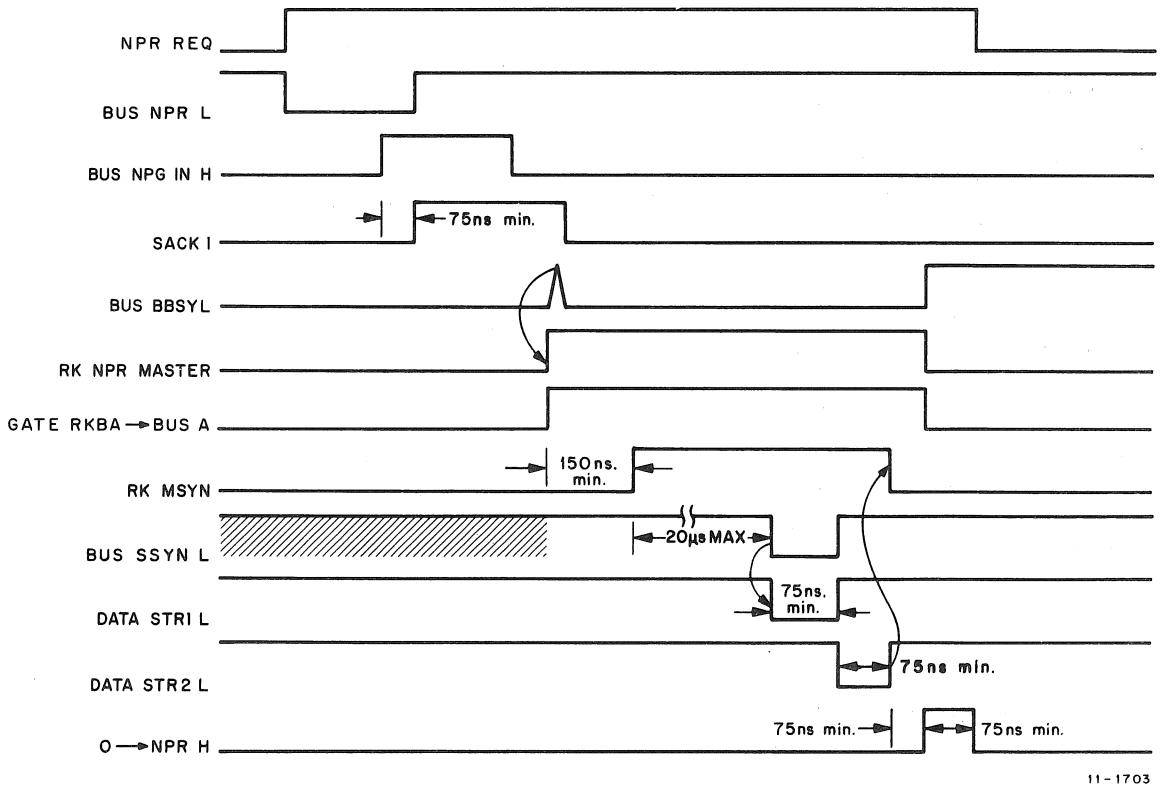



Figure 4-1 Non-Processor Request (NPR) Timing Diagram for RK11 (Write or Write Check Function)

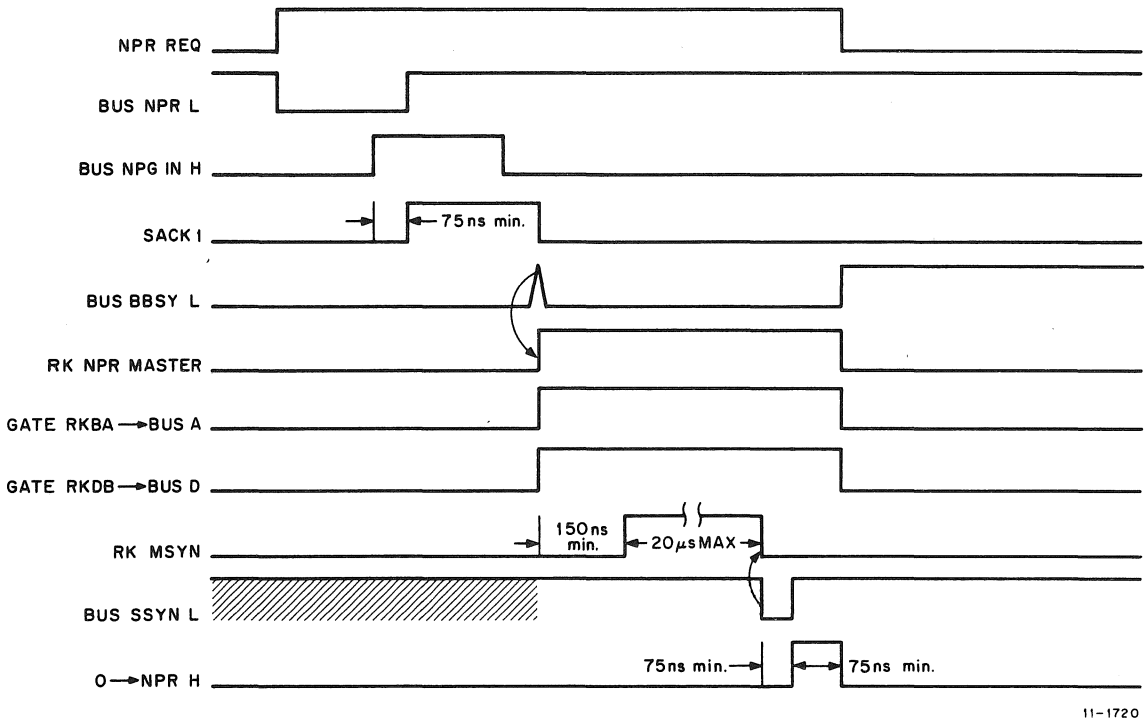



Figure 4-2 Non-Processor Request (NPR) Timing Diagram for RK11 (Read Function)

During a Write or Write Check function when BUS SSYN L is asserted on the Unibus by the bus slave device, RK SSYN L is asserted on the Unibus by the bus slave device, RK SSYN and RK MSYN trigger DATA STR 2, which loads Unibus data into the Data Paths.

For a Read function, RK NPR MASTER generates GATE DATA → BUS, which loads the data assembled by the disk drive from the RKDB onto the Unibus. MSYN is cleared 75 ns after the trailing edge of SSYN. MSYN is also cleared when NXM is set and RK NPR MASTER is asserted. For Write or Write Check functions, MSYN is cleared on the trailing edge of DATA STROBE 2.

A 75 ns 0 → NPR pulse clears NPR REQ, which, in turn, clears RK NPR MASTER to terminate the NPR operation and drop BUS BBSY L from the Unibus.

### 4.5.3 Interrupt Control Logic

Interrupt Control of the Unibus is initiated through the generation of RK INT REQ, which asserts BR OUT L (BUS 3). BR OUT L asserts the bus request lines for the RK11 (typically, BR5) onto the Unibus. With Interrupt Done Enable (RKCS 06, IDE) set, the positive transition of B CNTRL RDY (Buffered Control Ready) from the Status Control generates RK INT REQ, indicating the occurrence of an RK11 interrupt condition.

The processor grants the interrupt request (BR) by asserting BUS BG IN H, which is inhibited from setting the GRANT 2 flip-flop by RK INT REQ asserted. If the RK11 is not the BR device the bus is servicing (RK INT REQ unasserted), then BUS BG IN H sets the GRANT 2 flip-flop and asserts BUS BG OUT H onto the Unibus. BUS BG IN H sets the SACK 2 flip-flop if GRANT 2 is clear. SACK 2 set asserts BUS SACK L onto the Unibus to acknowledge the processor grant (BG) until BUS BBSY L, BUS SSYN L, and BUS BG are unasserted by the present bus master then the RK INT MASTER flip-flop is set. RK INT MASTER set reasserts BUS BBSY L onto the Unibus, and asserts the interrupt vector address and BUS INTR L from the Unibus drivers onto the Unibus data lines.

Figure 4-3 shows the interrupt timing sequence for the RK11 bus request.

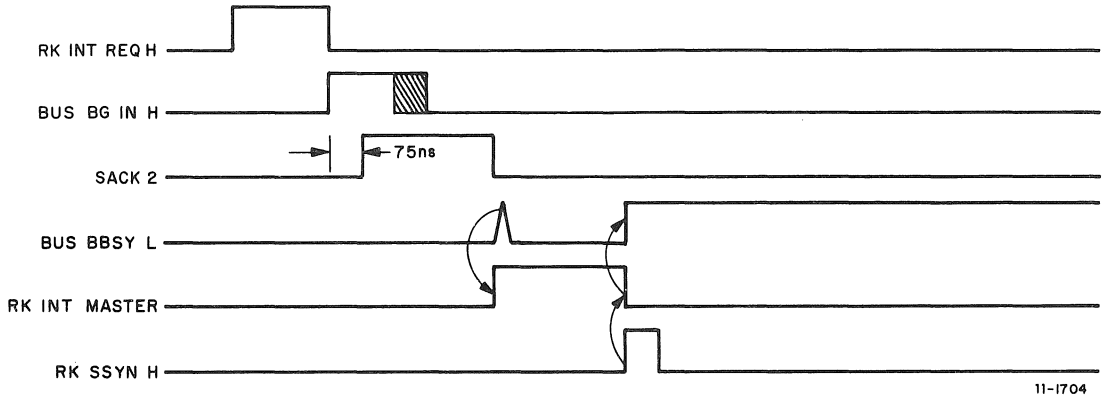



Figure 4-3 RK11 Bus Request Interrupt Timing Sequence

### 4.5.4 Unibus Drivers and Receivers

Unibus drivers and receivers consist of 8881s and 380s made specifically for use with the Unibus. Enabling levels for outputs and inputs are controlled within the Bus Control module, with no outside intervention required.

# CHAPTER 5
# MAINTENANCE

## 5.1 INTRODUCTION

The RK11 Controller is maintained by means of an inspection procedure, diagnostic software instructions, and operation of the KM11-A Maintenance Panel.

The inspection procedure consists of a preventive maintenance check of RK11 components for visible defects. The diagnostic software consists of three MAINDEC programs, which isolate RK11 hardware malfunctions. These diagnostics are primarily a troubleshooting tool designed to test total disk drive system operation with disk drives on-line.

The KM11-A Maintenance Panel is also a troubleshooting tool, and utilizes a transparent overlay to monitor RK11 Controller signal states.

## 5.2 INSPECTION

Table 5-1 lists visual checks for the RK11 Controller.

**Table 5-1**
**Visual Inspection Checklist**

| Item | Check |
|---|---|
| Mechanical Connections | a. Check that all screws are tight, and that all mechanical assemblies are secure. |
| | b. Check that all crimped lugs are secure and that all lugs are properly inserted in their mating connectors. |
| Wiring and Cables | a. Check all wiring and cables for breaks, cuts, frayed leads, or missing lugs. Check wire wraps for broken or missing pins. |
| | b. Check that no wire or cables are strained in their normal positions. |
| Modules and Components | a. Check that all modules are properly seated. |
| | b. Check for areas of discoloration on surfaces, which could indicate failed or inconsistent modules. |

## 5.3 DIAGNOSTICS

The RK11 software troubleshooting system diagnostics consist of three MAINDEC programs: MAINDEC-11-D5HA-PB1 (static test), MAINDEC-11-D5HA-PB2 (disk data test), and MAINDEC-11-DZRKG-A-PB (random seek exerciser). These programs and their listings are supplied with each RK11 shipped. Program listings contain descriptions and explanations of the programs, as well as instructions for running the diagnostics.

## 5.4 KM11-A MAINTENANCE PANEL

The KM11-A Maintenance Panel consists of a W130 Driver module and a W131 Indicator module (Figure 5-1). The KM11-A is an available option of the PDP-11 for general hardware maintenance functions. The RK11 internal states are displayed on a transparent RK11-D overlay (Figure 5-2), which defines the particular RK11 signal asserting each indicator light. The RK11-D overlay (part number 559081-0-11) fits over the W131 module as shown in Figure 5-1. The W131 also contains four control switches, but these are not used in testing the RK11-D or RK11-E.

The KM11-A is installed by plugging the W131 into the W130, then plugging the W130 into slot B3 of the RK11 system unit. When the RK11 Controller is operating, the W131 indicator lights reflect the logic states indicated on the RK11-D overlay.

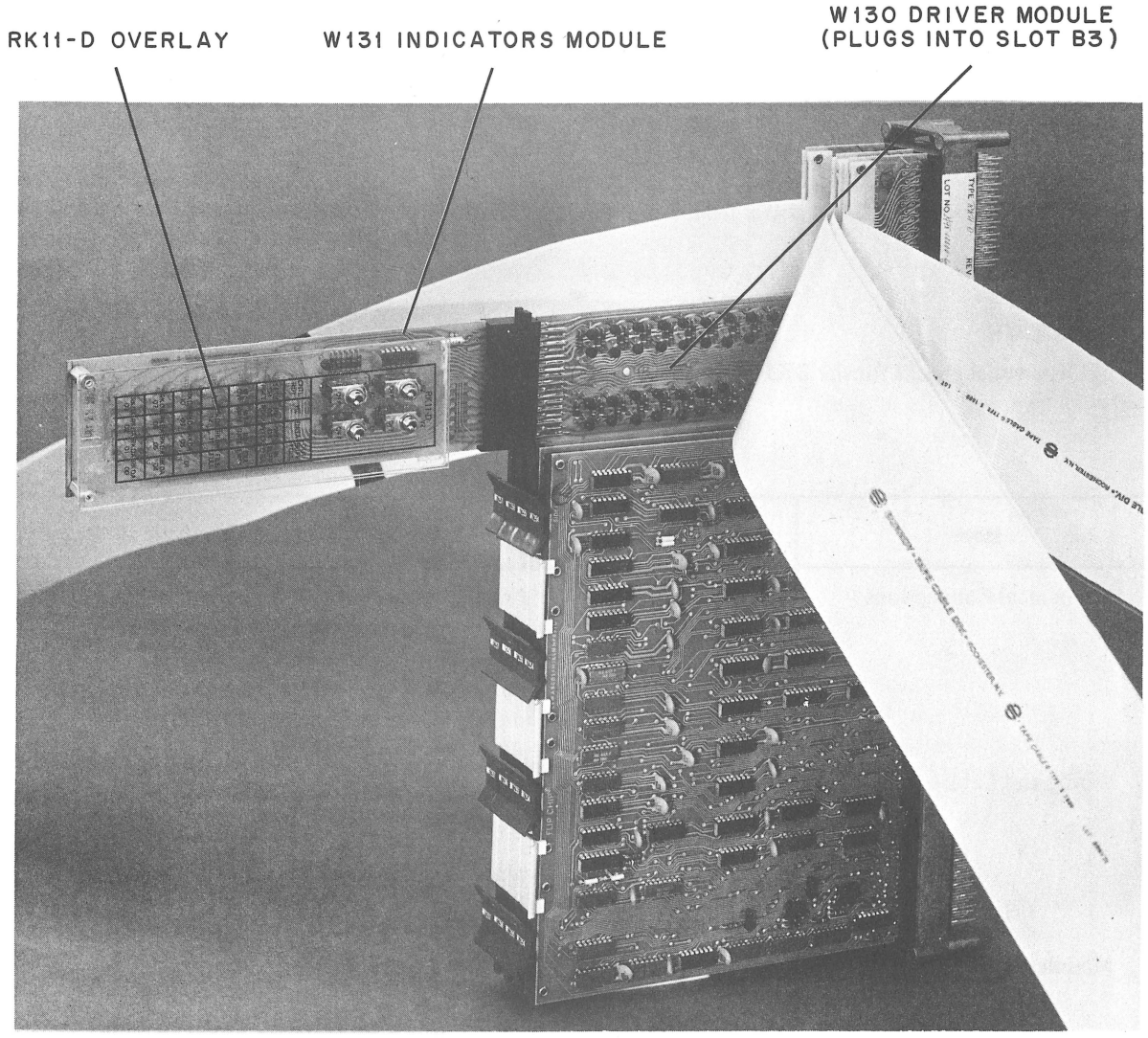



Figure 5-1 KM11-A Maintenance Panel Installed in RK11 Controller Unit

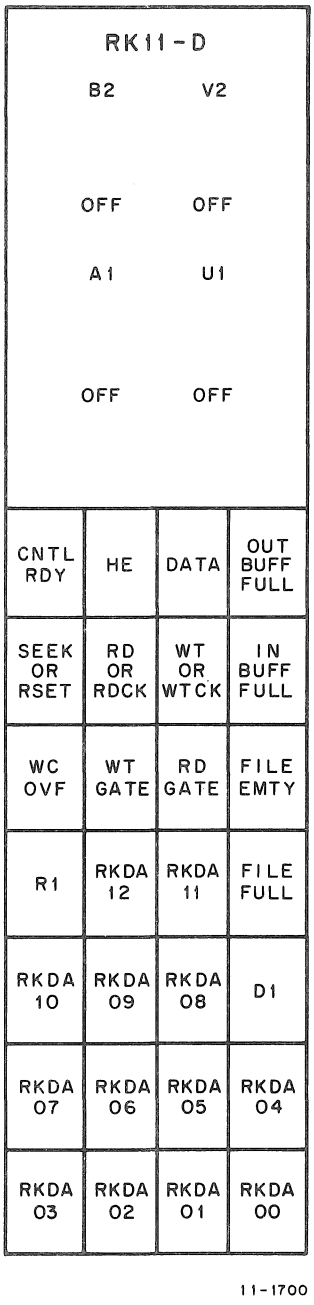



Figure 5-2 RK11-D Overlay for KM11-A Maintenance Panel

# APPENDIX A
# RK11-D AND RK11-E
# INTEGRATED CIRCUITS (ICs)

This appendix provides functional logic diagrams and pin designation information for all the MSI integrated circuits (ICs) used by the RK11-D and RK11-E. These ICs are indicated in the engineering drawings by manufacturer's part number and pin number.

Table A-1 lists the ICs described, along with the manufacturer's part number for each.

**Table A-1**
**RK11-D and RK11-E Medium Scale Integrated Circuits (MSI)**

| Name | Mfg. Part No. |
|---|---|
| Dual/Binary to One-of-Four Line Decoder | MC4007 |
| 4-Bit Shift Register | 8271 |
| 4-Bit Binary Counter/Storage Element | 8281 DC |
| 4-Line-to-10-Line Decoder | 7442 |
| Quad Bistable Latches | 7475 |
| 2-Bit Binary Full Adder | 7482 |
| 4-Bit Binary Counter | 7493 |
| 5-Bit Shift Register | 7496 |
| Dual Retriggerable Monostable Multivibrator | 74123 |
| 8-Line-to-1-Line Data Selector/ Multiplexer | 74151 |
| Dual 4-Line-to-1-Line Data Selector/ Multiplexer | 74153 |

Table A-1 (Cont)
**RK11-D and RK11-E Medium Scale Integrated Circuits (MSI)**

| Name | Mfg. Part No. |
|---|---|
| Quadruple 2-Line-to-1-Line Multiplexer | 74157 |
| Synchronous 4-Bit Binary Counter | 74161 |
| 4-by-4 Register File | 74170 |
| Hex D-Type Flip-Flop | 74174 |
| Quad D-Type Flip-Flop | 74175 |
| 4-Bit Binary Counter | 74193 |

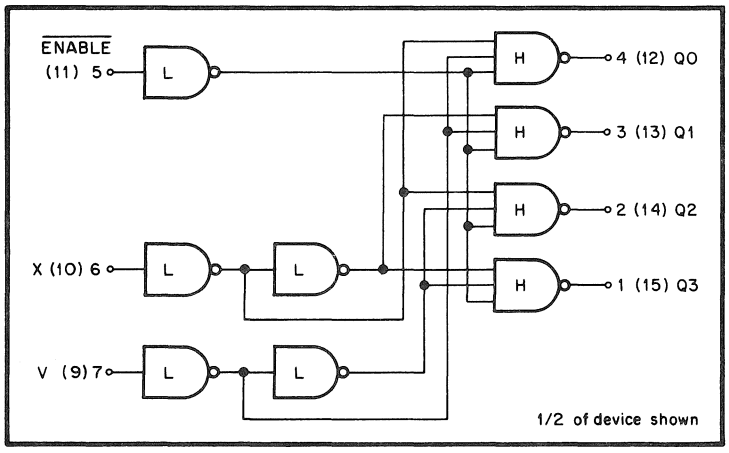



Figure A-1 MC4007 Dual/Binary-to-One-of-Four Line Decoder

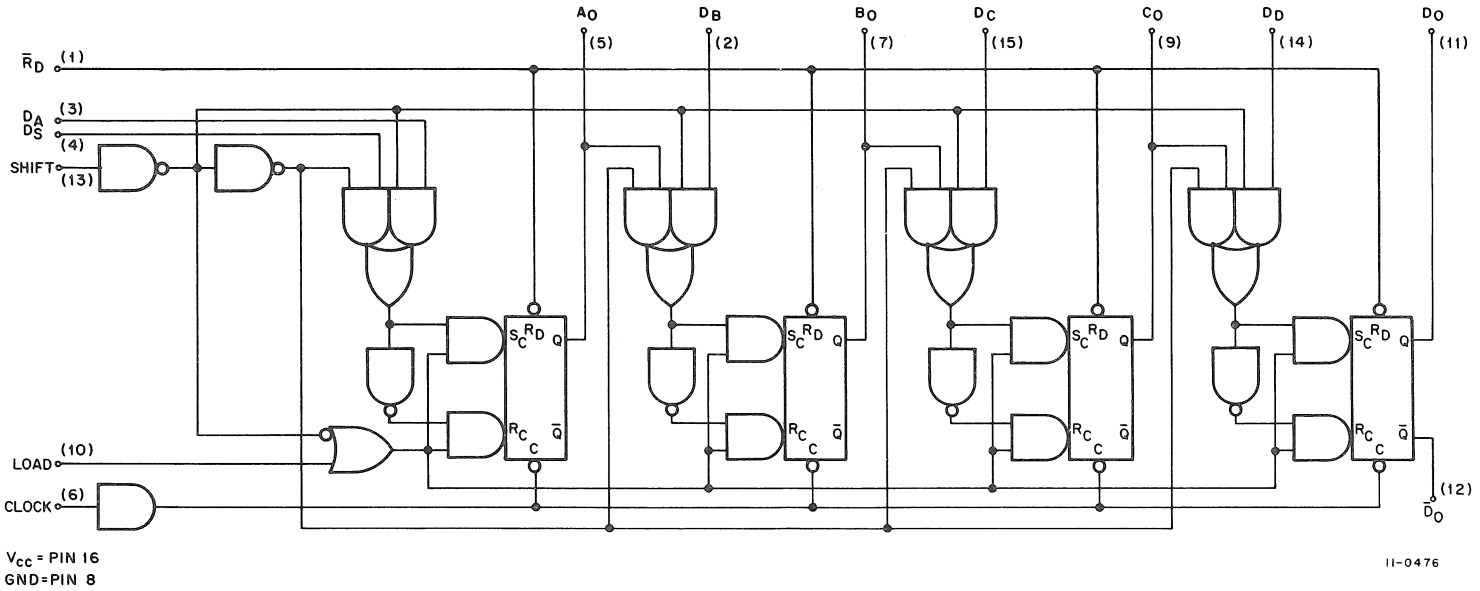



Figure A-2 8271 4-Bit Shift Register

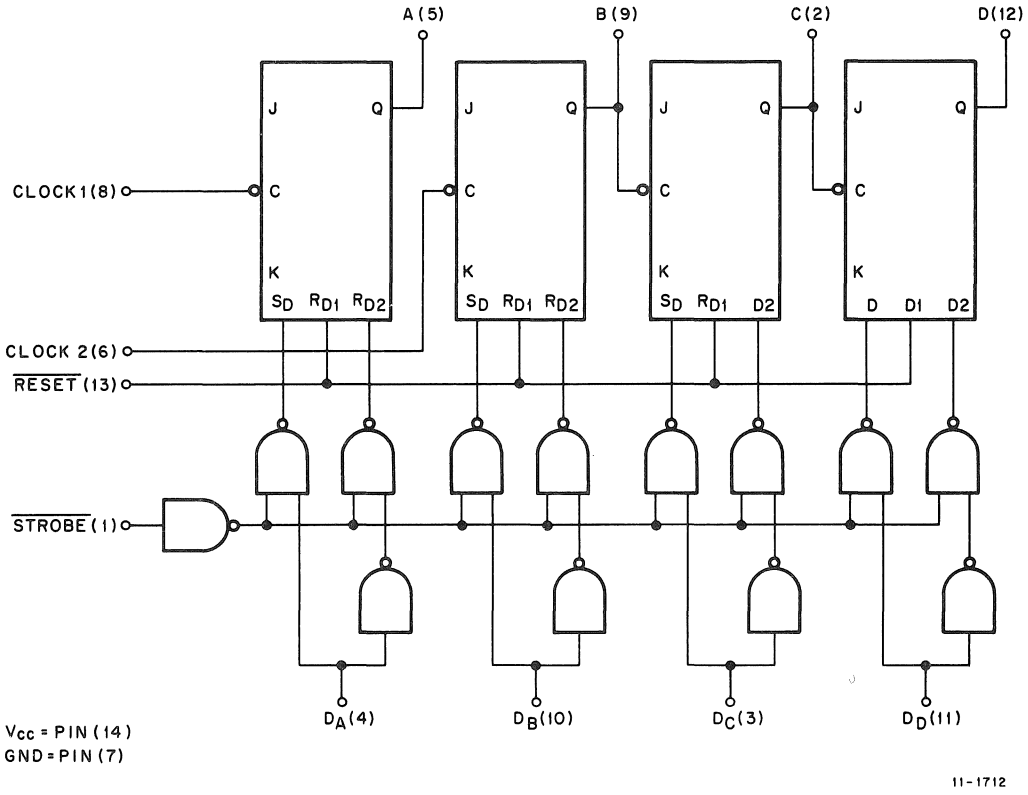



Figure A-3 8281 DC 4-Bit Binary Counter/Storage Element

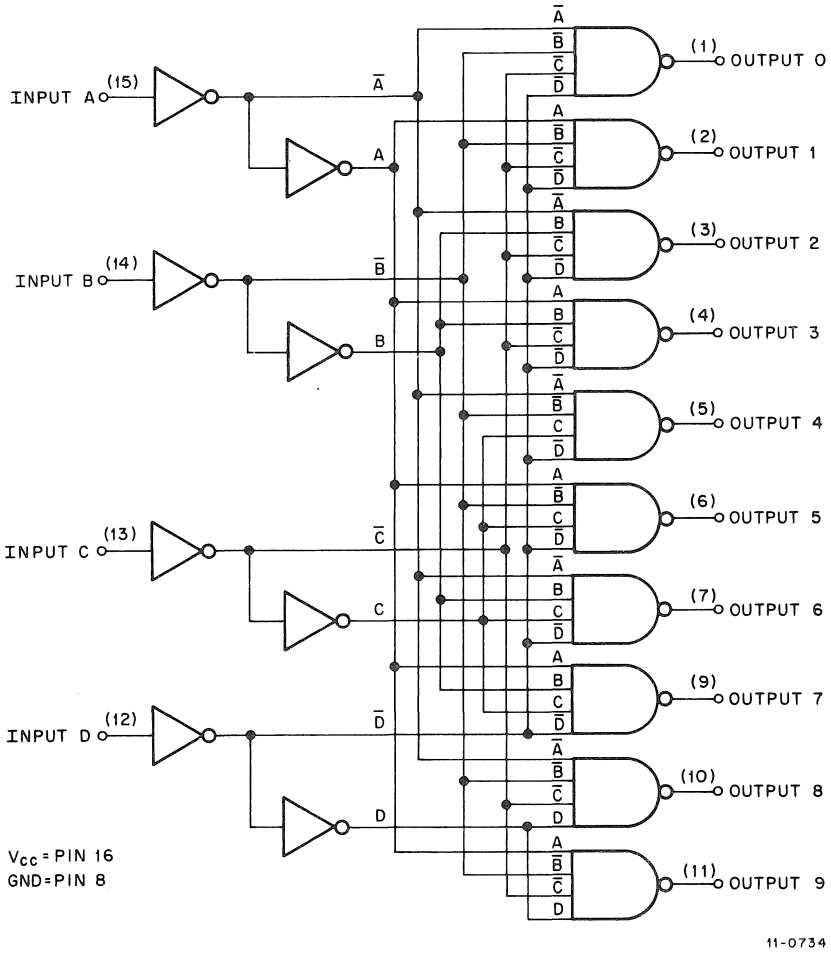
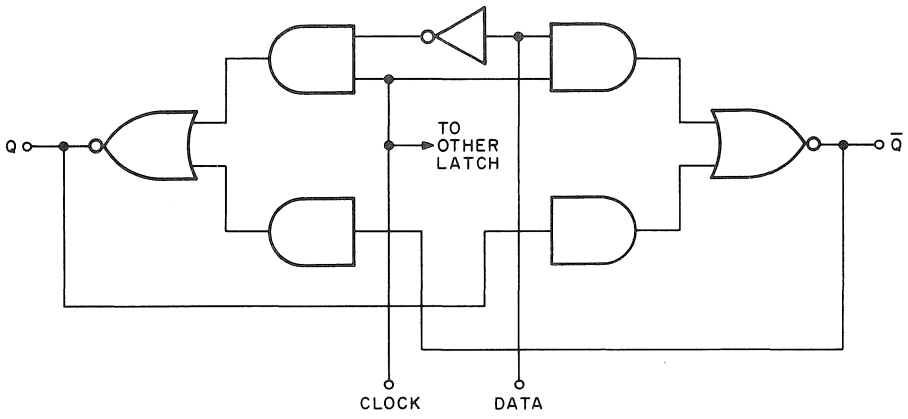



Figure A-4 7442 4-Line-to-10-Line Decoder



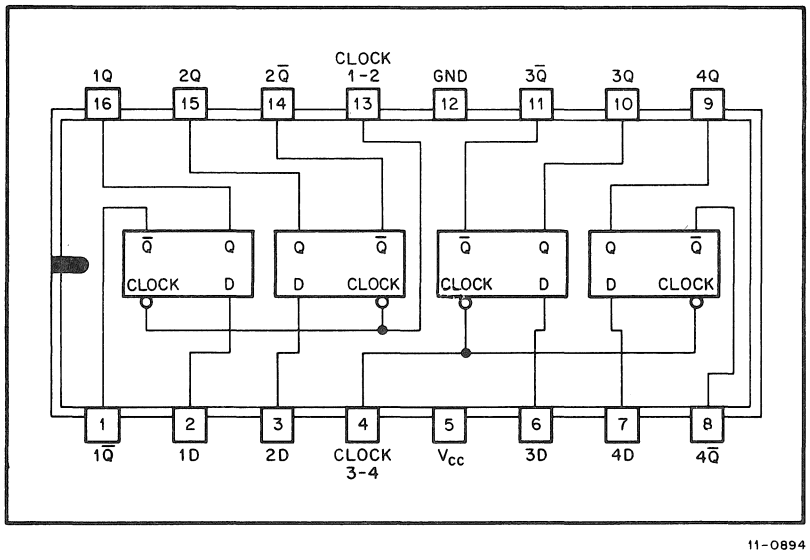
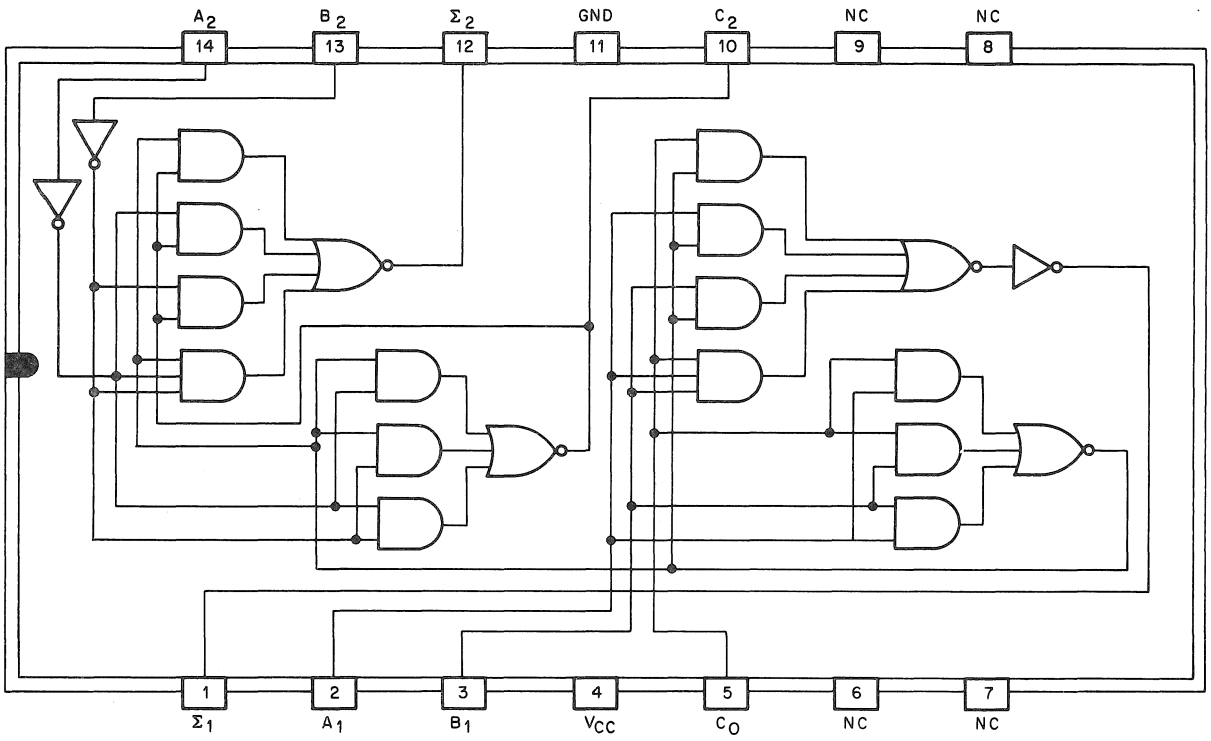




Figure A-5 7475 Quad Bistable Latches




11-1713

Figure A-6 7482 2-Bit Binary Full Adder

| TOGGLE INPUT PULSE | OUTPUT | | | |
|---|---|---|---|---|
| | Y1 | Y2 | Y3 | Y4 |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 |
| 11 | 1 | 1 | 0 | 1 |
| 12 | 0 | 0 | 1 | 1 |
| 13 | 1 | 0 | 1 | 1 |
| 14 | 0 | 1 | 1 | 1 |
| 15 | 1 | 1 | 1 | 1 |

*TRUTH TABLE

*Applies When 7493 Is Used As 4-Bit Ripple-Through Counter.

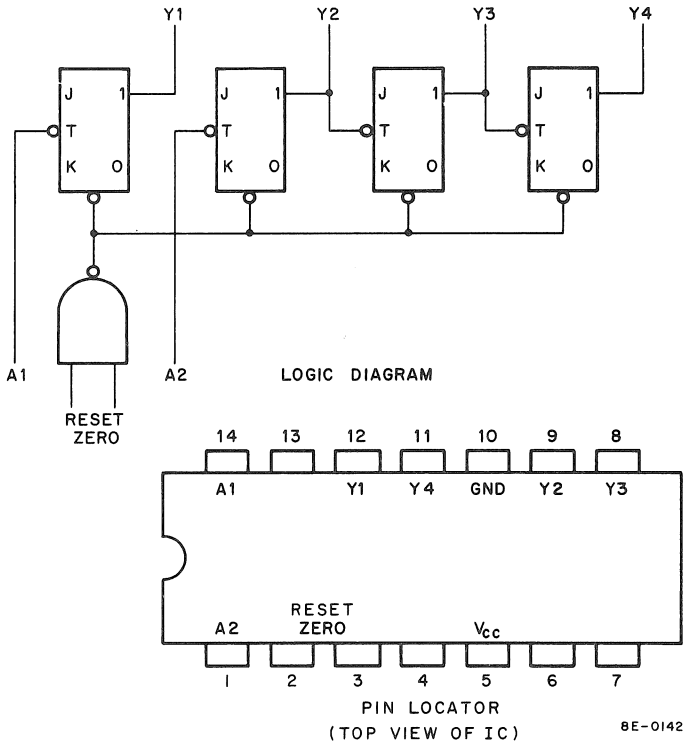



Figure A-7 7493 4-Bit Binary Counter

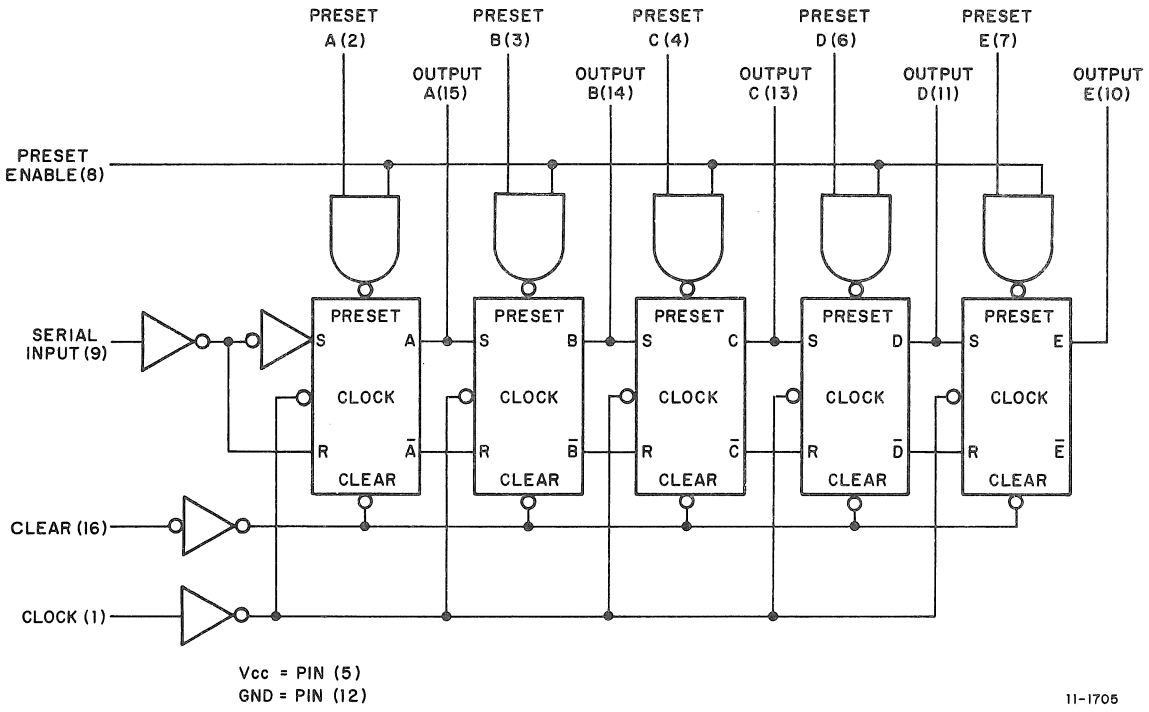



Figure A-8 7495 5-Bit Shift Register

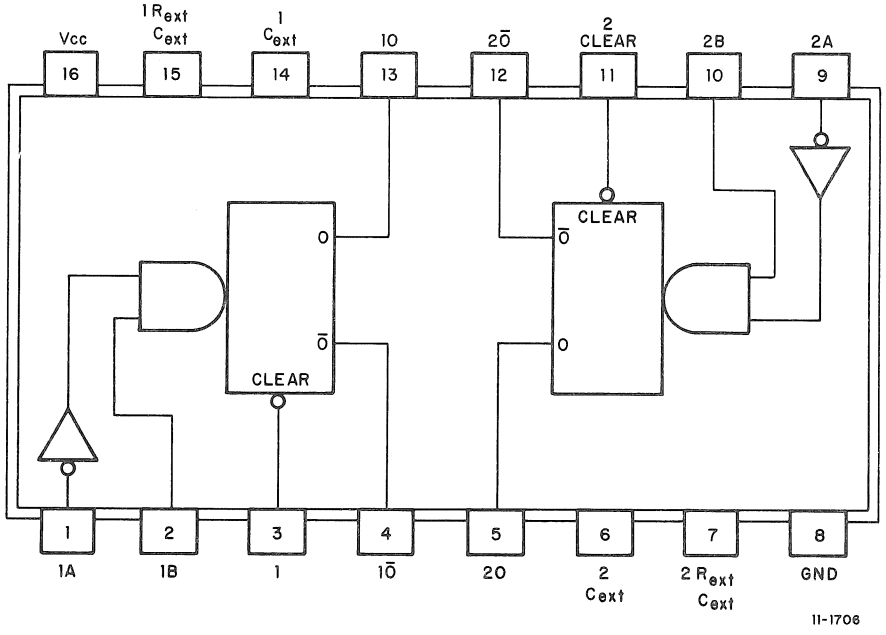



Figure A-9 74123 Dual Retriggerable Monostable Multivibrator

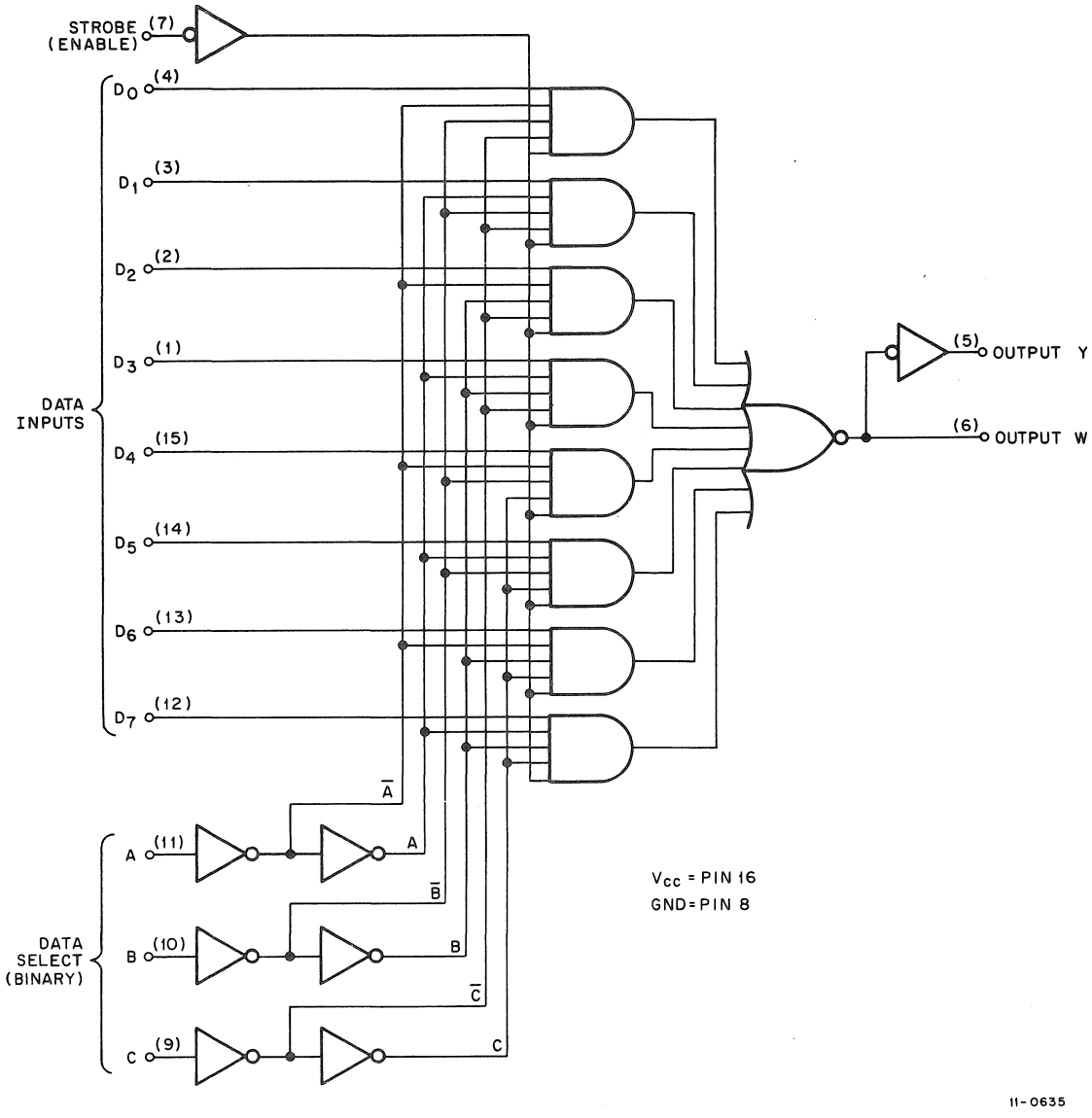



Figure A-10 74151 8-Line-to-1-Line Data Selector/Multiplexer

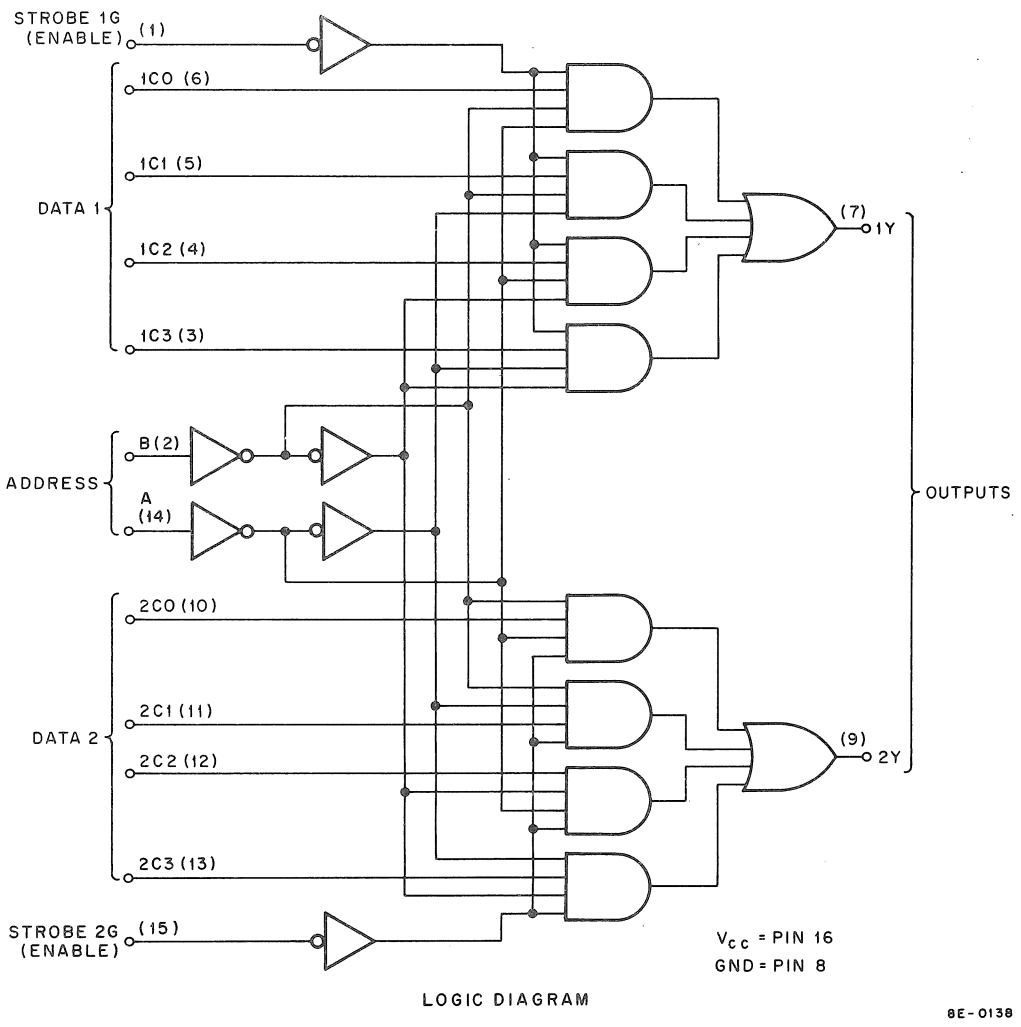



Figure A-11 74153 Dual 4-Line-to-1-Line Data Selector/Multiplexer

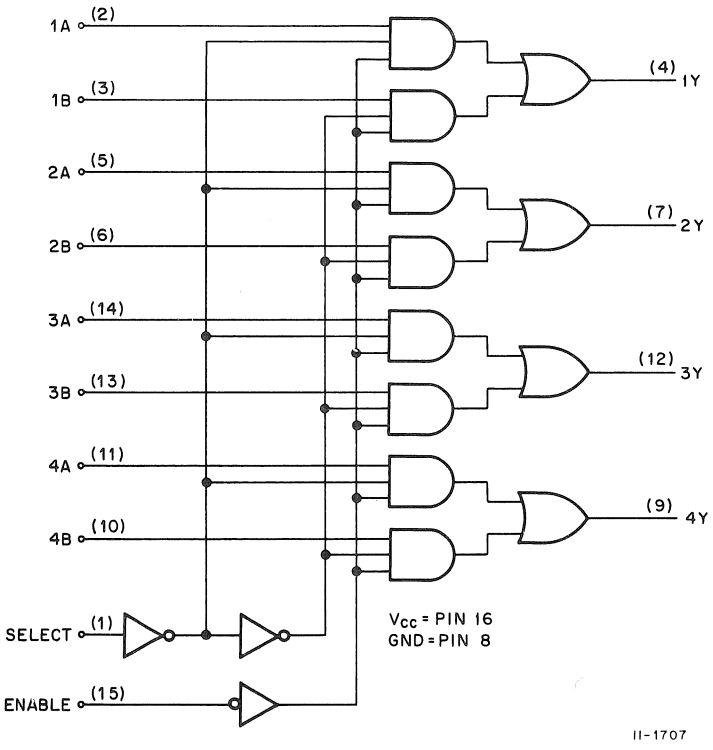



Figure A-12 74157 Quadruple 2-Line-to-1-Line Multiplexer

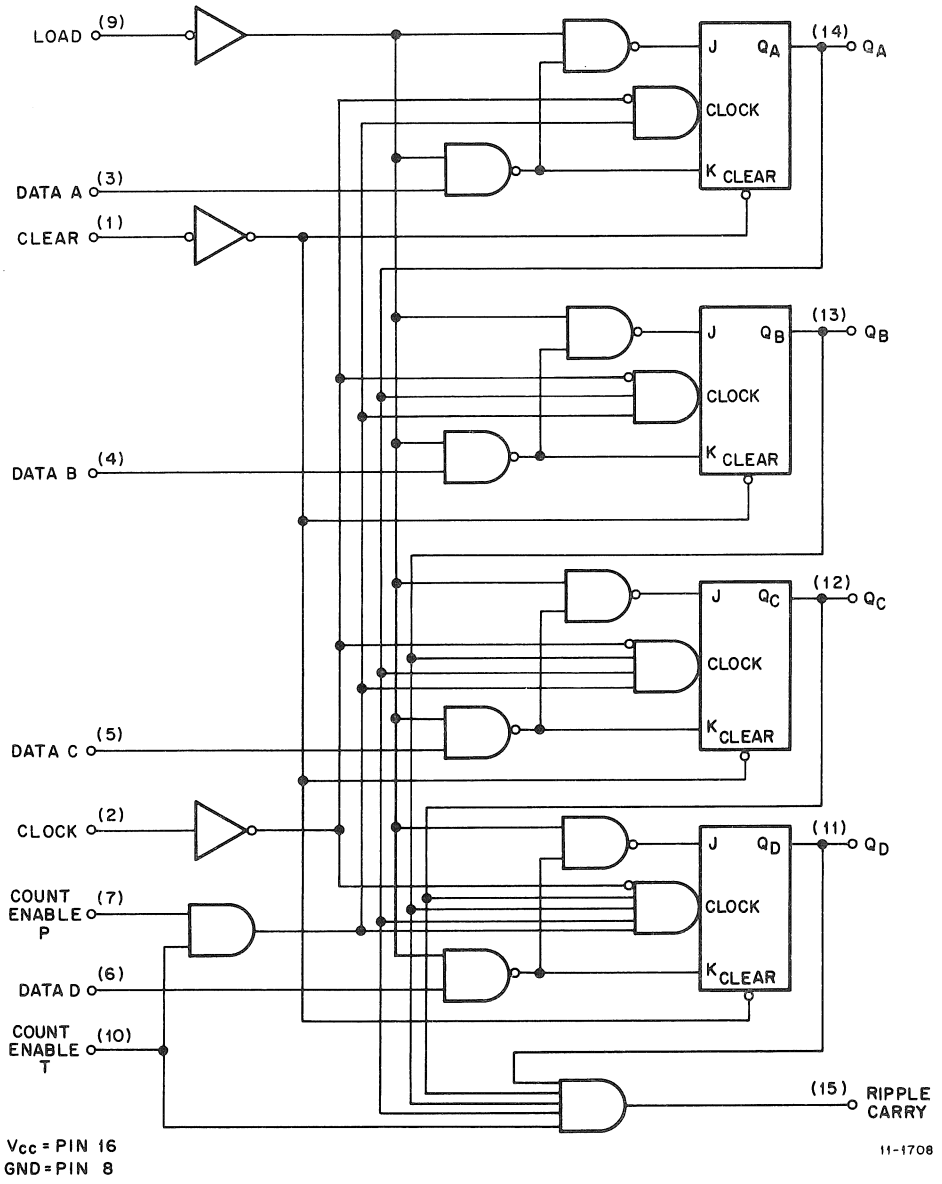



Figure A-13 74161 Synchronous 4-Bit Binary Counter

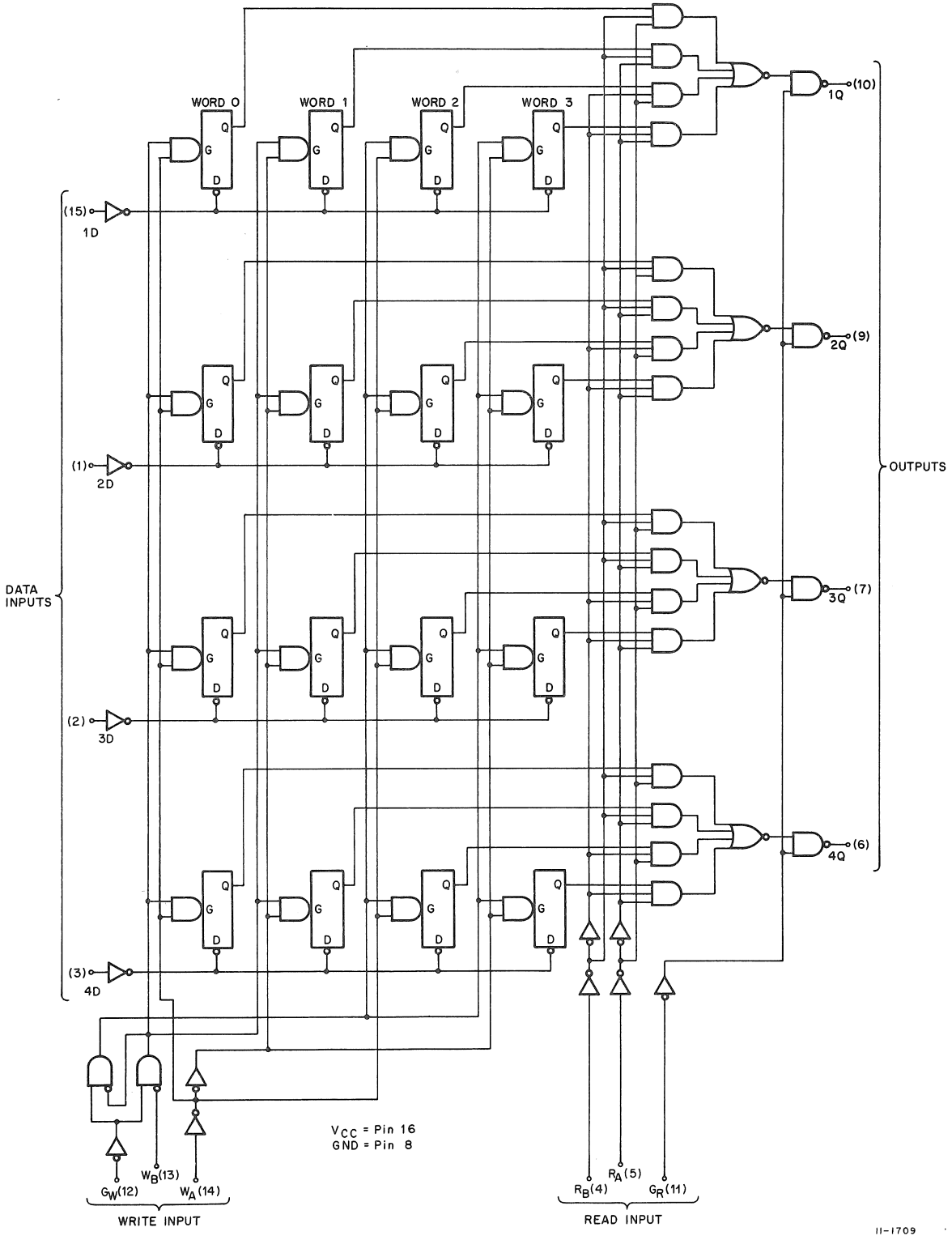



Figure A-14 74170 4-by-4 Register File

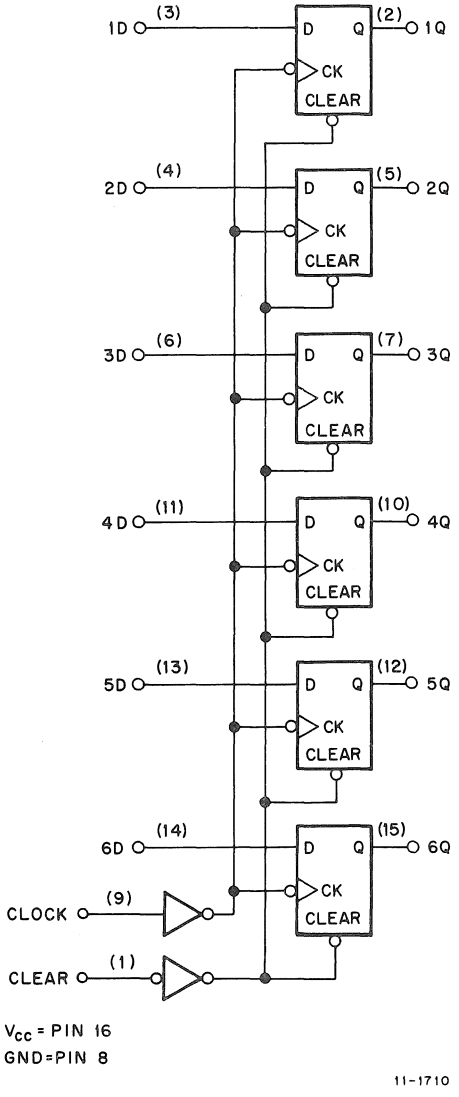



Figure A-15 74174 Hex D-Type Flip-Flop

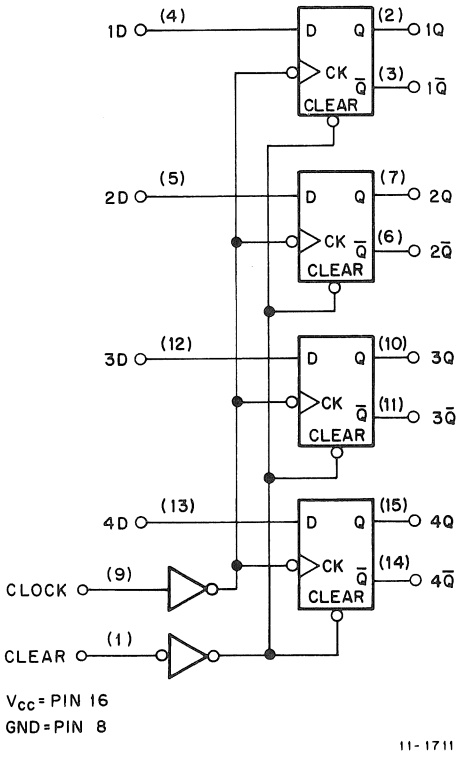



Figure A-16 74175 Quad D-Type Flip-Flop

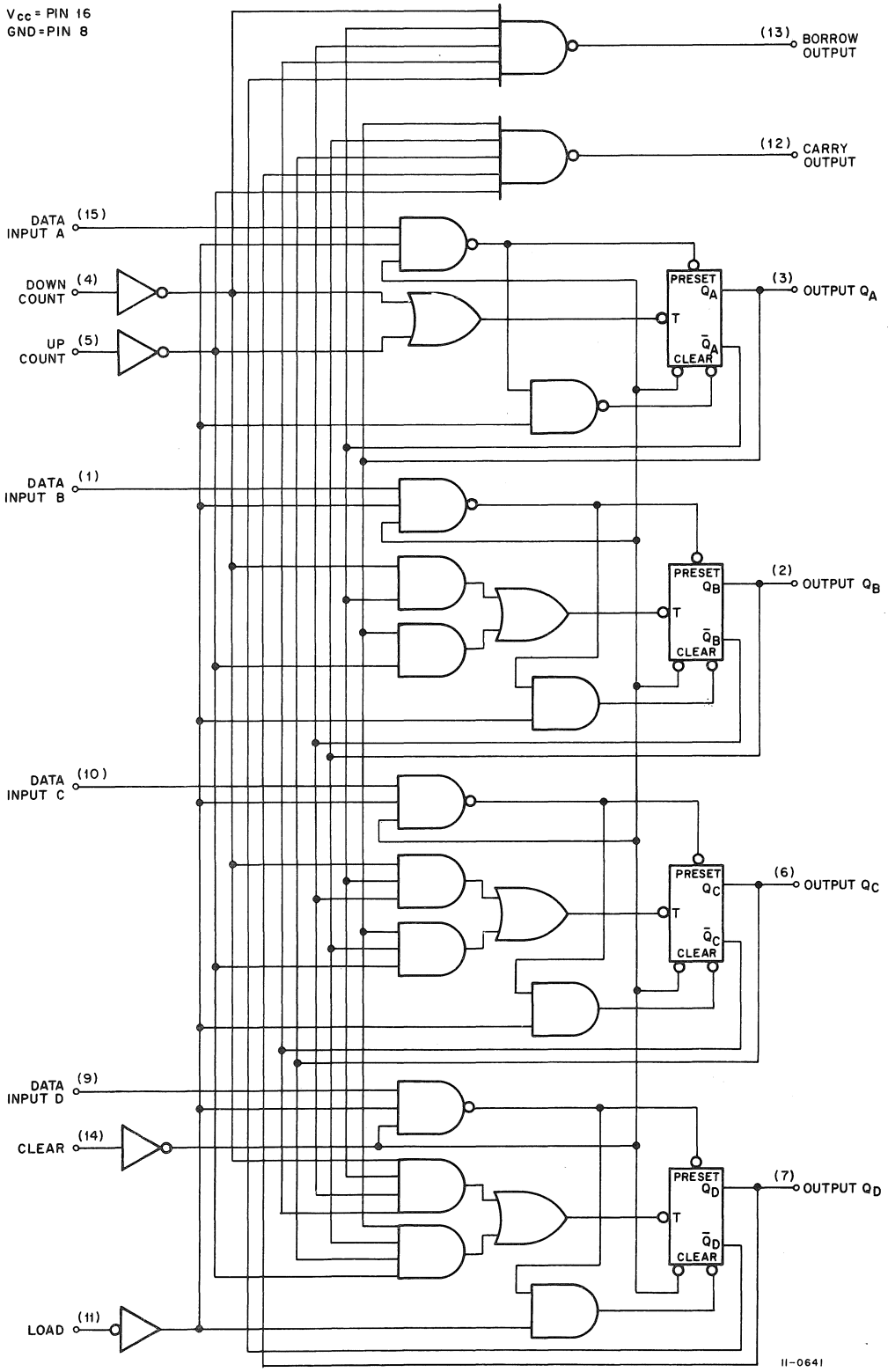



Figure A-17 74193 4-Bit Binary Counter

READER'S COMMENTS

RK11-D and RK11-E
MOVING HEAD DISK DRIVE
CONTROLLER
DEC-11-HRKDA-B-D

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults do you find with the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

Would you please indicate any factual errors you have found. _____

_____

_____

_____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

Fold Here

Do Not Tear - Fold Here and Staple

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

Postage will be paid by:

Digital Equipment Corporation
Technical Documentation Department
146 Main Street
Maynard, Massachusetts 01754

digital

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS 01754