PDP-11/34
system user's manual

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PDP-11/34
system user's manual

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CONTENTS

CONTENTS (CONT)

CONTENTS (CONT)

FIGURES

FIGURES (CONT)

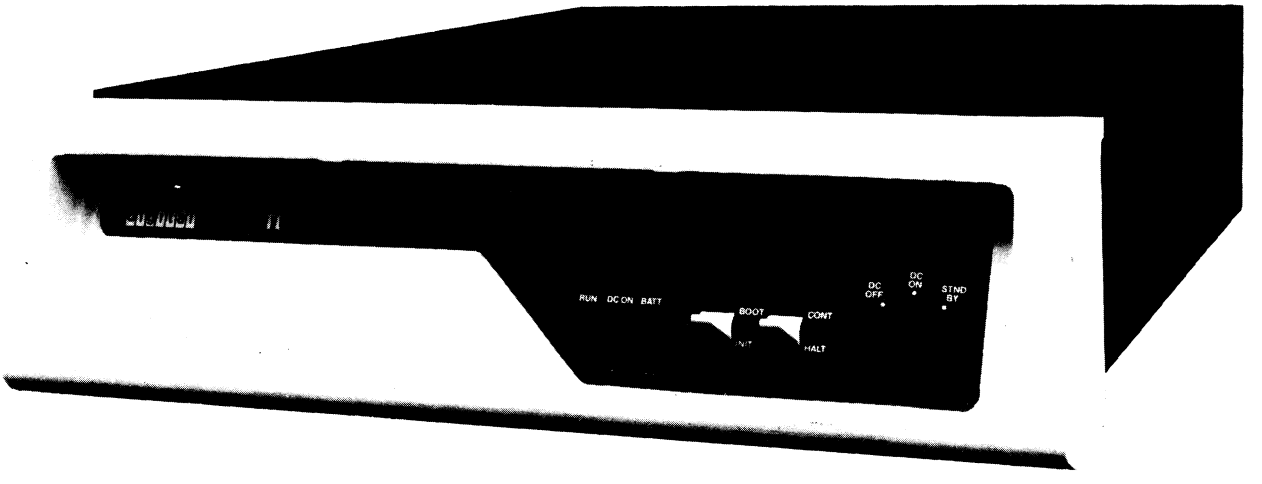
TABLES

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual is intended to provide an introduction to the PDP-11/34 computer system and present the information required by the user for configuration, installation, operation, familiarization with system components, and limited troubleshooting procedures.

The basic PDP-11/34 (Figure 1-1) includes a simple operator's console which does not contain a switch register and light display. Communication between the user and computer is implemented via the system terminal. A special bootstrap/terminator module allows the terminal to simulate the function of a traditional programmer's console.



8141-21

Figure 1-1 PDP-11/34 Computer System

A version of the 11/34, designated 11/34A, was developed to accommodate a floating point option (FP11-A). Functionally, the 11/34 and 11/34A are the same. The physical differences are as follows.

The 11/34 system includes the KD11-E central processor (M7265 and M7266 modules) and an M8264 Sack Timeout module.

The 11/34A system uses the KD11-EA central processor, consisting of the M8265 and M8266 modules. The new module set is a functional equivalent of the KD11-E version with modifications to include the sack timeout circuitry and the required connections for the floating point option. The capabilities of the power supplies have been increased to accommodate the floating point unit.

Unless specified otherwise, all references to 11/34 in this manual apply to both variations.

1.2 SYSTEM DESCRIPTION

The PDP-11/34 computer system comprises modular units that can be configured to suit the customer's application. The basic PDP-11/34 consists of the following equipment.

Central processor (KD11-E or KD11-EA)
Operator's console (KY11-LA)
Bootstrap/terminator (M9301-YA, YB, YF)
Unibus
Unibus terminator (M9302)
Core (MM11-CP, DP) or MOS (MS11-EP, FP, JP) memory
Mounting box (BA11-L or BA11-K)
Backplane (DD11-PK)
M8264 Sack Timeout module (11/34 only)
Parity controller (M7850)

Optional equipment available for the system includes:

Programmer's console (KY11-LB)
Serial line unit/real-time clock (DL11-W)
Battery backup unit for MOS memory (H775)
Standard PDP-11 peripherals
Expander backplane (DD11-CK, DK).

Figure 1-2 illustrates a block diagram of the PDP-11/34.

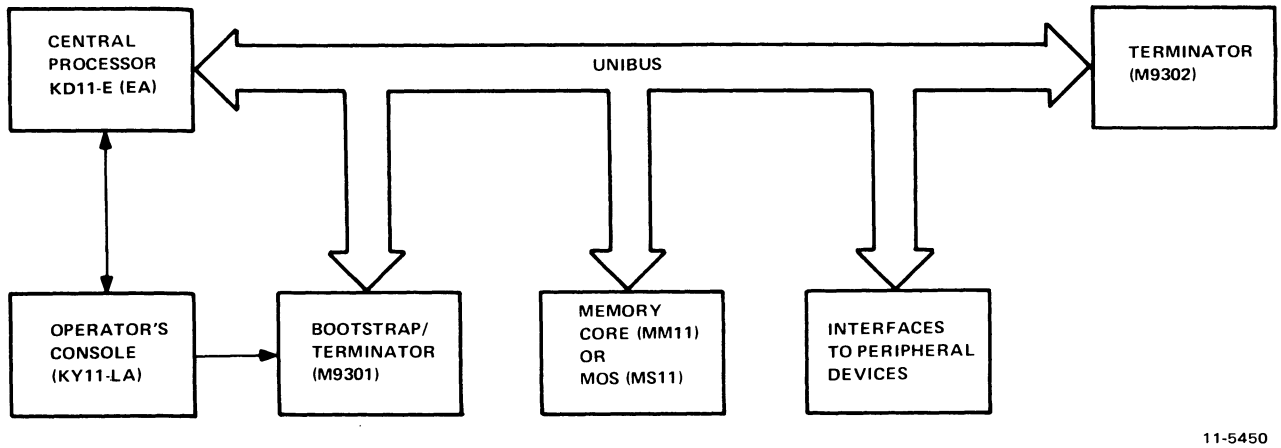


Figure 1-2 System Block Diagram

1.2.1 Unibus

All components of the PDP-11/34 computer system, including peripheral devices, are connected to and communicate with each other on a single high-speed bus known as the Unibus (Figure 1-1).

All devices on the Unibus communicate in the same manner. Addresses, data, and control information are sent along the 56 lines of the bus. Each Unibus device, including Processor registers, Peripheral Device registers, and memory locations, is assigned an address on the bus. Therefore, the central processor can access and manipulate Peripheral Device registers as easily as memory. (A detailed description of the Unibus can be found in the *Unibus Interface Manual* or the *PDP-11/34 Processor Handbook*.)

The PDP-11/34 computer system contains both standard and modified Unibus connections. The modified Unibus is similar to the standard Unibus except that certain pins have been redesignated to allow installation of memory modules in particular backplane slots (Paragraph 4.2.2.2).

1.2.2 KD11-E (EA) Central Processor

The KD11-E Central Processor Unit (CPU), designed for the PDP-11/34 computer series, is contained on two multilayer, hex-height modules, M7265 (Figure 1-3) and M7266 (Figure 1-4).

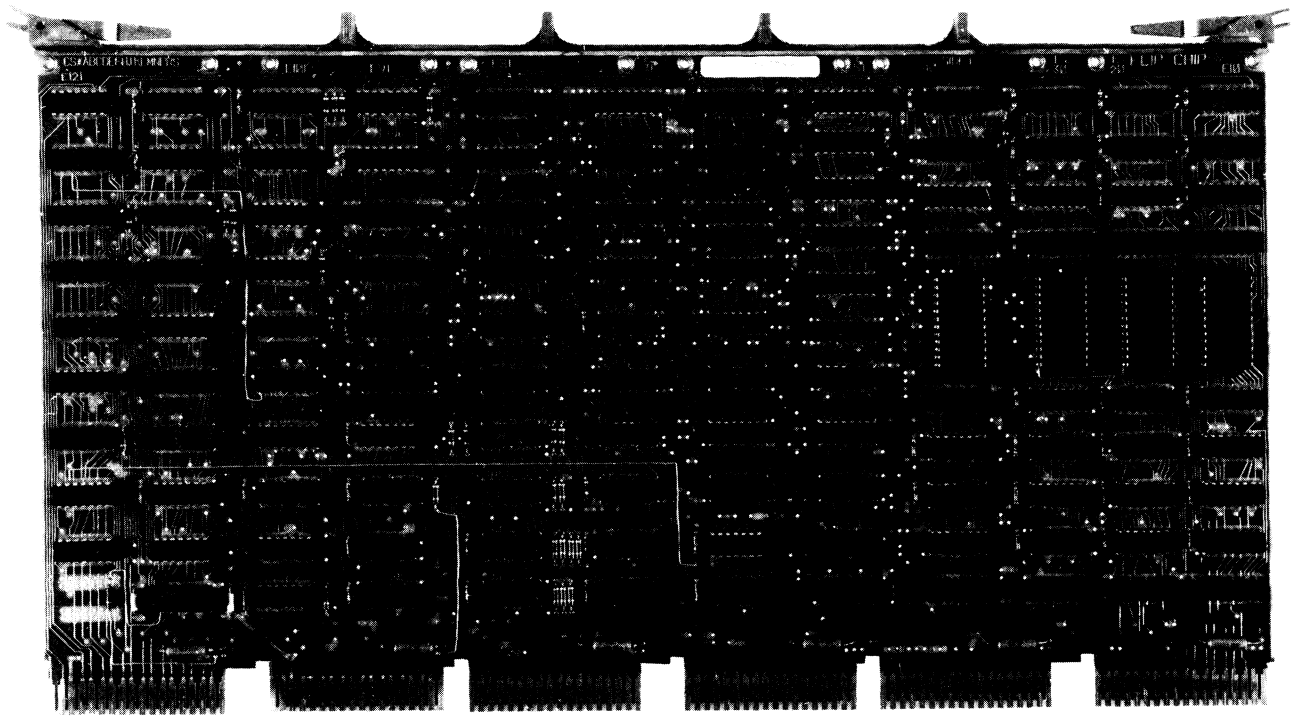


Figure 1-3 KD11-E Central Processor Unit (M7265 Module)

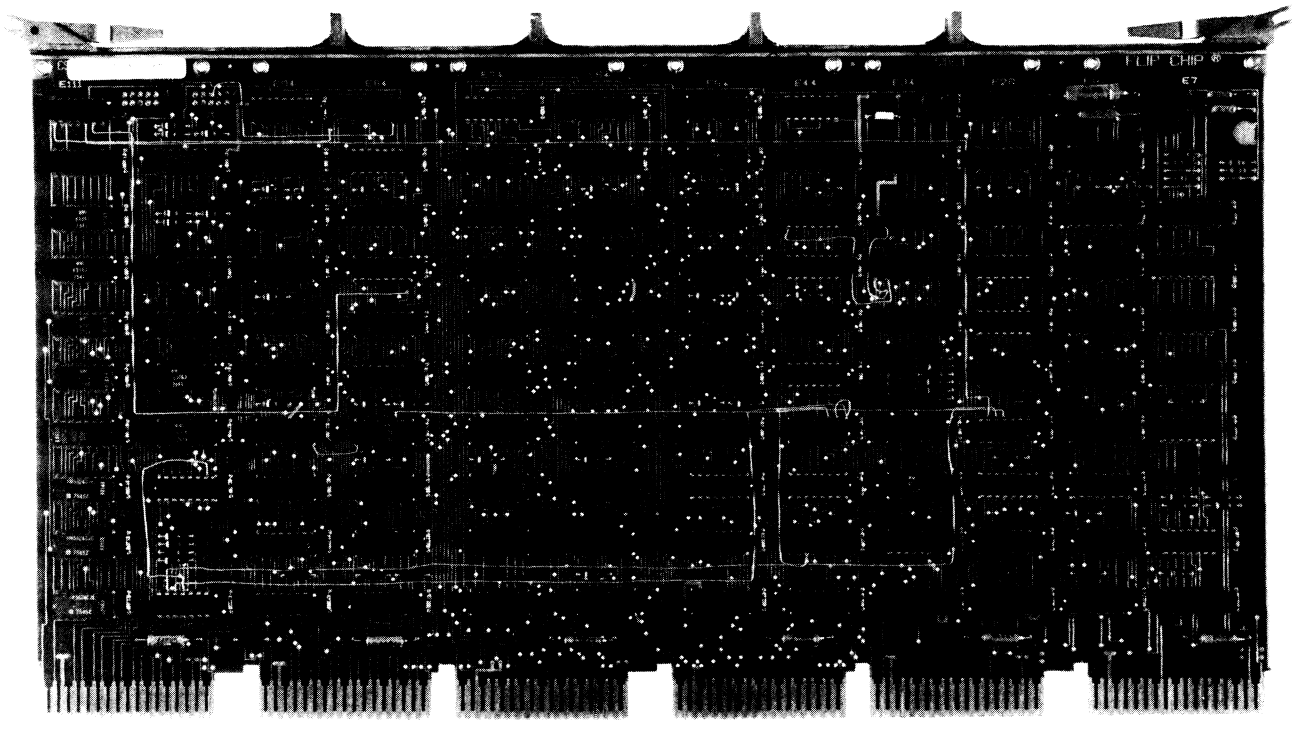


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Figure 1-4 KD11-E Central Processor Unit (M7266 Module)

The KD11-EA CPU, designed for the 11/34A, is contained on two multilayer, hex-height modules, M8265 and M8266.

The KD11-E (EA) connects to the computer system via the Unibus. The processor controls the time allocation of the Unibus for peripherals, and performs arithmetic operations, logic operations, and instruction decoding.

The Extended Instruction Set (EIS) is a standard feature of the KD11-E which provides the capability of performing hardware fixed-point arithmetic and allows direct implementation of multiply, divide, and multiple shifting. This feature allows double-precision 32-bit words to be processed.

The KD11-E also contains memory management logic which provides memory extension, relocation and protection. This allows the user to:

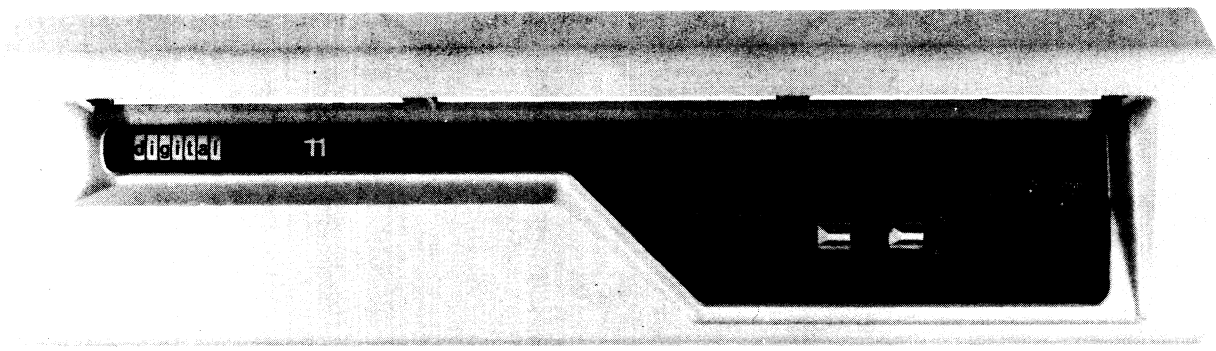
1. Extend memory space from 28K to 124K.

2. Allow efficient memory segmentation for multi-user environments.

3. Provide effective protection of memory segments in multi-user environments.

1.2.3 Operator's Console

The operator's console provides a front panel communication link between the user and computer. Unlike the traditional programmer's console, a minimum number of switches and lights are contained on the operator's console (Figure 1-5).



8107-25

Figure 1-5 Operator's Console

The three switches on the console are as follows.

Power	3-position rotary switch DC OFF, DC ON, STNDBY
HALT/CONT	2-position toggle switch HALT and CONTINUE
BOOT/INIT	Spring-action momentary switch that is normally in the BOOT position BOOT and INITIALIZE

The three indicators on the console are as follows.

BATT	Monitors conditions of battery
DC ON	Indicates presence of dc logic power
RUN	Indicates, when lighted, that the processor is in the RUN state or, when light is off, that the processor has halted.

1.2.4 M9301 Bootstrap/Terminator

The PDP-11/34 contains a special terminator module (M9301) that contains the required Unibus terminator resistors and 512 words of read-only memory (ROM). The M9301 is a double-height, extended module (Figure 1-6) that is available in three versions: M9301-YA, suited to the OEM user, M9301-YB, suited to the end user, and M9301-YF, suited to the OEM or end user.

The ROM in the M9301 contains diagnostic routines for verifying computer operation, several bootstrap loader programs for starting up the system, and the console emulator routine for issuing commands from the console terminal. The M9301 provides the PDP-11/34 with the capability of using a console terminal to replace the functions normally controlled through the programmer's console. A serial I/O terminal such as an LA36 DECwriter, VT50 Video Terminal, or an LT33 Teletype® and associated controller, when used in conjunction with the M9301, can be added to the system to provide most programmer's console functions.

Refer to the *M9301 Bootstrap/Terminator Maintenance Manual* for a complete description of the M9301.

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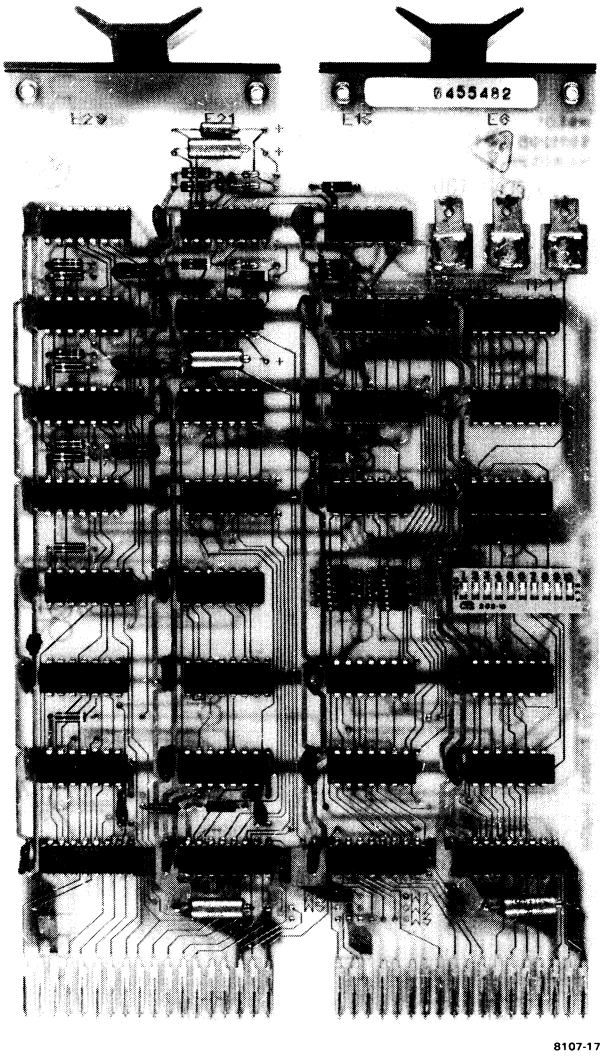


Figure 1-6 M9301 Bootstrap/Terminator Module

1.2.5 M9302 Terminator

The M9302 terminator is a double-height module (Figure 1-7) and must be installed at the end of the Unibus (furthest from the processor) in all PDP-11/34 systems. This module contains terminating resistors and additional logic which generate a BUS SACK signal if a processor GRANT signal ever reaches the end of the Unibus.

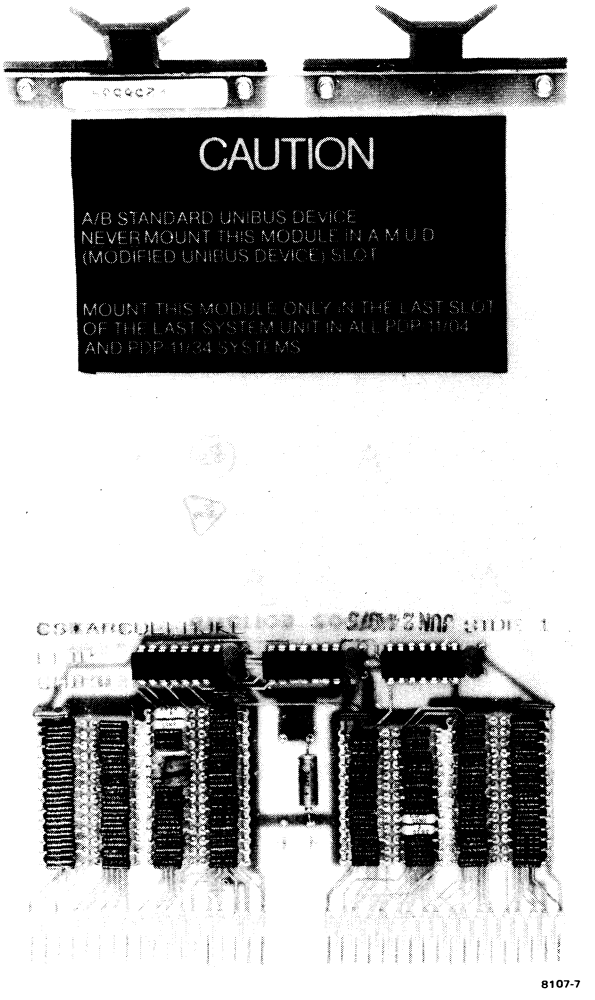
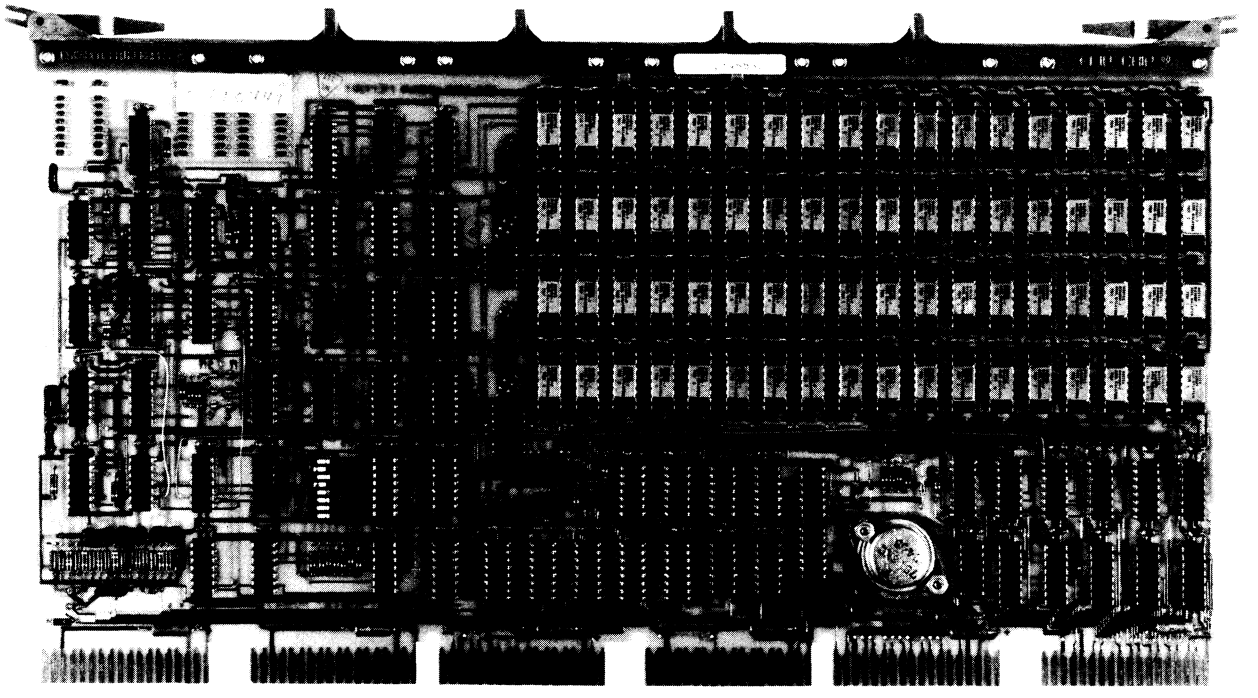


Figure 1-7 M9302 Terminator Module

1.2.6 Memory

The PDP-11/34 computer system is designed to operate with both MOS memory and core memory.

The MOS memory is available in 4K, 8K, or 16K (MS11-EP, MS11-FP, or MS11-JP) increments and each memory module consists of a single hex-height board (Figure 1-8). The MOS module contains an interface to the Unibus, timing and control logic, refresh circuitry, and an MOS storage array. (Refer to the *MS11-E-J MOS Memory Maintenance Manual* for a detailed description.) MOS memory is volatile and data is lost when power is removed. An optional battery backup unit (H775) is available that can supply the power required to preserve data in memory when system power is lost. When the system is operating in the battery backup mode, power is used for MOS memory refresh only.



8107-12

Figure 1-8 MS11-JP MOS Memory Module

Core memory is available in 8K or 16K (MM11-CP or MM11-DP) increments. The MM11-CP (Figure 1-9) consists of a hex-height, multilayer motherboard (G651) and a quad-height, bilayer daughterboard (H221). The MM11-DP (Figure 1-10) consists of a hex-height, multilayer motherboard (G652) and a hex-height, bilayer daughterboard (H222). The motherboard is inserted into the Unibus backplane and contains the Unibus interface logic, timing and control logic, X-Y drivers, and inhibit and sense circuitry. The daughterboard is attached to the motherboard and contains the core plane, stack diodes, and stack charge circuit. Core memory is not volatile and data will not be lost when system power is removed. (Refer to the associated memory manual for detailed information.)

1.2.7 Mounting Box, Backplane, and Power Supply

The PDP-11/34 system utilizes either the BA11-L [13.3 cm (5-1/4 inch) chassis] or BA11-K [26.6 cm (10-1/2 inch) chassis] mounting box. The BA11 houses the DD11 backplane and the power supply. The mounting box is divided into two sections, one containing all logic modules and the other containing the power supply. The operator's console assembly (KY11-LA) mounts on the front of the BA11 frame.

The DD11-PK backplane, implemented in the PDP-11/34, provides the electrical connections between the modules in the system. The DD11-PK consists of nine hex-height slots for module placement.

The H777 power supply is used with the BA11-L mounting box and the H765 power supply is used with the BA11-K mounting box. For cabinet-mounted PDP-11/34 systems, the 861 AC Power Controller is implemented. The 861 is used to control and distribute ac voltage to the power supplies, fans, and other electrical devices (within each cabinet) that require ac inputs within the system.

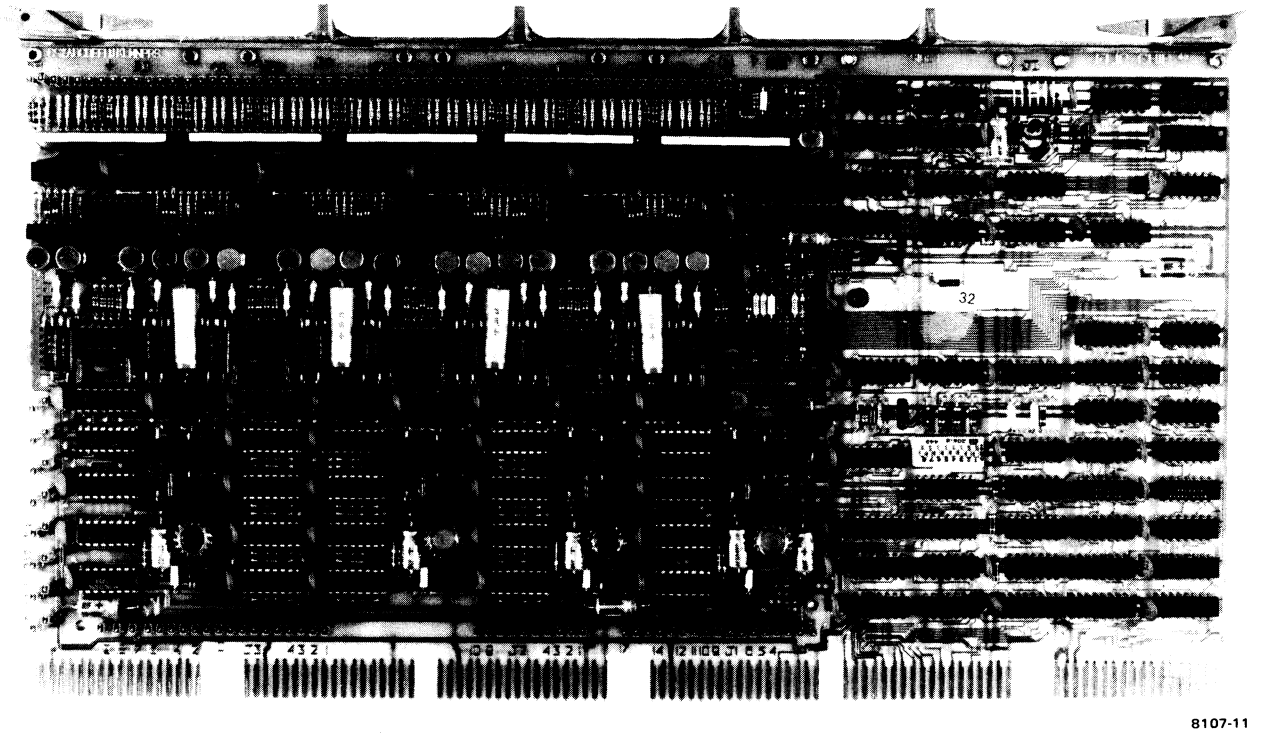


Figure 1-9 MM11-CP Core Memory Module

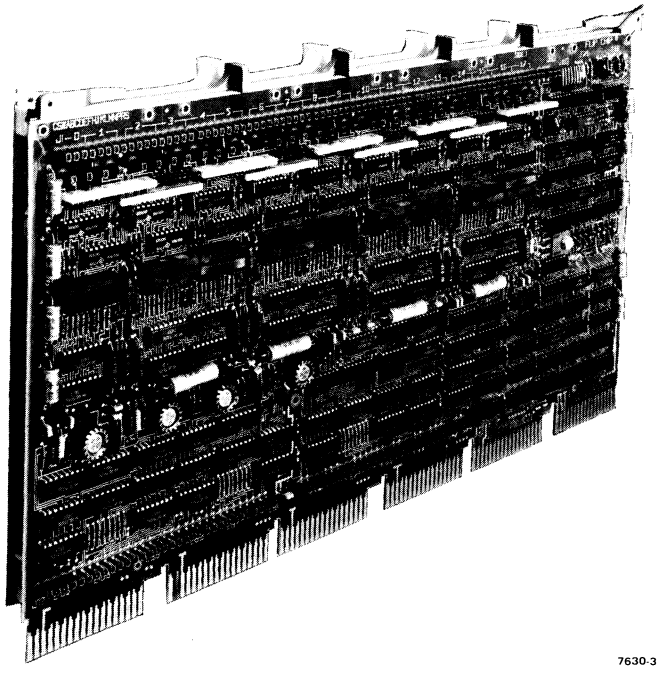


Figure 1-10 MM11-DP Core Memory Module

M7850 Parity Controller (Figure 1-11) – The M7850 Parity Controller is a double-height module that generates and checks parity on stored data in memory. This module also contains a 16-bit Control and Status register for diagnostic purposes.

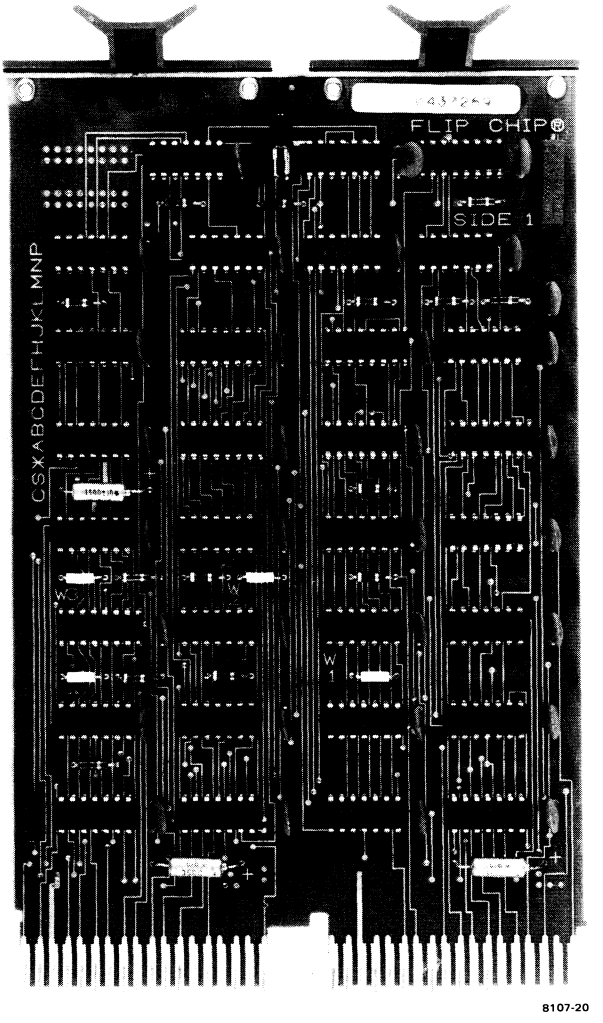


Figure 1-11 M7850 Parity Controller

1.2.8 Optional Equipment

The following options can be incorporated to expand system capabilities and meet specific requirements of the user.

DL11-W Serial Line Interface and Real-Time Clock (Figure 1-12) – The DL11-W provides an asynchronous serial line interface to an ASCII terminal (e.g., LA36, VT50, or LT33) and a line frequency clock. The serial line interface can handle data rates from 110 to 9600 baud and provides serial-to-parallel (and vice versa) data conversion for information transfer to or from the Unibus. The line clock senses the 50- or 60-Hz line frequency for internal timing and is program compatible with the standard line clock option (KW11-L) used with other PDP-11 computers.

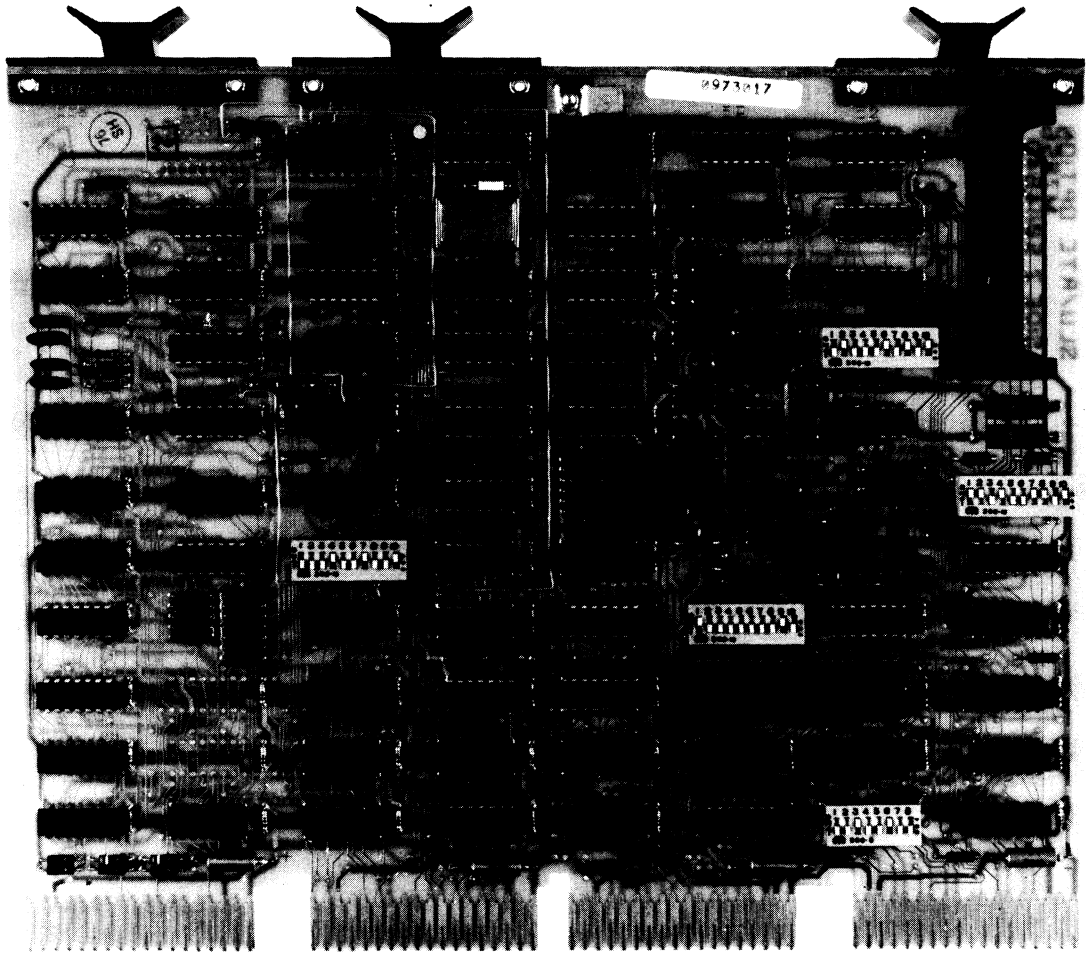
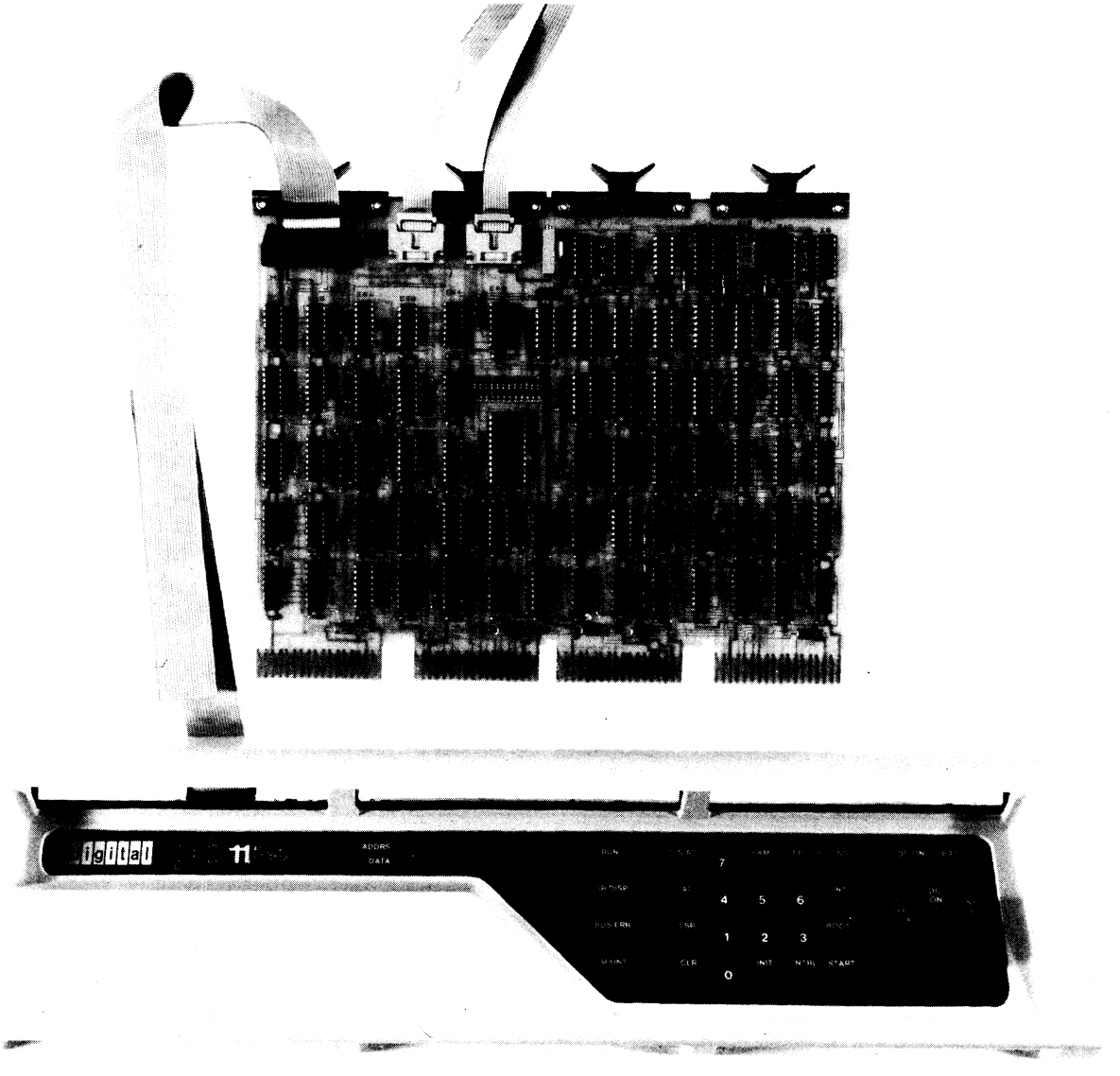


Figure 1-12 DL11-W Serial Line Interface and Real-Time Clock

KY11-LB Programmer's Console (Figure 1-13) – The PDP-11/34 programmer's console contains a 7-segment LED display and a keypad for entering and verifying data as well as controlling basic computer operations. The programmer's console can also be used in a maintenance mode which provides several hardware maintenance features (Appendix A). The console interfaces to the Unibus via a quad-height module (M7859).



8141-15

Figure 1-13 KY11-LB Console and Interface Module

H775 Battery Backup Unit – If system power is interrupted, the battery backup unit provides auxiliary power to preserve the contents of up to 32K words of MOS memory for about two hours. This auxiliary power unit is a battery that is charged by the main ac power when the computer system is operating normally. The battery backup unit is physically mounted outside the processor box to facilitate battery maintenance. The battery backup option is not available in PDP-11/34 systems using the BA11-K mounting box.

Expander Backplane – The DD11-CK (4-slot) and DD11-DK (9-slot) backplanes can be implemented by the user to expand the basic system. These expander backplanes allow greater flexibility for system configuration.

Standard PDP-11 Peripherals – The I/O capabilities of the PDP-11/34 system can be expanded through the implementation of such standard PDP-11 peripheral devices as card readers, alphanumeric display terminals, line printers, teletypewriters, or high-speed paper tape readers. Available storage devices include magnetic tapes and disk memories.

1.3 RELATED LITERATURE

For detailed information concerning each of the system components, refer to the following documents.

Manual	Document Number
BA11-K Mounting Box Manual	EK-BA11K-MM
BA11-L Mounting Box Manual	EK-BA11L-MM
DL11-W Maintenance Manual	EK-DL11W-MM
KD11-E Processor Manual (PDP-11/34)	EK-KD11E-TM
M9301 Bootstrap Terminator Maintenance Manual	EK-M9301-MM
MM11-C/CP Core Memory Manual	EK-MM11B-TM
MM11-D/DP Core Memory Manual	EK-MM11D-TM
MS11-E-J MOS Memory Maintenance Manual	EK-MS11E-MM
PDP-11 Peripherals Handbook	EP-PDP11-HB
PDP-11/34 Processor Handbook	EP-11034-HB
KD11-EA Processor Manual (PDP-11/34A)	EK-KD1EA-MM

CHAPTER 2
OPERATION

2.1 OPERATOR'S CONSOLE (KY11-LA)

In the PDP-11/34 system, communication between the user and computer is provided by the operator's console. The M9301 bootstrap/terminator allows the operator's console, in conjunction with an ASCII terminal, to provide programmer's console functions to the user.

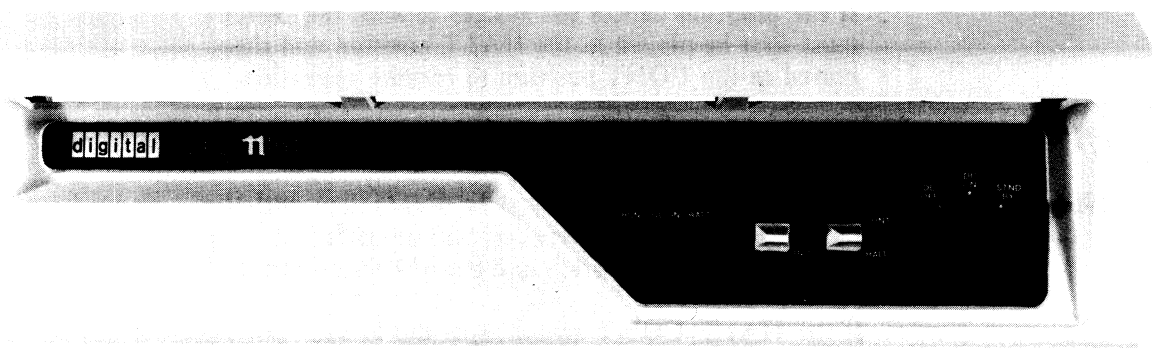


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Figure 2-1 PDP-11/34 Operator's Console

2.1.1 Console Switches

The operator's console contains three switches: power, HALT/CONT, and BOOT/INIT. The function of each switch and its effect on system operation is explained as follows.

Power (3-position rotary switch)

DC OFF	DC power is removed from the system; contents of MOS memory are lost and fans are off.
DC ON	Power is applied to the computer system.

STNDBY — Standby; dc power to the computer is off, but dc power is applied to MOS memory (to avoid data loss).

NOTE

STNDBY position is not functional in the BA11-K box.

WARNING

The DC OFF position does not remove ac power from the system. AC power is removed only by disconnecting the line cord.

HALT/CONT (2-position toggle switch)

HALT — The program is stopped. The system (including console emulator functions) cannot be run in this position.

CONT — The program is allowed to continue.

NOTE

If the program causes the system to halt, the switch must first be placed in the HALT position and then moved to the CONT position to resume operation.

BOOT/INIT (Spring-action momentary switch that is normally in the BOOT position)

INIT — When this switch is pressed to INITialize and then released (returned to BOOT position), an operation will be performed depending on the setting of the HALT/CONT switch and the M9301 switch settings (Paragraph 4.3.2).

If the HALT/CONT switch is in the HALT position when BOOT/INIT is pressed and released, only the processor will be initialized and Peripheral Device registers will not be cleared.

If the HALT/CONT switch is in the CONT position when BOOT/INIT is pressed and released; the processor will be initialized, Peripheral Device registers will be cleared, and the M9301 program will be executed.

NOTE

The BOOT operation is only initiated if the BOOT/INIT switch is pressed and released. Holding the switch in the INIT position will cause a continuous initialize.

CAUTION

Pressing the BOOT/INIT switch to the INIT position while running a program will abort the program in progress and may destroy general register and memory contents.

2.1.2 Console Indicators

The three indicators (BATT, DC ON, and RUN) on the operator's console provide the following information to the user.

BATT	Off	Battery voltage is below the minimum level required to maintain the contents of MOS memory, or the battery is not present in the system.
	Slow flash (1 flash/2 seconds)	Battery is charging and the voltage is above the minimum level required to maintain contents of MOS memory if power is removed. The amount of time that memory will be retained will depend on the degree of discharge of the battery. The flash rate is fixed and does not vary with the charge rate of the battery.
	Fast flash (10 flashes/second)	Indicates that primary power has been lost and the battery is discharging while maintaining MOS memory contents. The flash rate is fixed and does not indicate the charge level remaining on the battery.
	Continuous on	Battery is present and fully charged.
DC ON	On	Indicates that dc power is applied to the logic but does not imply that the power is within the required levels.
	Off	DC power is off.
RUN	On	Indicates either: 1. Processor is executing, or 2. Processor is attempting to run but is disabled due to a system failure.
	Off	Processor has halted.

2.1.3 Console Emulator

The M9301 module contains a console emulator routine in ROM memory. This routine allows the operator to use a console terminal to generate functions similar to those provided on the traditional programmer's console. The console emulator allows the user to perform LOAD, EXAMINE, DEPOSIT, START, and BOOT functions by typing in the appropriate code on the keyboard. The M9301 also contains non-destructive CPU diagnostic tests which are performed prior to entering the console emulator and additional CPU and memory diagnostics executed prior to entering a boot routine.

The following is a summary of the console emulator functions.

LOAD	Loads the address to be manipulated into the system.
EXAMINE	Allows the operator to examine the contents of the address that was loaded.
DEPOSIT	Allows the operator to write into the address that was loaded and/or examined.
START	Initializes the system and starts execution of the program at the address loaded.
BOOT	Allows the booting of a specified device by typing in a 2-character code and unit number (if required). If a number is not typed, the default number will be zero.

2.1.3.1 Entry Into the Console Emulator - In order to enter the console emulator, the M9301 bootstrap/terminator switches must be properly set. (Refer to Paragraph 4.3.2 to determine the correct switch settings.)

The console emulator can be entered in the following ways depending on the setting of the M9301 switches.

1. Move the power switch to the DC ON position.
2. Press and release the BOOT/INIT switch.
3. Automatic entry on return from a power failure.
4. Load address and start (via programmer's console).

2.1.3.2 Register Printout - Once the console emulator routine has started, a series of numbers representing the contents of R0, R4, SP, and "OLD PC" respectively, will be printed by the terminal. This sequence will be followed by a $ on the next line. The following is an example of the printout. (X signifies an octal number, 0–7.)

XXXXXX	XXXXXX	XXXXXX	XXXXXX
$			
R0	R4	R6 STACK POINTER (SP)	"OLD PC" PROGRAM COUNTER

PROMPT CHARACTER
on next line

NOTE

Whenever there is a power-up microroutine, or the BOOT/INIT switch is released from the INIT position, the current PC will be stored in R5. The contents of R5 are printed out as shown above (noted as "OLD PC").

When the BOOT/INIT switch is pressed and released, the system will print out R0, R4, SP, and "OLD PC" followed by a prompt character, as previously described. This feature is especially valuable when the system has halted unexpectedly. The operator can determine where the system has halted by examining the "OLD PC" and subtracting two.

CAUTION

Pressing the BOOT/INIT switch may alter the contents of the General Purpose registers and make it impossible to continue the program.

2.1.3.3 Console Emulator Functions – As previously mentioned, the console emulator can be used to perform LOAD, EXAMINE, DEPOSIT, START, and BOOT functions. Once the system has been powered up or initialized via the BOOT/INIT switch and R0, R4, SP, "OLD PC" and $ have been printed, the console emulator is entered.

The following symbols are used in the discussion of the keyboard input format:

Space bar: (SB)
Carriage return key: (CR)
Any number 0–7 (octal number) key: (X)

The capital letters L, E, D, and S on the keyboard are used to perform the functions LOAD, EXAMINE, DEPOSIT, and START, respectively. The keyboard input format required to perform each of the functions is as follows.

Function	Format
Load Address	L (SB) (X) (X) (X) (X) (X) (X) (CR)
Examine address loaded	E (SB)
Deposit contents into address loaded and/or examined	D (SB) (X) (X) (X) (X) (X) (X) (CR)
Start program	S (CR)

The first octal number that is typed (X) will be the most significant digit and conversely the last number typed will be the least significant digit. The console emulator routine can accept up to six octal numbers in the range of 0–32K (word locations). The lower 28K of memory and the 4K I/O page can be directly manipulated by the console emulator. If all six octal numbers are input, the most significant number must be a zero or a one. When an address or data word contains leading zeros, the leading zeros can be omitted when loading the address or depositing the data. Refer to Appendix B for the procedure required to examine and deposit in locations above 28K.

NOTE

1. **The console emulator will accept octal numbers only (i.e., typing 8 or 9 within the address will cause the entire address to be ignored).**

2. **The console emulator will accept even addresses only (i.e., the least significant digit must be a 0, 2, 4, or 6).**

3. **The General Purpose registers (GPR) cannot be addressed from the console emulator.**

2.1.3.4 Examples of Console Emulator Operation – The following example implements the LOAD, EXAMINE, DEPOSIT, and START functions.

If the operator wishes to:

1. Turn on power
2. Load address 700
3. Examine location 700
4. Deposit 777 into location 700
5. Examine location 700
6. Start at location 700

The operator performs the following:

	Operator	Terminal Display
1.	Turns on power	XXXXXX XXXXXX XXXXXX XXXXXX
2.	L (SB) 700 (CR)	$ L 700
3.	E (SB)	$ E 000700 XXXXXX
4.	D (SB) 777 (CR)	$ D 777
5.	E (SB)	$ E 000700 000777
6.	S (CR)	$ S

Successive examine operations are permitted using the console emulator. Successive examine commands issued by the operator will cause the address to increment by two and will display consecutive addresses and the contents of each.

The following example examines addresses 500 through 506.

Operator	Terminal Display
L (SB) 500 (CR)	$ L 500
E (SB)	$ E 000500 XXXXXX
E (SB)	$ E 000502 XXXXXX
E (SB)	$ E 000504 XXXXXX
E (SB)	$ E 000506 XXXXXX

Successive deposit operations are also permitted using the console emulator and the address will also increment by two with each deposit command.

The following example deposits 60 into location 500, 2 into location 502, and 4 into location 504.

Operator	Terminal Display
L (SB) 500 (CR)	$ L 500
D (SB) 60 (CR)	$ D 60
D (SB) 2 (CR)	$ D 2
D (SB) 4 (CR)	$ D 4

Alternate deposit-examine operations are permitted but the address will not increment after each command is typed. The address will contain the last data that was deposited.

The following example loads address 500, deposits 1000, 2000, and 5420 in that address, and then examines location 500 after each deposit:

Operator	Terminal Display
L (SB) 500 (CR)	$ L 500
D (SB) 1000 (CR)	$ D 1000
E (SB)	$ E 000500 001000
D (SB) 2000 (CR)	$ D 2000
E (SB)	$ E 000500 002000
D (SB) 5420 (CR)	$ D 5420
E (SB)	$ E 000500 005420

2.1.3.5 Booting from Peripheral Devices – The console emulator can be used to input bootstrap routines from peripheral devices. Once the prompt character ($) has been displayed on the terminal (as a result of power-up or activating BOOT/INIT switch), the system is ready to load a bootstrap routine from the selected device. The following procedure is implemented to boot from the keyboard:

1. Locate the 2-character code that corresponds to the peripheral to be booted (Tables 2-1 and 2-2).

Table 2-1 Bootstrap Routine Codes for M9301-YA and M9301-YB

Device	Description	Boot Command
RK11	Disk cartridge	DK
RP11	RP02/03 disk pack	DP
TC11	DECtape	DT
TM11	800 bits/inch magtape	MT
TA11	Magnetic cassette	CT
RX11	Diskette	DX
DL11	Terminal reader	TT
PC11	Paper tape reader	PR
RJS03/04*	Massbus fixed-head disk	DS
RJP04*	Massbus disk pack	DB
TJU16*	Massbus tape drive	MM
RJS03/04, RJP04, or TJU16*	Mixed combination of Massbus devices	MC

*Devices supported by M9301-YB (end-user version) only.

Table 2-2 Bootstrap Routine Codes for M9301-YF

Device	Description	Boot Command
RK11	RK03/05 disk cartridge control	DK
RP11	RP02/03 disk pack control	DP
TC11	TU56 DECtape control	DT
TM11	TU10 magtape control	MT
RX11	RX01 diskette control	DX
DL11	Terminal reader control	TT
PC11	Paper tape reader control	PR
RJS03/04	Massbus fixed-head disk	DS
RJP04/05/06	Massbus disk pack	DB
TJU16	Massbus tape drive	MM
RK611	RK06 disk drive control	DM

NOTE

The user can boot from a peripheral directly upon power up (M9301-YA or M9301-YF versions only) provided the switches on the M9301 module are set properly (Paragraph 4.3.2).

2. Load medium (paper tape, magtape, disk, etc.) into the peripheral, if required.

3. Verify that the peripheral indicators signify that the peripheral is ready (if applicable).

4. Type the 2-character code obtained from Table 2-1.

5. If more than one unit of a given peripheral exists, type the unit number to be booted (0–7). If a number is not typed, the default number will be 0.

6. Type (CR); this initiates the boot.

The following points should be remembered before attempting to boot from a peripheral device.

1. The medium (paper tape, disk, magtape, etc.) must be placed in the peripheral prior to booting.

2. The machine will not be under control of the console emulator after booting.

3. The program that is booted must be:

   a. Self-starting, or
   b. Restartable after the console emulator is recalled.

4. Actuating the BOOT/INIT switch will always abort the program being run. The contents of the General Purpose registers (R0–R7) may be altered.

2.1.3.6 Possible Operator Errors – This paragraph discusses the effect of erroneously pressing the BOOT/INIT switch and solutions to incorrect entries of information to the console emulator routine.

As previously mentioned, pressing the BOOT/INIT switch while a program is running will cause that program to be aborted. All devices that respond to system INIT will be cleared and the contents of all General Purpose registers may be modified. The console emulator will be activated (possible on M9301-YA, YB, or YF versions) or a peripheral routine will be booted (possible on M9301-YA or YF versions only). Critical data in the user's system will probably be lost and the possibility of retrieving that data will depend on the user's program.

Table 2-3 lists possible operator errors that may be encountered when implementing the LOAD, EXAMINE, DEPOSIT, or START functions.

NOTE

If an entry has not been completed and the user realizes that an incorrect character has been entered, the user can press the rubout or delete key and delete the entire entry.

Table 2-3 Load, Examine, Deposit, and Start Errors

Error	Result
L, E, S, or D was followed by a key other than space bar (SB).	Terminal display will return a prompt character ($) to signify an unknown code.
An illegal number (8 or 9) or incorrect alpha key (Y) is typed after the correct load sequence.	Upon receipt of the illegal number or alpha key, the entire address will be ignored and $ will be returned.
The most significant octal number in a 6-bit address is greater than 1.	The address will be loaded but the most significant digit will be interpreted as follows: Number typed (number accepted) 7(1), 6(0), 5(1), 4(0), 3(1), 2(0).
An extra (seventh) octal number is typed.	Any size word will be accepted but only the last six digits typed will be remembered.
A memory location is loaded whose address is nonexistent.	No errors will result unless a deposit, examine, or start is attempted.
Examine, start, or deposit is attempted at an odd memory location or at a nonexistent memory location.	The system will halt when (SB) is executed.
Examine is performed without loading an address prior to the first examine.	Examination of an unknown address will be performed and possibly the system could try to access a nonexistent address. **NOTE** **If a legal address is examined, the address and data will be typed out. If address is illegal, the computer will halt.**

Table 2-3 Load, Examine, Deposit, and Start Errors (Cont)

Error	Result
Start is performed without loading an address prior to starting.	Start at an unkown location will occur.
Deposit is performed without previously loading an address or without knowing what address had been previously loaded.	Data will be written over and lost or machine will halt.

2.2 PROGRAMMER'S CONSOLE (KY11-LB)

The optional PDP-11/34 programmer's console (KY11-LB) provides all the standard functions required for entering and verifying data as well as controlling basic computer operations. The programmer's console can also be used in a maintenance mode that provides several hardware maintenance features. (Refer to Appendix A for a discussion of the KY11-LB operation in the maintenance mode.) The KY11-LB contains a 20-pushbutton keypad for operator/programmer control, 6 indicator LEDs for monitoring system status, a 6-digit display for address or data, and a dc power switch. The programmer's console interfaces to the Unibus via a quad-height module (M7859) which must be installed in the processor backplane. Refer to the *Programmer's Console (KY11-LB) Maintenance Manual* for a detailed discussion.

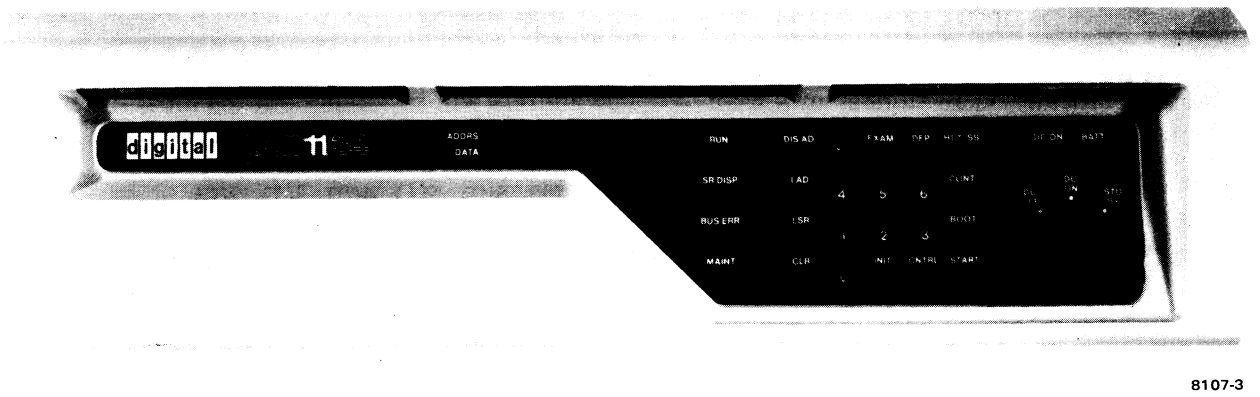


Figure 2-2 PDP-11/34 Programmer's Console

2.2.1 KY11-LB Controls and Indicators

The following provides a brief functional description of the 6-digit display, indicators, and the pushbutton keyboard provided on the programmer's console. The dc power switch and the BATT, DC ON, and RUN indicators function in the same manner as described for the operator's console (Paragraphs 2.1.1 and 2.1.2).

Display — The 7-segment display represents the current address or the contents of the current address. Each segment of the display will contain an octal digit (0–7). Six-digit numbers are generated as octal digits and are entered from the right and left-shifted.

Indicators

SR DISP	Switch Register Display – Indicates, when on, that the contents of the Switch register (address 777570) are being displayed.
MAINT	Maintenance – Indicates, when on, that the console is operating in maintenance mode.
BUS ERR	Bus Error – Indicates, when on, that an examine or deposit resulted in a SSYN timeout, or that HALT GRANT was not received after a HALT REQUEST was issued.

NOTE

This indicator reflects a bus error by the console only. The indicator does not reflect bus errors due to other devices such as the processor.

Pushbutton Keys

0, 1, 2, 3, 4, 5, 6, 7	Allow the operator to enter data (octal digits) into the display.
LSR	Load Switch Register – A copy of the contents of the display are placed in Unibus address 777570.
LAD	Load Address – The contents of the display become the current address. The display is cleared when LAD is pressed.
DIS AD	Display Address – The current address is displayed. The next examine or deposit will occur at the address displayed.
CLR	Clear – The display is cleared in preparation for entry of new data via the number keys.
EXAM	Examine – A copy of the data contained in the location specified by the current address is placed in the display. This key is operative only if the processor is halted.
DEP	Deposit – A copy of the data being displayed is transferred to the location specified by the current address. This key is operative only if the processor is halted.
CNTRL	Control – The control key is used in conjunction with other keys to provide certain functions. The requirement of having both CNTRL and the second key pressed at the same time prevents accidental use of these functions.

The following pushbutton keys must be used in conjunction with the CNTRL key to provide the function described. In each case, the CNTRL key must be pressed first and held down while the second key is pressed.

INIT (with CNTRL)	Initialize – Causes BUS INIT L to be generated for 150 ms. Key is operative only if processor is halted.

HALT/SS (with CNTRL)	Halt/Single Step – Halts the processor if the processor is running. To single instruction step the processor, halt the processor, then press the HALT/SS key without pressing the CNTRL key. After a halt, the display will contain the contents of R7 (program counter).
CONT (with CNTRL)	Continue – Allows the processor to continue from a halted state using its current program counter. The contents of the Switch register are displayed.
START (with CNTRL)	This key is operative only if the processor is halted. The function causes the program counter (R7) to be loaded with the current address. BUS INIT L is then generated and the processor is allowed to run. Switch register contents are then displayed.
BOOT (with CNTRL)	Causes the M9301 bootstrap/terminator to be activated if present in the system. Console will boot only if processor is halted.
No. 7 (with CNTRL)	When the No. 7 key and CNTRL key are both pressed, the current address plus the value presently being displayed plus 2 are added together. The result is then displayed. This function allows the console to calculate the correct offset address when mode 6 or 7, register 7 instructions are encountered. The required index must be in the display so that when the keys are pressed, the index will be added to the PC+2. The offset address is then displayed.
No. 6 (with CNTRL)	When the No. 6 key and CNTRL key are both pressed, the contents of the Switch register are added to the value presently being displayed. The result is then displayed. This function allows the console to calculate the correct offset address when mode 6 or 7 instructions that do not use register 7 are encountered. To implement this function, it is easiest to put the index in the Switch register, then examine the general register that contains the base address, thereby placing the base address in the display. Then, when the No. 6 key and CNTRL key are both pressed, the index and base address will be added and the correct offset address will be displayed.
No. 1 (with CNTRL)	Maintenance Mode – This key combination puts the console in maintenance mode. When the console is in maintenance mode, normal console mode keypad functions are not available (Refer to Appendix A for a description of the maintenance mode keypad functions.) The CLR key causes the console to exit from maintenance mode and enter console mode via a processor halt.

2.2.2 Notes on Operation

The input format required to perform each of the functions previously described is shown as follows. (X denotes an octal number, 0–7.)

XXXXXX	LSR
XXXXXX	LAD
XXXXXX	DEP

Note that, unlike the operator's console, the data must be entered before the function key is pressed.

Prior to entering a new 6-digit number, if the display is non-zero, the clear key (CLR) should be pressed to initially zero the display. If the display is not cleared, the new data will be left-shifted into the existing data and may result in an erroneous number in the display.

An erroneous display will also result if, while the processor is running and the Switch register is being displayed, a numeric key (0–7) is pressed. Although the SR DISP indicator will be on, the display will no longer reflect the actual contents of the Switch register. If any time while the processor is running the operator wishes to examine the contents of the Switch register, the CNTRL and CONT keys should be pressed simultaneously. This action will not affect processor operation.

The console requires an 18-bit address. This is especially important to remember when accessing Device registers (i.e., 777560 must be input rather than 177560 to address a Device register). If the 18-bit address is not used, access to memory or to a nonexistent address will occur.

In order to single instruction step the processor from a given starting address, the program counter (R7, Unibus address 777707) must be loaded with the starting address. For example, to single instruction step the processor from the beginning of a program starting at location 1000, the following sequence is required:

```
777707   LAD
  1000   DEP
         INIT (With CNTRL pressed)
HALT/SS
HALT/SS
etc.
```

The above procedure is required only if the program counter does not already contain the desired address.

2.2.3 Examples of Programmer's Console Operation

The following example implements the load address, load switch register, deposit, examine, display address, start, halt, continue, and single instruction step functions. To demonstrate these functions, the following program is loaded into memory.

PROGRAM

```
1000   12737  177777   1016   START:   MOV #177777,@#1016   ;LOAD LOCATION 1016
1006   00240                          NOP                  ;DO NOTHING
1010   00240                          NOP                  ;DO NOTHING
1021   00137  01000                   JMP START            ;LOOP
```

The program is loaded into memory by depositing the following data into each associated memory address.

Address	Data (instruction)
1000	012737
1002	177777
1004	001016
1006	000240
1010	000240
1012	000137
1014	001000
1016	000000

The data is loaded by first loading address 1000, and then making successive deposits. Note that the processor must first be halted if the RUN indicator is on (EXAM and DEP keys are operative only if the processor is halted).

Operator Input	Display
HALT/SS (with CNTRL pressed) (if processor is running)	
CLR	000000
1000 LAD	000000
12737 DEP and then CLR	012737 and then 000000
177777 DEP and then CLR	177777 and then 000000
1016 DEP and then CLR	001016 and then 000000
240 DEP and then CLR	000240 and then 000000
240 DEP and then CLR	000240 and then 000000
137 DEP and then CLR	000137 and then 000000
1000 DEP and then CLR	001000 and then 000000
DEP	000000
DIS AD	001016

Successive deposit operations cause the address to be incremented by 2. Note that the display must be cleared (if it is non-zero) before entering new data. Successive examine operations can also be performed. Again, the address is incremented by two after each successive examine.

NOTE

If the address is in the range 777710–777717 (address of general registers), successive examine will increment the address by one.

To verify that the above data has been deposited correctly, load address 1000 and perform successive examines as follows:

Operator Input	Display
CLR	000000
1000 LAD	000000
EXAM	012737
EXAM	177777
EXAM	001016
.	
.	
.	

Once the program has been loaded and verified, the program can be started, continued, halted and single instruction stepped. To demonstrate these functions, first load the Switch register with 125252 and then load the program starting address (1000).

Operator Input	Display	
125252 LSR	125252	
CLR	000000	
1000 LAD	000000	
START (with CNTRL pressed)	125252	Display shows contents of Switch register.
CLR	000000	
CONT (with CNTRL pressed)	125252	Display shows contents of Switch register.
HALT/SS (with CNTRL pressed)	001006	*See NOTE
HALT/SS	001010	
HALT/SS	001012	
HALT/SS	001000	
HALT/SS	001006	
HALT/SS	001010	
HALT/SS	001012	
CLR	000000	
001016 LAD	000000	
EXAM	177777	Result of instruction at address 1000.

NOTE

When the processor is halted via the HALT/SS (with CNTRL) key, the display will shown the current program counter (PC). The display contents will therefore depend on which instruction is currently being executed.

When the single instruction step function (HALT/SS key) is used, the display will show the current program counter and the program will be single instruction stepped from that location.

Refer to the *KY11-LB Maintenance Manual* for a more detailed discussion of the programmer's console operation.

CHAPTER 3
FUNCTIONAL SYSTEM DESCRIPTION

3.1 GENERAL

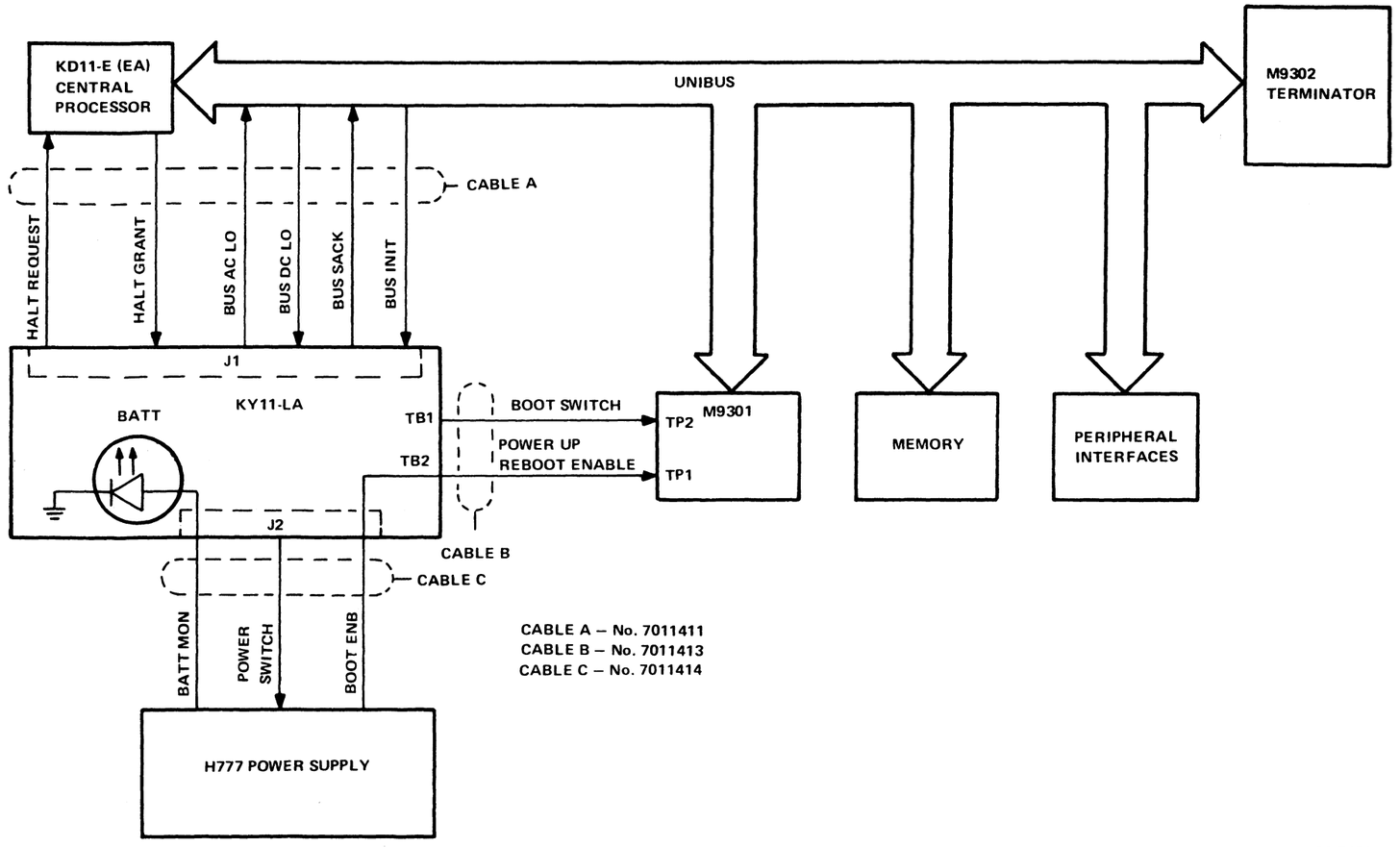
This paragraph provides a description of the interaction between PDP-11/34 system components. Figures 3-1 and 3-2 are block diagrams of the system showing interconnecting signals for the BA11-L and BA11-K mounting boxes, respectively.

3.1.1 Halt-Continue Function

The operator's console can be used to halt the processor via the HALT/CONT switch. When the HALT/CONT switch is moved to the HALT position, the console asserts the signal HALT RQST L which is recognized by the processor like a BUS request. The HALT request is therefore serviced according to its priority. The order of priority for all BUS requests and other traps is listed in Table 3-1. The processor responds to HALT RQST L by inhibiting the processor clock and returning the signal HALT GRANT H to the console. HALT GRANT H causes the console to assert BUS SACK L, thereby gaining control of the Unibus. BUS SACK L, in turn, causes the processor to drop HALT GRANT H. The user can keep the processor in the halted state indefinitely. In the halt state, BUS SACK L and HALT RQST L are asserted. When the HALT/CONT switch is returned to the CONT position, the console releases BUS SACK L and HALT RQST L and the processor continues operation.

Table 3-1 Priority Service Order

Priority	Service Order
Highest	Halt (Instruction)
	Odd Address
	Memory Management Error
	Timeout
	Parity Error
	Instruction Traps
	Trace Traps
	Stack Overflow
	Power Fail
	Halt Switch (on console)
	BR7
	BR6
	BR5
	BR4
Lowest	Next Instruction Fetch



11-5451

Figure 3-1 PDP-11/34 System Interconnections (BA11-L Mounting Box)

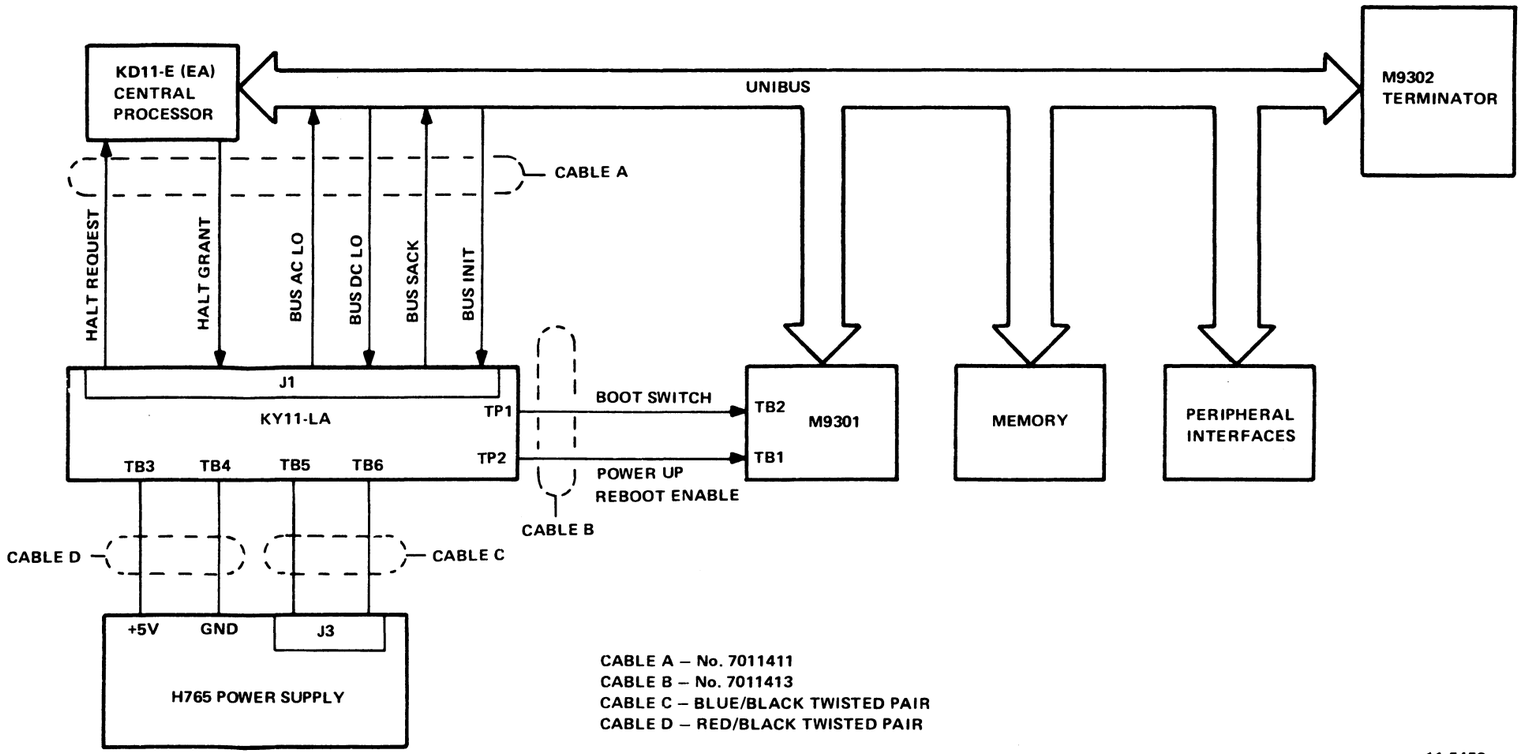


Figure 3-2 PDP-11/34 System Interconnections (BA11-K Mounting Box)

3.1.2 Boot-Initialize Function

The operator's console activates the M9301 bootstrap/terminator via the BOOT/INIT switch. BOOT/INIT is a spring-action momentary switch that is normally in the BOOT position. When the BOOT/INIT switch is pressed to the INIT position, the two signals BUS AC LO L and BOOT SW L are generated. BOOT SW L is the enabling signal for the M9301. When the switch is released from the INIT position to the BOOT position, the two signals BUS AC LO L and BOOT SW L allow the processor to start a power-up sequence. The processor then attempts to read a new processor status word (PSW) from memory location 26_8. Address 26_8 is logically ORed with the address asserted by the M9301 (address lines enabled by BOOT SW L) to generate 773026_8. This location is in the M9301 ROM address space and contains the starting address of an optionally selected routine. Once a new PSW is obtained from location 773026_8, the processor attempts to read a new program counter (PC) from memory location 24_8. Address 24_8 is also logically ORed with the address assertd by the M9301 to generate 773024_8, also located in the ROM address space. The specific routine initiated by the above sequence depends on the setting of switches located on the M9301.

NOTE

The PSW obtained from the M9301 (773026_8) sets the priority level of the CPU to 7.

3.1.3 Power-Up Reboot Enable Feature

The Power-Up Reboot Enable switch (S1-2) located on the M9301 provides the user with the option of automatically rebooting (activating the M9301) whenever the processor is powered up. If the switch is closed (ON position) and the processor begins a power-up routine, circuitry on the M9301 will be activated. The power-up sequence that follows will then be the same as that described for the BOOT-INIT function (i.e., the PSW and PC will be obtained from the M9301 ROM address space).

If the Power-Up Reboot Enable switch is open, (OFF position) the M9301 will be activated (during a power-up) only if the signal BOOT ENB is asserted low. BOOT ENB L is generated by the power supply and is transferred to the M9301 via the operator's console. Here, the operator's console functions only as a connector. BOOT ENB L is asserted if the +15 and -15 voltages are lost during battery backup operation. The voltage loss means that the contents of MOS memory are lost. BOOT ENB L will remain asserted until the signal BUS AC LO goes high. When BUS AC LO and BOOT ENB are both asserted low, the circuitry on the M9301 is enabled. When BUS AC LO goes high, the processor will begin a power-up routine. With the M9301 enabled, the processor will read the program counter and processor status word from the M9301 ROM address space (Paragraph 3.1.2). This feature allows the operator to automatically reboot on power up only if MOS memory contents are lost. If MOS memory has been retained during a power fail (by the battery backup unit) the processor will perform its normal power-up routine.

NOTE

In systems containing core memory, the black wire that connects to TP1 on the M9301 must be disconnected and taped. This will disable the power-up reboot enable feature.

3.1.4 Sack Turnaround Feature

The M9302 terminator provides circuitry that generates a BUS SACK signal if a GRANT signal ever reaches the end of the Unibus. The bus grant lines (BG4:BG7, and NPG) are ORed on the M9302 to produce BUS SACK L which is returned to the processor (Figure 3-3). BUS SACK L will cause the processor to drop the asserted grant line which will in turn cause BUS SACK L to be dropped.

3.2 KY11-LA DETAILED DESCRIPTION

The KY11-LA operator's console provides the means for controlling dc power (dc power switch), indicating systems status (BATT, DC ON, and RUN indicators), halting the processor (HALT/CONT switch) and activating the M9301 (BOOT/INIT switch).

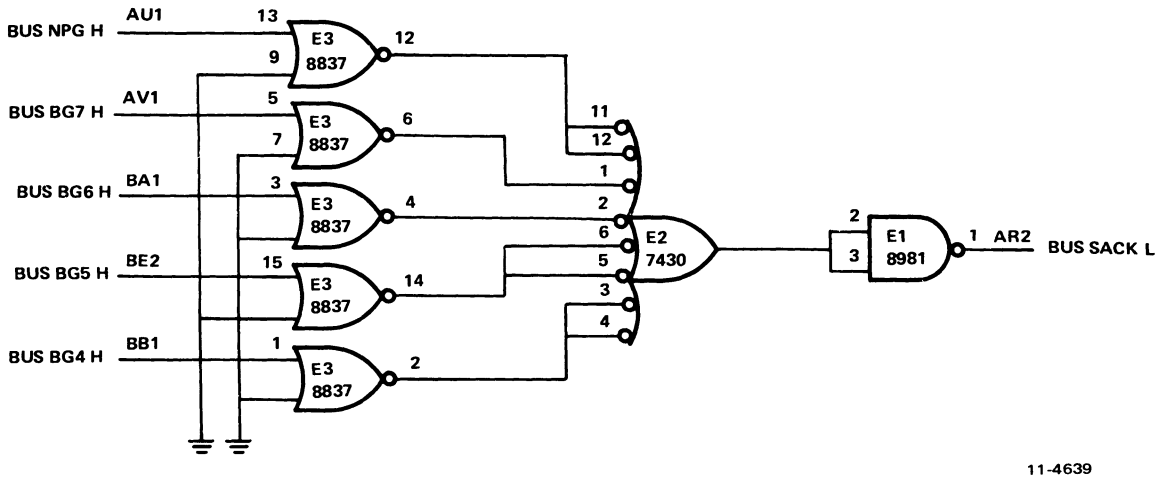


Figure 3-3 M9302 Sack Turnaround Logic

3.2.1 HALT/CONT Switch

This paragraph describes the logic associated with the HALT/CONT switch located on the operator's console (Figure 3-4).

The HALT/CONT switch allows the operator to halt the processor and keep it in the halted state as described in Paragraph 3.1.1. As shown in Figure 3-4, when the HALT/CONT switch is placed in the HALT position, the HALT RQST flip-flop is direct cleared. This position enables one input of the open-collector NAND gate that drives the HALT REQUEST L line.

The other input of the NAND gate is enabled if both BUS DC LO L and BUS INIT L are unasserted. HALT RQST L is transmitted to the processor and causes the processor to return HALT GRANT H to the console (Paragraph 3.1.1). HALT GRANT H direct sets the SACK flip-flop, thereby causing the operator's console to assert BUS SACK L. The processor is now halted and the operator's console has control of the Unibus. The processor will remain halted as long as BUS SACK L is asserted by the console. The SACK flip-flop can be cleared (and BUS SACK L dropped) by any of the following actions:

1. Bus INITialize
2. Pressing and releasing the BOOT/INIT switch
3. Moving the HALT/CONT switch to the CONT position.

When the HALT/CONT switch is moved to the CONT position, the HALT RQST flip-flop is direct set and HALT RQST L is dropped. The transition of the HALT RQST flip-flop output from clear to set causes the SACK flip-flop to be clocked. Since the data input is low, the SACK flip-flop clears on the low-to-high clock transition. When the SACK flip-flop is cleared, the RUN indicator turns on. The RUN indicator reflects the state of the SACK flip-flop. When the SACK flip-flop is set, the RUN indicator is off.

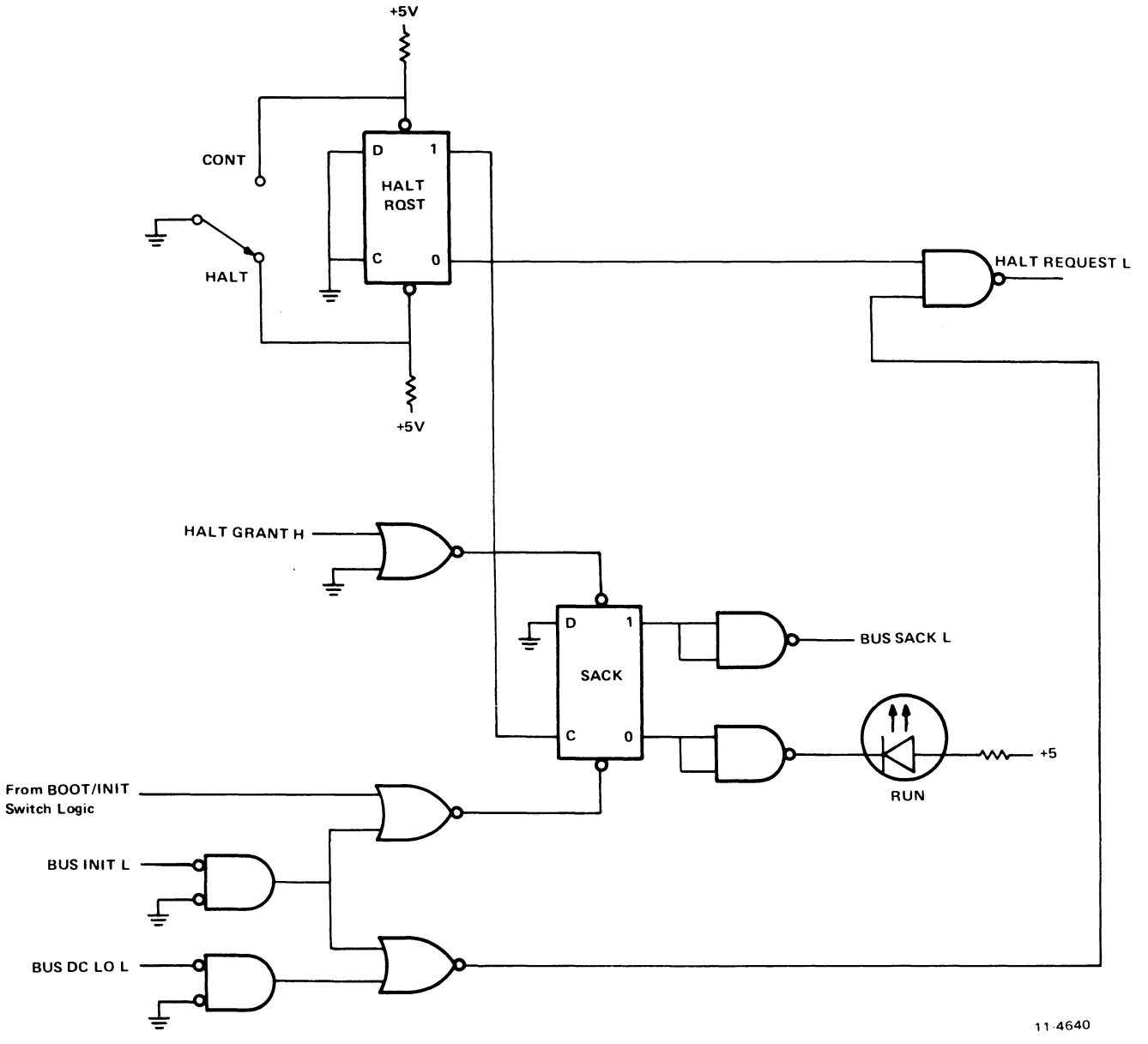


Figure 3-4 HALT/CONT Switch Logic

3.2.2 BOOT/INIT Switch

This paragraph provides a description of the logic associated with the BOOT/INIT switch located on the operator's console (Figure 3-5).

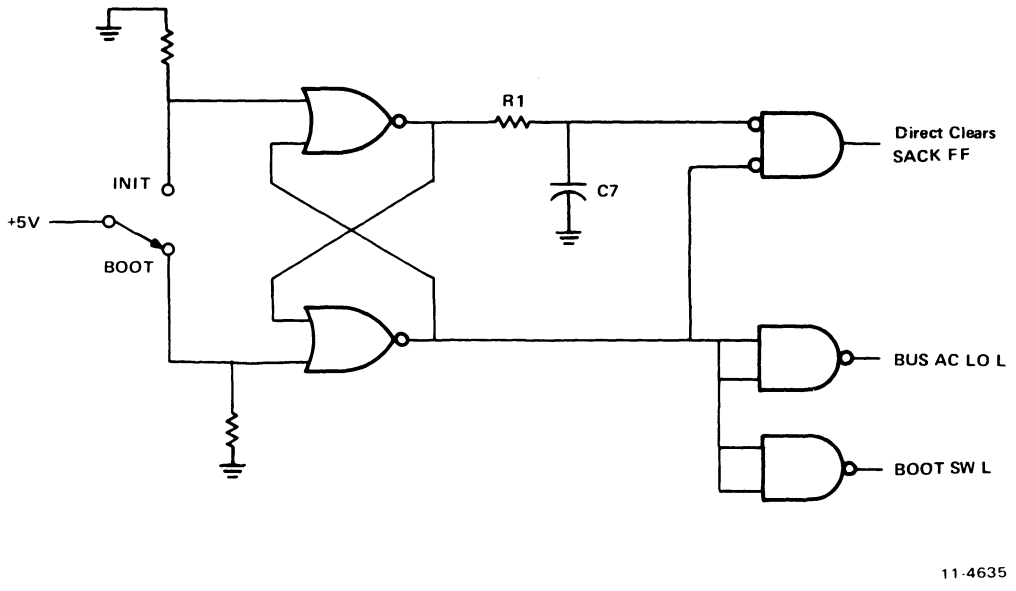


Figure 3-5 BOOT/INIT Switch Logic

The BOOT/INIT switch allows the operator to activate the M9301 bootstrap/terminator and the processor (via a simulated power fail) as described in Paragraph 3.1.2. The M9301 is activated by the signal BOOT SW L, generated by the operator's console. A power fail is simulated when the operator's console asserts BUS AC LO L on the Unibus. This boot sequence also requires that the SACK flip-flop be cleared. BOOT/INIT is a spring-action momentary switch that is normally in the BOOT position. Pressing the switch to the INIT position causes the two NAND gates to assert the signals BUS AC LO L and BOOT SW L (Figure 3-5). The INIT position also causes the capacitor (C7) to be discharged. When the switch is released to the BOOT position, BUS AC LO L and BOOT SW L are dropped, thereby allowing the processor to start a power-up sequence. Since the capacitor (C7) charges through a resistor (R1), a momentary low is maintained across the capacitor. This momentary low enables the signal that will direct clear the SACK flip-flop.

3.2.3 DC Power Switch

The dc power switch is a 3-position (DC OFF, DC ON, STNDBY) rotary switch that is always driving one of three signals to ground. These signals, when not grounded by the switch, are normally pulled high by the H777 power supply (Figure 3-6). When this switch is used with the H765 power supply, only the DC ON position is operational. The function of each position is described in Paragraph 2.1.1.

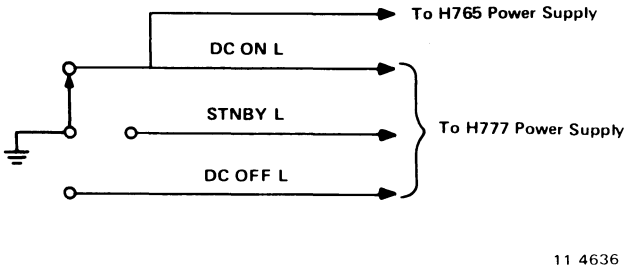


Figure 3-6 DC Power Switch

3.2.4 Indicators

The operator's console provides three indicators that monitor system status. The RUN indicator is discussed in Paragraph 3.2.1. The function of each of the console indicators is described in Paragraph 2.1.2.

The DC ON indicator is a light-emitting diode (LED) with a series current-limiting resistor connected between +5 Vdc and ground (Figure 3-7).

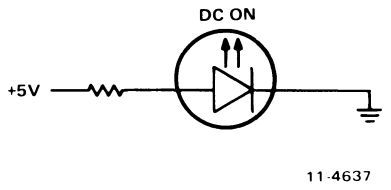


Figure 3-7 DC ON Indicator

The BATT (battery monitor) indicator is a LED driven by the +5 Vdc regulator board in the battery backup portion of the power supply (Figure 3-8). This indicator is not functional in a system without battery backup.

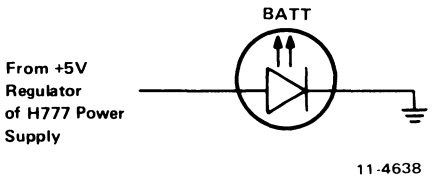


Figure 3-8 BATT Indicator

3.3 M9301 BOOTSTRAP/ROM FIRMWARE

The M9301 bootstrap/terminator contains a 512-word ROM (Read Only Memory). The memory is composed of four 512 × 4 bit tri-state ROMs organized in a 512 × 16 bit configuration. All four units share the same address lines and produce 16-bit PDP-11 instructions to be executed by the processor. The three versions of the M9301 (M9301-YA, M9301-YB, and M9301-YF) that are used in the PDP-11/04 system contain basic CPU and memory Go/No-Go diagnostics along with specific sets of bootstrap programs. The following list gives the function and order of each diagnostic test in the ROMs.

Test 1	All single operand instructions
Test 2	All double operand instructions
Test 3	Jump tests (modes 1, 2, and 3)
Test 4	Single operand, non-modifying, byte test
Test 5	Double operand, non-modifying test (source modes 1 and 4, destination modes 2 and 4)

Register Display Routine and Console Emulator

Test 6	Double operand, modifying, byte test
Test 7	JSR test
Test 8	Memory test

Bootstrap programs

3.3.1 Basic CPU Diagnostics

The following is a description of Tests 1–5.

Test 1 – Single Operand Test

This test executes all single operand instructions using destination mode 0. The basic objective is to verify that all single operand instructions function properly. It also provides a cursory check on the operation of each instruction, while ensuring that the CPU decodes each instruction in the correct manner.

Test 1 brings the Test Destination register through its three possible states: zero, negative, and positive. Each instruction operates on the register contents in one of four ways:

1. Data will be changed via a direct operation (i.e., increment, clear, decrement, etc.).
2. Data will be changed via an indirect operation (i.e., arithmetic shifts, add carry, and subtract carry).
3. Data will be unchanged, but will be operated upon via a direct operation (i.e., clear a register already containing zeroes).
4. Data will be unchanged via a non-modifying instruction (TST).

Note that when operating upon data in an indirect manner, the data is modified by the state of the appropriate condition code. Arithmetic shift will move the C bit into or out of the destination. This operation, when performed correctly, implies that the C bit was set correctly by the previous instruction.

There are no checks on the data integrity prior to the end of the test. However, a check is made on the result. A correct result implies that all instructions manipulated (or did not manipulate) the data in the correct way. *If the data is incorrect, the program will fall into a branch-self.*

Test 2 - Double Operand, All Source Modes, Destination Mode 0
This test verifies all double operand general and logical instructions - each in one of the seven modes (excludes mode 0). Thus, two operations are checked; the correct decoding of each double operand instruction, and the correct operation of each addressing mode for the source operand.

Each instruction in the test must operate correctly in order for the next instruction to operate. This interdependence is carried through to the last instruction (bit test) where, only through correct execution of all previous instructions, a data field is examined for a specific bit configuration. Thus, each instruction prior to the last serves to set up the pointer to test data.

Two checks on instruction operation are made in Test 2. One check, a branch-on condition, is made following the compare instruction, while the second is made as the last instruction in the test sequence.

Since the Go/No-Go test resides in a ROM memory, all data manipulation (modification) must be performed in destination mode 0 (register contains data). The data addressing constants used by Test 2 are contained in a literal pool within the ROM.

It is important to note that two different types of operations must execute correctly in order for this test to operate:

1. Those instructions that participate in computing the final address of the data mask for the final bit test instruction.

2. Those instructions that manipulate the test data within the register to generate the expected bit pattern.

Detection of an error within this test results in a branch-self.

Test 3 - Jump Test Modes 1, 2, and 3
The purpose of this test is to ensure correct operation of the Jump instruction. This test is constructed such that only a Jump to the expected instruction will provide the correct pointer for the next instruction.

There are two possible failure modes that can occur in this test:

1. The Jump addressing circuitry will malfunction causing a transfer of execution to an illogical instruction sequence or nonexistent memory.

2. The Jump addressing circuitry will malfunction in such a way as to cause the CPU to loop.

The latter case is a logical error indicator. The former, however, may manifest itself as an after-the-fact error. For example, if the Jump causes control to be given to other routines within the M9301, the interdependent instruction sequences would probably eventually cause a failure. In any case, the failing of the Jump instruction will eventually cause an out-of-sequence or illogical event to occur. This is a meaningful indicator of a malfunctioning CPU.

Test 4 - Single Operand, Non-Modifying, Byte Test
This test focuses on the one unique single operand instruction, the TST.TST, which is a special case in the CPU execution flow since it is a non-modifying operation. Test 4 also tests the byte operation of this instruction. The TSTB instruction will be executed in mode 1 (register deferred) and mode 2 (register deferred, auto-increment).

The TSTB is programmed to operate on data that has a negative value most significant byte and a zero (not negative) least significant byte.

In order for this test to operate properly, the TSTB on the LSB must first be able to access the even-addressed LSB, then set the proper condition codes. The TSTB is then reexecuted with the auto-increment facility. After the auto-increment, the addressing register should be pointing to the MSB of the test data. Another TSTB is executed on what should be the MSB. The N bit of the condition codes should be set by this operation.

Correct execution of the last TSTB implies that the auto-increment recognized that a byte operation was requested, thereby only incrementing the addressing by one, rather than two. *If the correct condition code was not set by the associated TSTB instruction, the program will fall into a branch-self.*

Test 5 - Double-Operand, Non-Modifying Test
There are two non-modifying double operand instructions - the compare (CMP) and bit test (BIT). These two instructions operate on test data in source modes 1 and 4, and destination modes 2 and 4.

The BIT and CMP instructions will operate on data consisting of all ones (177777). Two separate fields of ones are used in order to utilize the compare instructions, and to provide a field large enough to handle the auto-incrementing of the addressing register. Since the compare instruction (CMP) is executed on two fields containing the same data, the expected result is a true Z bit, indicating equality.

The BIT instruction will use a mask argument of all ones against another field of all ones. The expected result is a non-zero condition (Z bit cleared). *Failures will result in a branch-self.*

3.3.2 Register Display Routine
The register display routine prints the octal contents of Processor registers R0, R4, SP, and "OLD PC" on the console terminal. This sequence of numbers is followed by a prompt character ($) on the next line (Paragraph 2.1.3.2). The console emulator is entered before any memory-modifying diagnostics have been executed. Once the prompt character ($) has been received, the operator can execute the remainder of the diagnostics by typing a boot command for a non-existent device.

The console emulator is entered before any memory-modifying diagnostics have been executed.

3.3.3 Memory-Modifying Diagnostics
Prior to execution of device boots, the following memory-modifying diagnostics will be executed (if the diagnostics have been enabled on the M9301). The following is a description of Tests 6–8.

Test 6 - Double Operand, Modifying, Byte Test
The objective of this test is to verify that the double operand, modifying instructions will operate in the byte mode. Test 6 contains three subtests:

1. Test source mode 2, destination mode 1, odd and even bytes
2. Test source mode 3, destination mode 2
3. Test source mode 0, destination mode 3, even byte.

The move byte (MOVB), bit clear byte (BICB), and bit set byte (BISB) are used within Test 6 to verify the operation of the modifying, double operand functions.

Since modifying instructions are under test, memory must be used as a destination for the test data. Test 6 uses location 500_8 as a destination address. Later, in Tests 7 and 8, location 500_8 is used as the first available storage for the stack.

Note that, since Test 6 is a byte test, location 500_8 implies that both 500_8 and 501_8 are used for the byte test (even and odd, respectively). Thus, in the word of data 500_8, both odd and even bytes are caused to be all zeroes and all ones throughout the test. Each byte is modified independently of the other. *Errors detected in this test will result in a halt.*

Test 7 – JSR Test
The JSR is the first test in the Go/No-Go sequence that utilized the stack. The Jump subroutine command (JSR) is executed in modes 1 and 6. After the JSR is executed, the subroutine that was given control, will examine the stack to ensure that the correct data was deposited in the correct stack location (500_8).

The routine will also ensure that the Link Back register points to the correct address. *Errors detected in this test will result in a halt.*

Test 8 – Memory Test
Although this test is intended to test both core and MOS memories, the data patterns used are designed to exhibit the most taxing operations for MOS. Before the details of the test are described, it would be appropriate to discuss the assumptions placed upon the failure modes of the MOS technology.

The test is intended to check for two types of problems that may arise in the memory:

1. Solid element or sense amplifier failures
2. Addressing malfunctions external to the chip.

The simplest failure to detect is a solid read or write problem. If a cell fails to hold the appropriate data, it is expected that the Memory Test will easily detect this problem. In addition, the program attempts to saturate a chip in such a way as to cause marginal sense amplifier operation to manifest itself as a loss or pick-up of unexpected data. The 4K × 1 bit chip used in the memory consists of a 64 × 64 matrix of MOS elements. Each 64-bit section is tied to a common sense amplifier. The objective of the program is to saturate the section with, at first, all zeroes and one 1 bit. This 1-bit is then floated down through the section. At the end, the data is complemented, and the test repeated.

For external addressing failures it is assumed that if two or more locations are selected at the same time, and a write occurs, it is likely that both locations will assume the correct state. Thus, prior to writing any test data, the background data is checked to ensure that there was no crosstalk between any two locations. *Failures will result in a program halt as do failures in Tests 6 and 7.* After the halt, it is expected that the operator will press the BOOT switch causing R0 (expected data), R4 (received data), SP (failing address), and "OLD PC" (PC indicating memory failure) to be displayed. Refer to Paragraph 6.2.2 (Action 3).

NOTES

1. **The M9301-YF Memory Test performs both a dual-addressing and data check of all available memory on the system.**

2. **If the expected and received data are the same, it is highly probable that an intermittent failure has been detected (i.e., timing or margin problem). The reason the expected and received data can be identical is that the test program rereads the failing address after the initial non-compare is detected. Thus, a failure at CPU speed is detected, and indicated by the reading of the failing address on a single reference (not at speed) operation.**

3.3.4 Bootstrap Programs

This paragraph provides a list of the peripheral bootstraps supported by the M9301-YA, M9301-YB, and M9301-YF modules. Which bootstrap program is run depends on the switch settings of the M9301. On systems utilizing the M9301-YA or M9301-YF, the bootstraps can be entered directly without running the CPU diagnostics (Paragraph 4.3.2).

Device Code	Device Unibus Address	Peripheral Bootstraps Supported by M9301-YA
TT	777560	Terminal paper tape reader
DK	777404	RK11 moving-head disk cartridge
DT	777342	TC11 DECtape
MT	772522	TM11 magnetic tape drive. Tape must be 7- or 9-track, 800 bits/inch, odd parity, and dump mode.
DP	776714	RP11 moving-head disk pack for RP04/03
CT	777500	TA11 cassette
PR	777550	PC11 high-speed paper tape reader. Tape must be in a special bootstrap format (such as ABSLDR).
DX	777170	RX11 diskette

Device Code	Device Unibus Address	Peripheral Bootstraps Supported by M9301-YB
TT	777560	Terminal paper tape reader
DS	772040	RJS03/04 Massbus fixed-head disk
MM	772440	TJU16 Massbus tape drive. Tape must be 9-track, 800 bits/inch, and odd parity.
MC	776300	Mixed combination of Massbus devices. The actual device is determined by the specified unit number. The device can be a TJU16, RJP04, or RJS03/04.
DB	776700	RJP04/05/06 disk pack. Format 22, ECC inhibit.
DK	777404	RK11 moving head disk cartridge
DT	777342	TC11 DECtape
MT	772522	TM11 magnetic tape drive. Tape must be 7- or 9-track, 800 bits/inch, odd parity, and dump mode.
DP	776714	RP11 moving-head disk pack for RP02/03
CT	777500	TA11 cassette
PR	777550	PC11 high-speed paper tape reader. Tape must be in a special bootstrap format (such as ABSLDR).
DX	777170	RX11 diskette

Device Code	Device Unibus Address	Peripheral Bootstraps Supported by M9301-YF
TT	777560	DL11 control for terminal paper tape reader
DS	772040	RJS03/04 Massbus fixed-head disk
MM	772440	TJU16 Massbus tape drive
DB	776700	RJP04/05/06 Massbus disk pack
DK	777404	RK11 moving head disk cartridge control for RK03/05
DT	777342	TC11 control for TU56 DECtape
MT	772522	TM11 control for TU10 magtape
DP	776714	RP11 moving-head disk pack control for RP02/03
PR	777550	PC11 high-speed paper tape reader
DX	777170	RX11 control for RX01 diskette
DM	777440	RK611 control for RK06

CHAPTER 4
CONFIGURATION

4.1 GENERAL

The PDP-11/34 computer system is contained in either the BA11-L [13.3 cm (5-1/4 inch) chassis] or BA11-K [26.6 cm (10-1/2 inch) chassis] mounting box. The BA11 mounting box houses the backplane and power supply. For a detailed discussion of the BA11-L mounting box (and H777 power supply) or BA11-K mounting box (and H765 power supply), refer to the associated maintenance manual.

4.2 BACKPLANE

Three types of backplane can be used with the PDP-11/34: processor backplane, expander backplane, or special purpose backplane.

The DD11-PK is used as the basic PDP-11/34 processor backplane. The DD11-CK or DD11-DK can be used for expanding the system. Special purpose backplanes are wired to accommodate particular options and are supplied with systems containing such options.

4.2.1 Physical Description

The DD11-PK is a 9-slot backplane and the DD11-CK is a 4-slot backplane (Figure 4-1). Each backplane is prewired (via wire-wrap connections on pin side) to accommodate certain types of modules in each slot location. Details of signal connections and module placement are discussed in Paragraphs 4.2.2.2 and 4.2.3, respectively. Figure 4-1 shows the module connection side of each of the two backplanes.

Each system module plugs into one of the slots that is properly wired to provide all necessary power and signal connections for that particular module.

The DD11-DK (9-slot expander backplane) is the same as the DD11-PK processor backplane except for slot 1 and slot 2, which have special interconnections for the KD11-E and KD11-EA processor modules. Slots 1 and 2 of the DD11-DK are not dedicated to processor modules and therefore the DD11-DK can be used as an expander backplane.

4.2.2 Electrical Connections

This paragraph describes the power connections to the backplane and the signal connections of the backplane itself.

4.2.2.1 Power – Power is supplied to the backplane via a wire harness that connects to the dc distribution board of the power supply. The wires exit from the backplane to a set of Mate-N-Lok connectors that plug directly into the distribution board.

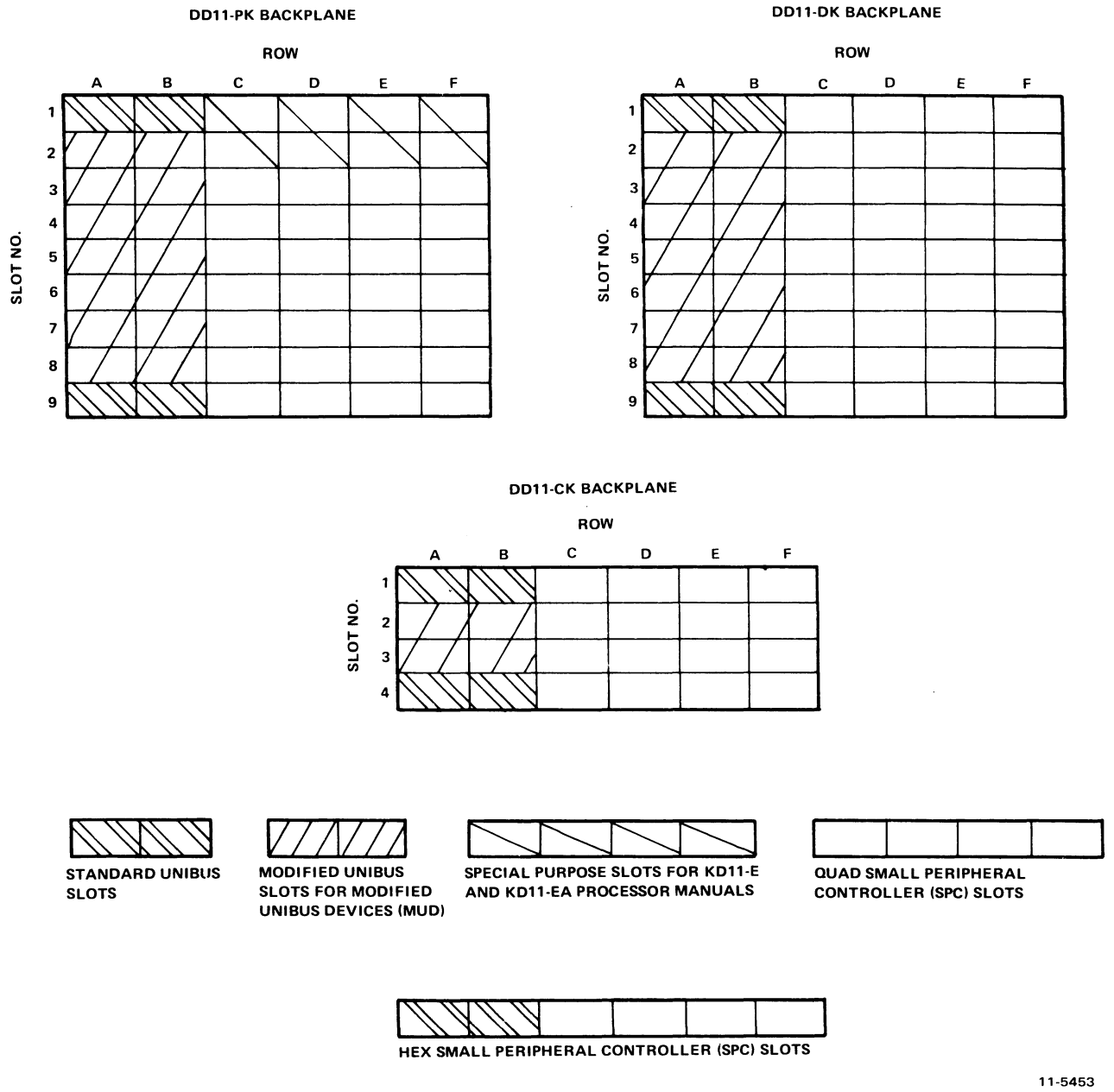


Figure 4-1 PDP-11/34 Backplanes

The power harness from the DD11-PK and DD11-DK backplanes contains two large connectors (15-pin Mate-N-Lok) and one small connector (6-pin Mate-N-Lok).

The DD11-CK backplane has only one 15-pin connector and one 6-pin connector. The connector pin locations are shown in Figure 4-2 and the signal assignments for each pin are shown in Table 4-1 (DD11-PK and DD11-DK) and Table 4-2 (DD11-CK).

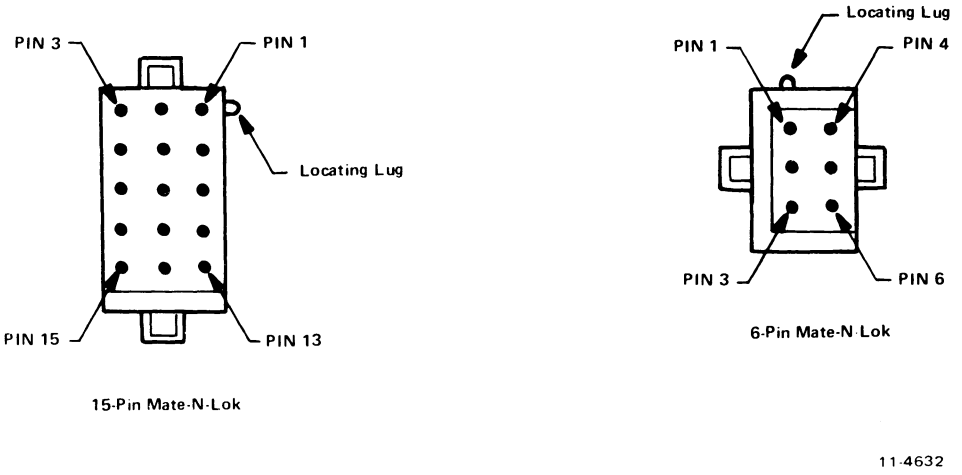


Figure 4-2 Mate-N-Lok Connector Pin Locations (Viewed from Wire Side)

Table 4-1 Power Connector Signal Assignments for DD11-PK and DD11-DK

15-Pin Mate-N-Lok Connector 1			
Pin	**Signal**	**Wire**	**Color**
1	+5 V	No. 14	Red
2	+15 V	No. 18	Gray
3	+20 V	No. 14	Orange
4	+5 V	No. 14	Red
5	Spare (not connected)	-	-
6	Spare (not connected)	-	-
7	Spare (not connected)	-	-
8	Ground	No. 14	Black
9	Ground	No. 14	Black
10	Spare (not connected)	-	-
11	Spare (not connected)	-	-
12	+5 Bat	No. 14	Red
13	Spare (not connected)	-	-
14	-5 V	No. 18	Brown
15	Spare (not connected)	-	-

Table 4-1 Power Connector Signal Assignments for DD11-PK and DD11-DK (Cont)

15-Pin Mate-N-Lok Connector 2

Pin	Signal	Wire	Color
1	+5 V	No. 14	Red
2	Spare (not connected	-	-
3	+20 V	No. 14	Orange
4	+5 V	No. 14	Red
5	Spare (not connected)	-	-
6	+15 Bat	No. 18	White
7	Spare (not connected)	-	-
8	Ground	No. 14	Black
9	Ground	No. 14	Black
10	Spare (not connected)	-	-
11	Spare (not connected)	-	-
12	Spare (not connected)	-	-
13	-15 V	No. 18	Blue
14	Spare (not connected)	-	-
15	-15 Bat	No. 18	Green

6-Pin Mate-N-Lok Connector

Pin	Signal	Wire	Color
1	LO GND	No. 14	Black
2	LTC (line clock)	No. 18	Brown
3	DC LO	No. 18	Violet
4	AC LO	No. 18	Yellow
5	Spare (not connected)	-	-
6	Spare (not connected)	-	-

Table 4-2 Power Connector Signal Assignments for DD11-CK

15-Pin Mate-N-Lok Connector

Pin	Signal	Wire	Color
1	+5 V	No. 14	Red
2	+15 V	No. 18	Gray
3	+20 V	No. 18	Orange
4	+5 V	No. 14	Red
5	Spare (not connected)	–	–
6	+15 Bat	No. 18	Green
7	Ground	No. 14	Black
8	Ground	No. 14	Black
9	Spare (not connected)	–	–
10	Spare (not connected)	–	–
11	Spare (not connected)	–	–
12	+5 Bat	No. 14	Red
13	-15 V	No. 18	Blue
14	- 5 V	No. 18	Brown
15	-15 Bat	No. 18	White

6-Pin Mate-N-Lok

Pin	Signal	Wire	Color
1	LO GND	No. 14	Black
2	LTC (line clock)	No. 18	Brown
3	DC LO	No. 18	Violet
4	AC LO	No. 18	Yellow
5	Spare (not connected)	–	–
6	Spare (not connected)	–	–

4.2.2.2 Backplane Signal Connections – In the following discussion, particular areas of the backplane will be referred to according to slot number (1–9) and section (A–F). Refer to Figure 4-1.

Signal connections between the backplane and operator's console are made via a single cable which terminates in a 10-pin 3M connector and plugs into connector J1 on the operator's console. Figure 4-3 shows the 3M connector pin locations and Table 4-3 lists the signal designation of each pin.

NOTE
The 3M connector is installed only if the operator's console is present.

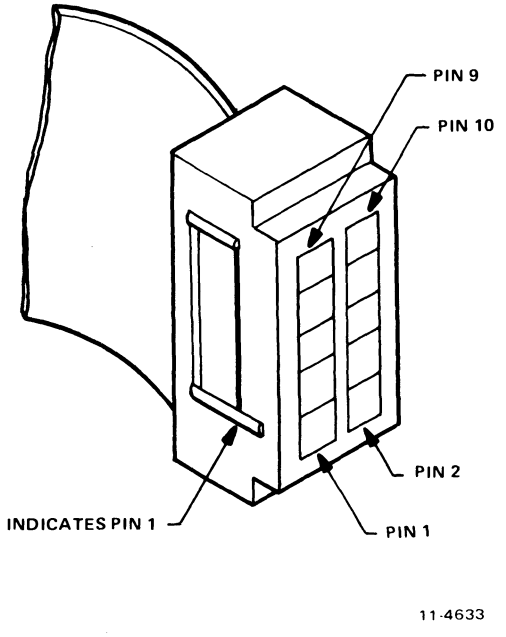


Figure 4-3 3M Connector Pin Locations
(Viewed from Pin Side)

Table 4-3 10-Pin 3M Connector Signal Designations

Pin	Signal
1	Ground
2	DC LO
3	Ground
4	AC LO
5	Ground
6	HALT REQUEST
7	HALT GRANT
8	SACK
9	Ground
10	INIT

Standard Unibus Slots – Slot 1 (sections A and B) of the DD11-PK, DD11-CK, and DD11-DK is the Unibus IN slot. Slots 1 and 2 of the DD11-PK backplane are dedicated to the processor modules. However, slot 1 (sections A and B) of the expander backplane (DD11-CK and DD11-DK) can accept any dual module that can plug into standard Unibus slots (i.e., BC11-A Unibus cable or M9202 Unibus jumper cable). Slot 9 (sections A and B) is the Unibus OUT slot of the DD11-PK and DD11-DK backplanes and slot 4 (sections A and B) is the Unibus OUT slot of the DD11-CK backplane. These sections must contain either a Unibus terminator (M9302) or a Unibus output cable (BC11-A or M9202). Figure 4-4 shows the pin designations of the standard and modified Unibus connectors.

Modified Unibus Device (MUD) Slots – Slots 2 through 8 (sections A and B) are the modified Unibus of the DD11-PK and DD11-DK backplanes. Slots 2 and 3 (sections A and B) are the modified Unibus of the DD11-CK backplane.

The modified Unibus differs from the standard Unibus in that certain pins have been redesignated (Figure 4-4). Some ground connections, BUS GRANT signals, and the NPG signal have been removed from the standard Unibus and have been redesignated with core memory voltage pins, battery backup voltage pins for MOS memory, parity signal pins, several reserved pins, and test point pins.

Small Peripheral Controller (SPC) Slots – The sections that accommodate small peripheral controller modules are slots 3 through 9 (sections C–F) of the DD11-PK backplane, slots 1 through 4 (sections C–F) of the DD11-CK backplane, and slots 1 through 9 (sections C–F) of the DD11-DK backplane. These sections provide the signal connections required by hex-height or quad-height modules (SPC modules) containing control logic for peripheral devices (i.e., serial line controller, programmer's console interface). Figure 4-5 shows the pin designations for the SPC connectors.

Non-Processor Grant (NPG) Line – The NPG line is the Unibus grant line for devices that perform data transfers without processor intervention. The NPG line grant continuity is provided by wire-wrap jumpers on the backplane. When an NPG module is placed in a slot, the corresponding jumper wire from pin CA1 to pin CB1 of that slot must be removed. The routing of the NPG signal through the backplane is shown in Figure 4-6. Grant priority decreases from slot 1 to slot 9 (i.e., slot 1 has highest priority and slot 9 lowest).

NOTE
If an NPG module is removed from a slot, the jumper wire from CA1 to CB1 must be reconnected.

Standard Unibus Pin Designations

Side / Pin	Column A 1	Column A 2	Column B 1	Column B 2
A	INIT L	+5V	BG6 H	+5V
B	INTR L	GND	BG5 H	GND
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	GND	BR4 L
E	D04 L	D03 L	GND	BG4 H
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	GND	PB L	A11 L	A10 L
P	GND	BBSY L	A13 L	A12 L
R	GND	SACK L	A15 L	A14 L
S	GND	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	NPG H	BR6 L	SSYN L	C0 L
V	BG7 SO	GND	MSYN L	GND

Modified Unibus Pin Designations

Side / Pin	Column A 1	Column A 2	Column B 1	Column B 2
A	INIT L	+5V	RESV PIN	+5V
B	INTR L	TP	RESV PIN	TP
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	+5 BAT	BR4 L
E	D04 L	D03 L	INT SSYN	PAR DET
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	PAR P1	PB L	A11 L	A10 L
P	PAR P0	BBSY L	A13 L	A12 L
R	+15 BAT	SACK L	A15 L	A14 L
S	-15 BAT	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	+20 (CORE)	BR6 L	SSYN L	C0 L
V	+20 (CORE)	+20 (CORE)	MSYN L	-5 (CORE)

11-4631

NOTE: indicates a redesignated pin.

Figure 4-4 Standard and Modified Unibus Pin Designations

	Column C		Column D		Column E		Column F	
Side / Pin	1	2	1	2	1	2	1	2
A	NPG (IN)	+5V	TP	+5V	GND A	+5V	ABG OUT	+5V
B	NPG (OUT)	-15V	TP	-15V	ASSYN IN H	-15V	ABG IN	-15V
C	PA L	GND	A SEL 6	GND	A12 L	GND	SSYN L	GND
D	LTC	D15 L	A OUT LOW	BR7 L	A17 L	A15 L	BBSY L	FO1 N1
E	TP	D14 L	A SEL 4	BR6 L	MSYN L	A16 L	FO1 V2	D02 L
F	TP	D13 L	A SEL 0	BR5 L	A02 L	C1 L	D05 L	D06 L
H	D11 L	D12 L	A IN	BR4 L	A01 L	A00 L	D07 L	A INT ENB B
J	A INT B	D10 L	A SEL 2	A BR OUT	SSYN L	C0 L	NPR L	GND A
K	TP	D09 L	A OUT	BG7 SO	A14 L	A13 L	D08 L	A INT B
L	A INT ENBB	D08 L	INIT L	BG7 OUT	A11 L	TP	D03 L	FO1 L2
M	TP	D07 L	AINT ENBA	BG6 SO	AIN	AOUT HIGH	INTR L	FO1 M2
N	DC LO	D04 L	A INT A	BG6 OUT	A OUT LOW	A08 L	FO1 N1	D04 L
P	HALT REQ	D05 L	TP	BG5 S0	A10 L	A07 L	ABR OUT	FO1 P2
R	HALT GRT	D01 L	TP	BG5 OUT	A09 L	ASEL 4	FO1 L2	FO1 N1
S	PB L	D00 L	TP	BG4 S0	ASEL 6	ASEL 0	FO1 M2	FO1 P2
T	GND	D03 L	GND	BG4 OUT	GND	ASEL 2	GND	SACK L
U	+15/+8	D02 L	TP	ABG IN	A06 L	A04 L	A INT A	ABR OUT
V	AC LO	D06 L	ASSYN IN H	ABG OUT	A05 L	A03 L	A INT ENB A	FO1 FO1

11-4630

Figure 4-5 SPC Pin Designations

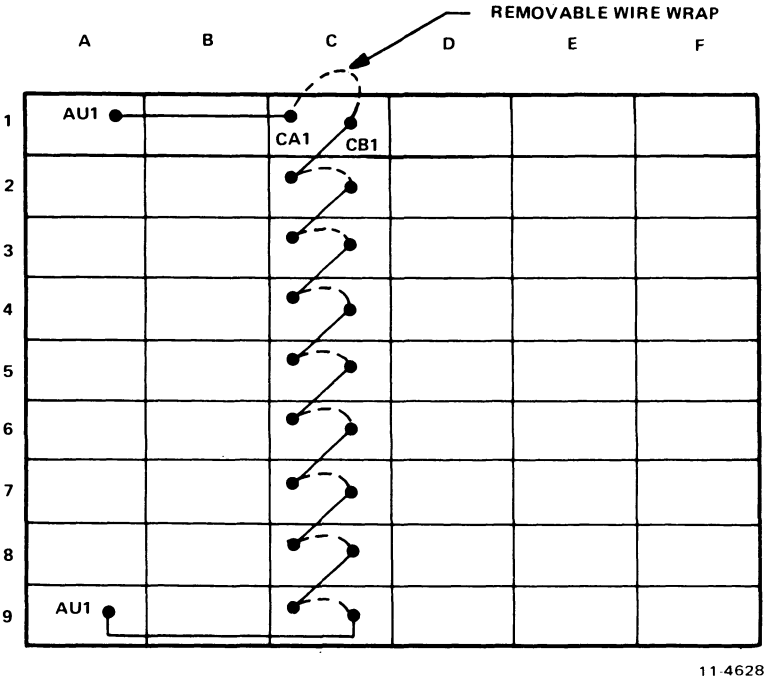


Figure 4-6 NPG Signal Path

Bus Grant (BG) Lines - The bus grant lines (BG4:BG7) for devices requiring processor intervention during data transfers are routed through each small peripheral controller section in connector D. Each of the four GRANT signals is routed on a separate line. Figure 4-7 shows the routing of one of the grant lines. The other three lines follow a similar path. Grant priority for each level decreases from slot 1 to slot 9.

NOTE

A bus grant jumper card (G727) must be placed in connector D of any unoccupied SPC section. If an SPC section is left open, bus grant continuity will be lost and the system will hang.

4.2.3 Module Placement

The PDP-11/34 backplanes are wired to accommodate particular types of modules in each section. Figure 4-8 illustrates which modules can be placed in each backplane slot.

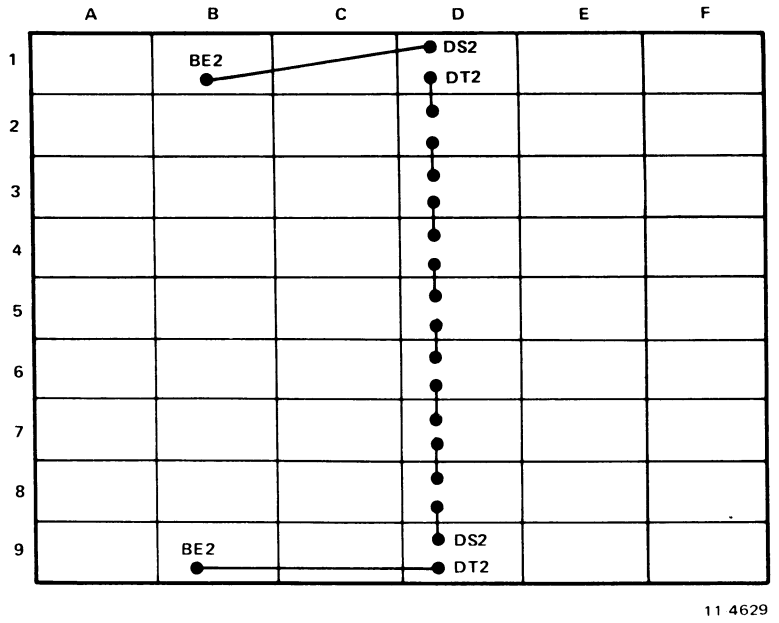
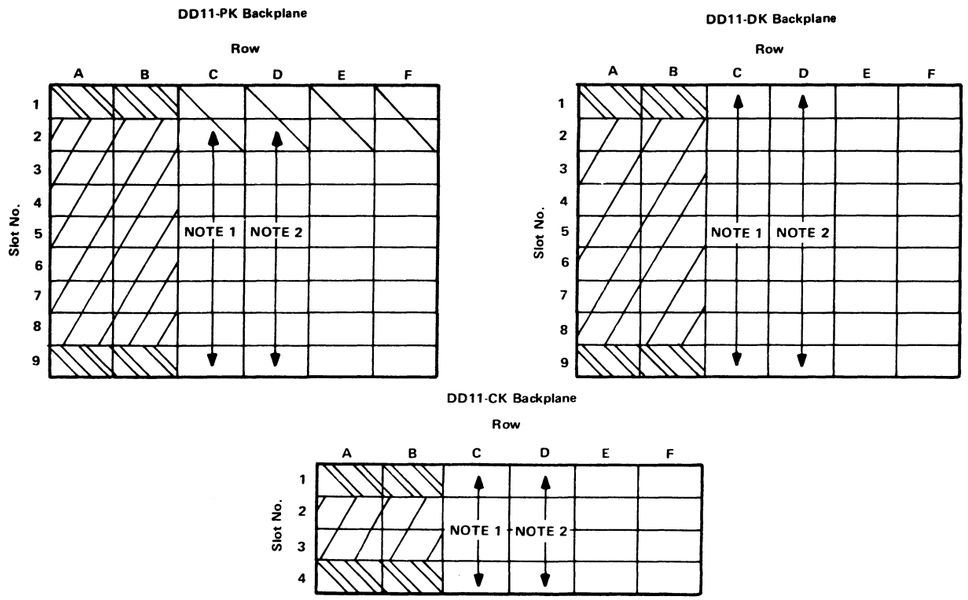


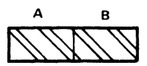
Figure 4-7 BG Signal Path (BG4 Line)



NOTES:

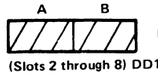
1. Remove CA1 to CB1 wire-wrap jumper from the appropriate slot to install an NPR option in that SPC slot.
2. A G727 card is required in any unused SPC slot to provide bus grant continuity.
3. Grant direction is slot 1 to slot 9 (or slot 4).
4. Use M9202 to interconnect system units instead of M920. M9202 is a 2-ft. Unibus jumper cable used to distribute Unibus loading.
5. The M9302 sack/terminator must never be installed in any slot other than slot 9 (sections A and B) in the DD11-PK and slot 4 (sections A and B) in the DD11-CK.

CAUTION
Power supply voltages will be shorted out if this terminator is mounted in the modified Unibus slots. Also, Unibus cables (i.e., BC11A) must never be plugged into a modified Unibus slot.



(Slots 2 through 8) DD11-PK
or
(Slots 1 and 4) DD11-CK

– Standard Unibus – ACCOMMODATES DUAL-HEIGHT MODULES WHICH ARE STANDARD UNIBUS COMPATIBLE:
EXAMPLE: M9202 (NOTE 4), BC11A CABLE, M9302 SACK/TERM (NOTE 5)

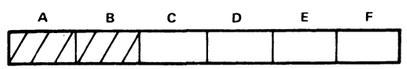


(Slots 2 through 8) DD11-PK
or
(Slots 2 and 3) DD11-CK

– Modified Unibus – ACCOMMODATES DUAL-HEIGHT MODULES WHICH ARE MODIFIED UNIBUS COMPATIBLE:
EXAMPLE: M9301 BOOT/TERM, M9306 TERM, M7850 PARITY CONTROLLER.

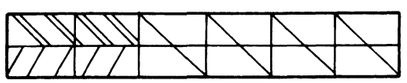
(Slots 3 through 9) DD11-PK
or
(Slots 1 through 4) DD11-CK

– ACCOMMODATES SMALL PERIPHERAL CONTROLLER (SPC).
EXAMPLE: PROGRAMMER'S CONSOLE INTERFACE (M7859), DL11-W (M7856)



(Slots 2 through 8) DD11-PK
or
(Slots 2 and 3) DD11-CK

– ACCOMMODATES HEX-HEIGHT MODULES WITH MODIFIED UNIBUS SIGNALS.
EXAMPLE: MS11 MOS MEMORY MODULES
MM11 CORE MEMORY MODULES



(Slots 1 and 2) DD11-PK Only

– SPECIAL PURPOSE CONNECTORS; SLOT 1 IS DEDICATED TO THE M7266 OR M8266 PROCESSOR MODULE.
SLOT 2 IS DEDICATED TO THE M7265 OR M8265 PROCESSOR MODULE.

11-5454

Figure 4-8 Module Placement

4.3 SWITCHES AND JUMPERS

This paragraph provides a definition of all switch settings and jumper locations associated with the PDP-11/34 system components.

4.3.1 KD11-E Processor

There are only two jumpers (W1 and W2) on each of the two processor modules. No switches are associated with the modules. Jumper W1 is OUT and W2 is IN on the M7266 module and both W1 and W2 are IN on the M7265 module.

4.3.2 KD11-EA Processor

The M8266 module has only one jumper (W1) which is IN. The M8265 module has two jumpers (W1 and W2) which are both IN.

4.3.3 M9301 Bootstrap/Terminator

The M9301 module has only one switch pack (S1) which contains 10 switches (S1 through S10). The five jumpers (W1, W2, W3, W4, and W5) should always be removed when the M9301 is installed in the PDP-11/34 system.

The function of each switch in the module switchpack is as follows:

S1 — Low ROM Enable switch. When this switch is placed in the OFF position, the lower 256 words of the M9301 ROM (Unibus addresses 765000 through 765776) are disabled. Placing S1 in the OFF position results in the following:

M9301-YA: The cassette boots, floppy boots, and diagnostics are unavailable and the paper tape boot will default to the lower 4K.

M9301-YB: Switch is not used.

M9301-YF: The paper tape boot and console emulator are unavailable.

S2 — Power-Up Reboot Enable switch. When this switch is in the ON position, the M9301 will be activated automatically when the system returns from a power fail. With this switch in the OFF position, the processor will perform a normal power-up routine through locations 24 and 26. If the BOOT/INIT switch on the console is pressed and released, the M9301 will be activated regardless of the position of switch S2.

NOTE

This switch should be in the ON position in systems using MOS memory without the battery backup option. Systems using MOS memory and containing the battery backup option or systems with core memory should have this switch in the OFF position. Refer to Paragraph 3.1.3.

S3–S10 — ROM Address Switches. The setting of switches S3 through S10 determines the ROM starting address that will be used as the new PC by the processor during a power-up routine (providing the M9301 has been enabled). The M9301-YA, YB, and YF allow the operator to select (via switches S3–S10) the function performed upon activation of the bootstrap/terminator.

Tables 4-4, 4-5, and 4-6 show the correspondence between switch settings and the function selected for the M9301-YA, M9301-YB, and M9301-YF respectively.

Table 4-4 M9301-YA ROM Starting Address Selection

Function	M9301-YA Switch Settings							
	S3	S4	S5	S6	S7	S8	S9	S10
CPU diagnostics → Console emulator	ON	ON	ON	ON	ON	ON	ON	ON
CPU diagnostics → Vector through location 24	ON	ON	ON	ON	ON	ON	ON	OFF
Console emulator (without diagnostics)	ON	ON	ON	ON	OFF	OFF	ON	ON
CPU diagnostics → Boot RK11	OFF	ON	ON	OFF	ON	ON	ON	ON
Boot RK11 (without diagnostics)	OFF	ON	ON	OFF	ON	ON	ON	OFF
CPU diagnostics → Boot RP11	OFF	ON	ON	OFF	OFF	ON	OFF	OFF
Boot RP11 (without diagnostics)	OFF	ON	ON	OFF	OFF	OFF	ON	ON
CPU diagnostics → Boot TC11	OFF	ON	OFF	ON	ON	ON	OFF	OFF
Boot TC11 (without diagnostics)	OFF	ON	OFF	ON	ON	OFF	ON	ON
CPU diagnostics → Boot TM11	OFF	ON	OFF	ON	OFF	ON	OFF	ON
Boot TM11 (without diagnostics)	OFF	ON	OFF	ON	OFF	ON	OFF	OFF
CPU diagnostics → Boot TA11	OFF	OFF	ON	ON	OFF	ON	OFF	ON
Boot TA11 (without diagnostics)	OFF	OFF	ON	ON	OFF	ON	OFF	OFF
CPU diagnostics → Boot RX11	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Boot RX11 (without diagnostics)	OFF	OFF	ON	OFF	ON	ON	ON	ON
CPU diagnostics → Boot DL11	OFF	OFF	ON	OFF	ON	OFF	ON	ON
Boot DL11 (without diagnostics)	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
CPU diagnostics → Boot PC11	OFF	OFF	ON	OFF	OFF	ON	ON	ON
Boot PC11 (without diagnostics)	OFF	OFF	ON	OFF	OFF	ON	ON	OFF

Note: ON = logic 0; OFF = logic 1

Table 4-5 M9301-YB ROM Starting Address Selection

Function	M9301-YB Switch Settings							
	S3	S4	S5	S6	S7	S8	S9	S10
CPU diagnostics → Console Emulator	ON	ON	ON	ON	ON	ON	ON	ON
CPU diagnostic → Vector through location 24	ON	ON	ON	ON	ON	ON	ON	OFF
Console emulator	ON	OFF	ON	ON	OFF	ON	OFF	OFF

Note: ON = logic 0, OFF = logic 1

Table 4-6 M9301-YF ROM Starting Address Selection

Function	M9301-YF Switch Settings							
	S3	S4	S5	S6	S7	S8	S9	S10
CPU diagnostics → Console emulator	ON	ON	ON	ON	ON	ON	ON	ON
Console emulator (without diagnostics)	ON	ON	ON	ON	ON	ON	ON	OFF
CPU diagnostics → Vector through location 24	OFF	OFF	ON	OFF	ON	ON	OFF	ON
Vector through location 24 (without diagnostics)	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
CPU diagnostics → Boot RP11	ON	ON	ON	OFF	ON	ON	ON	ON
Boot RP11 (without diagnostics)	ON	ON	ON	OFF	ON	ON	ON	OFF
CPU diagnostics → Boot RJP04/05/06	ON	OFF	ON	ON	OFF	ON	OFF	ON
Boot RJP04/05/06 (without diagnostics)	ON	OFF	ON	ON	OFF	ON	OFF	OFF
CPU diagnostics → Boot RJS03/04	OFF	ON	ON	OFF	ON	ON	ON	ON
Boot RJS03/04 (without diagnostics)	OFF	ON	ON	OFF	ON	ON	ON	OFF
CPU diagnostics → Boot RK11	ON	ON	OFF	OFF	ON	ON	OFF	ON
Boot RK11 (without diagnostics)	ON	ON	OFF	OFF	ON	ON	OFF	OFF
CPU diagnostics → Boot RK611	OFF	OFF	ON	OFF	OFF	ON	ON	OFF
Boot RK611 (without diagnostics)	OFF	OFF	ON	OFF	OFF	ON	OFF	ON

Note: ON = logic 0; OFF = logic 1.

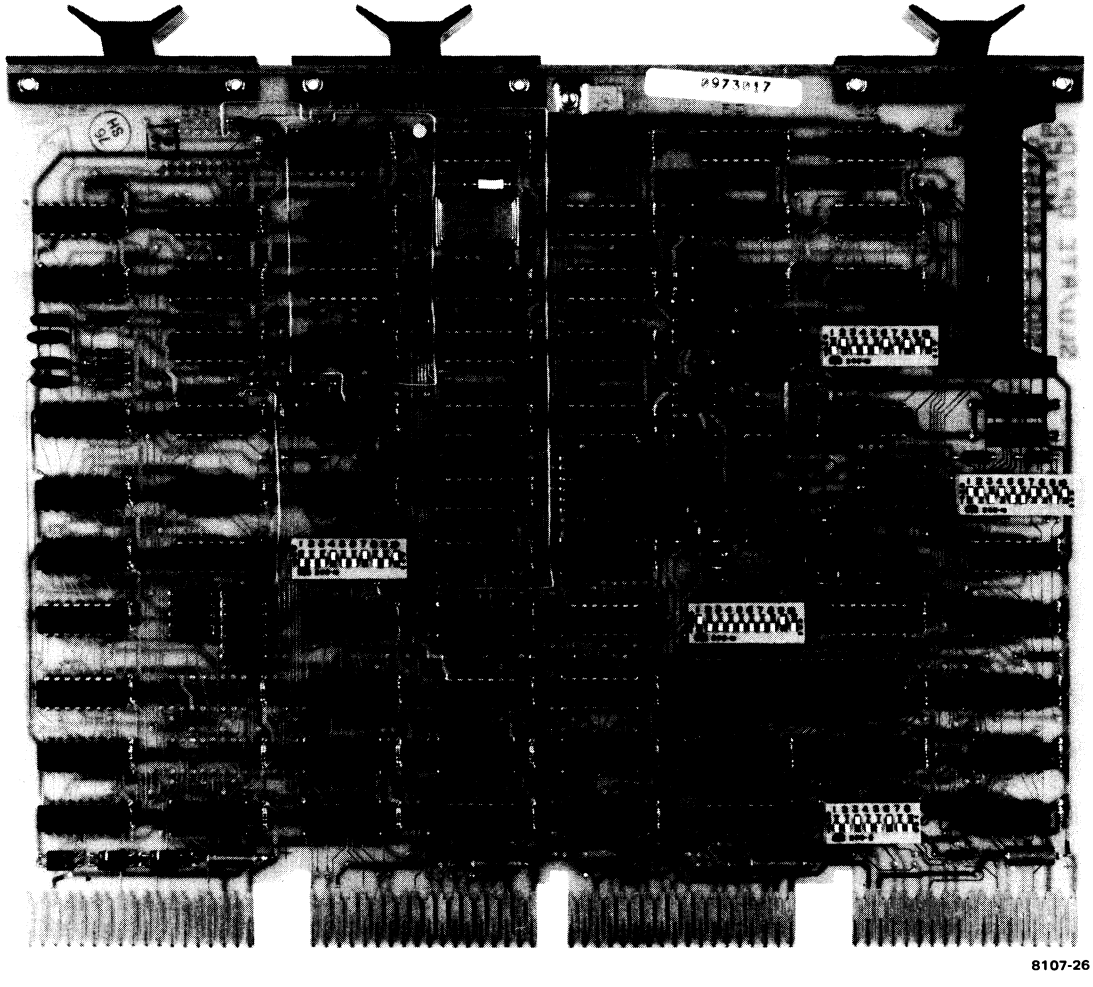
Table 4-6 M9301-YF ROM Starting Address Selection (Cont)

Function	M9301-YF Switch Settings							
	S3	S4	S5	S6	S7	S8	S9	S10
CPU diagnostics → Boot RX11	OFF	ON	OFF	OFF	ON	ON	OFF	ON
Boot RX11 (without diagnostics)	OFF	ON	OFF	OFF	ON	ON	OFF	OFF
CPU diagnostics → Boot TC11	ON	ON	OFF	OFF	OFF	OFF	OFF	ON
Boot TC11 (without diagnostics)	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
CPU diagnostics → Boot TM11	OFF	ON	ON	OFF	OFF	OFF	OFF	ON
Boot TM11 (without diagnostics)	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
CPU diagnostics → Boot TJU16	ON	ON	ON	OFF	ON	OFF	OFF	ON
Boot TJU16 (without diagnostics)	ON	ON	ON	OFF	ON	OFF	OFF	OFF
CPU diagnostics → Boot DL11	ON	OFF	OFF	OFF	OFF	ON	OFF	ON
Boot DL11 (without diagnostics)	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
CPU diagnostics → Boot PC11	OFF	OFF	OFF	ON	ON	ON	OFF	ON
Boot PC11 (without diagnostics)	OFF	OFF	OFF	ON	ON	ON	OFF	OFF

Note: ON = logic 0; OFF = logic 1.

4.3.4 DL11-W Serial Line Interface and Real-Time Clock

The DL11-W (M7856) contains 5 switch packs labeled S1 through S5. Each switch pack contains either 8 or 10 individual slide or toggle switches. The switch packs are labeled with each switch numbered 1 through 8 or 10. Each pack is also labeled showing the on and off positions (Figure 4-9).



8107-26

Figure 4-9 DL11-W (M7856) Switch Locations

Switch selections on the DL11-W allow the interface to directly replace a DL11-A, B, C, or D in most applications. Through proper setting of the switches, the user can select the desired baud rate, character size, stop-code length, parity, error detection, and 20-mA current loop modes. Table 4-7 lists the function of each of the switches. The switches are used separately or in conjunction with other switches to select the parameters discussed in the following paragraphs.

NOTE

In boxes other than BA11-L, there is not sufficient drive capability on the LTC L signal to drive multiple loads. Since each DL11-W constitutes a load (even if the line clock is disabled by the switch), multiple DL11-Ws in a box will overload the LTC L signal causing line clock failures. To alleviate the loading effect of the additional DL11-Ws, remove resistor R63 from all DL11-W modules except the one being used as a line clock. If multiple DL11-Ws are used on the same system, the line clock must be enabled (via switches) only on the DL11-W being used as a line clock.

In the following description, the switch will be indicated by its switch pack and switch number (e.g., S4-5 indicates switch pack 4, switch 5).

4.3.4.1 Device Address – The standard Unibus address assignment for the console device is 777560. However, the address of the DL11-W may be selected by the following switches:

Address Bit	Corresponding Switch
10	S5-3
09	S5-2
08	S5-1
07	S5-4
06	S5-5
05	S5-6
04	S5-8
03	S5-7

Note: Switch ON = logical 0; OFF = logical 1.

Figure 4-10 shows the bit values for the standard address and the correspondence between the address bits and switches.

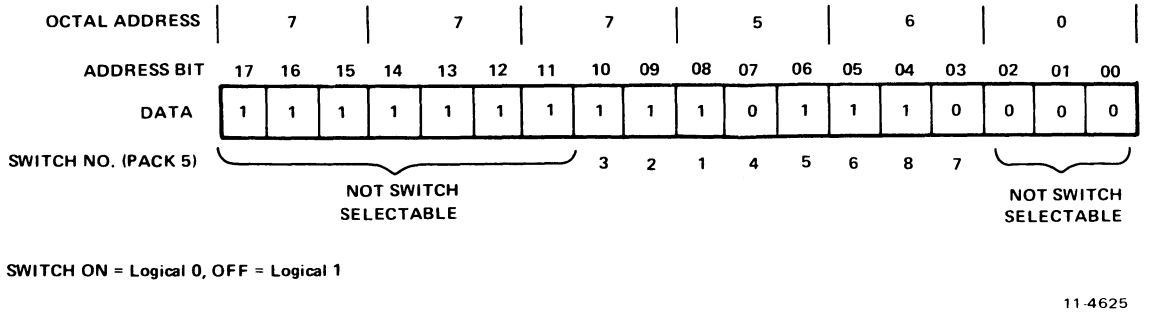


Figure 4-10 DL11-W Device Address Selection

The switches may be set so that the DL11-W responds to any address within the range of 774000 to 777777.

4.3.4.2 Vector Address - The standard vector address assignment for the console device is 060. The vector address may be selected by the following switches:

Vector Address Bit	Corresponding Switch
08	S2-8
07	S2-7
06	S2-5
05	S2-3
04	S2-6
03	S2-4

Note: Switch ON = logical 1; OFF = logical 0.

Figure 4-11 shows the bit values for the standard vector address and the correspondence between address bits and switches.

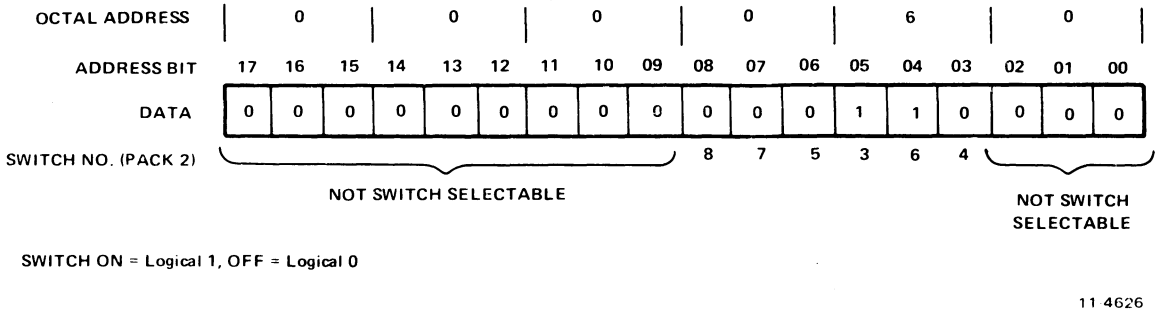


Figure 4-11 DL11-W Vector Address Selection

4.3.4.3 Baud Rate - Switches provided on the DL11-W allow the user to select independent receiver and transmitter baud rates. The following shows the correspondence between switch positions and baud rates.

	Switch Positions					
	Transmit			Receive		
Baud Rate	S4-10	S3-1	S3-4	S3-2	S3-3	S3-5
110	ON	ON	ON	OFF	OFF	OFF
150	OFF	ON	ON	ON	OFF	OFF
300	ON	OFF	OFF	OFF	ON	ON
600	ON	OFF	ON	OFF	ON	OFF
1200	ON	ON	OFF	OFF	OFF	ON
2400	OFF	OFF	OFF	ON	ON	ON
4800	OFF	OFF	ON	ON	ON	OFF
9600	OFF	ON	OFF	ON	OFF	ON

4.3.4.4 20-mA Current Loop Mode – The DL11-W provides two modes of operation (active and passive) for use with 20-mA current loop devices. In the active mode, the DL11-W is the source of the 20-mA current (all standard DEC terminals). In the passive mode, the external device must provide the required current (LA36, LA30, and VT52 options). The following shows the switch settings for the active and passive modes for the transmitter, receiver, and paper tape reader enable.

	Switch Positions				
Transmitter	**S1-1**	**S1-2**	**S1-3**	**S1-6**	**S1-7**
Active	ON	ON	OFF	OFF	ON
Passive	OFF	OFF	ON	ON	OFF
Receiver	**S3-6**	**S3-7**	**S3-8**	**S3-9**	**S3-10**
Active	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF
Paper Tape Reader Enable	**S1-4**	**S1-5**	**S1-8**	**S1-9**	**S1-10**
Active	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF

4.3.4.5 Data Format – The data format consists of a start bit, 5 to 8 data bits, a parity bit (or no parity bit), and 1, 1-1/2, or 2 stop bits. The following shows the switch selections for the desired format.

	Switch Positions	
No. of Data Bits/Character	**S4-4**	**S4-3**
5	ON	ON
6	ON	OFF
7	OFF	ON
8	OFF	OFF

No. of Stop Bits/Character	**S4-5**
1	ON
2	OFF (1.5 stop bits with 5 data bits)

Parity	**S4-6**
Enable	ON
Disable	OFF
	S4-2
Odd	ON
Even	OFF

4.3.4.6 DL11-W Compatibility Switches – The DL11-W can replace a DL11-A, B, C, or D in *most* applications if the following switches are set properly.

Function	Switch	Description
Break Bit	S4-1	The break bit is enabled if S4-1 is in the ON position. S4-1 should be OFF if replacing a DL11-A or DL11-B and ON if replacing a DL11-C or DL11-D.
Error Bits	S4-7	Error bit reporting is enabled if S4-7 is in the ON position. S4-7 should be OFF if replacing a DL11-A or DL11-B and ON if replacing a DL11-C or DL11-D.
Real-Time Clock	S5-9 and S5-10	The real-time clock is enabled if S5-9 is in the OFF position and S5-10 is in the ON position. To disable the real-time clock, S5-9 must be ON and S5-10 must be OFF. The real-time clock must be disabled if the DL11-W is not used as the console terminal control. If both S5-9 and S5-10 are ON, the DL11-W is used as a line clock only and the serial line unit section does not respond to any address. If the DL11-W is used as a line clock only, the address selection switches must be set for 77754X.

Table 4-7 lists each of the switch packs and the associated function of each switch.

Table 4-7 DL11-W Switch Functions

Switch Pack	Switch No.	Function
1	1 2 3	Transmitter (Active/Passive mode of 20-mA loop)
	4 5	Reader Enable (Active/Passive mode of 20-mA loop)
	6 7	Transmitter (Active/Passive mode of 20-mA loop)
	8 9 10	Reader Enable (Active–Passive mode of 20-mA loop)
2	1 2	Not Functional
	3 4 5 6 7 8	Vector Address

Table 4-7 DL11-W Switch Functions (Cont)

Switch Pack	Switch No.	Function
3	1	Transmitter baud rate
	2	Receiver baud rate
	3	
	4	Transmitter baud rate
	5	Receiver baud rate
	6	Receiver (Active/Passive mode of 20-mA loop)
	7	
	8	
	9	
	10	
4	1	Break enable
	2	Parity select (odd or even)
	3	No of Data bits
	4	
	5	No. of Stop bits
	6	Parity enable
	7	Error bit enable
	8	Not functional
	9	
	10	Transmitter baud select
5	1	Device Address
	2	
	3	
	4	
	5	
	6	
	7	
	8	
	9	Real-Time Clock Enable
	10	

4.3.5 MS11-EP, MS11-FP, and MS11-JP MOS Memory

The MS11 MOS memory module (M7847) has one switch pack containing eight individual switches. The switches are identified by etched letters A–J on the printed circuit board. Switches A through E are used to select the memory starting addresses and switches F through H are normally in the OFF position for PDP-11/34 systems (switch H is ON if MS11-JP memory is used). Table 4-8 shows the correspondence between the switch settings and the address banks assigned to the memory module. Jumpers on the module allow more than one 4K address bank to be assigned. For example, the MS11-JP (16K memory) would require all four address banks. When switch H is ON, bank D is enabled. The following lists the memories by size and indicates the jumpers installed (and setting of switch H) for normal use.

Memory Designation	Memory Size	Eyelet Pairs Connected by Jumpers			
		W3–W4	W1–W2	W5–W6	Switch H
MS11-EP	4K	IN	OUT	OUT	OFF
MS11-FP	8K	IN	IN	OUT	OFF
MS11-JP	16K	IN	IN	IN	ON

Table 4-8 Switch Settings for MS11 Address Assignments

Switch Selection A	B	C	D	E	Bank A	Bank B	Bank C	Bank D
OFF	OFF	OFF	ON	ON	0–4K	4–8K	8–12K	12–16K
OFF	OFF	ON	OFF	OFF	4–8K	8–12K	12–16K	16–20K
OFF	OFF	ON	OFF	ON	8–12K	12–16K	16–20K	20–24K
OFF	OFF	ON	ON	OFF	12–16K	16–20K	20–24K	24–28K
OFF	OFF	ON	ON	ON	16–20K	20–24K	24–28K	28–32K
OFF	ON	OFF	OFF	OFF	20–24K	24–28K	28–32K	32–36K
OFF	ON	OFF	OFF	ON	24–28K	28–32K	32–36K	36–40K
OFF	ON	OFF	ON	OFF	28–32K	32–36K	36–40K	40–44K
OFF	ON	OFF	ON	ON	32–36K	36–40K	40–44K	44–48K
OFF	ON	ON	OFF	OFF	36–40K	40–44K	44–48K	48–52K
OFF	ON	ON	OFF	ON	40–44K	44–48K	48–52K	52–56K
OFF	ON	ON	ON	OFF	44–48K	48–52K	52–56K	56–60K
OFF	ON	ON	ON	ON	48–52K	52–56K	56–60K	60–64K
ON	OFF	OFF	OFF	OFF	52–56K	56–60K	60–64K	64–68K
ON	OFF	OFF	OFF	ON	56–60K	60–64K	64–68K	68–72K
ON	OFF	OFF	ON	OFF	60–64K	64–68K	68–72K	72–76K
ON	OFF	OFF	ON	ON	64–68K	68–72K	72–76K	76–80K
ON	OFF	ON	OFF	OFF	68–72K	72–76K	76–80K	80–84K
ON	OFF	ON	OFF	ON	72–76K	76–80K	80–84K	84–88K
ON	OFF	ON	ON	OFF	76–80K	80–84K	84–88K	88–92K
ON	OFF	ON	ON	ON	80–84K	84–88K	88–92K	92–96K
ON	ON	OFF	OFF	OFF	84–88K	88–92K	92–96K	96–100K
ON	ON	OFF	OFF	ON	88–92K	92–96K	96–100K	100–104K
ON	ON	OFF	ON	OFF	92–96K	96–100K	100–104K	104–108K
ON	ON	OFF	ON	ON	96–100K	100–104K	104–108K	108–112K
ON	ON	ON	OFF	OFF	100–104K	104–108K	108–112K	112–116K
ON	ON	ON	OFF	ON	104–108K	108–112K	112–116K	116–120K
ON	ON	ON	ON	OFF	108–112K	112–116K	116–120K	120–124K
ON	ON	ON	ON	ON	112–116K	116–120K	120–124K	124–128K
OFF	OFF	OFF	ON	OFF	116–120K	120–124K	124–128K	0–4K
OFF	OFF	OFF	OFF	ON	120–124K	124–128K	0–4K	4–8K
OFF	OFF	OFF	OFF	OFF	124–128K	0–4K	4–8K	8–16K
					To enable bank A, jumper W3–W4 is IN.	To enable bank B, jumper W1–W2 is IN.	To enable bank C, jumper W5–W6 is IN.	To enable bank D, switch H is ON.

4.3.6 MM11-CP Core Memory

The MM11-CP core memory module has one switch pack (E39) which contains eight switches (SW1–SW8). These switches are used to select the Unibus addresses that the 8K memory will occupy. Table 4-9 lists the memory bank, Unibus address range, and corresponding switch positions.

Table 4-9 MM11-CP Memory Address Selection

Memory Bank	Unibus Address Range	Switch Settings			
		SW1, 2	SW3, 4	SW5, 6	SW7, 8
0K–8K	000000–037776	ON	ON	ON	ON
8K–16K	040000–077776	OFF	ON	ON	ON
16K–24K	100000–137776	ON	OFF	ON	ON
24K–32K	140000–177776	OFF	OFF	ON	ON
32K–40K	200000–237776	ON	ON	OFF	ON
40K–48K	240000–277776	OFF	ON	OFF	ON
48K–56K	300000–337776	ON	OFF	OFF	ON
56K–64K	340000–377776	OFF	OFF	OFF	ON
64K–72K	400000–437776	ON	ON	ON	OFF
72K–80K	440000–477776	OFF	ON	ON	OFF
80K–88K	500000–537776	ON	OFF	ON	OFF
88K–96K	540000–577776	OFF	OFF	ON	OFF
96K–104K	600000–637776	ON	ON	OFF	OFF
104K–112K	640000–677776	OFF	ON	OFF	OFF
112K–120K	700000–737776	ON	OFF	OFF	OFF
120K–128K	740000–777776	OFF	OFF	OFF	OFF

4.3.7 MM11-DP Core Memory

The MM11-DP core memory module contains four jumpers (W1, W2, W3, W4) that are installed (or removed) to select the Unibus addresses that the 16K memory will occupy. Table 4-10 lists the memory bank, Unibus range, and corresponding jumper assignment.

Table 4-10 MM11-DP Memory Address Selection

Memory Bank	Unibus Address Range	Jumper Assignment			
		W1	W2	W3	W4
0K–16K	000000–077776	OUT	OUT	OUT	IN
8K–24K	040000–137776	OUT	OUT	IN	OUT
16K–32K	100000–177776	OUT	OUT	IN	IN
24K–40K	140000–237776	OUT	IN	OUT	OUT
32K–48K	200000–277776	OUT	IN	OUT	IN
40K–56K	240000–337776	OUT	IN	IN	OUT
48K–64K	300000–377776	OUT	IN	IN	IN
56K–72K	340000–437776	IN	OUT	OUT	OUT
64K–80K	400000–477776	IN	OUT	OUT	IN
72K–88K	440000–537776	IN	OUT	IN	OUT
80K–96K	500000–577776	IN	OUT	IN	IN
88K–104K	540000–637776	IN	IN	OUT	OUT
96K–112K	600000–677776	IN	IN	OUT	IN
104K–120K	640000–737776	IN	IN	IN	OUT
112K–128K	700000–777776	IN	IN	IN	IN

4.3.8 M7850 Parity Controller

The M7850 Parity Control module contains four jumpers which are used to determine the Unibus address of the Control and Status register (CSR). The following shows the correspondence between the CSR address and jumper arrangement:

CSR Address	Jumper Arrangement			
	W4	W3	W2	W1
772100	IN	IN	IN	IN
772102	IN	IN	IN	OUT
772104	IN	IN	OUT	IN
772106	IN	IN	OUT	OUT
772110	IN	OUT	IN	IN
772112	IN	OUT	IN	OUT
772114	IN	OUT	OUT	IN
772116	IN	OUT	OUT	OUT
772120	OUT	IN	IN	IN
772122	OUT	IN	IN	OUT
772124	OUT	IN	OUT	IN
772126	OUT	IN	OUT	OUT
772130	OUT	OUT	IN	IN
772132	OUT	OUT	IN	OUT
772134	OUT	OUT	OUT	IN
772136	OUT	OUT	OUT	OUT

NOTE

There is no correlation between the CSR address of the M7850 and the memory block(s) it controls. Only one M7850 is required in each backplane containing parity memory.

CHAPTER 5
INSTALLATION

5.1 GENERAL
This chapter provides the information necessary for site preparation, unpacking, inspection, and first-time start-up of the basic PDP-11/34 system.

5.2 SITE CONSIDERATIONS
The computer room environment should have an air distribution system that provides cool, well-filtered, humidified air. The room air pressure should be kept higher than that of adjacent areas to prevent dust infiltration.

Computer area environment can have a substantial effect upon the overall reliability of the system. Temperature cycling and thermal gradients induce temporary or permanent microscopic changes in materials that can affect performance or endurance. High temperatures tend to increase the rate of deterioration for nearly every material. High absolute humidity (dew point) causes moisture absorption that can result in dimensional and handling changes in paper and plastic media (line printer paper, cards, paper tape, magnetic tape, etc.)

Low humidity allows static electricity to build up, while lack of air cleanliness results in dust that reduces tape life and leads to excessive head wear and early data errors in all moving magnetic storage media (drums and disks). This combination of static electricity and airborne dust is especially detrimental to magnetic tapes.

Vibration can also cause slow degradation of mechanical parts and, when severe, may cause errors on disks and drums.

Hardware errors can also be caused by electromagnetic interference (EMI). EMI sources that have been known to cause failures include: radar installation, lightning strikes, power transmission lines, vehicle ignition systems, broadcast transmitters, arc welders, etc.

5.2.1 Humidity and Temperature
PDP-11/34 systems are designed to operate in a temperature range of 5° C (41° F) to 50° C (122° F) at a relative humidity of 10 to 95 percent, without condensation. However, system configurations that use I/O devices such as magnetic tape units, card readers, disks, etc., require an operational temperature range from 15° C (60° F) to 27° C (80° F) at a relative humidity of 40 to 60 percent, without condensation. Nominal operating conditions for a system configuration are a temperature of 20° C (70° F) and a relative humidity of 45 percent.

5.2.2 Air-Conditioning
When used, computer room air-conditioning equipment should conform to the requirements of the *Standard for the Installation of Air-Conditioning and Ventilating Systems (Non-Residential)* N.F.P.A. No. 90A, as well as the requirements of the *Standard for Electronic Computer Systems*, N.F.P.A. No. 75.

5.2.3 Acoustical Damping
Some peripheral devices (such as line printers and magnetic tape transports) are quite noisy. In installations that use a group of high noise level devices, an acoustically damped ceiling will reduce the noise.

5.2.4 Lighting
If CRT peripheral devices are part of the system, the illumination surrounding these peripherals should be reduced to enable the operator to conveniently observe the display.

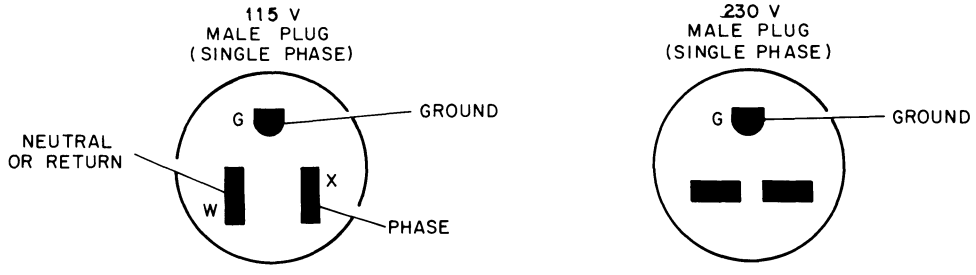
5.2.5 Special Mounting Conditions
If the system will be subjected to rolling, pitching, or vibration of the mounting surface (e.g., aboard ship), the cabinetry should be securely anchored to the installation floor by mounting bolts. Since such installations require modifications to the cabinets, DEC must be notified when the order is placed so that the necessary modifications can be made.

5.2.6 Static Electricity
Static electricity can be an annoyance to operating personnel and can (in extreme cases) affect the operational characteristics of the PDP-11/34 system and related peripheral equipment. If carpeting is installed on the computer floor, it should be of a type designed to minimize the effects of static electricity. Flooring consisting of metal panels, or flooring with metal edges, should be adequately grounded.

5.3 ELECTRICAL REQUIREMENTS
The PDP-11/34 system can be operated from a 115/230 Vac ± 10%, 47- to 63-Hz power source. The primary ac operational voltages should be within the defined tolerances. The primary power outlets at the installation site must be compatible with the PDP-11/34 primary power input connectors, or compatible with the primary power input connectors of the 861 Power Controller if the system is cabinet mounted. Refer to the related mounting box manual for details concerning power requirements.

Two types of connectors are used with the PDP-11/34, depending on whether the system is configured for 115 Vac or 230 Vac operation. Figure 5-1 shows the plug portion of each connector and a table provides specifications for both plugs and receptacles.

If the system is cabinet mounted, the 861 Power Controller is used. The power controller requires different connectors from those used with the BA11-L or BA11-K mounting box. The 861-C Power Controller is used for 115 Vac operation and the 861-B is used for 230 Vac operation. Figure 5-2 illustrates these connectors and the associated table provides connector specifications.



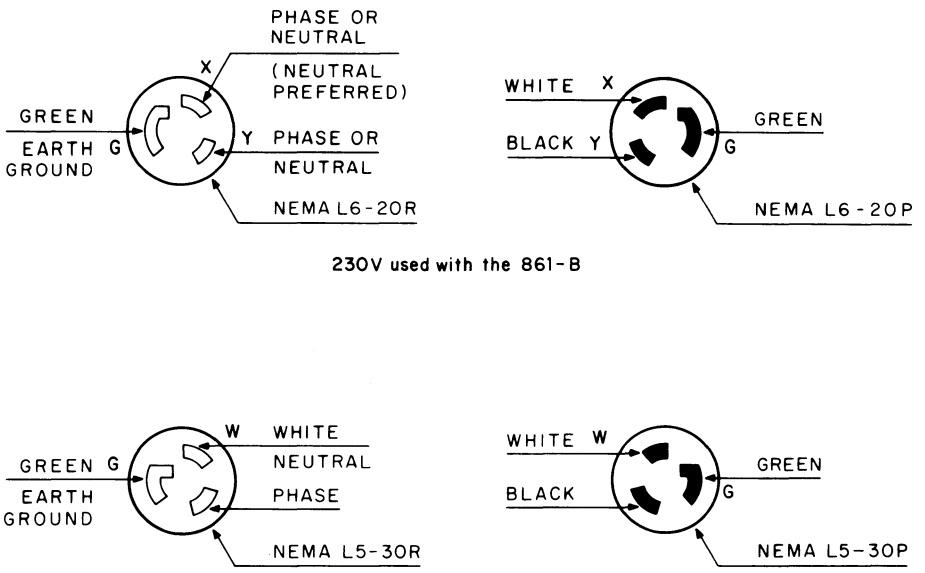
CONNECTOR SPECIFICATIONS

DESCRIPTION	NEMA* CONFIGURATION	POLES	WIRES	PLUG	RECEPTACLE
				DEC PART NO.	DEC PART NO.
115V, 15 AMP	5-15	2	3	90-08938	12-05351
230V, 15 AMP	6-15	2	3	90-08853	12-11204

*ADD P SUFFIX FOR PLUG
ADD R SUFFIX FOR RECEPTACLE

11-2572

Figure 5-1 Connector Specifications for BA11-L and BA11-K Boxes



CONNECTOR SPECIFICATIONS

MODEL NUMBER	POWER	RATING	PLUG NEMA CODE	RECEPTACLE (SUPPLIED BY CUSTOMER)	
				NEMA CODE	DEC PART NO.
861-C	115 V SINGLE PHASE	30 A	L5-30P	L5-30R	12-11191
861-B	230 V SINGLE PHASE	20 A	L6-20P	L6-20R	12-11194

Figure 5-2 Connector Specifications for 861-B and 861-C Power Controllers

5.3.1 System Grounding

The PDP-11/34 3-prong power connector, when inserted into a properly wired receptacle, should ground the computer chassis. It is unsafe to operate the computer unless the case is grounded because normal current leakage from the power supply flows to the metal parts of the chassis. If the integrity of the ground circuit is questionable, the user is advised to measure with a voltmeter the potential between the computer case and a known ground, or to notify the Field Service representative.

Computer systems are often sensitive to the interferance present on some ac power lines. If the computer is to be installed in an electrically noisy environment, it is necessary to provide primary power to the computer on a separate power line from lighting, air-conditioning, etc., so that computer operation is not affected by voltage surges of fluctuations.

Any questions regarding power requirements and installation wiring should be directed to the DIGITAL Sales representative or Field Service engineer.

5.3.2 Specifications Summary

Physical

Dimensions

13.3-cm (5-1/4-inch) chassis	13-1/2 cm h × 64 cm w × 48 cm l (5-1/4 in h × 25 in w × 19 in l)
26.3-cm (10-1/2-inch) chassis	26 cm h × 64 cm w × 48 cm l (10-1/2 in h × 25 in w × 19 in l)

Weight

13.3-cm (5-1/4-in) chassis	20 kg (45 lb)
26.3-cm (10-1/2-in) chassis	50 kg (110 lb)

Expansion Space

13.3-cm (5-1/4-in) chassis	7 slots
26.3-cm (10-1/2-in) chassis	7 slots plus space for 3 system units

Electrical

System Power	115/230 Vac ± 10%, 47–63 Hz
13.3-cm (5-1/4-in) chassis	350 W
26.3-cm (10-1/2-in) chassis	800 W

Logic Power

PDP-11/34	
BA11-L [13.3 cm (5-1/4 in) chassis]	25 A available for processor backplane
BA11-K [26.3 cm (10-1/2 in) chassis]	25 A available for processor backplane and 25 A available for expander backplanes
PDP-11/34A	
BA11-L [13.3 cm (5-1/4 in) chassis]	32 A available for processor backplane
BA11-K [26.3 cm (10-1/2 in) chassis]	32 A available for processor backplane and 32 A available for expander backplanes

The following is a list of typical PDP-11/34 components and the current required for each. Appendix B provides current requirements and other pertinent information for PDP-11 optional equipment.

Typical System Components	Current Required At:				
	+5 Vdc	+15 Vdc	-15 Vdc	+20 Vdc	-5 Vdc
KD11-E (M7265 and M7266)	10.5 A				
KD11-EA (M8265 and M8266)	11.5 A				
M9301	2.0 A				
M9302	1.2 A				
MM11-CP (Active)	3.0 A			3.5 A	0.2 A
MM11-DP (Active)	4.0 A			4.0 A	0.5 A
MS11-EP (Active)	2.0 A	0.8 A	0.1 A		
MS11-FP (Active)	2.0 A	0.85 A	0.1 A		
MS11-JP (Active)	2.0 A	0.95 A	0.1 A		
Parity Controller (M7850)	1.0 A				
KY11-LB Interface (M7859)	3.0 A				
DL11-W (M7856)	2.0 A	0.05 A	0.15 A		

Functional

Word Length	16 bits
Memory Access Time	
MOS with parity	700 ns
MM11-DP core memory with parity	570 ns
DMA Rate	
MOS memory	1.4 M words/second
Core memory	1.0 M words/second
Unibus Rate	2.5 M words/second
Addressing Space	128K words (124K memory and 4K I/O page)

Environmental

Temperature	5° C (41° F) to 50° C (122° F)
Relative Humidity	10% to 95% (non-condensing)

5.4 UNPACKING

The basic PDP-11/34 system is shipped in the package shown in Figure 5-3 [26.3 cm (10-1/2 inch) mounting box] or Figure 5-4 [13.3 cm (5-1/4 inch) mounting box]. Please study these figures before unpacking the computer.

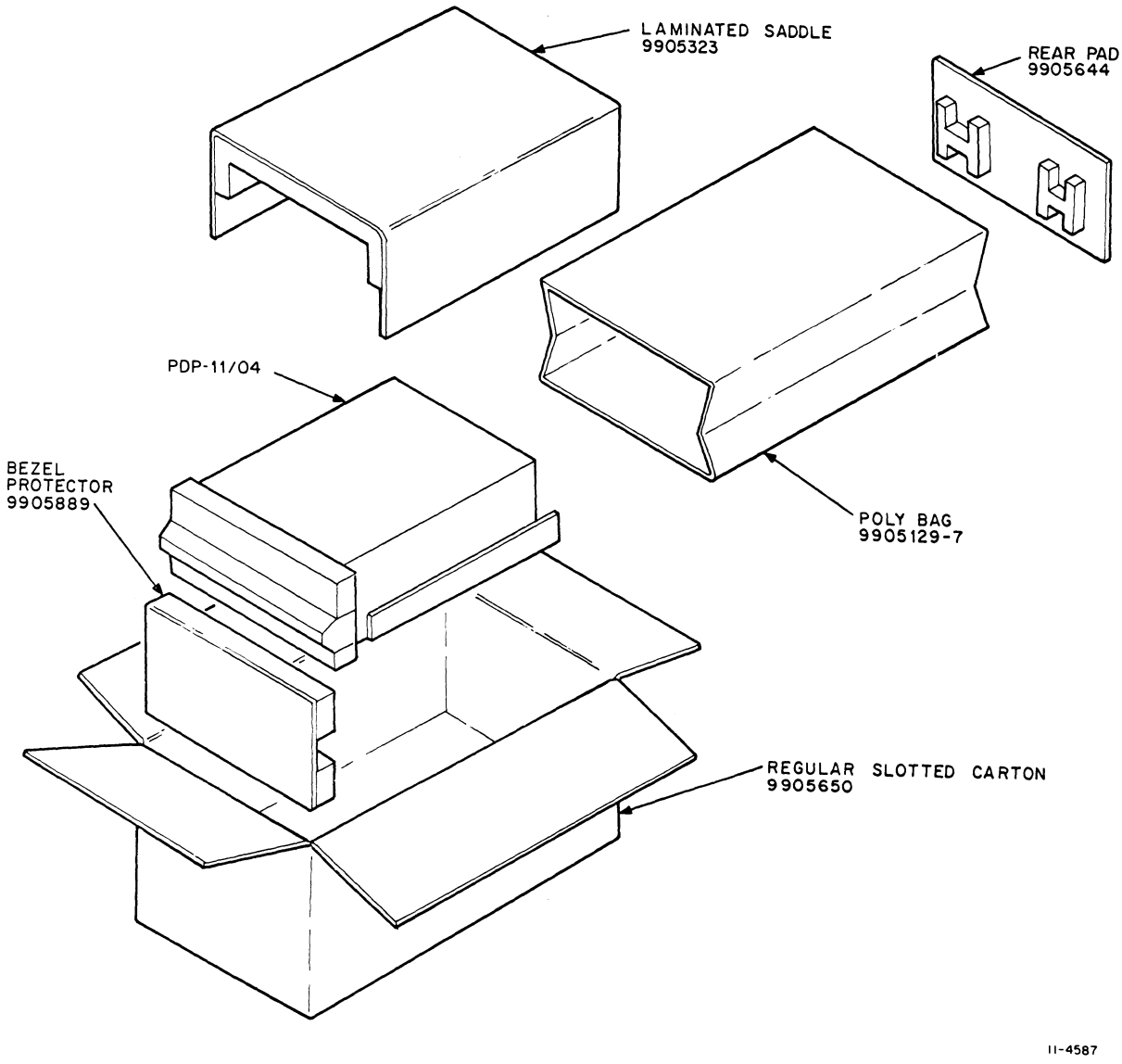


Figure 5-3 Packaging of PDP-11/34 [26.3 cm (10-1/2 inch Box)]

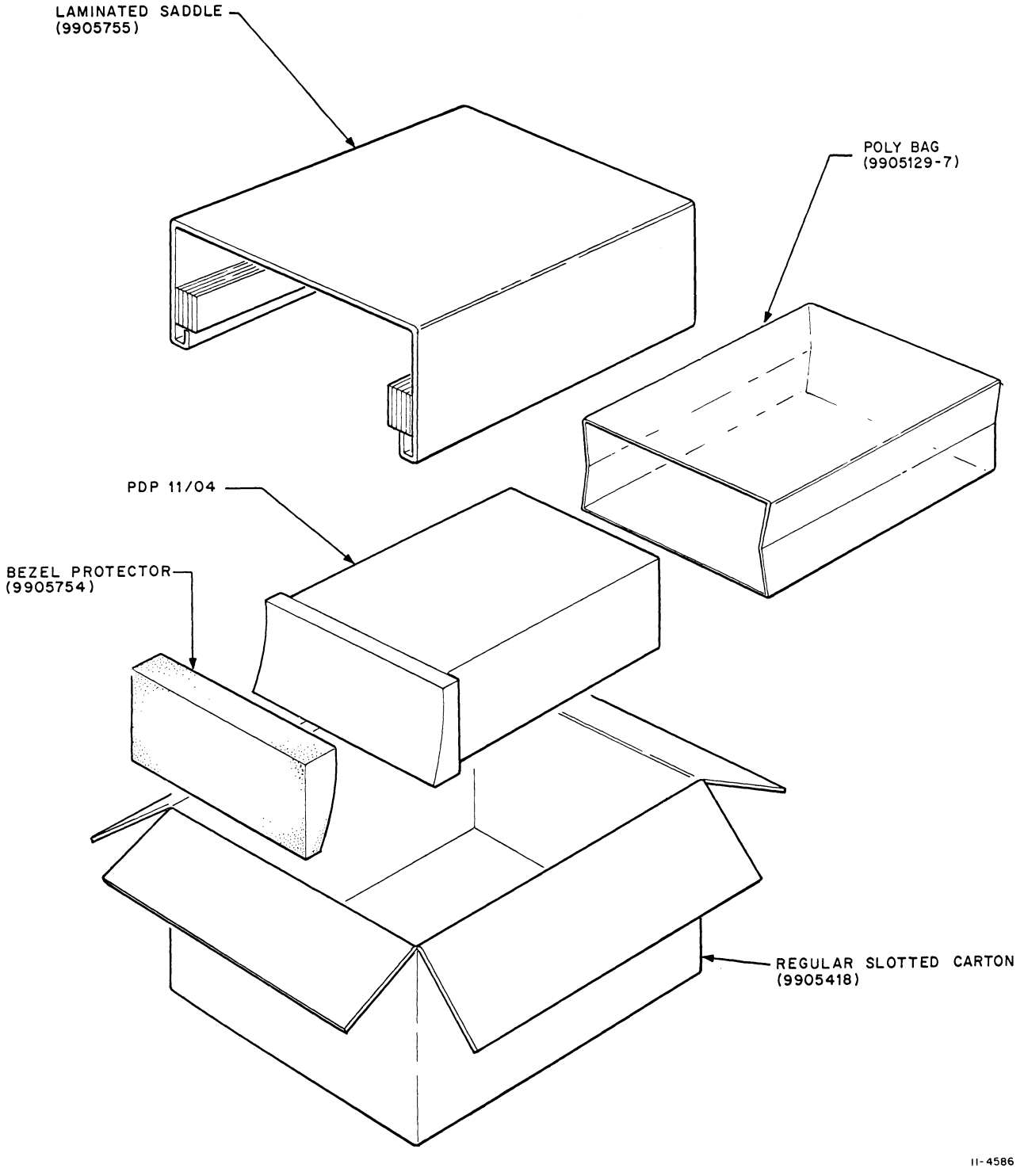


Figure 5-4 Packaging of PDP-11/34 [13.3 cm (5-1/4 inch Box)]

5.5 MODULE UTILIZATION IN TYPICAL SYSTEMS

Figure 5-5 shows the module placement in typical PDP-11/34 (11/34A) systems. Refer to Paragraph 4.2.3 for a detailed discussion of the backplane module utilization.

PDP-11/34 (11/34A) WITH 16K MOS MEMORY

	A	B	C	D	E	F
1	M7266 (M8266) CPU CONTROL					
2	M7265 (M8265) CPU DATA PATH					
3	M9301	DL11-W OR QUAD SPC SLOT				
4	MS11-JP 16K MOS MEMORY					
5	M7850	QUAD SPC SLOT				
6	HEX OR QUAD SPC SLOT					
7	HEX OR QUAD SPC SLOT					
8	HEX OR QUAD SPC SLOT					
9	M9302 *	QUAD SPC SLOT				

PDP-11/34 (11/34A) WITH 16K CORE MEMORY

	A	B	C	D	E	F
1	M7266 (M8266) CPU CONTROL					
2	M7265 (M8265) CPU DATA PATH					
3	M9301	DL11-W OR QUAD SPC SLOT				
4	MM11-DP 16K CORE MEMORY					
5						
6	M7850	QUAD SPC SLOT				
7	HEX OR QUAD SPC SLOT					
8	HEX OR QUAD SPC SLOT					
9	M9302 *	QUAD SPC SLOT				

PDP-11/34 (11/34A) WITH 32K MOS MEMORY

	A	B	C	D	E	F
1	M7266 (M8266) CPU CONTROL					
2	M7265 (M8265) CPU DATA PATH					
3	M9301	DL11-W OR QUAD SPC SLOT				
4	MS11-JP 16K MOS MEMORY					
5	MS11-JP 16K MOS MEMORY					
6	M7850	QUAD SPC SLOT				
7	HEX OR QUAD SPC SLOT					
8	HEX OR QUAD SPC SLOT					
9	M9302 *	QUAD SPC SLOT				

PDP-11/34 (11/34A) WITH 32K CORE MEMORY

	A	B	C	D	E	F
1	M7266 (M8266) CPU CONTROL					
2	M7265 (M8265) CPU DATA PATH					
3	M9301	DL11-W OR QUAD SPC SLOT				
4	MS11-DP 16K CORE MEMORY					
5						
6	MM11-DP 16K CORE MEMORY					
7						
8	M7850	QUAD SPC SLOT				
9	M9302 *	QUAD SPC SLOT				

* M9302 or Unibus "OUT" Connector

NOTE:
The M7850 Parity Controller can be installed in any available modified Unibus slot (slots 2 through 8, A and B)

11-5455

Figure 5-5 PDP-11/34 Module Utilization

5.6 INITIAL INSPECTION

After unpacking the computer, extend the wire frame assembly containing the logic and power subassemblies. Refer to Figure 5-6 for the 13.3 cm (5-1/4 inch) box and Figure 5-7 for the 26.3 cm (10-1/2 inch) box. Examine the following areas:

1. Check the overall appearance for scratches, dents, chipped paint, dust, etc.
2. Check for loose or missing hardware (screws, nuts, etc.).
3. Toggle front panel switches to make certain each switch operates freely and unrestricted.
4. Examine backplane for bent pins.
5. Check power and console harness for proper connection to the power supply and front console. Refer to Figure 5-8 for connector placement and Paragraph 4.2.2.1 for connector pin locations and signal assignments.
6. Remove the shipping brackets from both the BA11-L and BA11-K boxes.

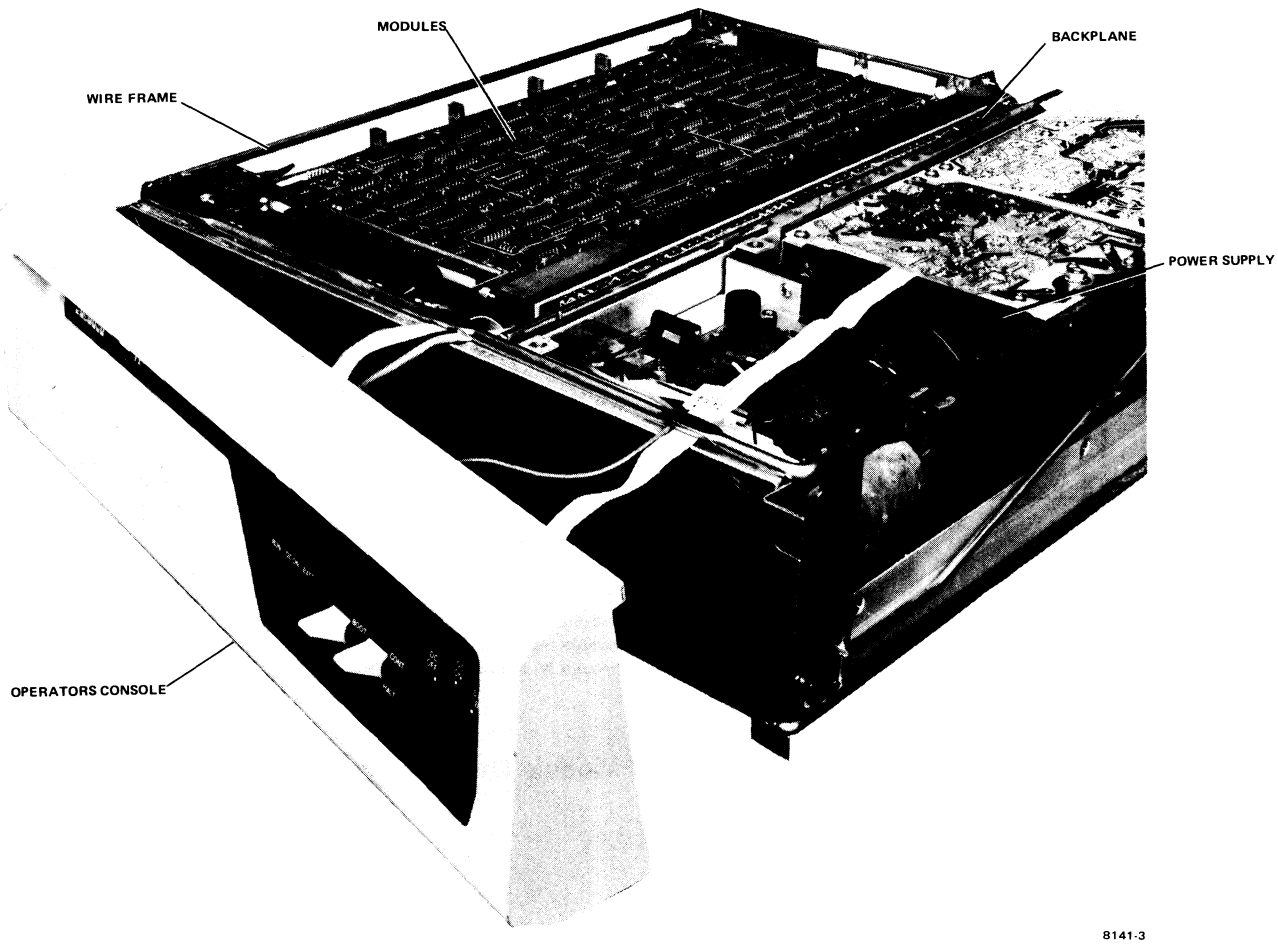


Figure 5-6 Computer Subassemblies of BA11-L Mounting Box

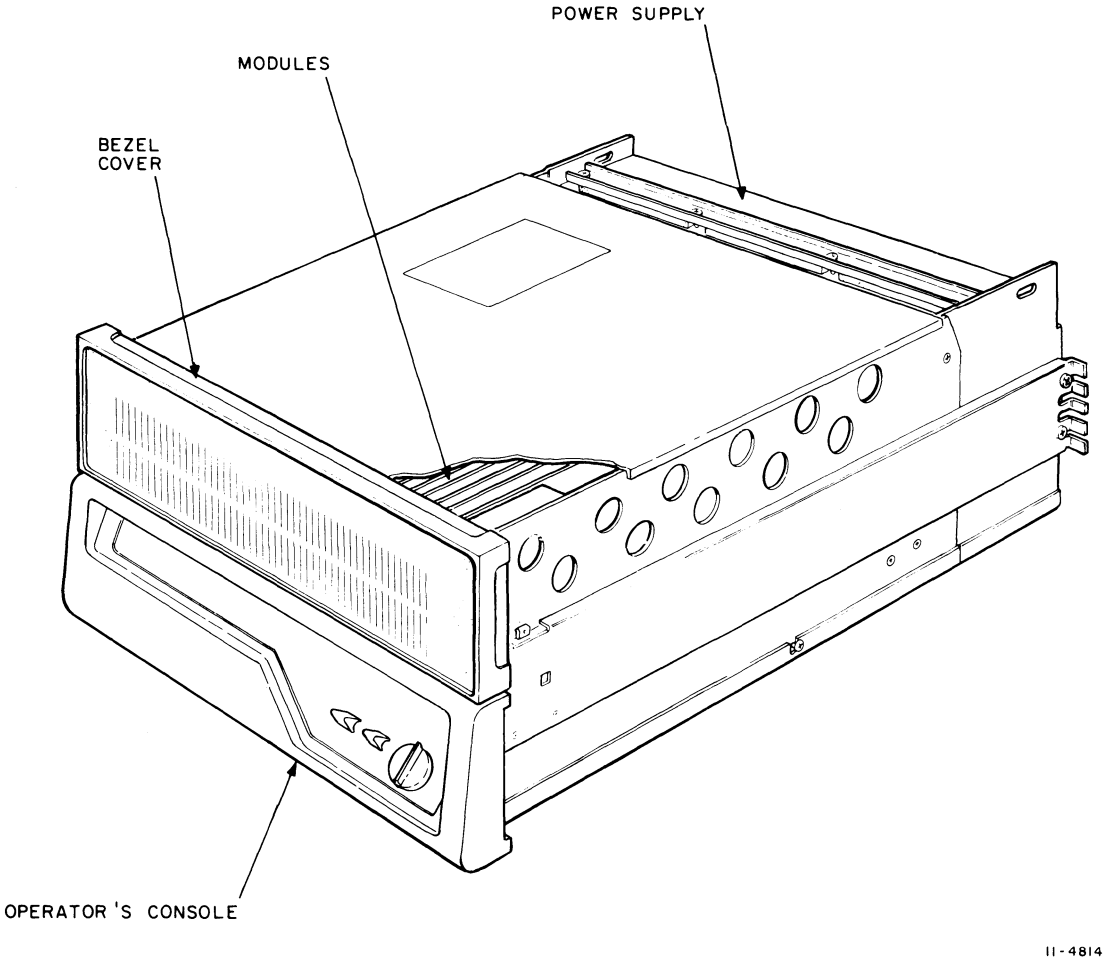


Figure 5-7 Computer Subassemblies of BA11-K Mounting Box

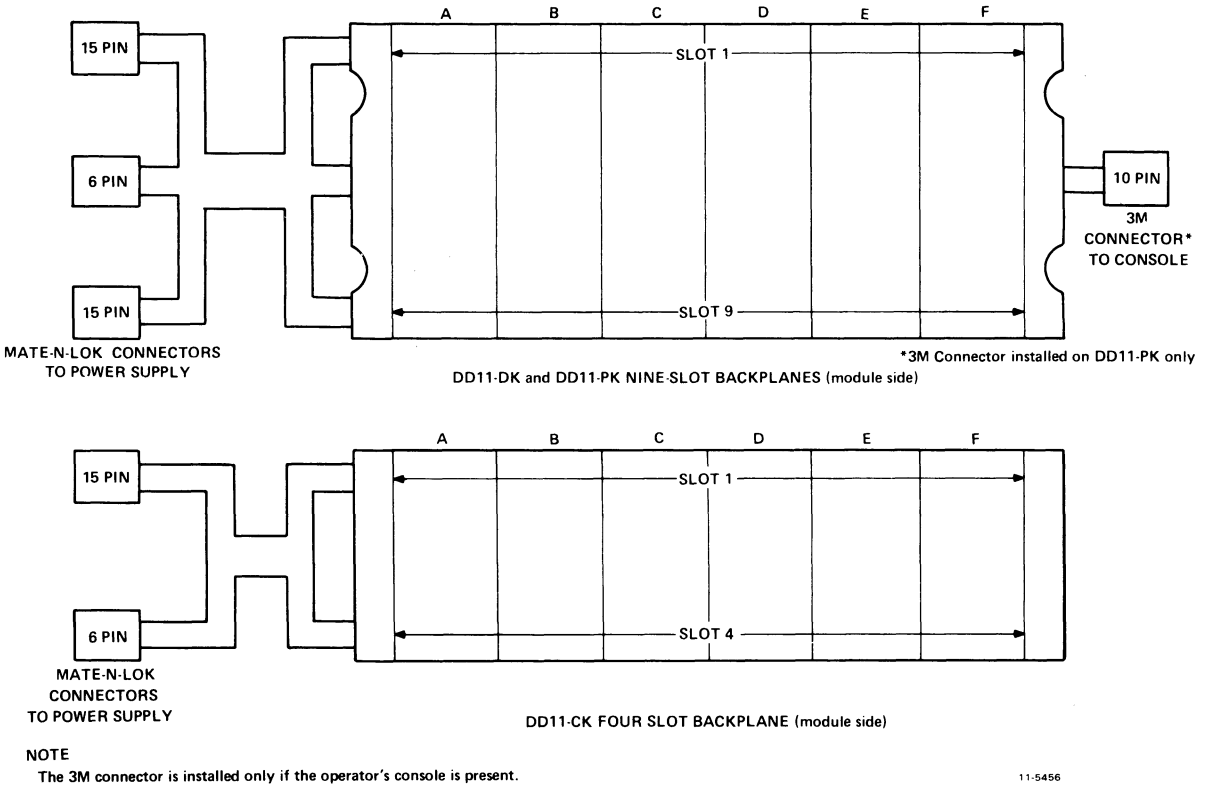


Figure 5-8 Backplane Connectors

5.7 TYPICAL SWITCH SETTINGS OF MODULES

Figure 5-9 shows the typical switch settings of each of the modules in the system. The specific settings for a particular user's system will depend upon the configuration. Refer to Paragraph 4.3 for a detailed discussion of the switch functions on each module.

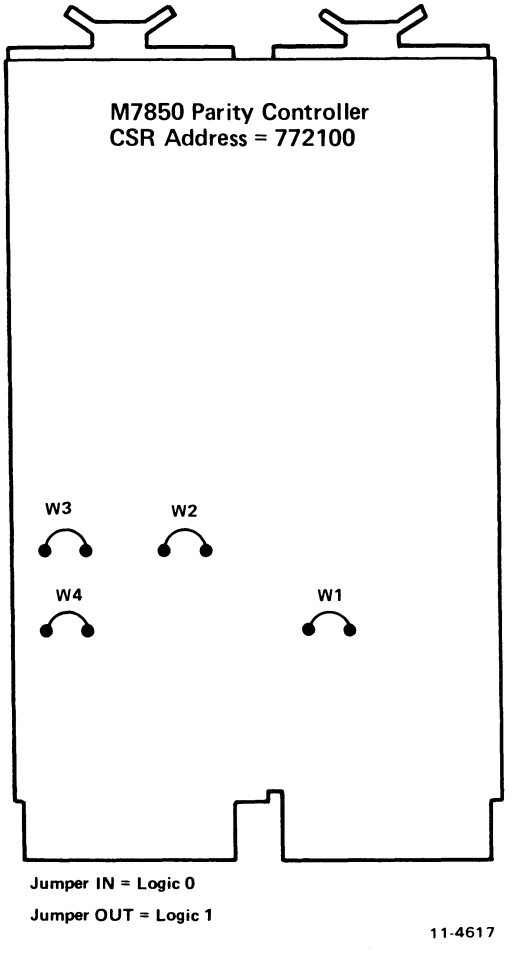


Figure 5-9 Typical Jumper Placement and Switch Settings of Modules
(Sheet 1 of 9)

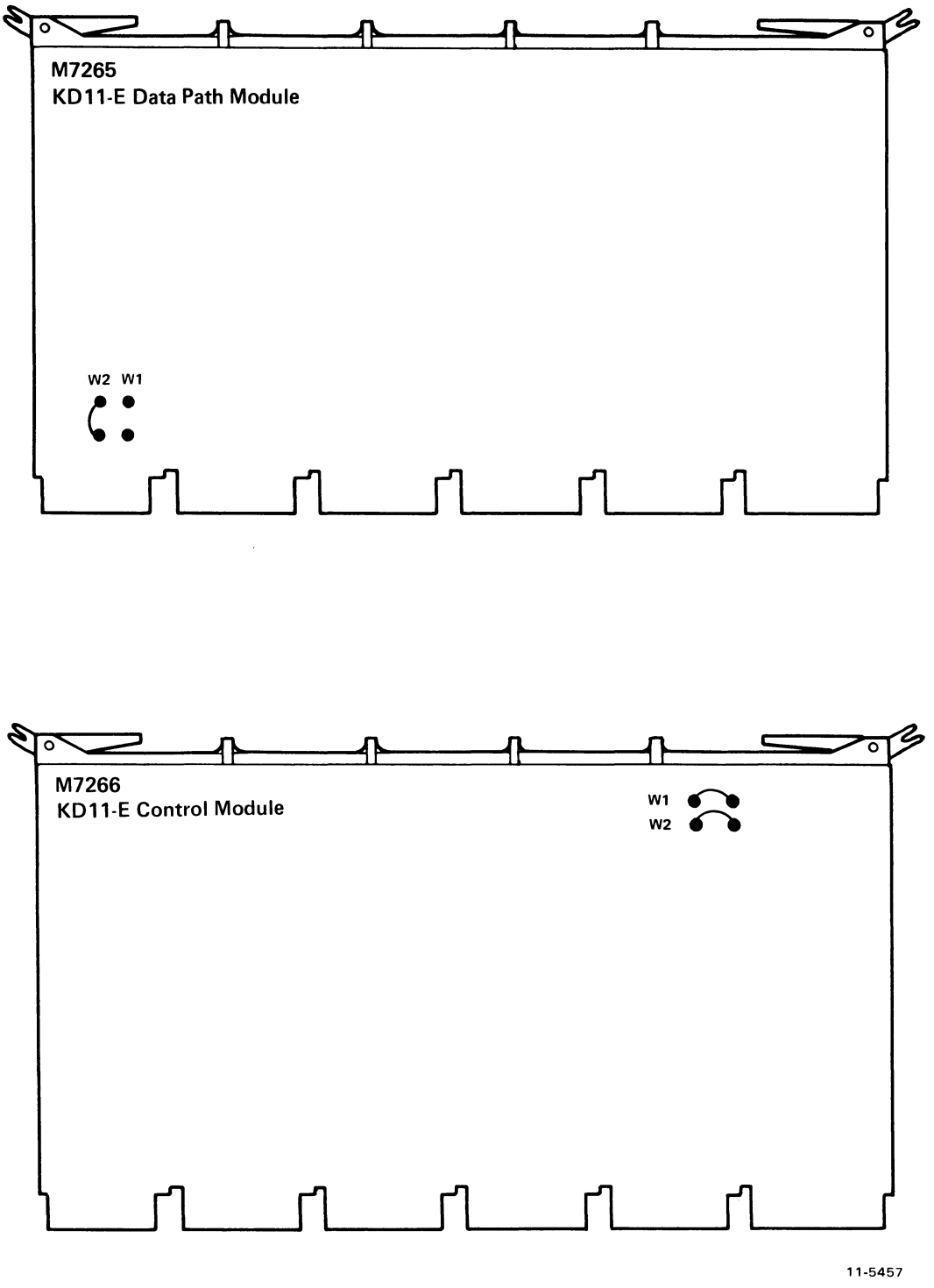


Figure 5-9 Typical Jumper Placement and Switch Settings of Modules
(Sheet 2 of 9)

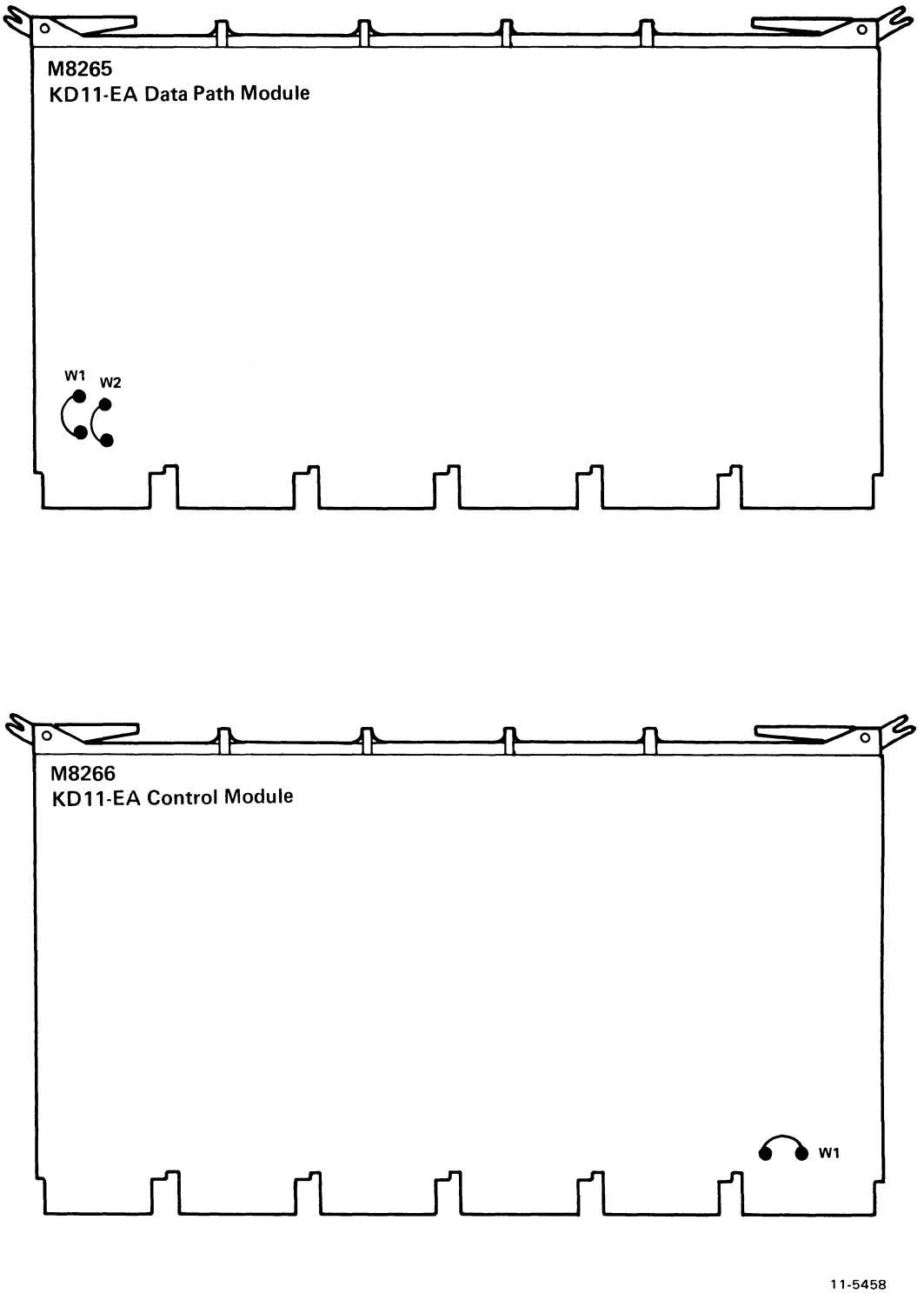


Figure 5-9 Typical Jumper Placement and Switch Settings of Modules
(Sheet 3 of 9)

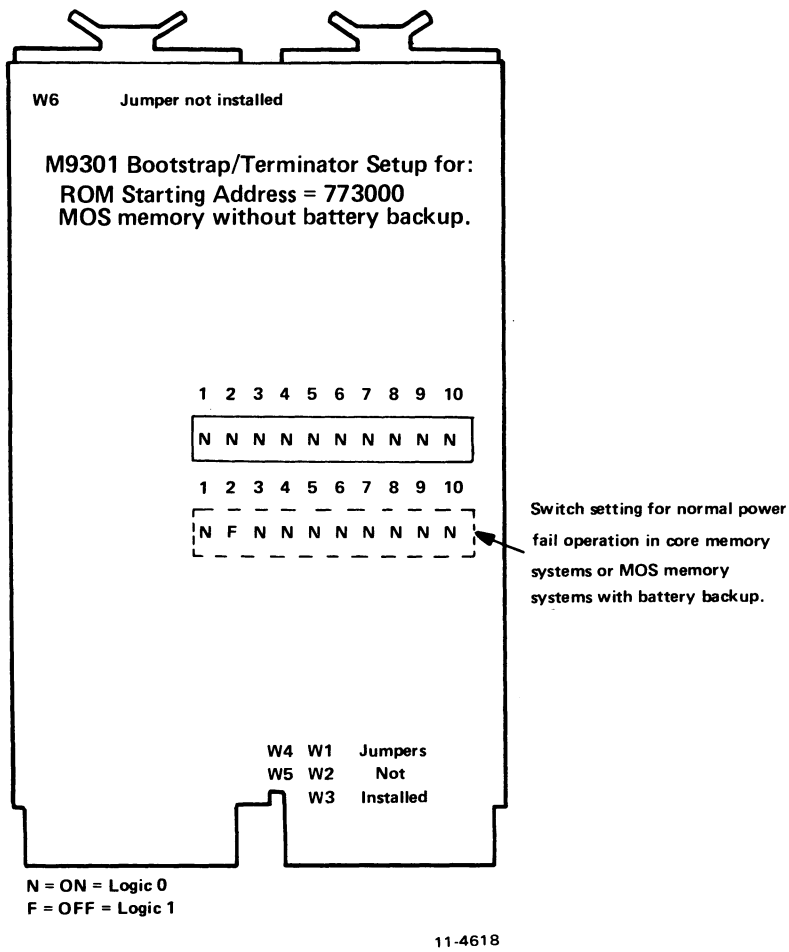


Figure 5-9 Typical Jumper Placement and Switch Settings of Modules (Sheet 4 of 9)

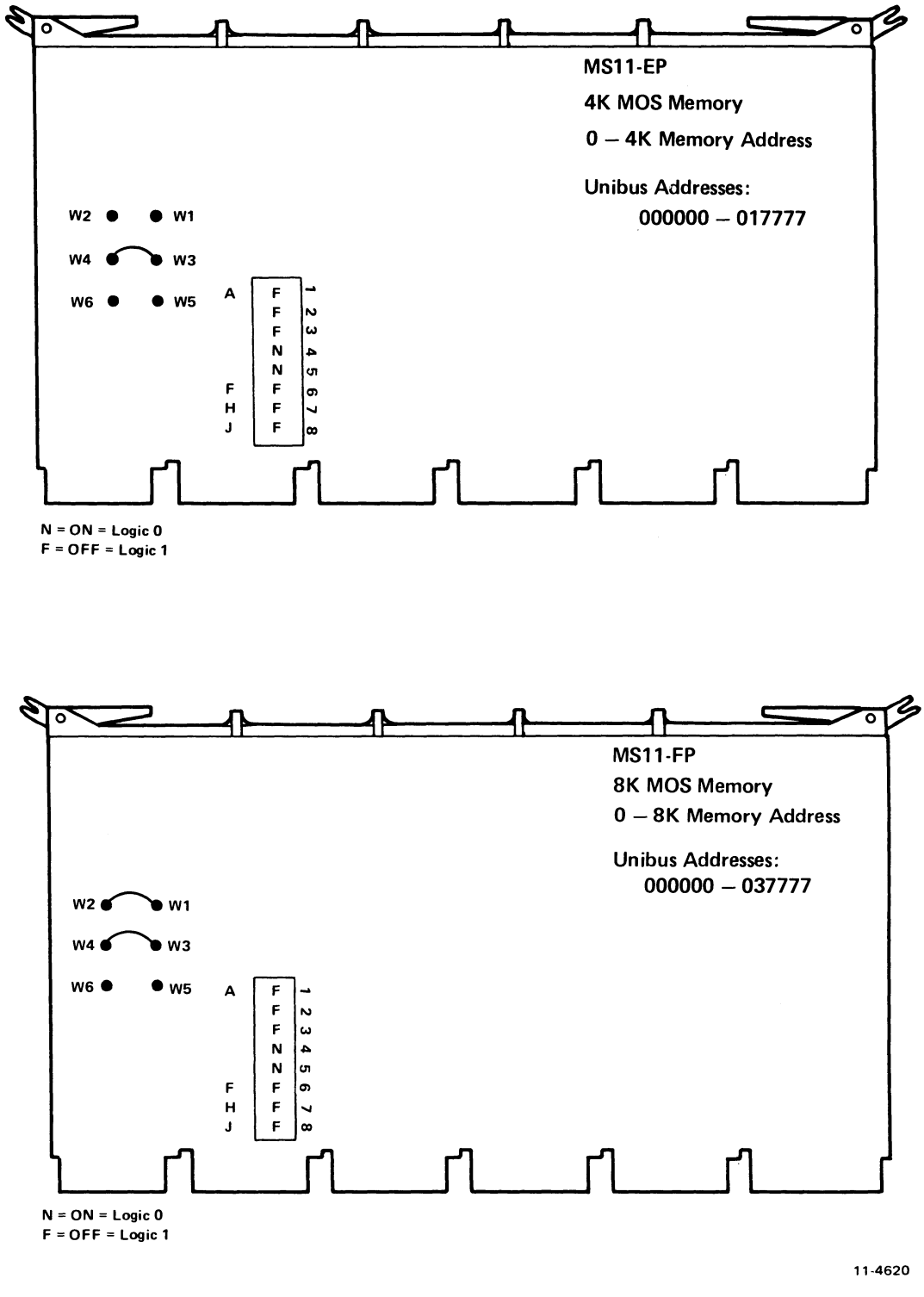


Figure 5-9 Typical Jumper Placement and Switch Settings of Modules (Sheet 5 of 9)

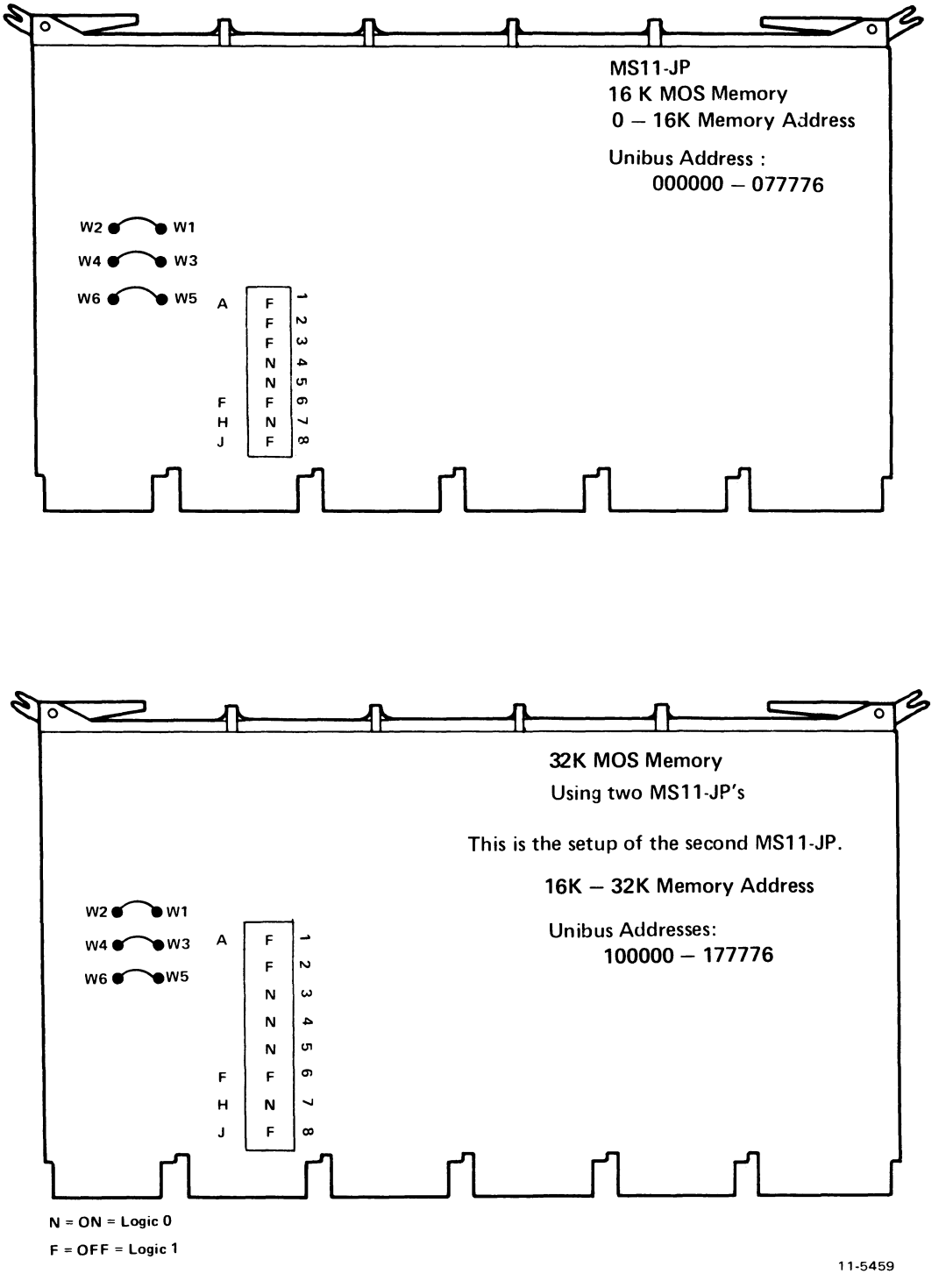


Figure 5-9 Typical Jumper Placement and Switch Settings of Modules (Sheet 6 of 9)

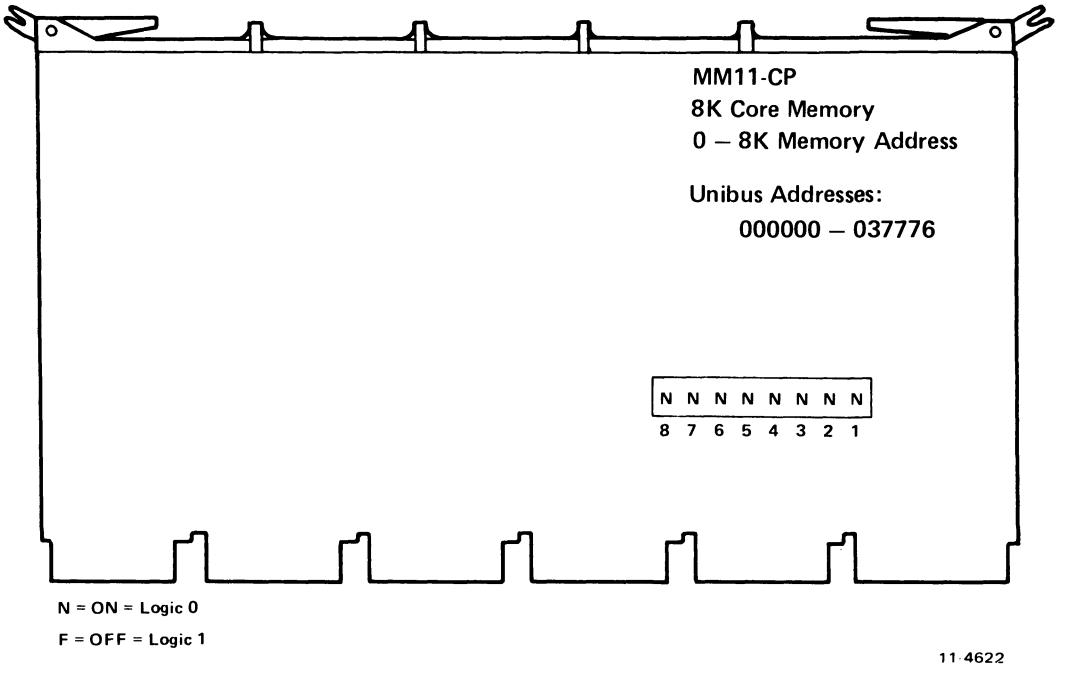
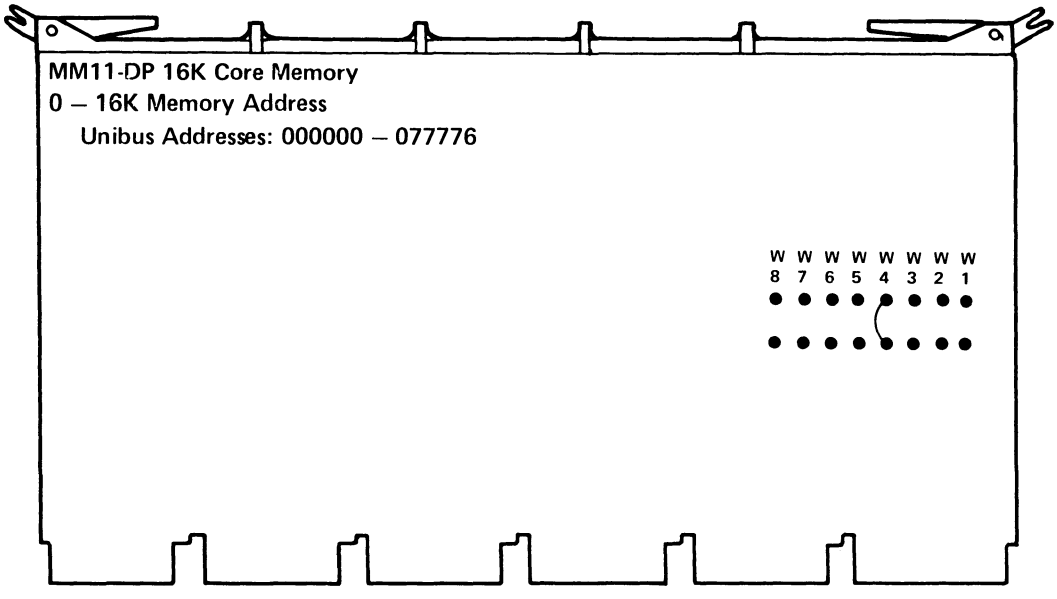


Figure 5-9 Typical Jumper Placement and Switch Settings of Modules
(Sheet 7 of 9)



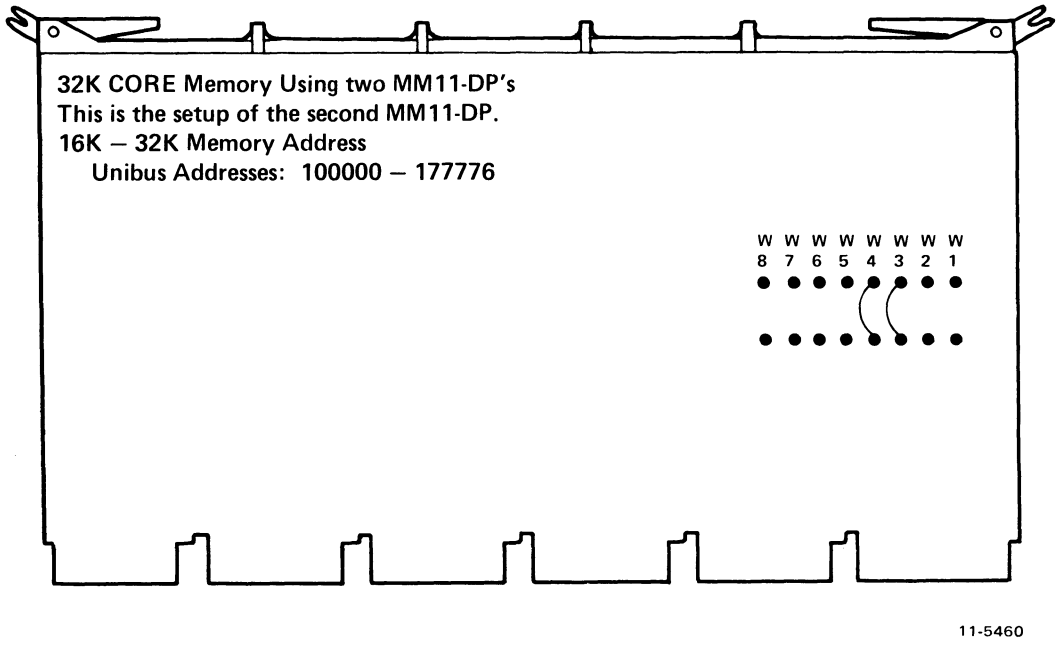


Figure 5-9 Typical Jumper Placement and Switch Settings of Modules
(Sheet 8 of 9)

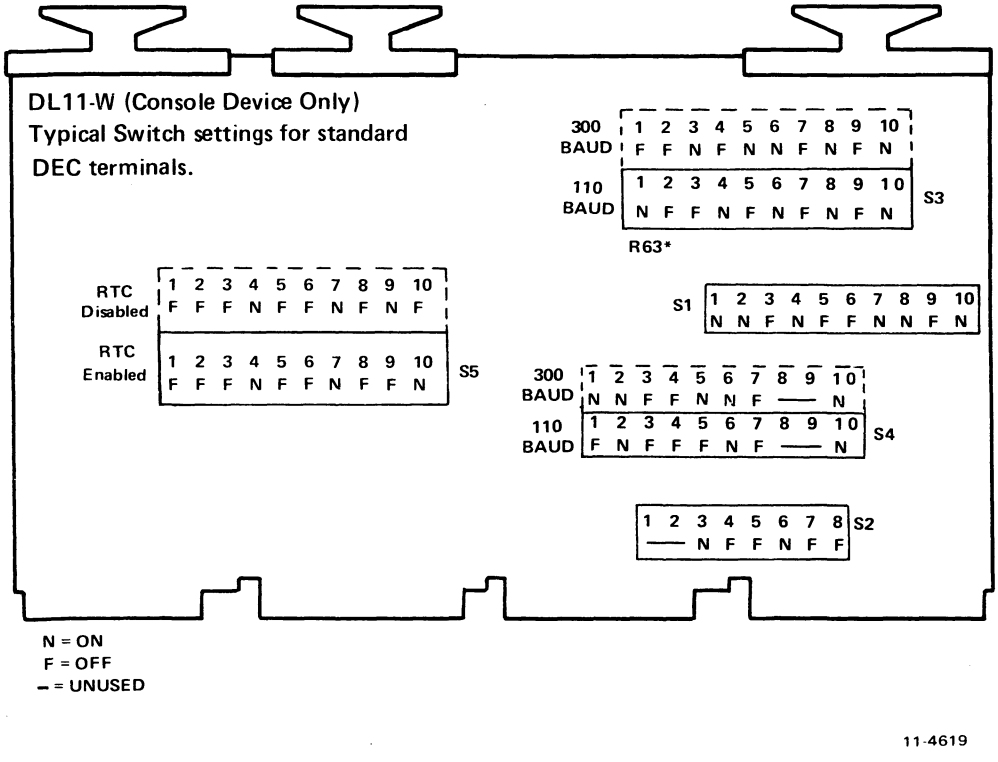


Figure 5-9 Typical Jumper Placement and Switch Settings of Modules (Sheet 9 of 9)

5.8 FIRST-TIME START-UP PROCEDURE

The following start-up procedure should be performed in sequence and no steps should be omitted. The procedure requires the following.

- Serial Line Controller (DL11-W or equivalent) is installed.
- Console terminal is ON-LINE.
- Operator's console (KY11-LA) or programmer's console (KY11-LB) is installed.
- All M9301 switches are ON.

WARNING

Placing the power switch in the OFF position does not prevent ac power from being applied to some areas of the computer when the line cord is plugged into the ac receptacle.

Step 1

1. Place the power switch in the OFF position.
2. Plug the line cord into the ac receptacle.
3. Place the HALT/CONT switch in the CONT position.
4. Place the OFF/ON/STNDBY switch in the ON position.

Step 2
Check for the following indications:

1. Fan rotation
2. DC power indicator ON
3. BATT status indicator on or blinking (BATT indicator is off if battery backup option is not present).
4. Console terminal printed register printout and prompt character ($).

NOTE
If switch 2 of the M9301 is OFF, the BOOT/INIT switch must be pressed and released to get the register printout and prompt character.

5. RUN indicator on.

Step 3
Perform the following quick verification routine. (Refer to Paragraph 6.2 if any of the tests yield incorrect results.)

Action	Correct Result
1. Load address 173024 and examine that location.	1. The contents will be 173000.
2. Type a boot command for a non-existent device.	2. Register printout will be typed on console terminal and RUN light will be on. **NOTE** **If the M9301-YF is implemented, this action will result in a halt, (i.e., register printout is not typed and RUN light is off).**
3. Load address 0. Examine location 0. Deposit 777 into location 0 and examine. Start.	3. The keyboard will no longer respond and the RUN light will be on.
4. HALT the processor.	4. The RUN light will be off.
5. CONTinue the processor from the halted state.	5. The RUN light will be on.
6. HALT the processor. Initiate the BOOT function. Move the HALT/CONT switch back to CONT (KY11-LA only).	6. Register printout will be typed on console terminal. The "OLD PC" will be 0.

NOTE
Return all switches to their proper positions.

Step 4
Run the PDP-11/34 diagnostic as follows:

1. Bootstrap load a diagnostic from a peripheral device as described in Paragraph 2.1.3.5.

2. After booting, refer to the diagnostic writeup for instructions. Let the diagnostic run for two passes.

Table 5-1 lists the diagnostics associated with the PDP-11/34 system.

5.8.1 Check of Standby Operation

After proper operation of the computer has been verified by the diagnostics, a check of standby operation (BA11-L only) can be made as follows.

NOTE
MOS memory must be installed in the system to make this check.

1. HALT the processor (via the console).

2. Place the OFF/ON/STNDBY switch in the STNDBY position and check the following indications:

   a. DC ON indicator will go off.

   b. BATT indicator will be on blinking. (BATT indicator will be off if battery backup is not present.)

   c. Remain in the STANDBY mode for approximately 1 minute.

3. Continue processor operation from the halted state and place the OFF/ON/STNDBY switch in the ON position. Rerun the PDP-11/34 CPU diagnostic (MAINDEC-11-DFKAA).

Table 5-1 PDP-11/34 Diagnostics

Title	Number
PDP-11/34 CPU Test	MAINDEC-11-DFKAA
PDP-11/34 Trap Test	MAINDEC-11-DFKAB
PDP-11/34 Memory Management Exerciser PDP-11/34 EIS Instruction Tests	MAINDEC-11-DFKTG MAINDEC-11-DFKAC
MOS/CORE Memory Exercisers	MAINDEC-11-DZKMA MAINDEC-11-DZQMC (Rev. C or later)
Combined Parity Memory Test	MAINDEC-11-DCMFA (Rev. C or later)
PDP-11 Power Fail (if system contains core memory or MOS memory with battery backup)	MANDEC-11-DZKAQ (Rev. E or later)
DL11-W Serial Line Unit/Real-Time Clock Diagnostic	MAINDEC-11-DZDLD
NOTE **The DL11-W diagnostic is preferred; however, if it is unavailable, the following diagnostics may be implemented.**	
KL11/DL11-A Teletype Test (if system contains console serial line unit)	MAINDEC-11-DZKLA (Rev. E or later)
Line Frequency Clock Test (if the line frequency clock is enabled)	MAINDEC-11-DZKWA (Rev. E or later)

CHAPTER 6
TROUBLESHOOTING

6.1 PDP-11/34 CHARACTERISTICS SUMMARY

This paragraph provides a listing of operation and installation notes peculiar to the PDP-11/34.

6.1.1 Operation (KY11-LA)

1. Pressing the BOOT/INIT switch while a program is running will cause that program to be aborted.

2. The console emulator will accept octal numbers only.

3. The console emulator will accept even addresses only (i.e., least significant digit must be a 0, 2, 4, or 6).

4. First octal number typed is the most significant digit.

5. The console emulator can accept up to six octal digits. If all six numbers are input, the most significant number must be a zero or a one.

6. If the program causes the system to halt, the HALT/CONT switch must first be placed in the HALT position and then moved to CONT to resume operation.

6.1.2 Operation (KY11-LB)

1. Examine and deposit functions are operative only if processor is halted.

2. The control key (CNTRL) must be pressed to enable the initialize, halt/single step, continue, start, and boot functions.

3. The display must be cleared before entering any new data.

4. The programmer's console requires an 18-bit address.

5. In order to single instruction step the processor from a given starting address, the program counter (R7, Unibus address 777707) must be loaded with the starting address.

6. The BUS ERR indicator reflects a bus error by the console only. The indicator does not reflect bus errors due to the processor.

6.1.3 Installation

1. The KD11-E (KD11-EA) processor modules must be installed in the first two backplane slots of the system.

2. The M9302 terminator module must be installed in the last backplane slot of the system. The M9302 must *not* be installed in a modified Unibus slot. The modified Unibus slots are:

   DD11-CK - Slots 2 and 3 (sections A and B)
   DD11-DK - Slots 2 through 8 (sections A and B)
   DD11-PK - Slots 2 through 8 (sections A and B)

3. The DC OFF position of the power switch does not remove ac power from the system. AC power is removed only by disconnecting the line cord.

4. The DC ON light indicates that dc power is applied to the logic but does not imply that the power is within required levels.

5. A bus grant jumper card (G727) must be placed in connector D of any unoccupied SPC section or grant continuity will be lost.

6. Unibus cables (i.e., BC11-A) must never be plugged into a modified Unibus slot.

7. In boxes other than BA11-L, there is not sufficient drive capability on the LTC L signal to drive multiple loads. Since each DL11-W constitutes a load (even if the line clock is disabled by the switch), multiple DL11-Ws in a box will overload the LTC L signal causing line clock failures. To alleviate the loading effect of the additional DL11-Ws, remove resistor R63 from all DL11-W modules except the one being used as a line clock. If multiple DL11-Ws are used on the same system, the line clock must be enabled (via switched) *only* on the DL11-W being used as a line clock.

6.2 TROUBLESHOOTING PROCEDURES

This paragraph provides the user with a quick method for isolating major problem areas of the system. The quick verification routine consists of seven tests that should be performed in sequence. The associated flowchart for each test lists the possible problem areas that may have caused incorrect test results. Each flowchart is accompanied by a detailed explanation containing additional tests to help further isolate the problem. *These troubleshooting procedures assume that the system has been installed and configured according to Chapters 4 and 5 and that the M9301 switches are set as in Figure 5-8.*

6.2.1 Quick Verification Routine

The quick verification tests should be performed in sequence. If an incorrect result is obtained, refer to the flowchart and explanation associated with that test. These procedures are applicable for both the KY11-LA and optional KY11-LB consoles.

Action	Correct Result
1. Turn power on.	1. Register printout will be typed on console terminal and RUN light will be on.
2. Load address 173024 and examine that location.	2. The contents will be 173000.
3. Type a boot command for a non-existent device.	3. Register printout will be typed on console terminal and RUN light will be on. **NOTE** **If the M9301-YF is implemented, this action will result in a halt (i.e., register printout is not typed and RUN light is off).**
4. Load address 0. Examine location 0. Deposit 777 into location 0 and examine. Start.	4. The keyboard will no longer respond and the RUN light will be on.
5. Halt the processor.	5. The RUN light will be off.
6. CONTinue the processor from the halted state.	6. The RUN light will be on.
7. Halt the processor. Initiate the BOOT function. Move the HALT/CONT switch back to CONT (KY11-LA only).	7. Register printout will be typed on console terminal. The "OLD PC" will be 0.

NOTE
Return all switches to their proper positions.

The following is a brief explanation of each of the quick verification tests:

Action 1	Correct Result
Turn power on.	Register printout will be typed on console terminal and RUN light will be on.

When the system is powered up, the first five processor diagnostics of the M9301 are executed. The diagnostic tests performed are:

1. All single operand instructions tests (Test 1)
2. All double operand instructions tests (Test 2)
3. Jump test (modes 1, 2, and 3) (Test 3)
4. Single operand, non-modifying, byte test (Test 4)
5. Double operand, non-modifying test (source modes 1 and 4, destination modes 2 and 4) (Test 5).

Paragraph 3.3 contains a description of each of the above diagnostic tests.

Once the fifth diagnostic test has been performed, the M9301 will enter the register display routine. The console teletype will print out the contents of R0, R4, R6, and R5 (Paragraph 2.1.3.2). R5 contains the "OLD PC" since the microcode moves the contents R7 into R5 before entering the power-up routine. The sequence of register contents is followed on the next line by a prompt character ($) which indicates that the console emulator is waiting for a command. If the prompt character is received, it can be assumed that a portion of the processor, M9301, console interface, console terminal, and Unibus are functioning properly.

If the terminal does not type out the register sequence and prompt character, refer to Figure 6-1.

Action 2	Correct Result
Load address 173024 and examine that location.	The contents will be 173000.

This test checks a portion of the console emulator routine and the switch settings of the M9301. If the contents of location 173024 are not 173000, the switch settings of the M9301 are incorrect. It is possible to receive the register display and prompt character in Action 1 without performing any diagnostics. All M9301 switches should be on. If they are not on, set them correctly and repeat Action 1. Refer to Figure 6-2 if incorrect results are obtained.

Action 3	Correct Result
Type a boot command for a non-existent device.	Register printout will be typed on console terminal and RUN light will be on. NOTE **If the M9301-YF is implemented, this action will result in a halt (i.e., register printout is not typed and RUN light is off).**

This test allows the user to execute the remainder of the M9301 diagnostics without actually booting from a peripheral device. The remaining diagnostic tests performed are:

1. Double operand, modifying byte test (Test 6)
2. JSR test (modes 1 and 6) (Test 7)
3. Memory test.

The bootstrap routine will try to boot from the non-existent peripheral. After failing to boot, the console terminal will type the register printout and the prompt character ($). After successful completion of the remaining diagnostic tests, the user can assume that a large portion of the processor, M9301, console interface, and terminal are functioning and that memory (up to 28K) contains no major errors. Refer to Figure 6-3 if the register printout and prompt character are not received.

Action 4	Correct Result
Load address 0. Examine location 0. Deposit 777 into location 0 and examine. Start	The keyboard will no longer respond and the RUN light will be on.

This test checks the remainder of the console functions, specifically DEPOSIT and START. Refer to Figure 6-4 if an incorrect response is obtained.

Action 5	Correct Result
Halt the processor.	The RUN light will be off.

This test checks the logic on the console and processor that is associated with the HALT function. Refer to Figure 6-5 if the RUN light remains on.

Action 6	Correct Result
CONTinue processor operation from the halted state.	The RUN light will be on.

This test checks the logic on the console and processor that is associated with the CONT function. Refer to Figure 6-6 if the RUN light does not come on.

Action 7	Correct Result
Halt the processor. Initiate the BOOT function. Move the HALT/CONT switch back to CONT (KY11-LA only).	Register printout will be typed on console terminal. The "OLD PC" will be 0.

This test checks the BOOT switch on the console, the cable connecting the console and M9301 and the portion of the M9301 associated with the BOOT function. Refer to Figure 6-7 if the register printout and prompt character are not received or if the "OLD PC" is wrong.

6.2.2 Troubleshooting Flowcharts and Explanations

This paragraph provides a chart and explanation for each of the quick verification tests.

Action 1	Correct Result
Turn power on.	Register printout will be typed on console terminal and RUN light will be on.

Action 1 has failed if the register printout and prompt character were not received on power up. The following symptoms will help the user locate the problem area (Figure 6-1).

1. RUN light flashes once but does not stay on.
   There are several possible problem areas that may cause this symptom.

   a. The HALT/CONT switch could be in the HALT position. Place the switch in the CONT position and repeat Action 1.

   b. Switch number 2 on the M9301 may be in the off position. Press and release the BOOT/INIT switch. If the register printout and prompt character are then received, the only problem is that switch 2 is in the off position.

   c. There may be a problem with the console terminal interface (i.e., interface not present in system or not set to correct address).

   d. The HALT GRANT or HALT REQUEST signals may be causing the Unibus to hang. Check the BUS SACK signal line on the processor module. If this line is low, trace the error back through the console HALT GRANT and HALT REQUEST signals. If BUS SACK is not low, there may be an internal problem with the console.

   e. A problem may exist with the processor modules and one of the first five diagnostic tests could have failed.

   f. The M9301 module may be functioning incorrectly.

2. RUN light is off but DC ON light is on.
   The DC ON light does not necessarily indicate that dc power is within the required levels. However, when it is off, it does indicate that +5 V is not present. BUS INIT will turn the RUN light ON if +5 V is present. BUS INIT can be generated by pressing the BOOT/INIT switch with the HALT/CONT switch in the CONT position (KY11-LA) or by pressing INIT and CNTRL simultaneously (KY11-LB). If the RUN light still does not turn on, a problem may exist with the console.

3. RUN light is on.
If the RUN light is on but the register printout and prompt character are not received, a further test may be performed to isolate the problem area. The RUN light, when on, indicates that the processor is not halted. Therefore, if there are no other errors in the system, the RUN light being off indicates that a HALT was executed by the processor or the console. The user can determine if the Unibus is hung or if there is a grant problem by halting and then continuing processor operation. This action will issue a halt command and if the Unibus is functioning the RUN light will go off and then back on.

a. If the RUN light does not obey the HALT function and remains on:

(1) Check the Grant cards. If any of the cards are missing or installed with the etch facing away from the processor module, all the Grant lines will go high (except NPG). Assertion of a Grant line will cause the M9302 to issue BUS SACK L and the processor will turn off its clock. If the Unibus is lightly loaded, remove the M9302. If Unibus is heavily loaded, replace the M9302 with an M930 terminator. If the register printout is then received, there is a Grant problem and the user should proceed to step (2).

(2) Check the BUS SACK signal line on the processor module. If BUS SACK is asserted low, then check the Grant lines on the M9302 module. The NPG signal line is continued by backplane jumpers and not with grant continuity cards.

If BUS SACK is not asserted, check the MSYN and SSYN lines to see if either signal is asserted.

b. If the RUN light obeys the HALT function and goes off and then back on:

(1) A console teletype error may be causing the program to loop on the READY bit. This condition can be checked by removing the interface, inserting a grant continuity card, and repeating Action 1. If the RUN light goes out after performing Action 1, the console interface or terminal is causing the error.

(2) The processor may be executing a program loop in memory (this is unlikely with MOS memory and no battery backup).

(3) One of the first five M9301 diagnostic tests may have failed, causing the processor to execute a branch self instruction.

4. Any symptom not described above:

Cursory checks should be made by the user if other symptoms are encountered.

Checking areas such as power connections, module placement, and switch and jumper settings will help to solve most simple problems.

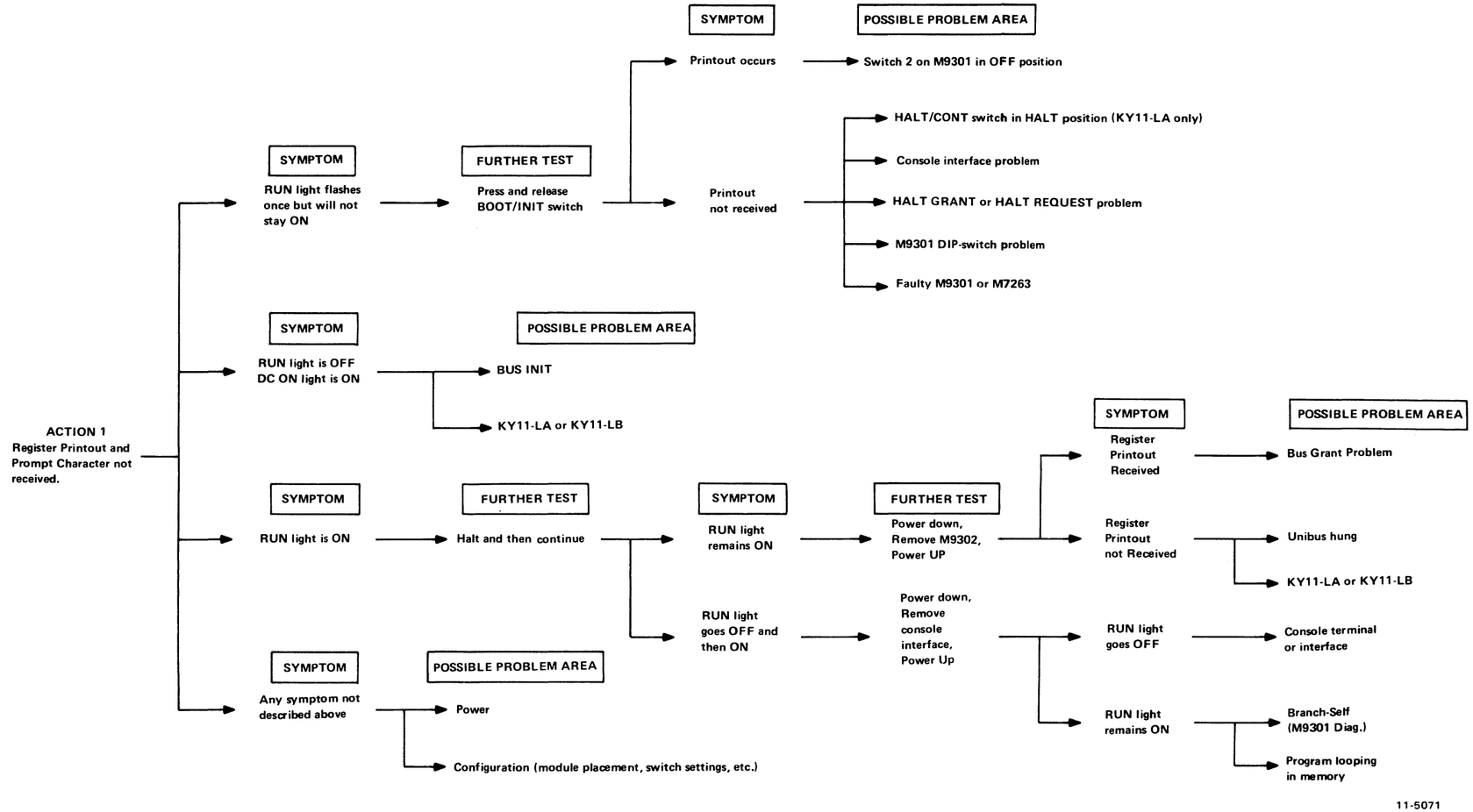


Figure 6-1 Action 1

Action 2	Correct Result
Load address 173024 and examine that location.	The contents will be 173000.

Location 173024 is the address of the M9301 dip-switch pack. If location 173024 is examined and the contents are not 173000, the switches on the M9301 may be set incorrectly. For these tests, all switches on the M9301 should be on. If the switches are set correctly and location 173024 does not contain 173000, there may be an M9301 hardware failure. If some other symptom results, an error in the input format may have been made or the console emulator may have failed. Refer to Figure 6-2.

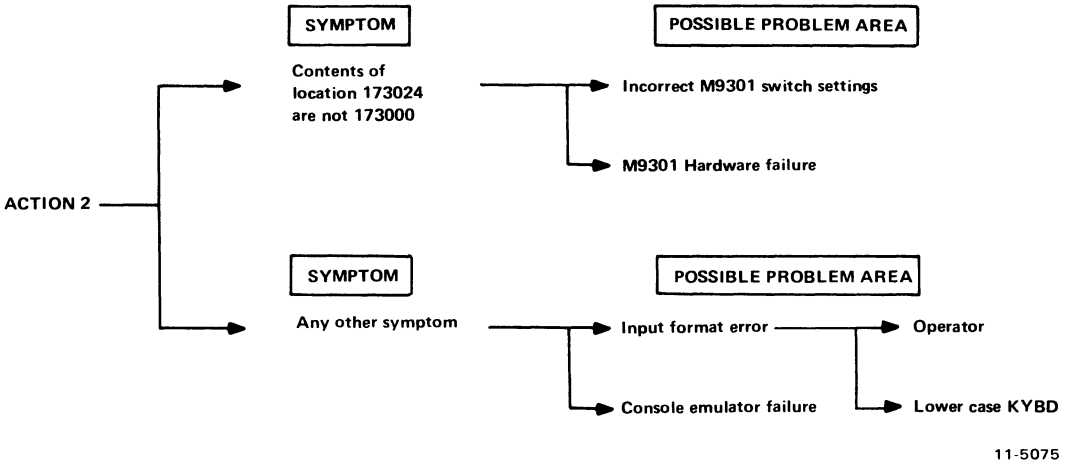


Figure 6-2 Action 2

Action 3	Correct Result
Type a boot command for a non-existent device.	Register printout will be typed on console terminal and RUN light will be on. NOTE **If the M9301-YF is implemented, this action will result in a halt, (i.e., register printout is not typed and RUN light is off).**

If the M9301 (YA, YB, and YF versions) diagnostic tests 6, 7, or memory test fails, the result is a halt. If the M9301-YF diagnostic tests 6, 7, and memory test are all successful, the result is *also* a halt. Therefore, if the RUN light goes off after booting from a non-existent device, it can be assumed that one of the diagnostics has failed (M9301-YA, YB, and YF versions) or that the diagnostics were successful (M9301-YF only). Proceed as follows:

1. Halt the processor and initiate the BOOT function.
2. Return the HALT/CONT switch to CONT (KY11-LA only).

3. The register printout will be typed and the value of the "OLD PC" will indicate which test has failed.

	"OLD PC" (M9301-YA)	"OLD PC" (M9301-YB)	"OLD PC" (M9301-YF)
Failed Test 6	165320	173452	165650
Failed Test 7	165350	173472	165664
Failed Test 7	165372	173514	165700
Failed Memory Test	165536	173764	166000
All Tests Successful	-	-	000002

It is possible to fail at location 165250 (M9302-YA), 173402 (M9301-YB), or 165600 (M9301-YF) if address 500 does not return SLAVE SYNC. If the memory test fails, additional information can be evaluated.

The register printout also includes:

M9301-YA and YB	**M9301-YF**
R0=Expected data	R0=Failing address
R4=Received data	R4=Received data
R6=Failing address	R6=Expected data

If the expected data and received data are the same, it is highly probable that an intermittent failure has been detected (i.e., timing or margin problem). Other failures such as double bus errors could cause the RUN light to go off.

If the register printout is not received after the nonexistent boot, and the RUN light remains on, reboot the system via the BOOT switch. This action will reboot the system and cause the register printout to be typed. The user can then determine where the processor is running by examining the "Old PC."

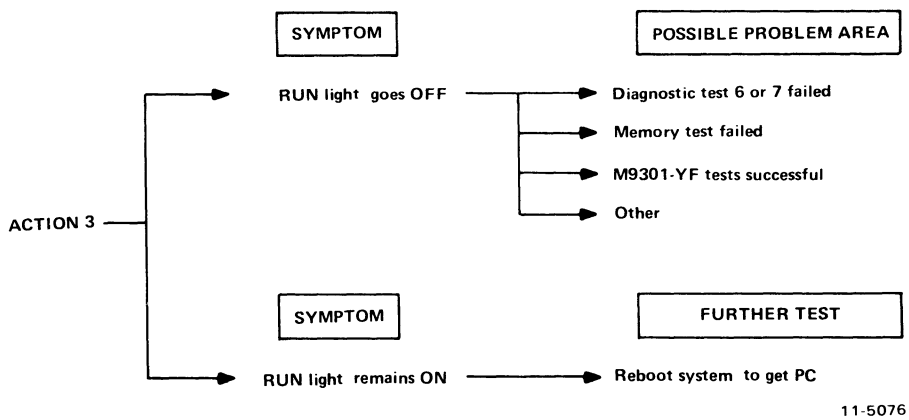


Figure 6-3 Action 3

Action 4	Correct Result
Load address 0. Examine location 0. Deposit 777 into location 0 and examine. Start.	The keyboard will no longer respond and the RUN light will be on.

If an incorrect response results from Action 4 (i.e., keyboard continues to respond, RUN light is off, etc.), two possible problems may exist. The input format on the terminal may have been erroneous or there may be a fault in the M9301 firmware.

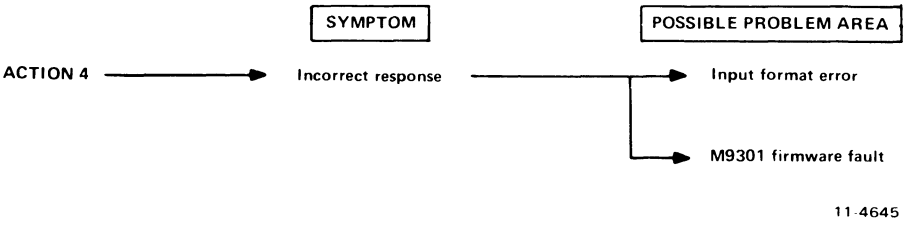


Figure 6-4 Action 4

Action 5	Correct Result
Halt the processor.	The RUN light will be off.

If the HALT function is initiated and the RUN light remains on, a problem may exist with the HALT REQUEST or HALT GRANT signals or the console may be malfunctioning.

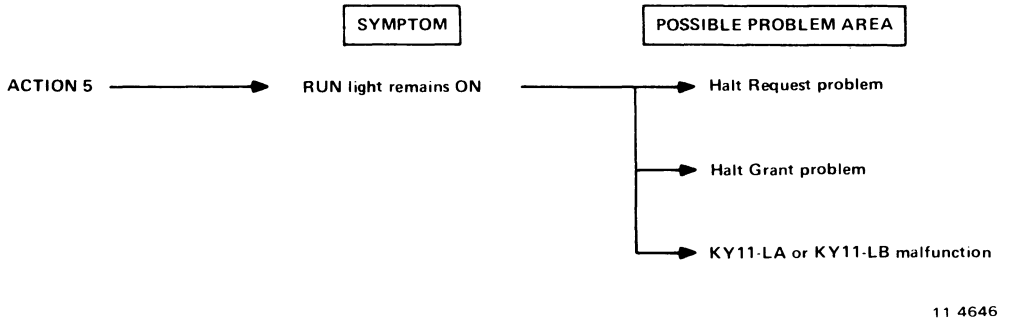


Figure 6-5 Action 5

Action 6	Correct Result
CONTinue processor operation from the halted state.	The RUN light will be on.

If the CONTinue function is implemented and the RUN light does not come on, the console is malfunctioning.

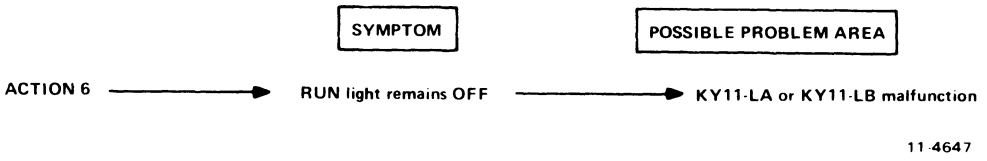


Figure 6-6 Action 6

Action 7	Correct Result
Halt the processor. Initiate the BOOT function. Move the HALT/CONT switch back to CONT (KY11-LA only).	Register printout will be typed on console terminal. The "OLD PC" will be 0.

If the register printout does not result from Action 7, the boot cable (from the console to the M9301) may be faulty or connected improperly.

If the register printout occurs but the wrong "OLD PC" is received, the BOOT/INIT switch may have been pressed twice (KY11-LA only) or there may be noise on the boot cable.

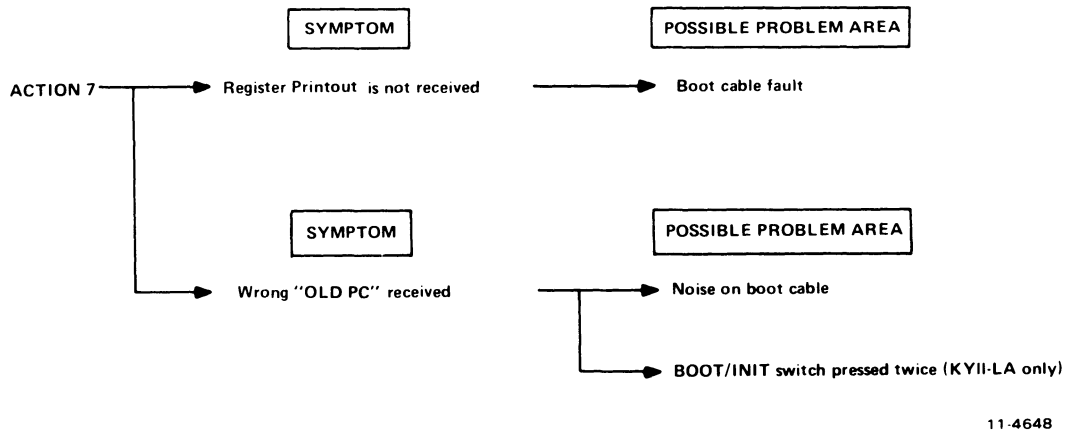


Figure 6-7 Action 7

APPENDIX A
KY11-LB MAINTENANCE MODE OPERATION

A.1 INTRODUCTION

This chapter covers the keypad facilities of the programmer's console available for hardware maintenance of the processor.

A.2 MAINTENANCE MODE KEY OPERATIONS

The following definitions apply to a subset of the same keys used in console mode; however, the functions and operations differ from those in console mode. In general, console mode functions are not available while in maintenance mode, and many keys have no function in maintenance mode.

NOTE

Maintenance mode operation is indicated by the MAINT indicator being on.

In order to use the hardware maintenance features available in maintenance mode, the maintenance cables must be connected between the KY11-LB interface board (M7859) and the processor board (M7266) (Figure A-1). An exception to this is the No. 5 (maintenance mode) operation which is used to allow the console to examine or deposit into memory or device registers without the processor being either present or functional.

NOTE

The maintenance mode is entered by pressing the No. 1 key and the CNTRL key at the same time.

DIS AD (Maintenance Mode) - Used to display Unibus address lines.

1. Press and release the DIS AD key.
2. Unibus address lines will be sampled (read once) and displayed, i.e., display will not be updated as address lines change.

EXAM (Maintenance Mode) - Used to display Unibus Data lines.

1. Press and release the EXAM key
2. Unibus data lines will be sampled and displayed.

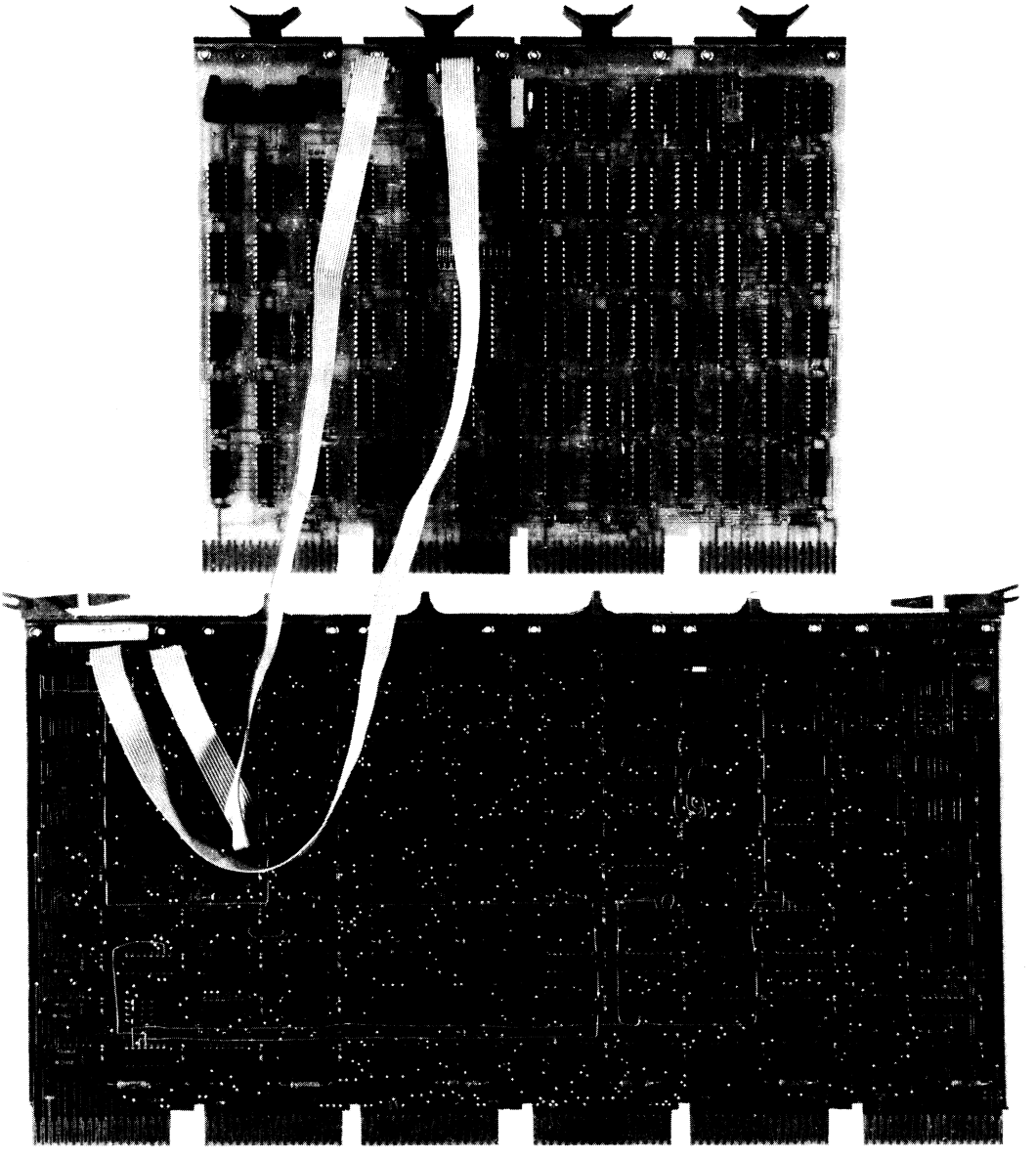


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Figure A-1 KY11-LB Maintenance Cable Connection

HLT/SS (Maintenance Mode) - Asserts MANUAL CLOCK ENABLE and displays MPC (micro-program counter).

1. Press and release HLT/SS key.
2. MANUAL CLOCK ENABLE will be asserted.
3. MPC will be sampled and displayed.

CONT (Maintenance Mode) - Single micro-steps the processor through one micro-state and displays the MPC.

1. Press and release the CONT key.
2. MANUAL CLOCK will be pulsed.
3. New MPC will be sampled and displayed.

BOOT (Maintenance Mode) - Boots the M9301. If MANUAL CLOCK ENABLE is asserted, the M9301 routine will not be entered but because the M9301 simulates a power fail the processor will power up through location 24.

1. Press and release BOOT key.
2. The display is not affected. If MANUAL CLOCK ENABLE is asserted, the MPC is now at the beginning of the power-up sequence. To see the new MPC, use HLT/SS key.

START (Maintenance Mode) - Drops MANUAL CLOCK ENABLE.

1. Press and release START key.
2. MANUAL CLOCK ENABLE is released.
3. Samples and displays MPC.

CLR (Maintenance MODE) - Returns console to console mode operation.

1. Press and release CLR key.
2. MAINT indicator is off.
3. Processor should halt.
4. Program counter should be displayed.

No. 5 (Maintenance Mode) - Allows the console to take control of the Unibus if a processor is not in the system.

1. Press and release the No. 5 key.
2. The MAINT indicator will be off (console mode operation now).
3. Console attempts to read the program counter which is not present and therefore the BUS ERR indicator will be on.

A.3 NOTES ON OPERATION

If the single micro-step feature in maintenance mode is to be used, it is preferable that the processor be halted prior to entering maintenance mode. The assertion of MANUAL CLOCK ENABLE, which turns the processor clock off if it is running, cannot be synchronized with the processor clock. Therefore, if the processor is not halted, the clock may be running and the assertion of MANUAL CLOCK ENABLE may cause an erroneous condition to occur.

In order to single micro-step the processor from the beginning of the power-up sequence, the following steps may be used.

1. Halt the processor if possible.

2. Use CNTRL No. 1 to enter maintenance mode.

3. Use HLT/SS to assert MANUAL CLOCK ENABLE (RUN indicator should come on).

4. Use BOOT to generate a simulated power-fail (will work only if M9301 is present in the system).

5. Use HTL/SS to display the MPC (microprogram counter) for the first micro-step in the power-up routine.

6. Use CONT to single micro-step the processor through the power-up routine. (The new MPC will be displayed at each step.)

7. Unibus address lines and Unibus Data (see the note below) lines may be examined at any micro-step by using DIS AD and EXAM keys respectively. Use of these keys does not advance the microprogram. To redisplay the current MPC without advancing the microprogram, use the HLT/SS key.

8. To return from maintenance mode to console mode, use the CLR key.

9. To single micro-step through a program, the program counter (R7) must first be loaded with the starting address of the program as in signal instruction stepping the processor, prior to entering maintenance mode.

APPENDIX B
EXTENDED ADDRESSING

B.1 INTRODUCTION

This appendix applies to use of the M9301-YA, -YB, and -YF in PDP-11/34 systems which do not have a programmer's console. When the memory of a PDP-11 system is extended beyond 28K, the processor is able to access upper memory through the memory management system. However, the console emulator normally allows the user to access only the lower 28K of memory. This appendix explains how the user can gain access to upper memory in order to read or modify the contents of any location. The reader should be familiar with the concepts of memory management in the KD11-E processor.

B.2 VIRTUAL AND PHYSICAL ADDRESSES

Addresses generated in the processor are called virtual addresses and are 16 bits in length. Physical addresses refer to actual locations in memory. They are asserted on the Unibus and are 18 bits in length.

B.3 ADDRESS MAPPING WITHOUT MEMORY MANAGEMENT

With memory management disabled (as is the case following depression of the boot switch), a simple hardware mapping scheme converts virtual addresses to physical addresses. Vitual addresses in the 0 to 28K range are mapped directly into physical addresses in the range from 0 to 28K. Virtual addresses of the I/O page, in the range from 28K to 32K (160000–177776), are mapped into physical addresses in the range from 124K to 128K.

B.4 ADDRESS MAPPING WITH MEMORY MANAGEMENT

With memory management enabled, a different mapping scheme is used. In this scheme, a relocation constant is added to the virtual address to create a physical or "relocated" address.

Virtual address space consists of eight 4K banks, where each bank can be relocated by the relocation constant associated with that bank. The procedure specified in this section allows the user to:

1. Create a virtual address to type into the Load Address command.

2. Determine the relocation constant required to relocate the calculated virtual address into the desired physical address.

3. Enable or disable the memory management hardware.

B.5 CREATION OF A VIRTUAL ADDRESS

The easiest way to create a virtual address is to divide the 18-bit physical address into two separate fields – a virtual address and a physical bank number. The virtual address is represented by the lower 13 bits, the physical bank by the upper 5 bits. The lower 3 bits of the physical bank number (bits 13, 14, 15) represent the virtual bank number. Thus, if bits 13, 14, and 15 are all zeros, the virtual bank selected is zero. The user should calculate the relocation constant according to Table B-2; then, deposit this constant in the relocation register associated with virtual bank 0 (Table B-1).

One relocation register exists for each of the eight virtual banks. In addition to the relocation registers, each bank has its own descriptor register which provides information regarding the types of access allowed (read only, read or write, or no access).

The memory management logic also provides various forms of protection against unauthorized access. The corresponding descriptor register must be set up along with the relocation register to allow access anywhere within the 4K bank.

B.6 AN EXAMPLE

For example, assume a user wishes to access location 533720. The normal access capability of the console is 0 to 28K. This address (533720) is between the 28K limit and the I/O page (760000–777776) and consequently must be accessed as relocated virtual address with memory management enabled. The virtual address is 13720 in physical bank 25 and is derived as follows.

All locations in bank 25 may be accessed through virtual addresses 000000–017776. The relocation and descriptor registers in the KD11-E are still accessible since their addresses are within the I/O page. Note that access to the I/O page is not automatically relocated with memory management, while access to the I/O page is automatically relocated when memory management is not used.

The relocation constant for physical bank 25 is 005200. This constant is added in the relocation unit to the virtual address, as shown, yielding 533720.

013720	Virtual Address
520000	Relocated Constant (Table B-2)
533720	Physical Address

The Unibus addresses of the relocation registers and the descriptor registers are given in Table B-1. The relocation constant to be loaded into the relocation register for each 4K bank is provided in Table B-2. The data to be loaded in the descriptor register to provide read/write access to the full 4K is always 077406.

The Unibus address of the control register to enable memory management is 177572. This register is loaded with the value 000001 to enable memory management; it is loaded with 0 to disable it.

To complete the example previously described (accessing location 533720), the console routine would be as follows:

```
$L      172340      /Access relocation register for virtual bank 0
$D        5200      /Deposit code for physical bank 25
$L      172356      /Access relocation register for virtual bank 7
$D        7600      /Deposit code for the I/O page
$L      172300      /Access descriptor register, virtual bank 0
$D       77406      /Deposit code for read/write access to 4K
$L      172316      /Access descriptor register virtual bank 7
$D       77406      /Deposit code for read/write access to 4K
$L      177572      /Access control register
$D           1      /Enable memory management
$L       13720      /1  Load virtual address of location desired
$E                  /Examine the data in location 533720
                    /Data will be displayed
```

Table B-1 Unibus Address Assignments

Virtual Address	Virtual Bank	Relocation Register	Descriptor Register
160000–177776	7	172356	172316
140000–157776	6	172354	172314
120000–137776	5	172352	172312
100000–117776	4	172350	172310
060000–077776	3	172346	172306
040000–057776	2	172344	172304
020000–037776	1	172342	172302
000000–017776	0	172340	172300

Table B-2 Relocation Constants

Physical Bank Number	Relocation Constant	Physical Bank Number	Relocation Constant
37	007600	17	003600
36	007400	16	003400
35	007200	15	003200
34	007000	14	003000
33	006600	13	002600
32	006400	12	002400
31	006200	11	002200
30	006000	10	002000
27	005600	7	001600
26	005400	6	001400
25	005200	5	001200
24	005000	4	001000
23	004600	3	000600
22	004400	2	000400
21	004200	1	000200
20	004000	0	000000

Loading a new relocation constant into the relocation register for virtual bank 0 will cause virtual addresses 000000–017776 to access the new physical bank. A second bank can be made accessible by loading the relocation constant and descriptor data into the relocation and descriptor registers for virtual bank 1 and accessing the location through virtual address 020000–037776. Seven banks are accessible in this manner, by loading the proper constants, setting up the descriptor data, and selecting the proper virtual address. Bank 7 (I/O page) must remain relocated to physical bank 37 as it is accessed by the CPU to execute the console emulator routine.

Memory management is disabled by clearing (loading with 0s) the control register 177572. It should always be disabled prior to typing a "boot" command.

The start command automatically disables memory management and the CPU begins executing at the physical address corresponding to the address specified by the previous Load Address command. Depressing the boot switch automatically disables memory management. The contents of the relocation registers are not modified.

The HALT/CONTINUE switch has no effect on memory management.

APPENDIX C
SUMMARY OF
EQUIPMENT SPECIFICATIONS

This table provides mechanical, environmental, and programming information for PDP-11 optional equipment. The equipment is arranged in alphanumeric order by model number.

NOTES

1. Mounting Codes

   CAB = Cabinet mounted. If a cabinet is included with the option, it is indicated by an X in the "Cab Incl" column.

   FS = Free standing unit. Height × Width × Depth dimensions are shown in inches.

   TT = Table top unit.

   PAN = Panel mounted. Front panel height is shown in inches. An included cabinet is indicated when applicable.

   SU = System Unit. SU mounting assembly is included with the option.

   SPC = Small Peripheral Controller. Option is a module that mounts in a quad module, SPC slot.

   MOD = Module. Height is single, double, or quad.

   () = Option mounts in the same space as the equipment shown within the parentheses.

   Some options include 2 separate physical parts and are indicated by use of a plus (+) sign.

2. Cabinet and peripheral equipment (such as magnetic tape) are included in the specifications.

3. Relative humidity specifications mean without condensation.

4. Equipment that can supply current is indicated by parentheses () around the number of amps in the "POWER" columns. *MEMORY POWER:* MF11- and MM11- require the same amount of power. In this table, MF11- power figures show the power required when the memory is active, while MM11- figures reflect that required by an inactive unit.

5. Non-Processor Request devices are indicated by an X in the "NPR" column.

CONVERSION FACTORS

(inches)	× 2.54	=	(cm)
(lbs)	× 0.454	=	(kg)
(Watts)	× 3.41	=	(Btu/hr)
[(°C)×9/5] + 32		=	(°F)

Model Number	Description	MECHANICAL				ENVIRONMENTAL		POWER			PROGRAMMING		UNIBUS			Model Number
		Mounting Code	Size H × W × D (inches)	Cab Incl	Weight (lbs)	Oper Temp (°C)	Rel Humid (%)	Cur needed/(supplied) +5 V (amps)	Cur needed/(supplied) 115 Vac / Other (amps)	Power Dis (W)	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	
AA11-D	D/A Subsystem	SU				10–50	20–95	3	0.5	60	776 756	140,144	4,5		1	AA11-D
AD01-D	A/D Subsystem	PAN	5¼			0–55	10–95		0.5	60	776 770	130	4–7		1	AD01-D
AFC11	A/D Subsystem	CAB				10–55	10–95		15	1700	772 570	134	4		1	AFC11
BA11-ES	Mounting Box	PAN	10½		100											BA11-ES
BA614	D/A Converter	(AA11-D)														BA614
BB11	Blank Mntg Panel	SU														BB11
BB11-A	Blank Mounting Panel (non-slotted blocks)	SU														BB11-A
BC11A	UNIBUS Cable															BC11A
BM792-Y	Bootstrap Loader	SPC						0.3							1	BM792-Y
CB11	Telephone Switching Interface	Cab		X	300	10–50	10–90		5.6	650	764 000	float	4–7		1,2	CB11
CD11-A	Card Reader	SU + TT	14 × 24 × 18		85	10–50	10–90	2.5	4	450	772 460	230	4	X	1	CD11-A
CD11-E	Card Reader	SU + TT	38 × 24 × 38		200	10–50	10–90	2.5	6	700	772 460	230	4	X	1	CD11-E
CM11-F	Card Reader	SPC + TT	11 × 19 × 14		60	10–50	10–90	1.5	4	400	777 160	230	6		1	CM11-F
CR11	Card Reader	SPC + TT	11 × 19 × 14		60	10–50	10–90	1.5	4	400	777 160	230	6		1	CR11
DA11-B	UNIBUS Link	SU						4			772 410	124	5	X	1	DA11-B
DA11-F	UNIBUS Window	SU						5				float	7	X	1	DA11-F
DB11	Bus Repeater	SU				5–50	10–95	3.2							1 + 1	DB11
DC11-A	Asynch Line Inter	SU				10–50	20–90		see Product Bull.		774 000	float	5		1	DC11-A
DD11-A	Periph Mntg Panel	SU														DD11-A
DD11-B	Periph Mntg Panel	SU														DD11-B
DD11-D	Periph Mntg Panel	2 SU														DD11-D
DECkit 01-A	Remote Analog Data Concentrator: 8 Channels, Serial	PAN	5¼ × 19 × 13		15	0–50	10–95		1.5 @ 115 Vac 0.75 @ 230 Vac	175						DECkit 01-A
DECkit 11-F	I/O Interface: 3 Words In/4 Words Out	SU				0–70	10–95	1.84			User	User	7		4	DECkit 11-F
DECkit 11-H	I/O Interface: 4 Words In/4 Words Out	SU				0–70	10–95	3.91			User	User	5–6		4	DECkit 11-H
DECkit 11-K	I/O Interface: 8 Words In	SU				0–70	10–95	1.97			User				2	DECkit 11-K
DECkit 11-M	I/O Interface: Instrumentation Interface	SU				0–70	10–95	1.75			User	User	4		2	DECkit 11-M
DF01-A	Acoustic Coupler	TT	6 × 7 × 12		6	0–60			0.3							DF01-A
DF11	Line Sig Cond	DF slot							see Product Bull.							DF11
DH11	Asynch Line MX	2 SU				5–45	10–95	8.4	0.24 A @ -15 V		float	float	5	X	2	DH11
DJ11	Asynch Line MX	SU						5	see Product Bull.		float	float	5		1	DJ11
DL11-A	Terminal Control	SPC						1.8	0.15 A @ -15 V		777 560	060,064	4		1	DL11-A
DL11 (others)	Asynch Line Inter	SPC						1.8	0.15 A @ -15 V		776 500	float	4		1	DL11 (others)
DL11-W	Asynchronous Interface and Line Clock	SPC	Quad Ht					2	0.05 A @ +15 V 0.15 A @ -15 V	10	Switch Selectable (SS)	A. Int.-SS Line CLK-104	A. Int.-4 Line CLK-6		1	DL11-W
DM11-BB	Modem Ctr. MUX	(DH11)						2.8			775 000	float			1	
DMC-11	Microprocessor and Line Unit	2 SPC	2 Hex Ht					4.5 3					5	X	1	
DN11	Auto Calling Unit	SU				0–40	20–90	1.4	0.10 A @ ± 15 V		775 200	float	4		1	DN11
DP11	Synch Line Inter	SU				0–40	20–90	2.5	0.10 A @ ± 15 V		774 400	float	5		1	DP11
DQ11	DMA Sync Line Interface	SU				10–50	10–90	5.7	0.04 A @ +15 V 0.07 A @ -15 V		float	float	5	X	1	DQ11
DR11-B	DMA Interface	SU				10–50	20–90	3.3			772 410	124	5	X	1	DR11-B
DR11-C	General Interface	SPC				10–50	20–90	1.5			767 770	float	5		1	DR11-C
DT03-F	UNIBUS Switch	PAN	5¼						2			user	7		1 + 1	DT03-F
DX11	IBM Chan. Interface	CAB		X	180	10–55	10–90		2.5	300	776 200	float	4–7	X	1	DX11-B
FP11-A	Floating Point for 11/34A	SPC	Hex Ht			10-50	20-90	7.0							1	FP11-A
GT40	Graphics Terminal	TT	18 × 20 × 24		150	15-35	20-80		15	1500	float	float			1	GT40

Model Number	Description	MECHANICAL				ENVIRONMENTAL		POWER				PROGRAMMING		UNIBUS			Model Number
		Mounting Code	Size (H X W X D) (inches)	Cab Incl	Weight (lbs)	Oper Temp (°C)	Rel Humid (%)	Cur needed/(supplied) +5 V (amps)	115 Vac / Other (amps)		Power Dis (W)	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	
H312-A H720-E H722 H742	Null Modem Power Supply Transformer Power Supply	(BA11) (PC11-A) (H960-D)			30	0–50	20–95	(22)	6 8	(10A) @ -15 V 1.5 A @ 230 Vac (1 A) @ +15 V	700						H312-A H720 H722 H742
H7420 H744 H745 H746	Power Supply +5 V Regulator -15 V Regulator MOS Regulator	(H960-D) (H7420 or H742) (H7420 or H742) (H7420 or H7420						(25) (25)		(10 A) @ -15 V (1.6 A) @ 23.2 V (3.3 A) @ 19.7 V (1.6 A) @ -5 V							H7420 H744 H745 H746
H754	+20, -5 V Regulator	(H742)								(8 A) @ +20 V (1 A) @ -5 V							H754
H933-C	Mounting Panel (H803 blocks)	SU															H933-C
H933-D	Mounting Panel (H808 blocks)	SU															H933-D
H960-C	Cabinet	FS	72 X 21 X 30	X	120												H960-C
H960-D	Cab (1 drawer)	FS	72 X 21 X 30	X	300			(75)	8	(20 A) @ -15 V	900						H960-D
H960-E	Cab (2 drawers)	FS	72 X 21 X 30	X	470			(150)	16	(40 A) @ -15 V	1800						H960-E
H961-A	Cab w/o side pan	FS	72 X 21 X 30	X	120												H961-A
KE11-A	Ext. Arith. Elem.	SU						4				777 300				1	KE11-A
KG11-A	Comm Arith Unit	SPC						1.5				770 700				1	KG11-A
KW11-L	Line Clock	MOD	single ht					0.8				777 546	100	6		1	KW11-L
KW11-P	Programmable Clock	SPC						1				772 540	104	6		1	KW11-P
LA30	DECwriter	FS	31 X 21 X 24		110	15–35	20–80		3		300						LA30
LC11-A	LA30 Control	SPC						1.5				777 560	060,064	4		1	LC11-A
LP11-F	Printer (80 col)	SPC + FS	46 X 24 X 22		200	10–43	15–80	1.5	2		250	777 514	200	4		1	LP11-F
LP11-J	Printer (132 col)	SPC + FS	46 X 48 X 25		575	10–43	15–80	1.5	4		500	777 514	200	4		1	LP11-J
LP11-R	Ptr (heavy duty)	SPC + FS	48 X 49 X 36		800	10–43	15–80	1.5	17		2000	777 514	200	4		1	LP11-R
LPS11	Lab Periph System	PAN	5¼		80	5–43	20–80		3		300	float	float	4–6	opt	2	LPS11-S
LS11	Line Printer	SPC + TT	12 X 28 X 20		155	5–38	5–90	1.5	3		300	777 514	200	4		1	LS11
LT33	Teletype	FS	34 X 22 X 19		60	15–35	20–80		2		200						LT33
LV11	Electrostatic Ptr	SPC + FS	38 X 19 X 18		160	10–43	20–80	1.5	5		600	777 514	200	4		1	LV11
M105	Adrs Select Module	MOD	single ht					0.34									M105
M783	Bus Transmitter	MOD	single ht					0.2									M783
M784	Bus Receiver	MOD	single ht					0.2									M784
M785	Bus Transceiver	MOD	single ht					0.3									M785
M792	Diode ROM	SPC						0.23				773 000				1	M792
M795	Word Count	MOD															M795
M796	Bus Control	MOD															M796
M920	Bus Jumper	MOD															M920
M930	Bus Terminator	MOD	double ht					1.25									M930
M1501	Bus Input Interface	MOD	single ht			0–70	10–95	0.3									M1501
M1502	Bus Output Interface	MOD	double ht			0–70	10–95	0.75									M1502
M1621	DVM Data Input Interface	MOD	quad ht			0–70	10–95	0.78									M1621
M1623	Instrument Remote Control Interface	MOD	quad ht			0–70	10–95	1.6									M1623
M1710	Unibus Interface Foundation	MOD & SPC	quad ht			0–70	10–95	0.79							opt		M1710
M1801	16-Bit Relay Output Interface	MOD	quad ht			0–70	10–95	1.46									M1801

Model Number	Description	MECHANICAL				ENVIRONMENTAL		POWER			PROGRAMMING		UNIBUS			Model Number
		~~Mounting~~ Code	Size (H X W X D) (inches)	Cab Incl	Weight (lbs)	Oper Temp (°C)	Rel Humid (%)	Cur needed/(supplied) +5 V (amps)	115 Vac / Other (amps)	Power Dis (W)	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	
M7820	Interrupt Control	MOD	single ht													M7820
M7821	Interrupt Control	MOD	single ht													M7821
M9301(-YA), (-YB), (-YD)	Bootstrap Terminator	Unibus Slot	Double Ht					2							1	M9301(-YA), (-YB), (-YD)
ME11-L	Core Memory (8K)	PAN	5¼			0–50	10–90		5	125					1	ME11-L
MF11-L	Core Memory (8K)	2 SU				0–50	10–90	3.4	6 A @ -15 V	125					1	MF11-L
MF11-LP	Parity Memory (8K)	2 SU				0–50	10–90	4.9	6 A @ -15 V	125					2	MF11-LP
MF11-U	Core Memory (16K)	2 SU				0–50	0–90	4.5	3.5 A @ 20 V 0.5 A @ -5 V	120					1	MF11-U
MF11-UP	Parity Memory (16K)	2 SU				0–50	0–90	6	3.4 A @ 20 V 0.5 A @ -5 V	120					2	MF11-UP
MM11-L	Core Memory (8K)	(MF11-L)				0–50	10–90	1.7	0.5 A @ -15 V	125					1	MM11-L
MM11-LP	Parity Memory (8K)	(MF11-LP)				0–50	10–90	1.7	0.5 A @ -15 V	125					1	MM11-LP
MM11-U								4.5	0.5 A @ 20 V 0.5 A @ -5 V							MM11-U
MM11-UP	Parity Memory (16K)	(MF11-UP)				0–50	0–90	4.5	0.5 A @ 20V 0.5 A @ -5 V							MM11-UP
MR11-DB	Bootstrap	2 SPC						0.6							2	MR11-DB
MS11	Semiconductor Mem	(11/45)				0–50	10–80				772 100	114			1	MS11
PC11	Paper Tape	SPC + PAN	10½		50	13–38	20–95	1.5	3	350	777 550	070,074	4		1	PC11
PDM70	Programmable Data Mover	TT	5¼ X 19 X 23	X	55	0–40	10–95		115 Vac 230 Vac	250 250						PDM70
PR11	Paper Tape (rdr)	SPC + PAN	10½		50	13–38	20–95	1.5	3	350	777 550	070	4		1	PR11
RC11-A	Disk & Control	PAN	10½		115	17–50	20–80		2.2	250	777 440	210	5	X	1	RC11-A
RF11-A	Disk & Control	PAN + PAN	16 + 16	X	500	17–33	20–55		6.5	750	777 460	204	5	X	1	RF11-A
RK05	Disk Drive	PAN	10½		110	15–43	20–80		2	160						RK05
RK11-D	Disk & Control	SU + PAN	10½	X	250	15–43	20–80	7.5	2	200	777 400	220	5	X	1	RK11-D
RP03	Disk Drive	FS	40 X 30 X 24		415	15–33	10–80		6 A @ 230 Vac	1300						RP03
RP11-C	Disk & Control	CAB + FS		X	740	15–33	10–80		7 6 A @ 230 Vac	2100	776 710	254	5	X	1	RP11-C
RS11	Disk Drive	PAN	16		100	17–33	20–55		2	200						RS11
RS64	Disk	PAN	10½		65	17–50	20–80		2.2	250						RS64
RT01	Numeric Data Entry Terminal	TT	6.5 X 12.5 X 15	X	12	0–40	10–90		0.25 @ 115 Vac 0.12 @ 220 Vac	30						RT01
RT02	Alphanumeric Data Entry Terminal	TT	6.3 X 14.4 X 16	X	14	0–40	10–90		110 Vac 220 Vac	50 50						RT02
TA11	Cassette	SPC + PAN	5¼			10–40	20–80	1.5	1	120	777 500	260	6		1	TA11
TC11-G	DECtape & Control	PAN + PAN	10½ + 10½	X	250	15–27	40–60		9	870	777 340	214	6	X	1	TC11-G
TM11	Magtape & Control	PAN + PAN	26 + 10½	X	500	15–27	40–60		9	1000	772 520	224	5	X	1	TM11
TU10	Magtape Transport	PAN	26	X	450	15–27	40–60		9	1000						TU10
TU56	DECtape Transport	PAN	10½		80	15–27	40–60		3	350						TU56
UDC11	I/O Subsystem	CAB				5–50	10–90		15	1700	771 774	234	4,6		2	UDC11
VR01	Display	PAN	10½		30	10–50	10–90		1	120						VR01
VR14	Display	PAN	10½		75	10–50	10–90		4	400						VR14
VT01	Display	TT	12 X 12 X 23		50	0–50	10–80		2.2	250						VT01
VT05	Alphanum Terminal	TT	12 X 19 X 30		55	10–43	8–90		2	130						VT05

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EK-11034-UG-001

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