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KW11-K
dual programmable real time clock user manual

digital

EK-KW11-K-OP-001

KW11-K
dual programmable
real time clock
user manual

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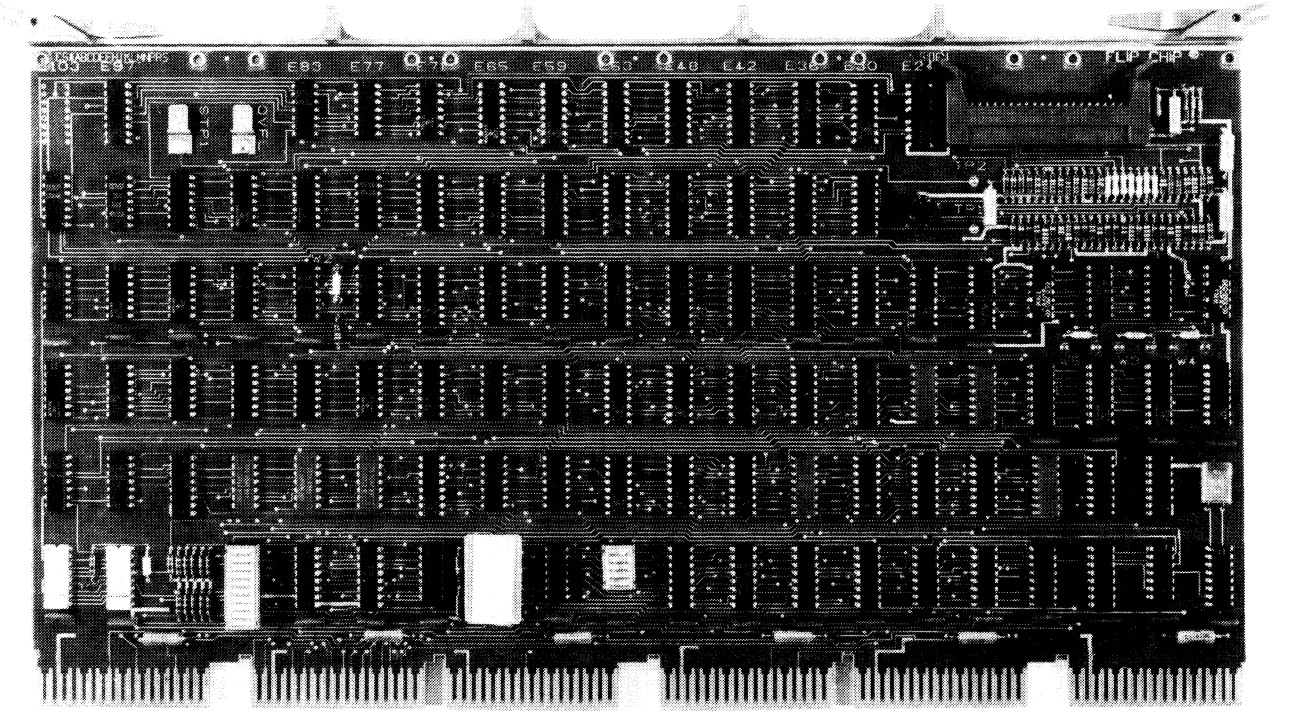

M7025 Module

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The KW11-K is a dual programmable real-time clock option used in PDP-11 Unibus computers. The clock features include:

Clock A

- 16-bit counter
- 16-bit programmable Preset/Buffer register
- Four modes of operation
- Two external inputs (Schmitt trigger)
- Eight clock rates, program selectable
- Five clock frequencies, crystal controlled for accuracy
- Synchronous to external events of processor actions
- Program-compatible with LPSKW

Clock B

- 8-bit counter
- 8-bit programmable preset register
- Repeated interval mode of operation
- One external input (Schmitt trigger)
- Seven clock rates, program selectable
- Five clock frequencies, crystal controlled for accuracy

1.2 GENERAL DESCRIPTION

Clock A is a 16-bit programmable real-time clock, which can accurately measure and count intervals of time and events. It can be used for processor synchronization to external events; generate events, such as an A/D conversion at programmed intervals; and generate events synchronized to an external event input. Clock A is controlled by the A Status Register which consists of enables, flags, and mode and rate selections.

Clock A operates in one of four programmable modes: Single interval, repeated interval, external event timing, and external event timing from zero base. Clock A can be program selected to operate at one of eight clock rates. The clock can operate from one of five crystal-controlled frequencies (1 MHz, 100 kHz, 10 kHz, 1 kHz and 100 Hz), an external (Schmitt Trigger One) input, line frequency or the overflow of Clock B (allowing a further dimension in Clock A input frequency selections).

Clock B is an 8-bit programmable real-time clock which can accurately time intervals or events. It can be used for generating interrupts at programmed intervals, for generating events (such as an A/D conversion) at programmed intervals, or to provide an input frequency to Clock A. Clock B is controlled by the B Status register which consists of flags, enables and rate selection. Clock B operates in one mode: repeated interval mode. Clock B can be program selected to operate at one of seven clock rates, one of five crystal-controlled frequencies (1 MHz, 100 kHz, 10 kHz, 1 kHz and 100 Hz), line frequency or external (Schmitt Trigger Three) input. An eighth selection is used as a stop frequency.

The KW11-K has three Schmitt trigger inputs which have threshold and slope control.

The KW11-K, when used in conjunction with an A/D converter which provides for an external A/D start, has the ability to perform sampling on a high frequency repetitive analog signal at effective rates as high as 1 MHz. A block diagram of the KW11-K is shown in Figure 1-1.

1.3 PHYSICAL DESCRIPTION

The KW11-K is packaged on a single M7025 hex module designed for use in one of the center SPC slots of a DD11-B or DD11-D.

1.4 POWER REQUIREMENTS

The KW11-K uses +5 Vdc at 3 A (max).

1.5 UNIBUS LOADING

All Unibus lines are one load except for data lines 02 through 08, which are two Unibus loads.

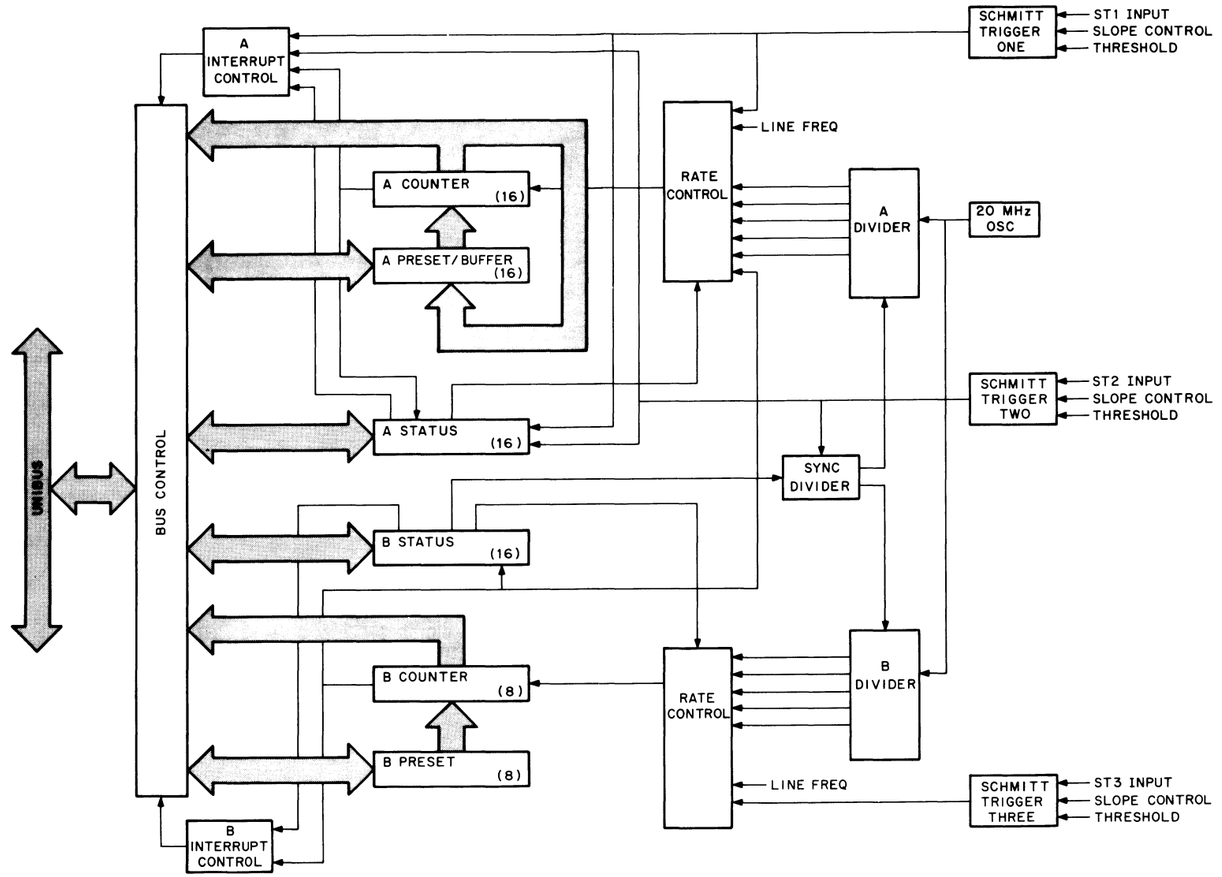

Figure 1-1 KW11-K Basic Block Diagram

CHAPTER 2
THEORY OF OPERATION

2.1 CLOCK A

2.1.1 Counter A Register

Clock Counter A is a 16-bit programmable up counter. Data is loaded into the register from the A Preset/Buffer register. Clock A can synchronize to the processor which allows the user to read Counter A while Clock A is in operation. Counter A has an overflow which occurs when the count sequence goes from all 1s to all 0s. This overflow is used for various functions (Paragraph 2.1.6), such as reloading the counter with the contents of the A Preset/Buffer. Whenever the A Preset/Buffer is loaded and Clock A is disabled (Counter A not running), the new A Preset/Buffer data is also loaded into Counter A. Since the counter is an up-counter, 2s complement preset values must be used.

2.1.2 A Preset/Buffer Register

The A Preset/Buffer Register is a 16-bit register. It is used to hold Counter A's preset value during modes 0 or 1. Each time Counter A Overflow occurs in these modes, Counter A is reloaded with the contents of the A Preset/Buffer. The A Preset/Buffer is used as a buffer for Counter A in modes 2 or 3. When Schmitt Trigger Two occurs in these modes, the contents of Counter A is loaded into the A Preset/Buffer Register.

When using Auto-Increment, the A Preset/Buffer contents (which is in 2s complement binary) is decremented each time a Clock A Overflow occurs, so that the subsequent interval is one count longer than the completed interval, (Paragraph 2.5).

2.1.3 A Status Register

The A Status Register is a 16-bit register used to the control Clock A. It consists of flags, enables, and mode and rate selections (Paragraph 3.3.1).

2.1.4 Modes of Operation

Clock A has four modes of operations which are controlled by the A Status Register. Figure 2-1 illustrates these modes in flow diagram form.

Mode 0 is Single Interval Mode. When Clock A is enabled to count (status bit 0), Counter A will count from the preset value to overflow and stop. The overflow can be used to generate an interrupt to the processor and can generate an external event.

Mode 1 is Repeated Interval Mode. When Clock A is enabled to count, Counter A will count from the preset value to overflow. Overflow will reload Counter A with the contents of the A Preset/Buffer Register and continue counting. The overflow can be used to generate an interrupt to the processor and generate an external event.

Mode 2 is External Event Timing Mode. When Clock A is counting, and if a Schmitt Trigger Two (ST2) event occurs, the contents of Counter A at the time of ST2 is loaded into the A Preset/Buffer Register. The counter continues to count and does not stop until the Clock A Counter enable (status bit 0) is clear.

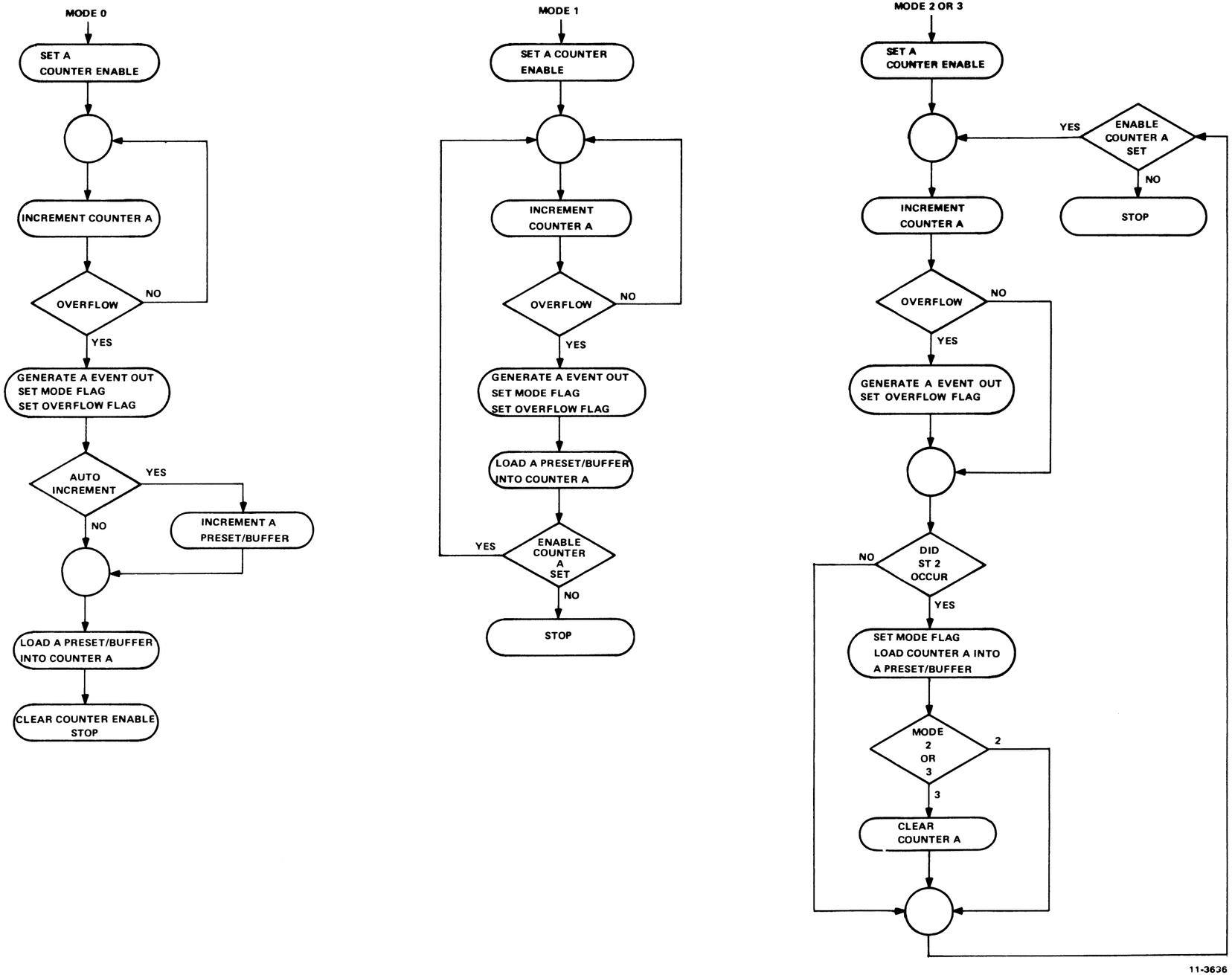

Figure 2-1 Clock A Mode Flow Diagram

A Overflow can generate an interrupt to the processor.

Mode 3 is External Event Timing from zero base mode. This mode is similar to mode 2 except when the ST2 event occurs, the counter is cleared to all zeros after it is loaded into the A Preset/Buffer.

2.1.5 Clock A Interrupts

There are two ways to generate interrupts. First, if the Mode Flag Interrupt Enable is set (A status bit 06), an interrupt will be generated if an A Overflow occurs in modes 0 or 1 or if an ST2 event occurs in modes 2 or 3. A Overflow can generate interrupts in modes 2 or 3 if jumper W2 is in place on the M7025 module. Second, if the ST1 Interrupt Enable is set (A status bit 14), an interrupt is generated if Schmitt Trigger One (ST1) event occurs.

2.1.6 Clock A Overflow

Clock A Overflow is the carry output of Counter A. It occurs when the counter's count sequence goes from all 1s to all 0s. In modes 0 or 1 the A Overflow is used to load the contents of the A Preset/Buffer Register into Counter A and is used to set the Mode Flag (A status bit 07). If jumper W2 is in place on the M7025 module, A Overflow will set the A Overflow Flag and generate an interrupt if the Mode Flag Interrupt Enable is set. If jumper W2 is removed, the KW11-K overflow logic becomes compatible with the LPSKW.

A Overflow is available on the H854 I/O connector and on a FAST-ON TAB for external use. The A Overflow is renamed A Event Out and can be used to start external events, such as an A/D conversion. The FAST-ON TAB can be used for internal computer connection to the AD11-K option.

2.1.7 Mode Flag

The Mode Flag (status bit 07) is used to signify that certain events occured within the KW11-K. In mode 0 or 1, this flag sets when an A Overflow occurs. In mode 2 or 3, this flag sets when Schmitt Trigger Two (ST2) event occurs. Setting the Mode Flag generates an interrupt to the processor if the Mode Flag Interrupt Enable is set (A status bit 06).

2.1.8 Clock A Rate Selection

Clock A can be selected by the A Status Register to operate in one of eight rates; one of five crystal-controlled frequencies (1 MHz, 100 kHz, 10 kHz, 1 kHz and 100 Hz), an external frequency (Schmitt Trigger One), line frequency or Clock B's Overflow rate. If the Feed B to A is set, Clock B's Overflow is used as a clock rate. If the Feed B to A is not set, the rate line is used as a stop rate.

2.2 CLOCK B

2.2.1 Clock Counter B

Clock Counter B is an 8-bit programmable up counter. Data is loaded into this counter from the B Preset Register. The counter can be read only if Clock B is enabled (B status bit 00) and rate 0 is selected.

Counter B has an overflow which occurs when the count sequence goes from all 1s to all 0s. This overflow is used for various functions (Paragraph 2.2.4) such as reloading the contents of B Preset Register into Counter B.

2.2.2 B Preset Register

Clock B Preset is an 8-bit register used to hold Counter B's preset value. Each time a B Overflow occurs, the contents of the B Preset is loaded into Counter B.

2.2.3 B Status Register

The B Status Register is a 16-bit register used to control Clock B. It consists of flags, enables, rate selection and maintenance (Paragraph 3.3.1).

2.2.4 Clock B Overflow

B Overflow is the carry output of Counter B and occurs when Counter B's count sequence goes from all 1s to all 0s. If the Interrupt Enable is set (B status bit 06), the overflow generates an interrupt to the processor. B Overflow sets the B Overflow Flag (B status bit 07) and is available on the I/O connector (B Event Output) for starting external events.

2.2.5 Clock B Rate Selection

Clock B can be selected by the B Status Register to operate in one of seven rates; one of five crystal-controlled frequencies (1 MHz, 100 kHz, 10 kHz, 1 kHz and 100 Hz), an external frequency (Schmitt Trigger Three), or line frequency. An eighth rate selection is provided as a stop frequency.

2.3 CRYSTAL-CONTROLLED OSCILLATOR

A 20 MHz (±0.01%) crystal-controlled oscillator is used in both Clock A and B. Divider networks in each clock generate 1 MHz, 100 kHz, 10 kHz, 1 kHz and 100 Hz. Clock A's divider network can synchronize to Schmitt Trigger One if the Auto-Increment bit (B status bit 04) is set. Clock B's divider network can synchronize to Schmitt Trigger One if both Auto-Increment and Feed B to A (B status bit 05) bits are set.

The 20 MHz is also used to generate timing pulses to synchronize Clock A to external events and processor operations. Clock B becomes synchronous if operating in both Auto-Increment and Feed B to A modes of operation.

2.4 FEED B TO A MODE

When Feed B to A (B status bit 05) is set and Clock A is selected for rate 0, the overflow of Counter B is used as a clock rate for Clock A. If the Feed B to A is not set, Clock A's rate 0 can be used as a stop function. Clock A should not be operating when changing to or from this mode of operation.

This operation allows Clock A to have more programmable frequencies by selecting the appropriate rate and preset value for Clock B. For example:

If the B Counter preset value is set for a count of 2 and a clock rate of 100 kHz (rate selection 2), the B Overflow will occur at a frequency of 50 kHz. Thus, if the Feed B to A mode is set and Clock A is set up for a rate selection of 0, Counter A will be incremented at 50 kHz (Figure 2-2).

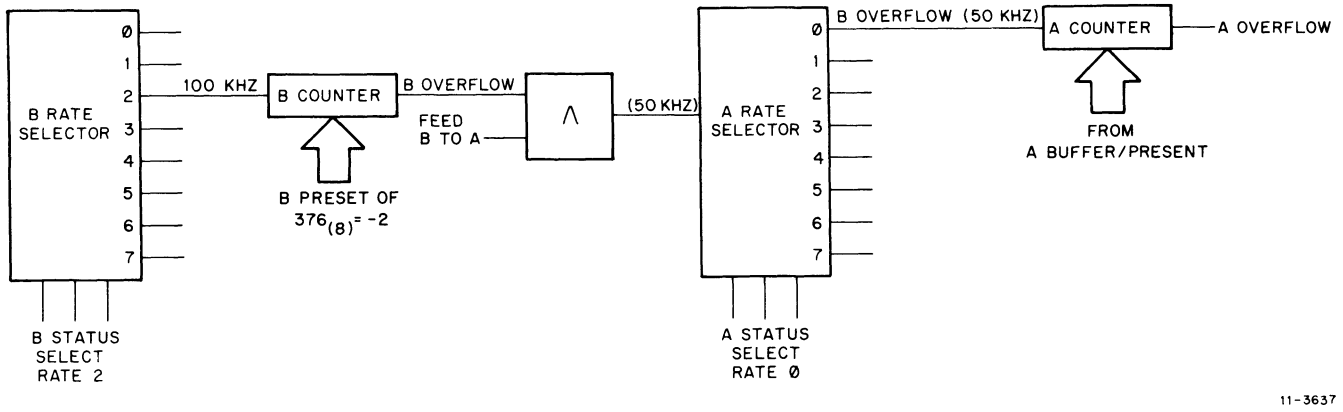

Figure 2-2 Feed B to A Block Diagram

2.5 AUTO-INCREMENTING

When the Auto-Increment bit of the B Status Register (bit 04) is set, A Overflow will decrement the contents of the A Preset/Buffer which is in 2s compliment binary. A Auto-Increment operates only in mode 0 (Single Interval mode). In mode 0, when Clock A is enabled (A status bit 00), the A Counter counts from a preset value to overflow and stops. The A Overflow decrements the A Preset/Buffer and reloads Counter A with the new A Preset/Buffer value. When Counter A is re-enabled, the overflow will occur one clock pulse later than the previous overflow, thus increasing the Single Interval.

This mode of operation is exemplified in conjunction with an A/D converter sampling a high-frequency repetitive waveform to achieve a high effective sampling rate (up to 1 MHz). By allowing Clock A to start counting on an ST1 event, initially setting up the A Preset/Buffer for a count of -1 for 1 MHz sampling, and selecting mode 0 and rate 1 (1 MHz), each A Overflow will occur 1 μsec further into the repetitive waveform synchronous to the ST1 event (Figure 2-3). The A/D converter uses A Overflow to initiate a conversion.

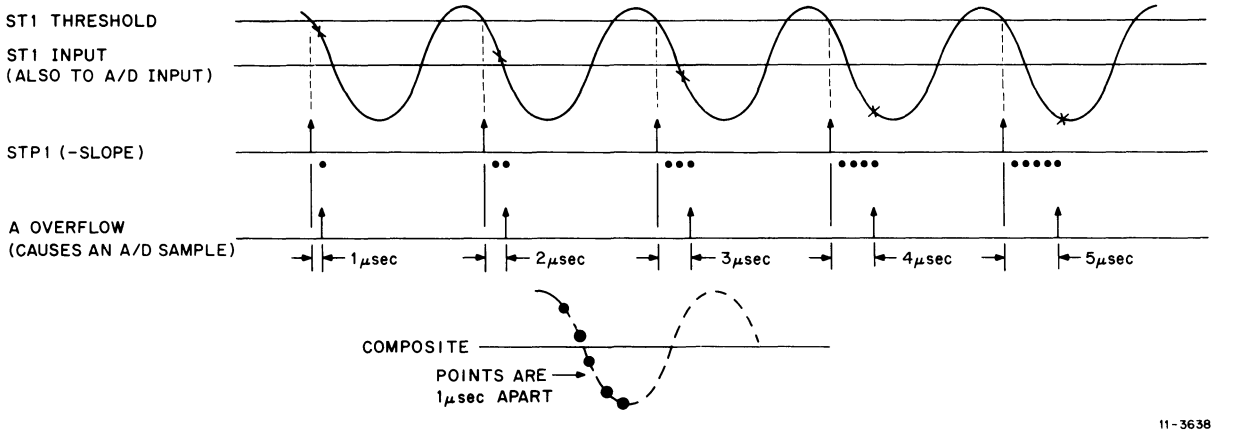

Figure 2-3 Using Auto-Incrementing to Sample Repetitive High Frequency Waveform in A/D Converter Application

2.6 SCHMITT TRIGGERS (ST1, ST2, AND ST3)

ST1 is used to start Clock A's counter if ST1 enable Clock A (A status bit 13) is set; is used as a counting function if Clock A rate 6 is selected; is used to set ST1 flag; and is used to generate an interrupt if the ST1 Interrupt Enable (A status bit 14) is set. ST1 is synchronized to internal clock timing to within ±1 μsec and re-designated STP1. If used in the Auto-Increment mode of operation, ST1 is synchronized to within 50 nsec. A non-synchronized ST1 is available at the H854 I/O connector and at a "FAST-ON" TAB. The TAB can be used for internal computer connection to the AD11-K (12-bit analog-to digital-converter).

ST2 is used by Clock A in modes 2 and 3 for clocking the contents of Counter A into the A Preset/Buffer and setting the Mode Flag (A status bit 07). ST2 is synchronized to internal clock timing to within 1 μsec and re-designated STP2. STP2 is available at the H854 I/O connector.

ST3 is used by Clock B as a clocking function if Clock B rate 6 is selected. ST3 is available at the H854 I/O connector.

All three Schmitt Triggers have an input operating range up to ±15 V, are operational up to 1 MHz, and have threshold control, slope selection, 110 K input impedance and 0.5 V (±0.2 V) of input hysteresis. Each of the Schmitt Trigger output lines can drive 50 mA and source 10 mA at +3 V. Input voltage should not exceed ±50 V. The Schmitt Trigger input circuitry is shown in Figure 2-4. The Schmitt Triggers have a solder jumper (Paragraph 2.9) on their inputs which allows TTL inputting (0 to +5 V). Protection is provided to ±10 V. A fuseable resistor will open if the input voltage exceeds ±10 V (Figure 2-4).

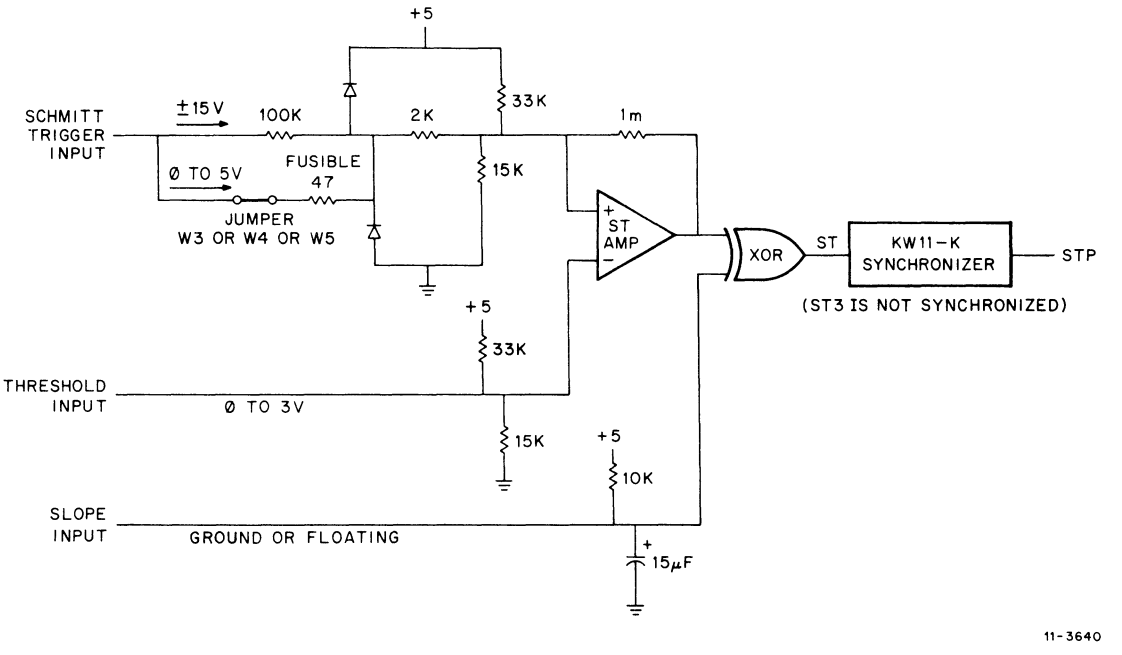

Figure 2-4 Schmitt Trigger Circuitry

2.7 THRESHOLD CONTROL

ST1, ST2, and ST3 have threshold control over an input range of ±15 V. The threshold line of each should range from 0 to +3 V and must not exceed +3 V. A threshold voltage source (+3 V at 5 mA max) is available and should be used as shown in Figure 2-5. Figure 2-6 shows the relationship between input voltage to the input threshold voltage.

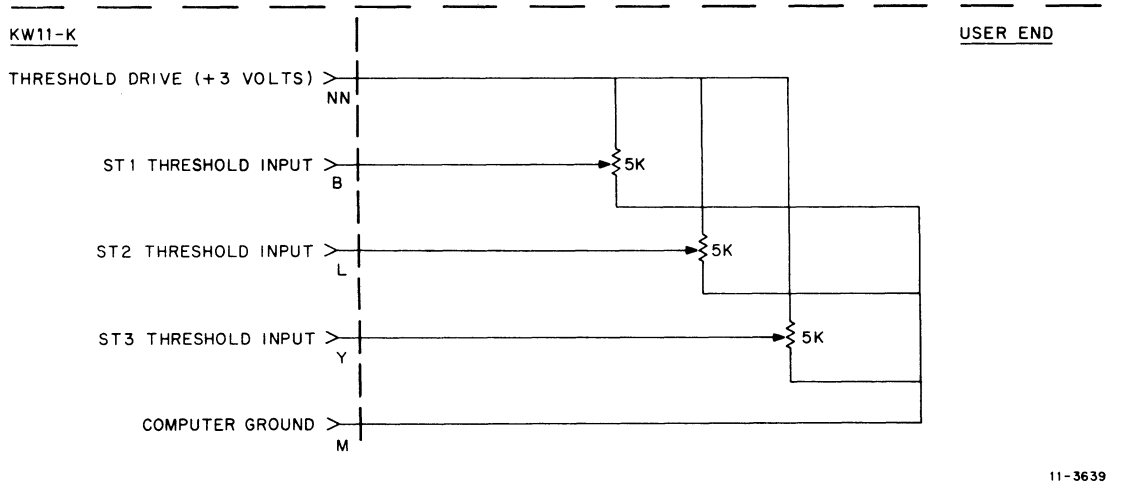

Figure 2-5 Threshold Control

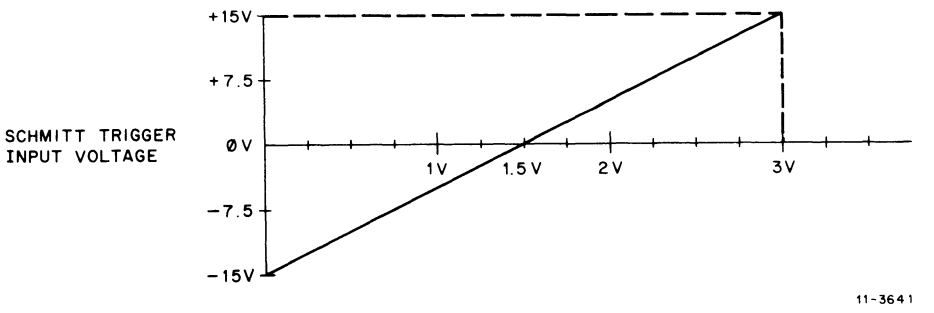

Figure 2-6 Input and Threshold Input Voltage Relationship

2.8 SLOPE CONTROL

ST1, ST2 and ST3 have slope control. If the respective slope line is grounded, the Schmitt Trigger pulse will occur on the positive slope of the input signal, depending on threshold setting (Figure 2-7). If the respective slope line is left open (floating), the Schmitt Trigger pulse will occur on the negative slope of the input signal, depending on the threshold setting, (Figure 2-7). Figure 2-8 shows a method for controlling the slope lines.

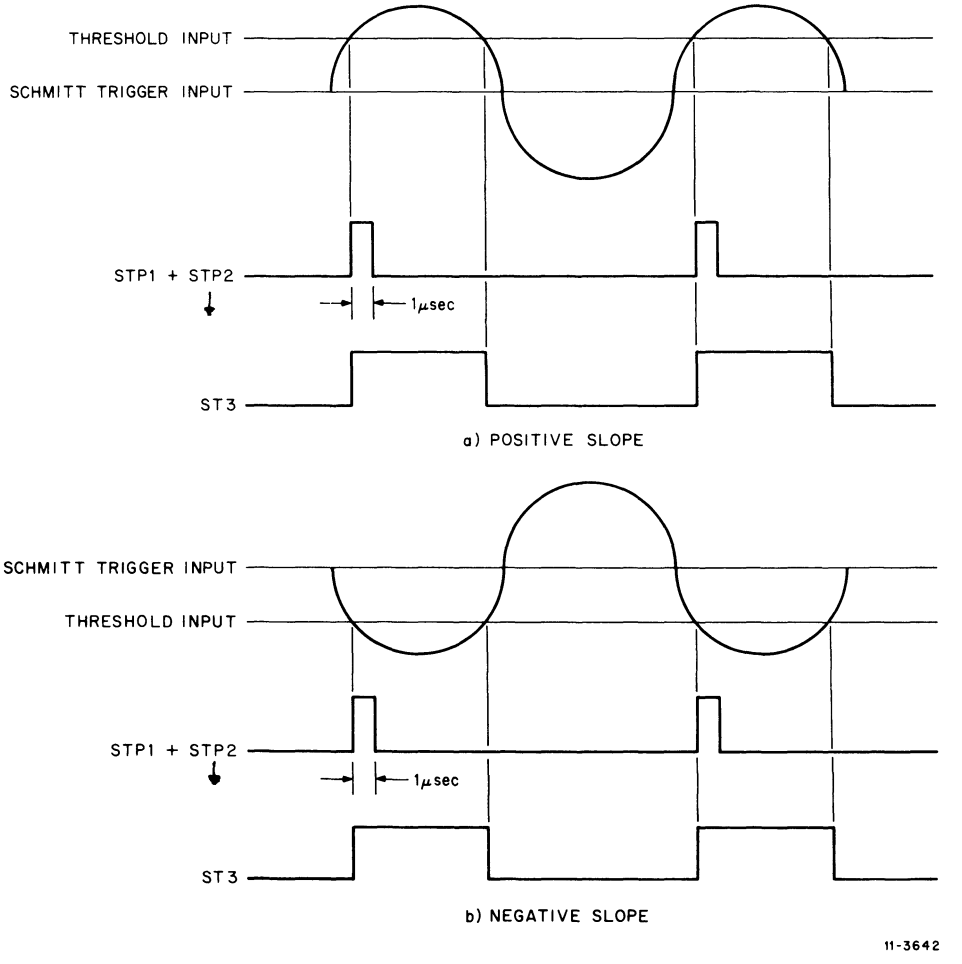

Figure 2-7 Schmitt Trigger Slope Relationship

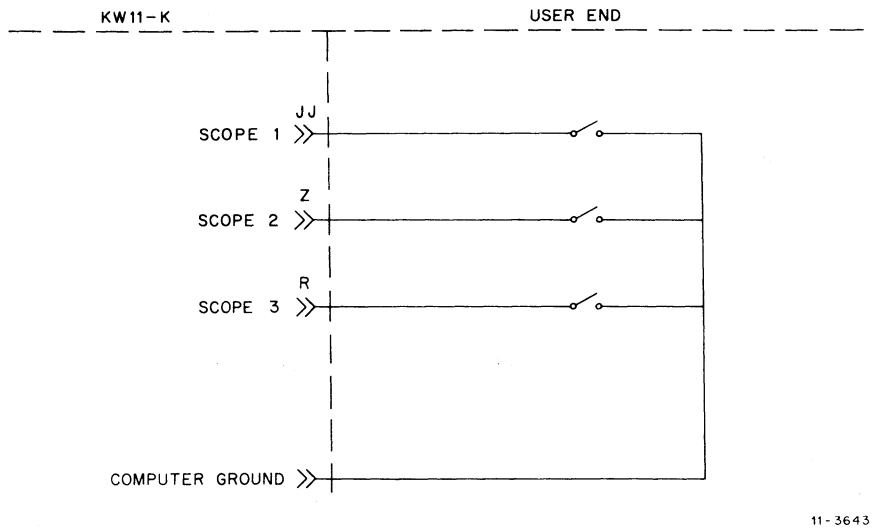

Figure 2-8 Scope Line Control

2.9 SWITCHES, JUMPERS AND CABLING

Single pole/single throw switches in switch packs are used to change the register and vector addressing of the KW11-K (Paragraph 3.1). The switch identifications for the address lines and vector lines are listed in Tables 2-1, 2-2 and in Figure 2-9. Register address lines are switched ON for a logical 0; vector address lines are switched ON for a logical 1.

On the M7025 there are solder jumpers which are used to select various functions. These functions are described in Table 2-3. The locations of these jumpers on the M7025 module are shown in Figure 2-9.

An H854, 40-pin I/O connector located on the top right of the M7025 module, is used for inputting and outputting signals. H854 pin designations are listed in Table 2-4. This I/O connector accepts a BC08R type cable or equivalent cable with an H856 connector. With a BC08R cable, the KW11-K can be connected to an H322 screw terminal distribution panel (Figure 2-10).

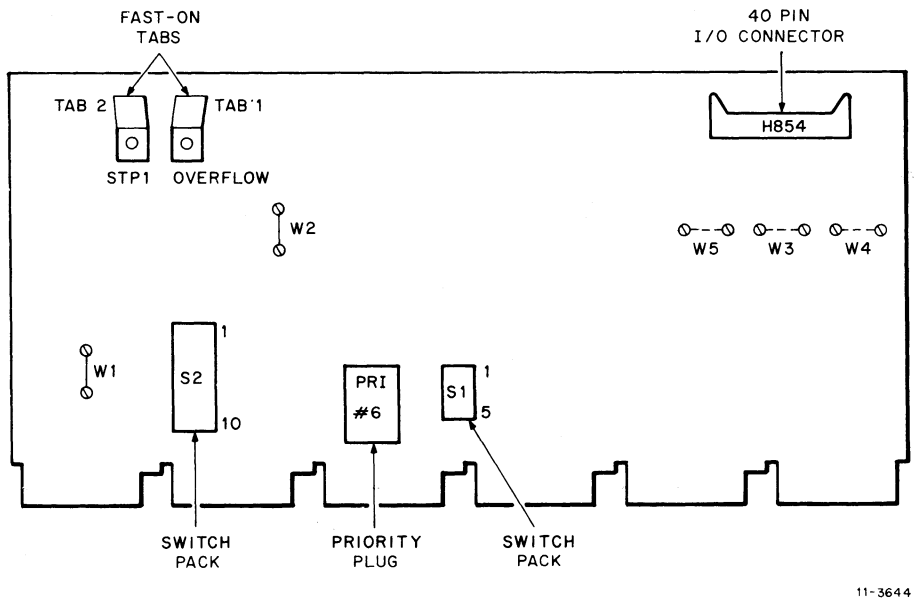

Figure 2-9 M7025 Module Component Locations

Table 2-1
Address Line Selection

Address Line	Switch Identification
A15	Not selectable
A14	Not selectable
A13	Not selectable
A12	S2–1
A11	S2–2
A10	S2–3
A09	S2–4
A08	S2–5
A07	S2–6
A06	S2–7
A05	S2-8
A04	S2–9
A03	Not selectable
A02	Not selectable
A01	Not selectable
A00	Not selectable

Table 2-2
Vector Line Selection

Vector Lines	Switch Identification
D03	S1–5
D05	S1–4
D06	S1–3
D07	S1–2
D08	S1–1

Table 2-3
M7025 Jumper Usage

Jumper Identification	Standard Placement	Description
W1	IN	NPR-Remove only if PDP-11/20 or 11/15 without a KH11 option.
W2	IN	This jumper allows A Overflow to generate interrupts in all modes and to set A Overflow flag. Remove for complete LPS11 Compatability.
W3	OUT	This jumper, if in place, allows ST1 to accept TTL inputs.
W4	OUT	This jumper, if in place, allows ST2 to accept TTL inputs.
W5	OUT	This jumper, if in place, allows ST3 to accept TTL inputs.

Table 2-4
H854 Pin

H854 Pin	Signal Name
D	Initialize output
L	ST3 output
N	Threshold 3 input
R	Slope 3 input
T	Schmitt Trigger 3 input
V	STP2 output
X	Threshold 2 input
Z	Slope 2 input
BB	Schmitt Trigger 2 input
DD	STP1 input
FF	Threshold 1 input
JJ	Slope 1 input
LL	Schmitt Trigger 1 input
NN	Pot drive
RR	Line frequency output
TT	B Event output
VV	A Event output
A, C, E, H, K, M, P, S, U W, Y, AA, CC, EE, HH KK, MM, PP, SS, UU	Computer Ground

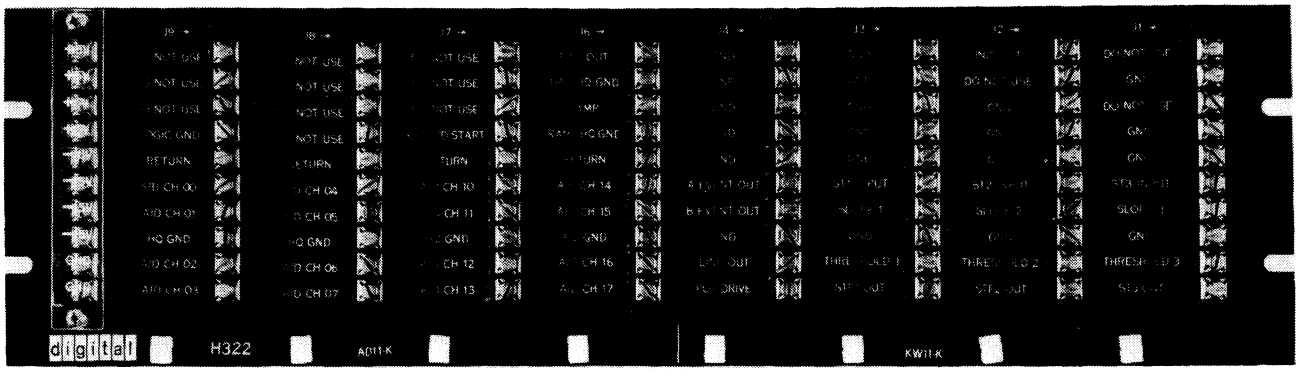

Figure 2-10 H322 Distribution Panel

CHAPTER 3
PROGRAMMING

3.1 REGISTER AND VECTOR ADDRESSING

Register and vector addresses are configured prior to shipment to a standard configuration, but may be changed by means of switches on the M7025 module. Paragraph 2.9 describes the procedure for changing the register and vector addresses.

The KW11-K has a floating address to allow the use of more than one KW11-K in a system or to avoid any device address conflicts with other options. The register address is selected by switches on the M7025 module representing address lines A12 through A05. The standard register addresses selected for the KW11-K are:

Clock A:		
A Status Register	R/W	770404
A Buffer Register	R/W	770406
A Counter Register	Read only	770430
Clock B:		
B Status Register	R/W	770432
B Buffer Register	R/W	770434
B Counter Register	Read only	770436

The vector address is selected by switches on the M7025 module representing vector lines (Unibus D lines) D08 through D03. The standard vector address for Clock A is 344_8 and for Clock B is 364_8.

3.2 PRIORITY LEVEL

The M7025 is normally shipped with priority level configuration BR6; this level may be changed by replacing the jumper module to that of another level.

3.3 REGISTERS

3.3.1 A and B Status Registers

The Status Registers are illustrated in Figure 3-1 and described in Tables 3-1 and 3-2.

3.3.2 A and B Counters

The A Counter is a 16-bit (word-oriented) counter and is illustrated in Figure 3-2. This counter is a read only register and can be read while in operation.

The B Counter is an 8-bit (low byte) counter and is illustrated in Figure 3-3. This counter is a read only register and can be read only when the counter is not enabled. If operating in Feed B to A and Auto-Increment, the B Counter can be read while operating.

Table 3-1
A Status Register Bit Descriptions

Function	Bit	Description
ST1 Flag	15	This flag sets when a Schmitt Trigger one (ST1) event or a maintenance ST1 has occurred.
ST1 Interrupt Enable	14	This status bit enables an interrupt to be generated if an ST1 event has occurred.
ST1 Enable Counter	13	This status bit enables the Enable Counter A (status bit 00) to be set when an ST1 event has occurred.
	12	For maintenance purposes, this status bit generates an ST1 event.
	11	For maintenance purposes, this status bit generates a 1 MHz-clock pulse in Clock A.
	10	For maintenance purposes, this status bit generates an ST2 event.
Mode	09–08	These mode bits select the mode of operation of Clock A.
	0 0	Single Interval mode – Counter counts from preset value to overflow, sets Mode Flag, sets Overflow Flag (if jumper W2 is in place), and stops. Overflow generates A Event Output.
	0 1	Repeated Interval mode – Counter counts from preset value to overflow, sets Mode Flag, sets Overflow Flag (if W2 is in place), transfers buffer to counter register and begins again. Overflow generates A Event Output.
	1 0	External Event Time mode – The counter is free running at the selected rate and a pulse from Schmitt Trigger two transfers contents of the counter register to the buffer register, sets Mode Flag, and continues counting.
	1 1	External Event Time mode from zero base – The counter is free running at the selected rate and a pulse from ST2 transfers contents of counter register to buffer register, sets Mode Flag, clears the counter and continues counting from zero.
Mode Flag	07	This status bit sets on Overflow or when a Counter to buffer transfer occurs.
Mode Flag Interrupt Enable	06	This status bit enables an interrupt to be generated when the Mode Flag sets (status bit 7).
A Overflow Flag	05	This status bit sets when an overflow from Counter A occurs. (If jumper W2 is installed).

Table 3-1 (Cont)
A Status Register Bit Descriptions

Function	Bit	Description
Rate	03–01	These status bits select the rate at which Clock A operates:

03	02	01	Clock A
0	0	0	No rate or B Overflow
0	0	1	1 MHz
0	1	0	100 KHz
0	1	1	10 KHz
1	0	0	1 KHz
1	0	1	100 Hz
1	1	0	STP1
1	1	1	Line Freq.

Function	Bit	Description
Enable Counter A	00	When this status bit is set, Clock A is enabled to count at the selected rate. This bit is set by either the status register or by an ST1 event and ST1 Enable (bit 14).

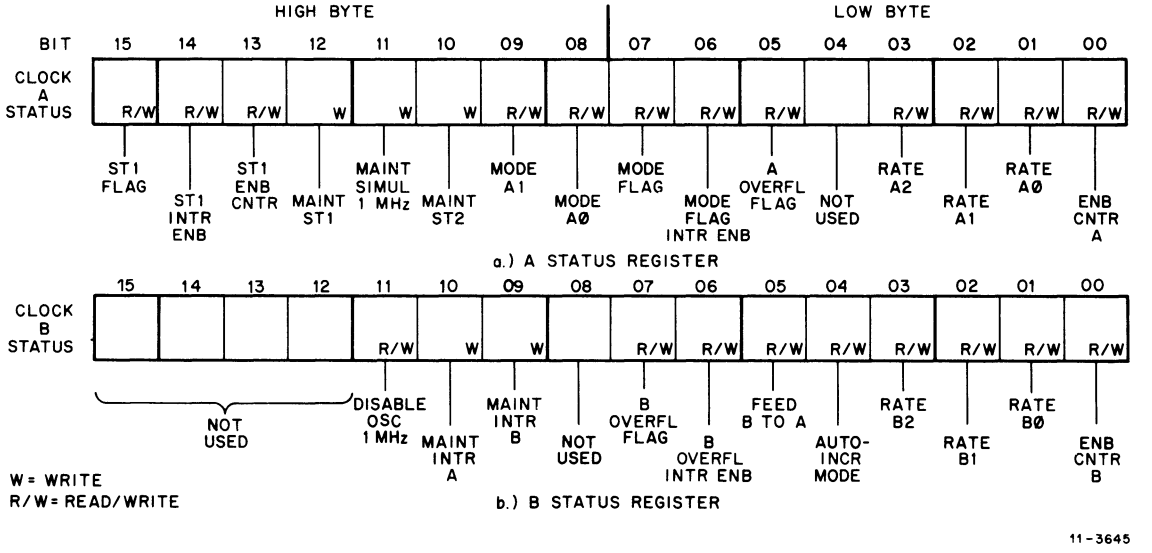

Figure 3-1 KW11-K A and B Register Formats

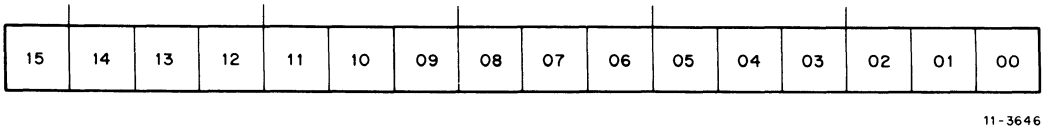

Figure 3-2 A Counter

Table 3-2
B Status Register Bit Descriptions

Function	Bit	Description
Maintenance	11	This status bit disables the 1 MHz oscillator (Clock A) which is used to generate the other crystal-controlled frequencies of Clock A.
Maintenance	10	For maintenance purposes, this status bit generates a Clock A interrupt.
Maintenance	09	For maintenance purposes, this status bit generates a Clock B interrupt.
B Overflow Flag	07	This status bit sets when an overflow from Counter B occurs.
B Overflow Interrupt Enable	06	This status bit enables an interrupt to be generated when a B Overflow occurs.
Feed B to A	05	If Clock A is selected for rate 0, the overflow of Clock B is used as the clocking frequency of Clock A.
Auto-Increment Mode	04	When this status bit is set, Buffer Register A is decremented in 2s complement when an A Overflow occurs. When an ST2 occurs, internal KW11-K clock timing is synchronized to it.
Rate	03–01	These status bits enable the rate at which Clock B is to operate: **03 02 01 Clock B** 0 0 0 No rate 0 0 1 1 MHz 0 1 0 100 KHz 0 1 1 10 KHz 1 0 0 1 KHz 1 0 1 100 Hz 1 1 0 STP3 1 1 1 Line Freq.
Enable Counter B	00	When this status bit is set, Clock B is enabled to count at the selected rate.

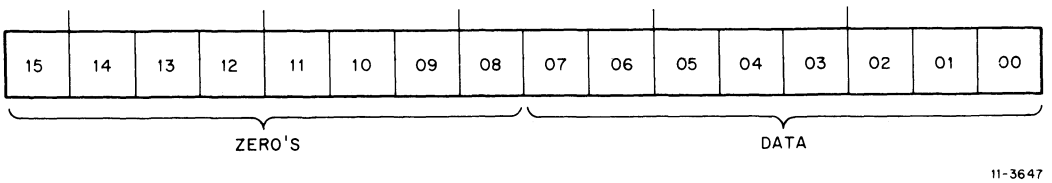

Figure 3-3 B Counter

3.3.3 A Preset/Buffer Register and B Preset Register

The A Preset/Buffer Register is a 16-bit (word-oriented) register and is illustrated in Figure 3-4. This register can be written into or read while Clock A is in operation.

The B Preset Register is an 8-bit (low byte) register and is illustrated in Figure 3-5. This register can be written or read, but not while Clock B is in operation.

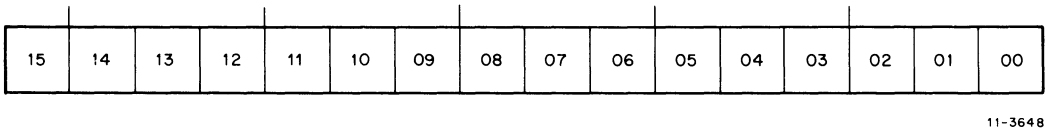

Figure 3-4 A Preset/Buffer Register

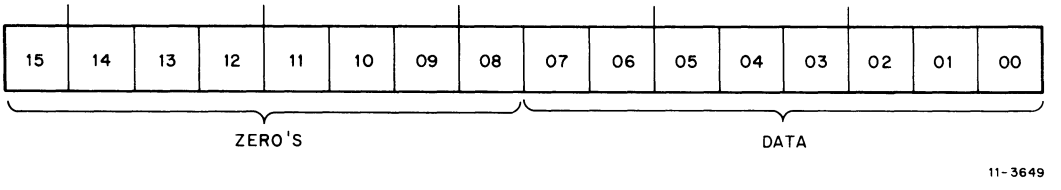

Figure 3-5 B Preset Register

KW11-K
DUAL PROGRAMMABLE
REAL TIME CLOCK
USER MANUAL

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