P R E L I M I N A R Y

M9301 BOOTSTRAP TERMINATOR

MAINTENANCE MANUAL

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M9301 MAINTENANCE MANUAL

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1.0 PREFACE

This manual describes the M9301 Bootstrap/Terminator module and its various versions. Complete understanding of its contents requires that the user have a general knowledge of digital circuitry and a basic understanding of PDP-11 computers. The following related documents may be valuable as references.

> PDP11 Peripherals Handbook
> PDP11 Processor Handbooks
> PDP-11/34, 11/39, USERS MANUAL

2.0 INTRODUCTION

2.1 General Description

The M9301 Bootstrap/Terminator is a double height extended module which plugs into a terminator slot on most PDP11 computers (see Installation Section 4). It contains a complete set of UNIBUS termination resistors along with 512 words of Read-Only memory which can be used for bootstrap programs. The module also provides circuitry for initiating bootstrap programs either on power ups or from an external or logic level switch closure. See Figure 1 for photo of module.

2.2 Features

- Combines UNIBUS termination and bootstrap capability on one double height module.

- Can be used in all PDP11 machines which can handle an extended length module in the terminator slots.

- Bootstrap programs can be initiated by the following means:

    1. Direct program jumps to the memory space occupied by the bootstrap.
    2. Programmer console Load address and start sequence.
    3. Power restarts (See Section 3.3)
    4. External Boot switch closure

- Provides capability of enabling or disabling boots on power restarts.

- Provides 512 words of user memory space which can be programmed by the user or purchased with standard patterns provided by DEC. (See sections 3.10 and 4.2).

Module Photo

To Be Supplied

Figure 1

2.3 Physical Description

The M9301 is a double height extended (8 1/2 x 5 1/2 inches) FLIP-CHIP
module which plugs into the A and B terminator slots on the PDP11
backplane. External connections are made via three FAST ON (TP1,TP2,
and TP3) tabs provided at the handle end of the module.

2.4 Electrical Specification

2.4.1 Power Consumption

+5V DC - 2.0 Amperes typical

2.4.2 Electrical Interfaces

The UNIBUS interface is standard using 8837 and 8640 receivers and
8881 drivers.

2.4.3 External Electrical Interfaces

The external interface consists of three FAST ON tabs (TP1, TP2 and
TP3), each having the following loading and usage constraints.

> TP1 Represents one standard TTL load with a 1K ohm
> pull-up. Input should be stable during a power up.
> Refer to Section 3.3 for TP1 usage.

> TP2 Represents two standard TTL loads with a 1K ohm
> pull-up resistor. Input signals should be limited to
> a 100ns minimum pulse width with all switch bounce
> noise restricted to a 5ms maximum duration. Note
> that triggering is initiated upon release of an input
> low (logic "0") pulse. On all power-ups, triggering
> is disabled until approximately 100ms after power
> returns (See Section 3.7) assuming that +5 VDC will
> be available from the power supply within 23ms.   It
> is also important to realize that this input has no
> over voltage protection capability and adequate
> filtering must be provided when remoting this input
> outside the standard DEC computer enclosure.   Refer
> to Section 3.5 for TP2 usage.

> TP3 Should be used as a ground return for external
> switches attached to TP1 and TP2. Note that there is
> no protection for large voltage spikes on this input
> so proper filters should be externally installed to
> guarantee adequate isolation.

2.4.4 Electrical Prerequistes

Refer to Section 4.0 for system constraints on specific version being
used.

2.4.5 Power and Ground Pinouts

    +5VDC: pin AA2, BA2
     GND: PINS AC2, AT1, BC2, BT1

2.4.6 M9301 MODIFIED UNIBUS Pin Assignments

See TABLE 1.

2.4.7 Timing

Figure 2 shows important timing constraints for the M9301. Values
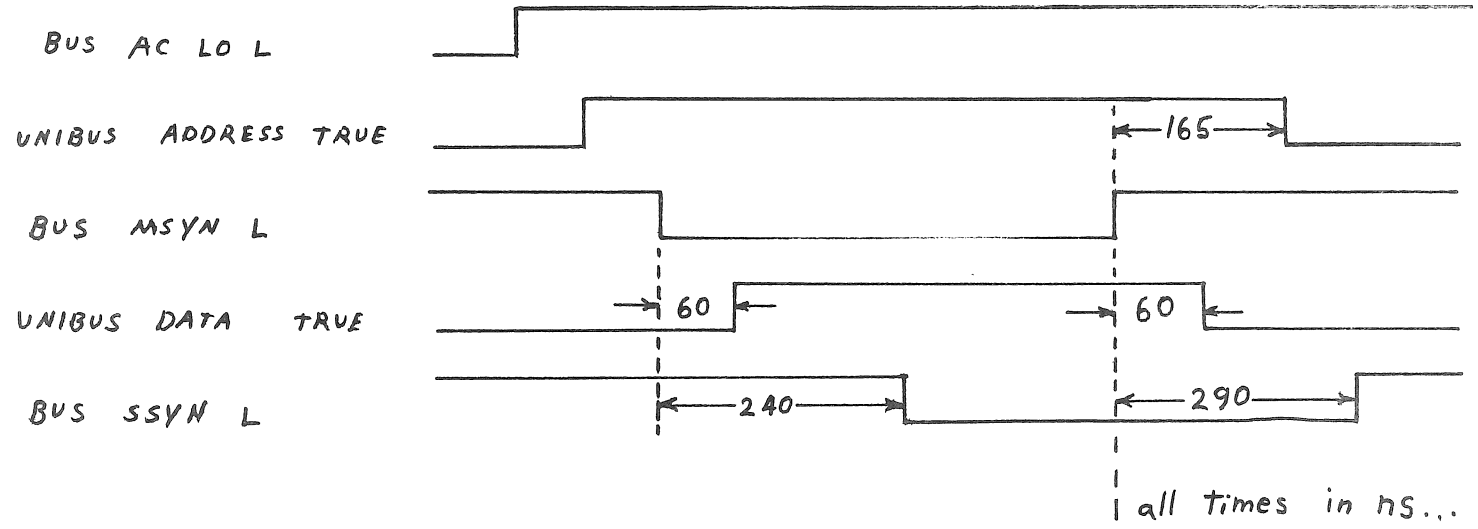shown are typical.

FIGURE 2
M9301 TIMING

2.5 Operating Environmental Specifications

2.5.1 Temperature Range   0 c to 70 c

2.5.2 Relative Humidity - 20% to 95%
                           (with out condensation)

BUS AC LO L

UNIBUS ADDRESS TRUE

BUS MSYN L

UNIBUS DATA TRUE

BUS SSYN L

165

60

60

240

290

all times in ns...

FIGURE 2
M9301 TIMING

TABLE 1

M9301 MODIFIED UNIBUS PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL
AA1	BUS INIT L	BA1	SPARE
AA2	POWER(+5V)	BA2	POWER (+5V)
AB1	BUS INTR L	BB1	SPARE
AB2	TEST POINT	BB2	TEST POINT
AC1	BUS D00 L	BC1	BUS BR 5L
AC2	GROUND	BC2	GROUND
AD1	BUS D02 L	BD1	BAT-BACKUP +5V
AD2	BUS D01 L	BD2	BR 4L
AE1	BUS DC4 L	BE1	INT. SSYN.
AE2	BUS D03 L	BE2	PAR: DET.
AF1	BUS D06 L	BF1	BUS ACLO L
AF2	BUS D05 L	BF2	BUS DCLO L
AH1	BUS D08 L	BH1	BUS A01 L
AH2	BUS D07 L	BH2	BUS A00 L
AJ1	BUS D10 L	BJ1	BUS A03 L
AJ2	BUS D09 L	BJ2	BUS A02 L
AK1	BUS D12 L	BK1	BUS A05 L
AK2	BUS D11 L	BK2	BUS A04 L
AL1	BUS D14 L	BL1	BUS A07 L
AL2	BUS D13 L	BL2	BUS A06 L
AM1	BUS PA L	BM1	BUS A09 L
AM2	BUS D15 L	BM2	BUS A08 L
AN1	P1	BN1	BUS A11 L
AN2	BUS PB L	BN2	BUS A10 L
AP1	P0	BP1	BUS A13 L
AP2	BUS BBSY L	BP2	BUS A12 L
AR1	BAT BACKUP +15V	BR1	BUS A15 L
AR2	BUS SACK L	BR2	BUS A14 L
AS1	BAT. BACKUP -15V	BS1	BUS A17 L
AS2	BUS NPR L	BS2	BUS A16 L
AT1	GROUND	BT1	GROUND
AT2	BUS BR 7L	BT2	BUS C1 L
AU1	+20V	BU1	BUS SSYN L
AU2	BUS BR 6L	BU2	BUS CO 1
AV1	+20V	BV1	BUS MSYN L
AV2	+20V	BV2	-5V

3.0   HARDWARE DESCRIPTION

3.1   Introduction

The following is a detailed circuit description of the M9301
Bootstrap/Terminals module. Various segments of this module will be
analyzed separately for clarity. M9301 circuit schematics will be
referenced throughtout the description. (CS M9301-0-1).

3.2 Definition of Terms

3.2.1 Bootstrap Program

A bootstrap program is any program which load another (usually larger)
program into computer memory from a peripheral device.

3.2.2 Boot

Boot is a verb which means to initiate execution of a bootstrap
program.

3.2.3 Bootstrap

Bootstrap and bootstrap program are used interchangeably.

3.3 Overview

Typically all PDP11 computers perform what is referred to as a power
up sequence each time power is applied to their CPU module(s). This
sequence is as follows:

3.3 Overview continued

+5VDC COMES TRUE

BUS DC LO L RELEASED
BY POWER SUPPLY

BUS AC LO L RELEASED
BY POWER SUPPLY

PROCESSOR ACCESSES MEMORY
LOCATION 24(8) FOR NEW PC

PROCESSOR ACCESSES MEMORY
LOCATION 26(8) FOR NEW PSW

PROCESSOR BEGINS RUNNING PROGRAM
AT NEW PC CONTENTS

WITH AN M9301 BOOTSTRAP/TERMINATOR IN THE PDP11 computer system, on power ups the user can optionally (a switch on the M9301 can enable or disable this feature) force the processor to read its new PC from a ROM memory location (unibus Location 773024(8)) and offset switch bank on the M9301. A new PSW will also be read from a location (UNIBUS Location 773026(8)) in the M9301 memory. This new PC and PSW will then direct the processor to a program (typically a bootstrap) in the M9301 ROM (UNIBUS memory locations 773000 thru 773776).

If booting on power ups is disabled an external switch or logic level and be used to force the processor to execute a boot program. Programs in the M9301 can also be initiated by program jumps to their starting addresses or through the START switch feature of a programmer's switch console if one is available in the system.

3.4 Power Up Booting Logic

AC LO and DC LO

The status of every PDP11 power supply is described by the two UNIBUS control lines BUS AC LO L and BUS DC LO L. The condition of these two lines in relation to the +5 volt output of the power supply is defined by UNIBUS specifications as summarized in Figure 3.

Figure 3   Power fail Sequence

Power Up or Power DOWN

On the M9301, Power up sequences are detected by the circuitry shown
in Figure 4.   When +5 volts first becomes true, both Bus AC LO, and
BUS DC LO are asserted low.   Assuming the POWER UP REBOOT ENABLE
switch (S1-2) is closed on, flip flop E29 will then be set. When BUS
DC LO L goes high followed by BUS AC LO L,   this flip-flop is then
cleared generating a low-to high transition on the output of E20 (pin
13). This transition triggers the one-shot E21 which asserts UNIBUS
address lines BUS A09 L, BUS A10 L, and BUS A12 L thru BUS A17 L for
300 ms.
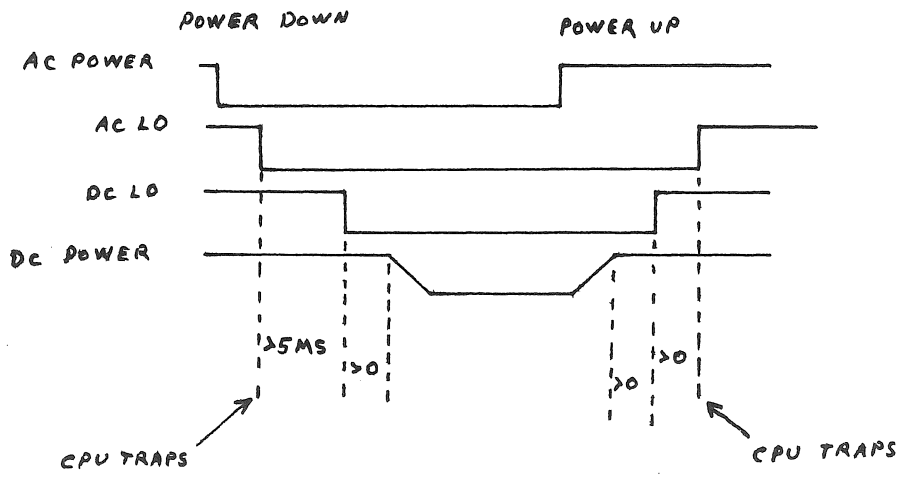
FIGURE 3   Power Fail Sequence

FIGURE 4
POWER UP BOOT LOGIC

Processor reads new program counter

During the 300 ms time-out of E21, the central processor will be
performing its power up sequence. When the processor attempts to read
a new program counter (PC) address from memory location 24(8), the
address bits enabled by the one-shot are logically ORed to generate
the address 773024(8). This location happens to be an address in the
M9301 rom space which contains the starting address of a specific (see
Section 3.9) boot routine.

Processor read new status word

Having obtained a new PC from location 773024(8); the processor then
attempts to read a new Processor Status Word (PSW) from memory
location 26(8). The address bits enabled by one-shot E21 are
logically ORed to generate the address 773026(8) which is also in the
M9301 ROM address space. Once this transfer is completed the removal
of MSYN from the bus will generate a ADDR CLR L signal (See Section
3.6) which clears the one-shot (E21) timeout removing address bits BUS
A09, BUS A10, and BUS A12 thru BUS A17. The 300 ms timeout length of
E21 was chosen to guarantee enough time for all PDP11 processors to
complete the two memory transfers described before releasing the
address lines.

POWER UP REBOOT ENABLE
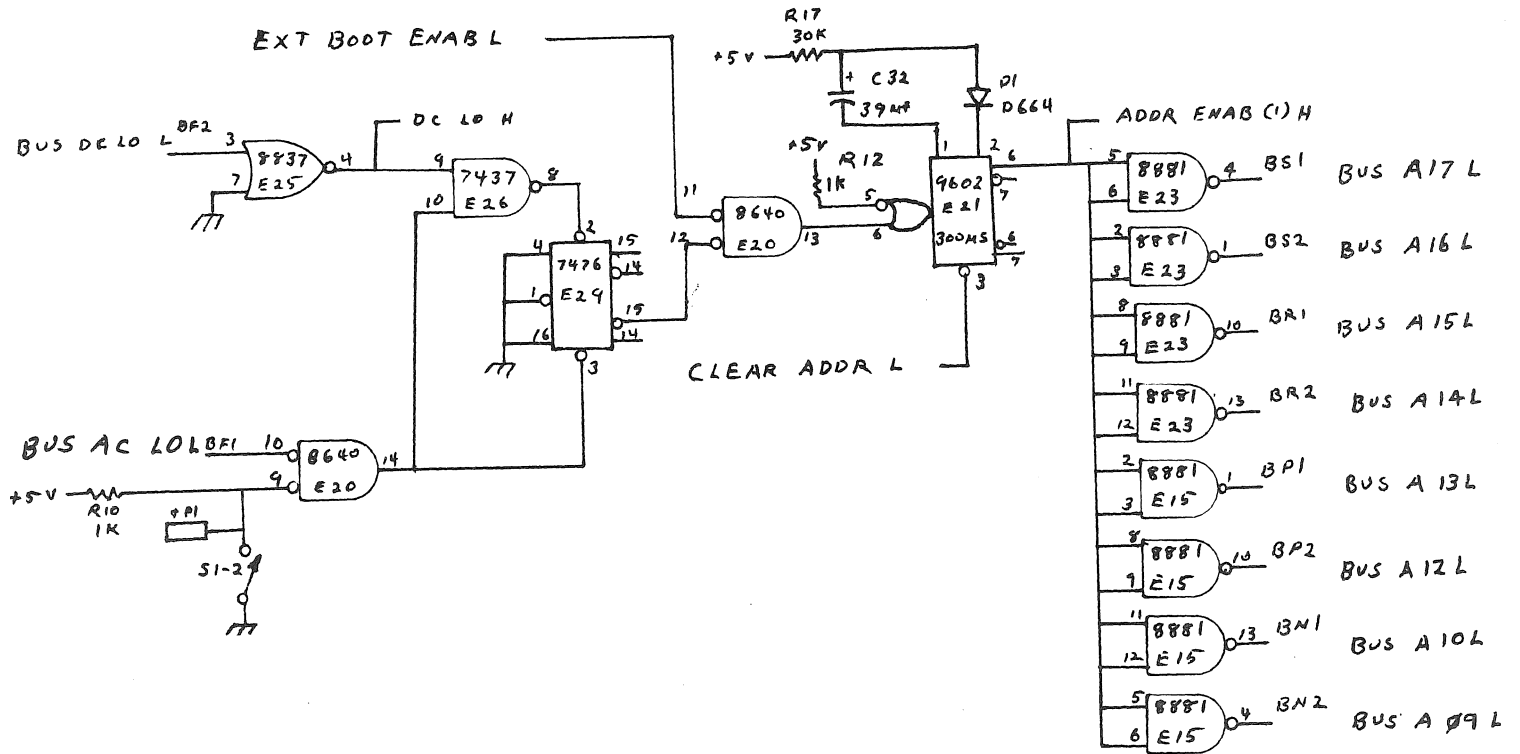
FIGURE 4

POWER UP BOOT LOGIC

The POWER UP REBOOT ENABLE switch (S1-2) can be used to disable the logic shown in Figure 4. With this switch open, the clear input to the flip-flop E29 will always be low, preventing it from ever being set on power restarts. FAST ON tab TP1 is provided to allow switch S1-2 to be remoted external to the module. Note that when an external switch is used, S1-2 must be left in the off position.

3.5 External Boot Circuit

The processor can be externally activated by grounding the FAST ON tab TP2 input, as shown in FIGURE 5. This low input sets flip-flop E13 which then generates a BUS AC LO L signal on the UNIBUS. Upon seeing this

FIGURE 5
EXTERNAL BOOT CIRCUIT

UNIBUS SIGNAL EVERY PDP11 processor will begin a power down routine anticipating a real power failure. After completing this routine, the processor will then wait for the release of BUS AC LO L at which time it will perform a power up sequence through location 24(8) and 26(8).

When the EXTERNAL BOOT input is released, the oneshot E21, is triggered causing an 8 ms timeout, and the set input to flip-flop E13 removed. At the end of the one-shot timeout, flip-flop E13 is clocked low releasing the BUS AC LO L line and firing the 300 ms one-shot (E21) mentioned in Section 3.4. The processor then is forced to read its new PC and PSW from location 773024 and 773026 respectively as described in Section 3.4.

FIGURE 5
EXTERNAL BOOT CIRCUIT

TP2 Switch
Closure

t

BUS AC LO L

E   ONE SHOT TIMEOUT

8ms

Processor Performs
POWER DOWN

Processor Performs
POWER UP
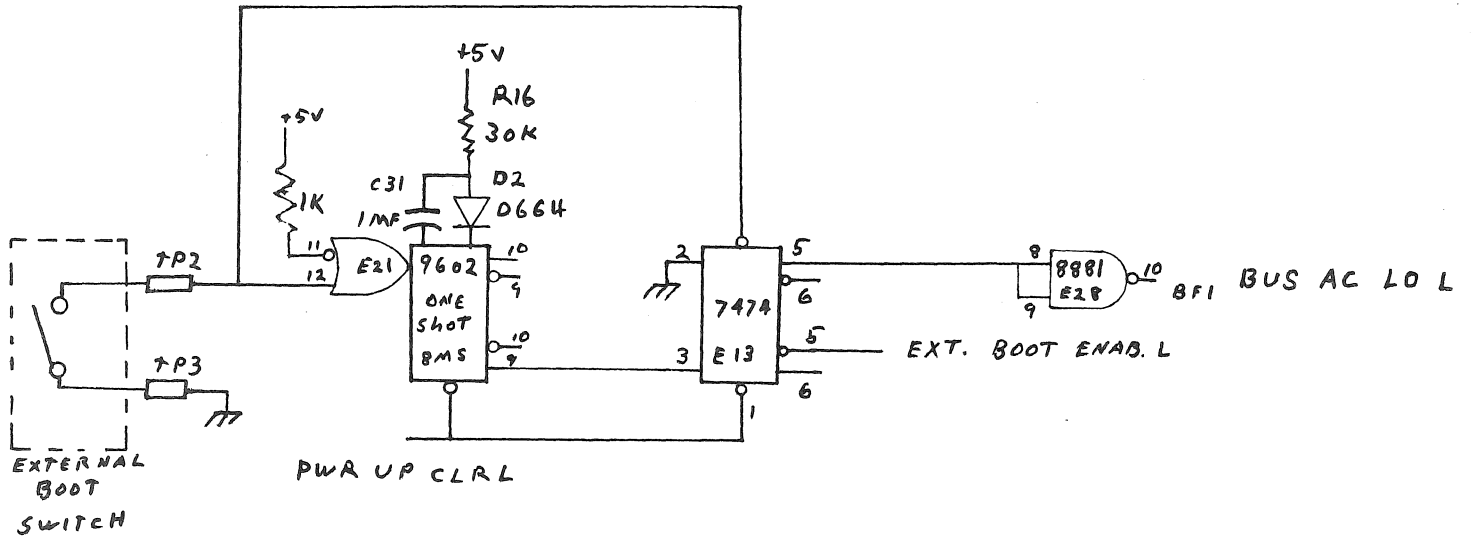
$$40 \, ns \leq t \leq \infty$$
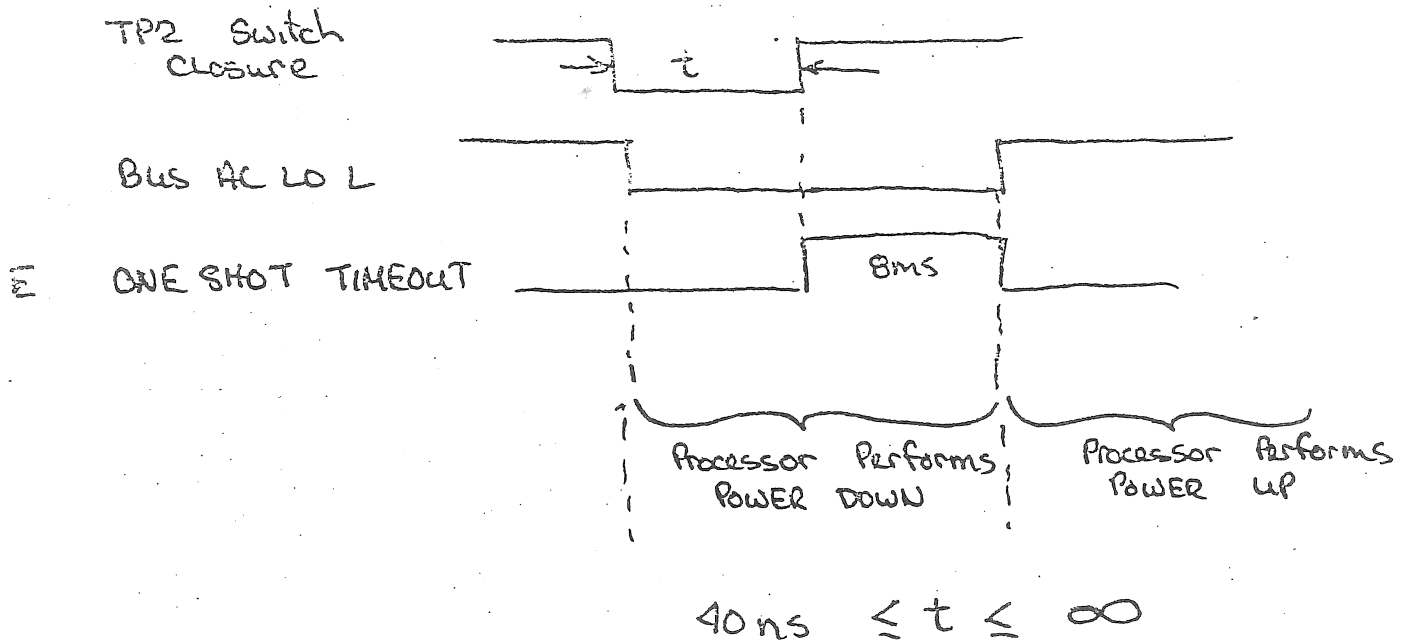
FIGURE 6
EXTERNAL   BOOT   TIMING

3.6 Power Up Transfer Detection Logic

FIGURE 7
TRANSFER DETECTION LOGIC

After BUS AC LO L and BUS DC LO L have performed their power up
sequence as described in Section 3.4, the logic shown in Figure 7
counts the first two DATI transfers on the UNIBUS and generates a 75
ns pulse on the CLR ADDR L line. The two UNIBUS transfers performed
will be to obtain a new PC and PSW as previously described. The CLR
ADDR L pulse resulting will be used to clear the one shot E21 shown in
Figure 4 releasing bus address line BUS A09, BUS A10, and BUS A12 thru
BUS A17.

3.7 Power Up Clear

The circuit shown in Figure 8 is included on the M9301 to guarantee
that specific storage elements on the module are cleared when power is
first applied the PWR CLR L signal will be held low for approximately
70 ms after the +5VDC has returned assuming the +5V supply has a rise
time of less than 20ms. The exact period of time for holding PWR CLR
L is a function of the rise time of the +5VDC power supply.

FIGURE 8
POWER UP CLEAR LOGIC
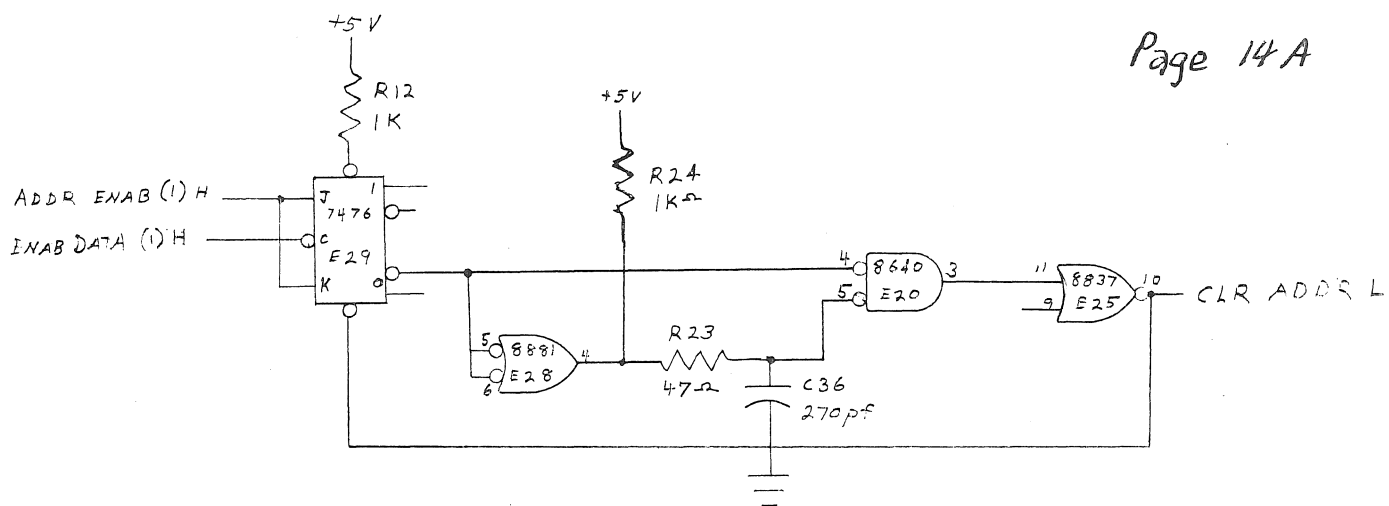
FIG. 7

TRANSFER DETECTION LOGIC
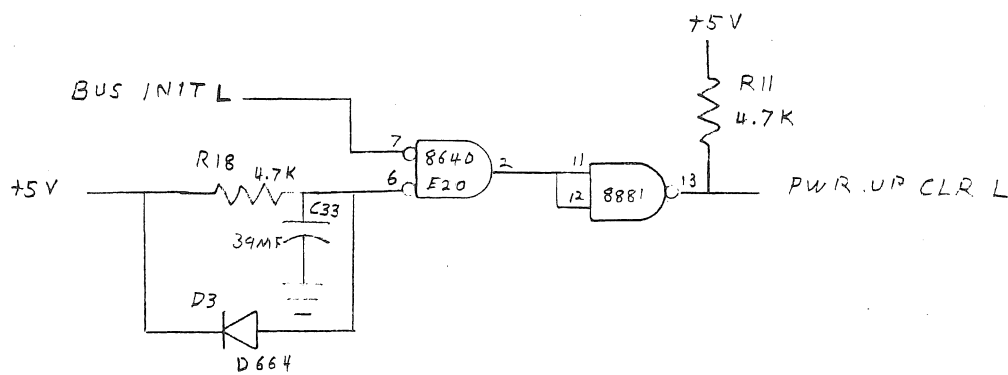
FIG. 8

POWER UP CLEAR LOGIC

3.8 Address Detection Logic

M9301 Address Space

Figure 9 shows the complete UNIBUS address detection logic on the M9301. The purpose of this circuitry is to detect UNIBUS addresses within the address space of the M9301 773000(8) - 773777(8) and 765000(8) - 765777(8)), and recognize the specific addresses 773024(8) and 773026(8) for the power up circuit previously described in Sections 3.4, and 3.5.
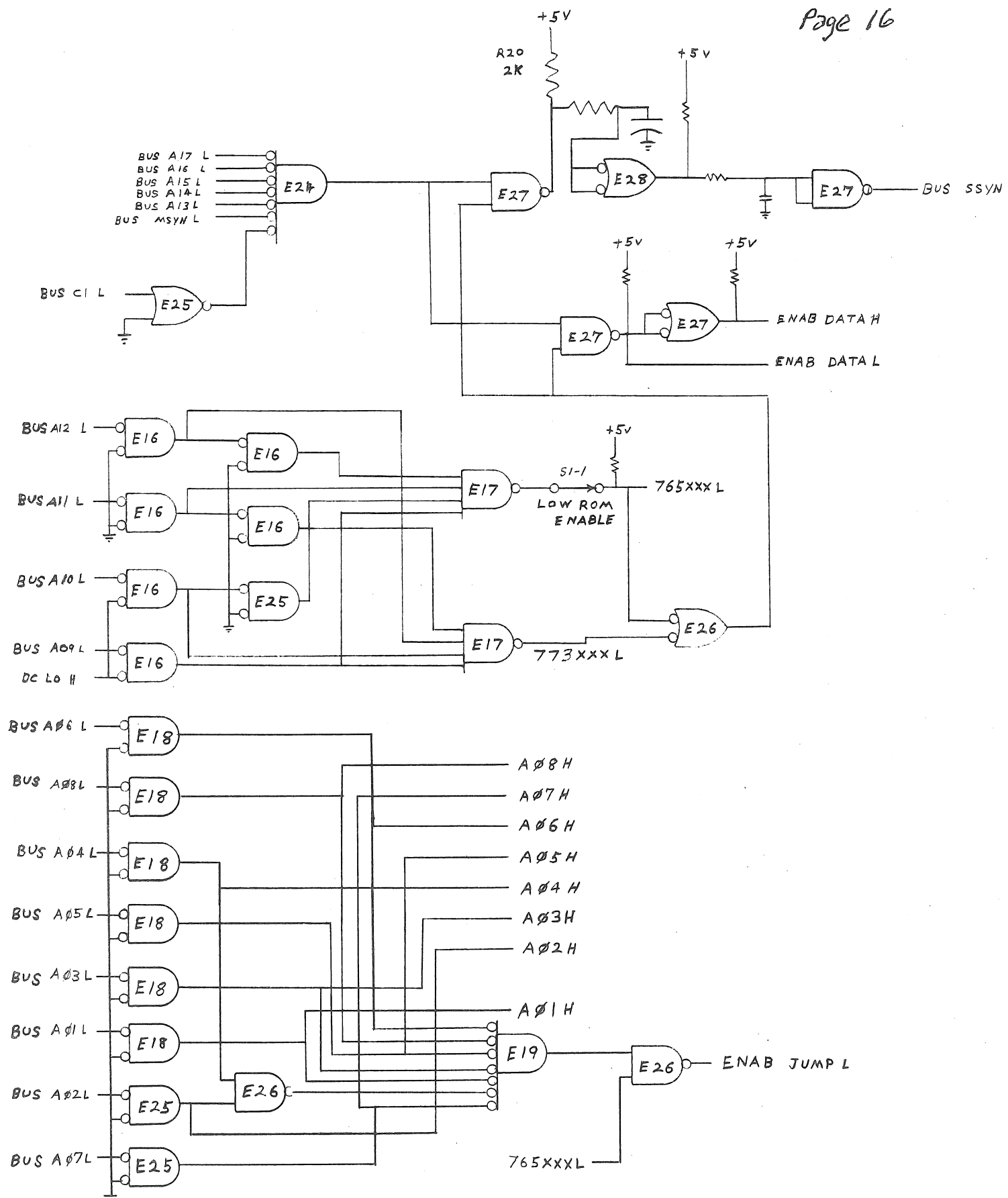
FIG. 9
ADDRESS DECODER LOGIC

M9301 Memory Access Constraints

The circuitry show in Figure 9 determines when the M9301 ROM address space is being accessed. Upon receiving a recognized UNIBUS address, and BUS MSYN, the ROM data outputs are enabled onto the UNIBUS data lines (BUS D00 L - BUS D15 L) and BUS SSYN L is enabled 200 ns later. Conditions which must be met before enabling the ROM data and returning BUS SSYN are as follows:

    1. Detection of the UNIBUS address 765XXX (dependent on position the of L ROM ENABLE switch S1-1) or 773XXX where XXX is redundant.

    2. Transfer being performed is a DATI operation where BUS C1 L is not asserted.

    3. A BUS MSYN L control signal has been obtained.

Low ROM Enable Switch

LOW ROM ENABLE switch (s1-1) shown in Figure 9 allows the user to disable the M9301 detection of UNIBUS addresses 765000 tru 765777. These addresses would normally represent the lower 256 words of the M9301 memory space. Disabling the detection of these addresses S1-1 is set to OFF position) becomes essential when that memory space is being used by other peripheral devices in the system. For M9301 modules containing standard DEC programs, users should note what program features will be eliminated by disabling M9301 address locations 765000 thru 765777.

ROM Address Generation

Logic shown in the lower half of Figure 9 performs two functions. First it receives the nine address inputs for the M9301 ROM memory (765XXXL and A01H thru A08H). Second it detects the UNIBUS address 773024 and generates the offset switch enable signal (See Section 3.9) ENAB JUMP L.

3.9 Address Offset Switch Bank

As previously mentioned in Section 3.4, on all boots, the M9301 processor obtains its new PC from location 773024(8) instead of location 24(8). When the M9301 address detection logic (Section 3.8) decodes the address 24(8), it enables (via ENABL JUMP L) the address offset switch bank (Figure 10) shown below. The contents of these switches, combined with the contents of the specified address in M9301 ROM memory, produce a new PC for the CPU. This new Pc will point the processor to the starting address of a specific program (usally a bootstrap routine) in the M9301 memory. Several programs can be included in the M9301 memory with any one being user selectable through the address offset switch selection

Example:

```
M9301 ROM address 773024 contains --   173000
Offset Switch Bank contains               254
                                       ------
New PC read by CPU                      173254
```

FIGURE 10
ADDRESS OFFSET
SWITCH BANK
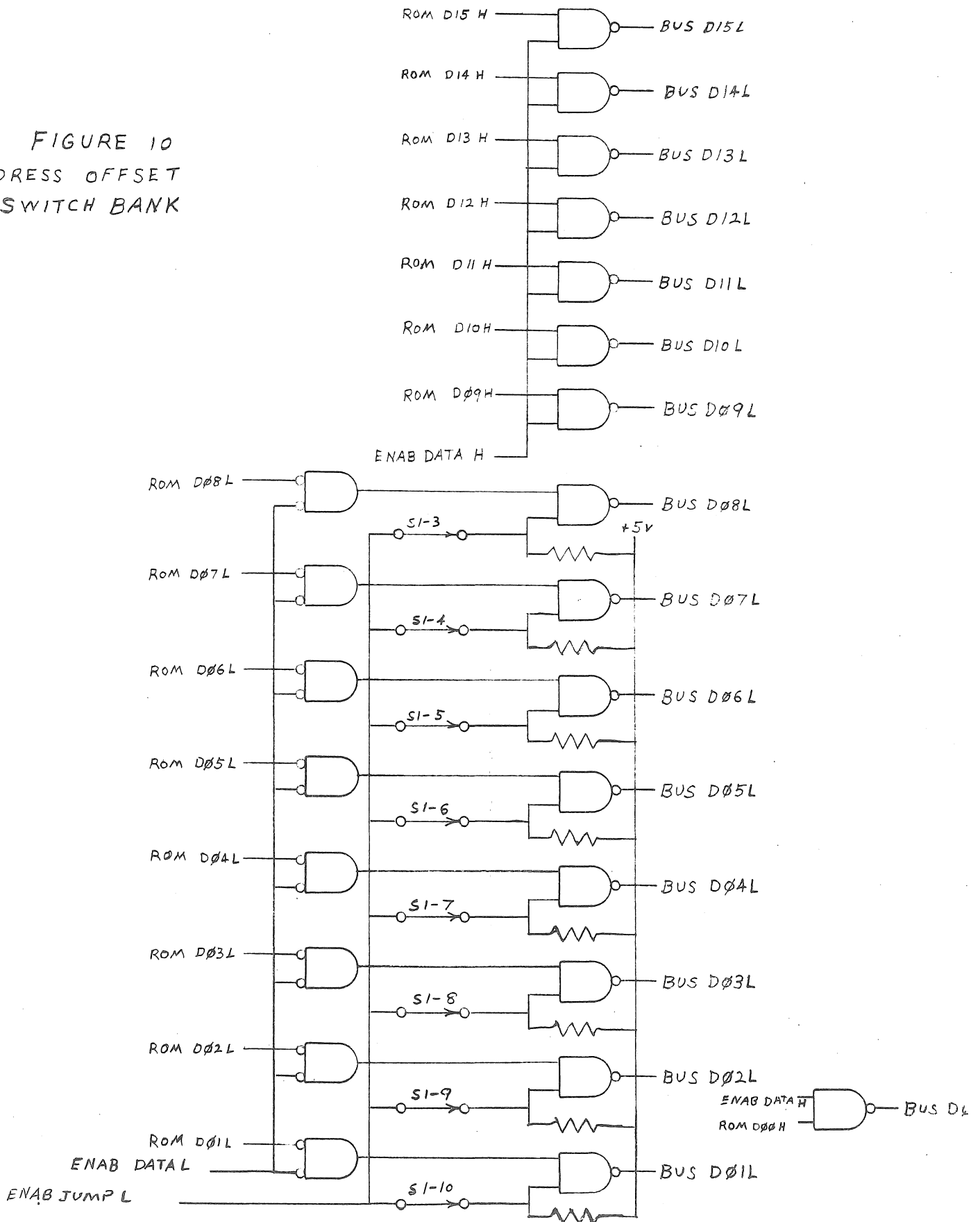
3.10 ROM Memory

The heart of the M9301 is the 512 word ROM (Read Only Memory) shown in Figure 11. It is composed of four 512 x 4 Bit Tri-state ROMS organized in a 512 x 16 bit configuration. All four units share the same address lines and produce 16-bit PDP-11 instructions for execution by the processor.

All four ROM outputs are always enabled, so any change in address inputs will result in a change in the UNIBUS data lines when the ENAB DATA signals in Figure 9 are enabled. For further information on M9301 compatible ROMS, CONSULT THE ROM Specifications shown in the Appendix.

M9301 users that program their own PROMS should note the following programming constraints.

1. There is no address or data output translation required.

2. UNIBUS address locations 773000(8) thru 773776(8) are located in the lower 256 words of PROM word space and UNIBUS address locations 765000(8) thru 765776(8) are resident in the upper 256 words.

3. When coding PROM patterns data bits D01 thru D08 must always contain the inverse of the data required to compensate for the extra inversion logic available in the M9301 Offset Switch Circuitry.
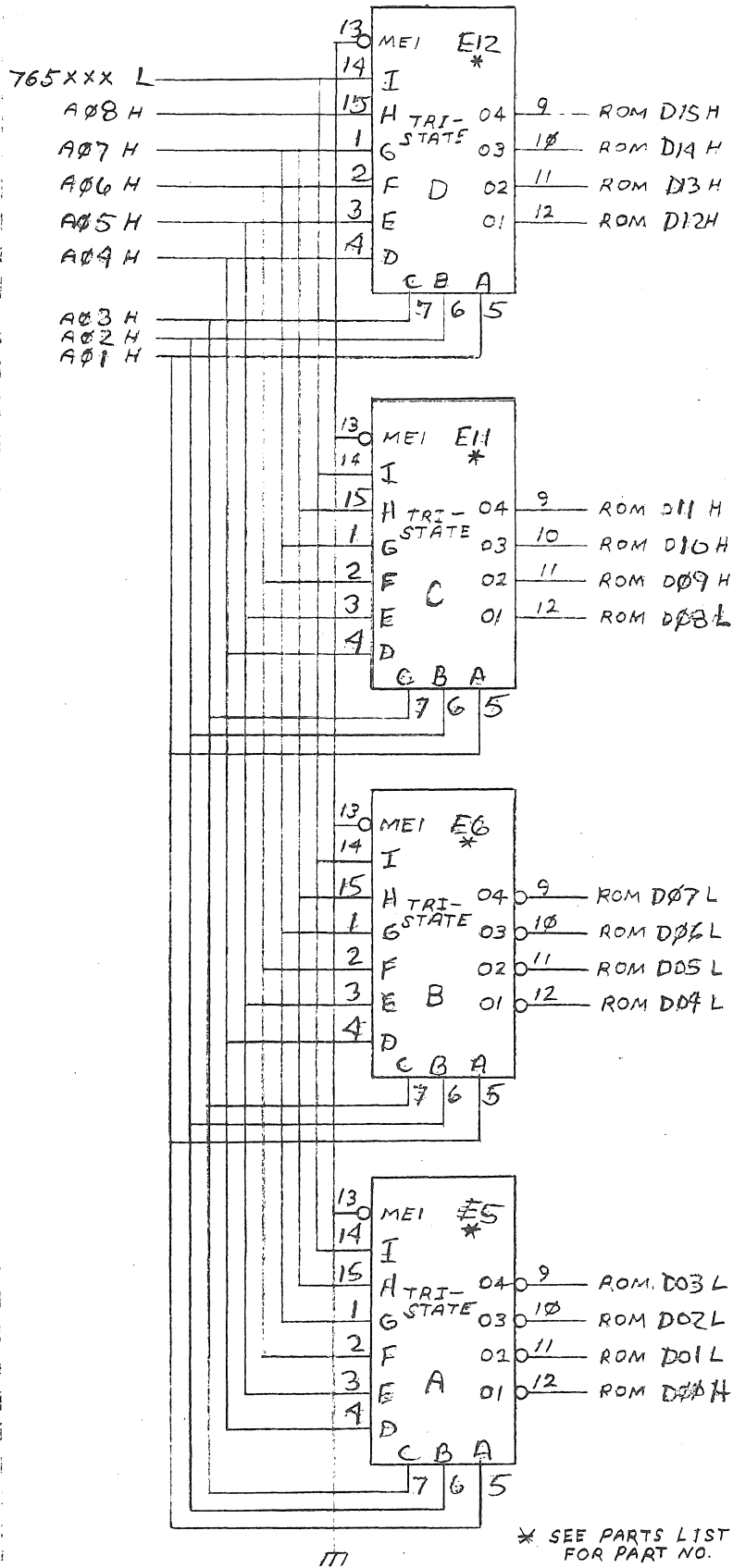
FIGURE 11
M9301 ROM MEMORY

765xxx L

A08 H
A07 H
A06 H
A05 H
A04 H

A03 H
A02 H
A01 H

E12
MEI
I TRI-STATE
H
G
F D
E
D
C B A
04 — 9 — ROM D15 H
03 — 10 — ROM D14 H
02 — 11 — ROM D13 H
01 — 12 — ROM D12 H
7 6 5

E11
MEI
I TRI-STATE
H
G
F C
E
D
G B A
04 — 9 — ROM D11 H
03 — 10 — ROM D10 H
02 — 11 — ROM D09 H
01 — 12 — ROM D08 L
7 6 5

E6
MEI
I TRI-STATE
H
G
F B
E
D
C B A
04 — 9 — ROM D07 L
03 — 10 — ROM D06 L
02 — 11 — ROM D05 L
01 — 12 — ROM D04 L
7 6 5

E5
MEI
I TRI-STATE
H
G
F A
E
D
C B A
04 — 9 — ROM D03 L
03 — 10 — ROM D02 L
02 — 11 — ROM D01 L
01 — 12 — ROM D00 H
7 6 5

* SEE PARTS LIST
FOR PART NO.

3.11   M9301 TERMINATOR

The terminator section of the M9301 consists of four resistor pack circuits each containing the required pull-up and pull-down resistors for proper UNIBUS termination. Since PDP11/04 and PDP11/34 computers incorporate BUS GRANT pull-up resistors on the processor modules, space has been left on the M9301 for five jumpers (W1 thru W5) which allow the user to select whether to include BUS GRANT pull-up resistors. TABLE 2 indicates which versions of the M9301 have BUS GRANT jumpers installed.

Caution should be taken when inserting M9301 modules in various PDP11 (PDP11/05, 11/10, 11/35, 11/40) computers. If the processor in question, does not have BUS GRANT pull-ups on the CPU, jumpers W1 through W5 on the M9301, should be inserted or the M9301 should be positioned at the end on the UNIBUS furthest from the CPU.

4.0 M9301 VARIATION

4.1 Overview

The M9301 Bootstrap/Terminator presently comes in five variations as described in the following sections. Table 2 summarizes the differences between each variation.

	M9301				
	-0	-YA	-YB	-YC	-YD
EXTERNAL BOOT SWITCH RESTART	*	YES	YES	NO	YES
POWER UP REBOOT ENABLE RESTART	*	YES	YES	NO	YES
PROGRAMMERS CONSOLE STANDARD WITH COMPUTER	*	NO	NO	YES	YES
READ ONLY MEMORY (ROM)	NO	YES	YES	YES	YES
SOCKETS SUPPLIED FOR PROGRAMMABLE (ROM/PROM)	YES	NO	NO	NO	NO
BUS GRANT PULL-UP TERMINATOR RESISTER (W1 THRU W5)	YES	NO	NO	YES	NO
SWITCH SELECTABLE BOOTING	*	YES	NO	YES	NO
STANDARD DEC BOOTSTRAPS AND MASSBUS DEVICE BOOTS	NO	NO	YES	NO	NO
STANDARD DEC BOOTSTRAPS	NO	YES	NO	NO	NO
PDP 11/70 USER PROGRAM	NO	NO	NO	YES	NO
DDCMP USER PRGRAM	NO	NO	NO	NO	YES

* INDICATES USER SELECTABLE

TABLE 2

M9301 VARIATION FEATURES

M9301 Variation Usage

General:
None of the following M9301 variations will function in a PDP11 system containing a UNIBUS repeater, unless the M9301 is inserted in a terminator position on the processor side of the repeater.

M9301 - 0 - Can be used in any PDP11 computer that accepts an extended length terminator. The user defines the bootstrap or program available in M9301 Rom space.

M9301 - YA - Used in most PDP11/04, and 34 OEM machines but is program compatible with all PDP11 machines that will accept an extended length terminator. Note however, that in other machines having CPUs which do not contain BUS GRANT pull up resistors, the M9301-YA must be placed at the end of the UNIBUS farthest from the CPU.

M9301 - YB - Same as the M9301-YA except it is intended for end user machines in the PDP11/04, and 34.

M9301 - YC - For use in only PDP11/70 machines.

M9301 - YD - Can be used in any PDP11 machine. Caution should be taken, however, when inserting the M9301 in some PDP11 computers. If the processor in question does not have BUS GRANT pull-up resisters on the CPU, jumpers W1 thru W5 on M9301 should be inserted or, the M9301 should be placed at the end of the UNIBUS furthest from the processor. (See Section 3.11).

4.2   M9301-0

The M9301-0 has been created as a universal bootstrap device which allows the user to program and install customized 512 x 4 bit ROMS. This module version comes with four 16-pin IC (integrated circuit) sockets in place of the Roms normally inserted on other module versions. For pinout and access time constraints on Roms used, consult the Rom Specification shown in the Appendix. When configuring Rom bit patterns for the M9301-0, care should be taken to arrange them to meet the address and data output pinouts on the module. (See section 3.10)

4.3   M9301-YA and M9301-YB Versions

Two versions of the M9301 have been created for use in the PDP 11/04, and 34, computers. One version, designated M9301-YA, is for OEM (original equipment manufacturer) use and the other designated M9301-YB is for end users. Both units contain basic CPU and memory GO-NO GO diagnostics along with specific sets of bootstrap programs as shown in Table 3 and Table 4.

4.3.1 Physical Differences from the M9301-0

The only physical difference between the M9301-YA/M9301-YB modules and the M9301-0 previously described, is that specially programmed Tri State 512 x 4 bit ROMs are inserted in the four locations occupied by 16-pin DIP sockets on the M9301-0.

4.3.2 M9301-YA and M9301-YB Program Memory Map

Table 5 is a program memory map of the M9301-YA and M9301-YB modules and briefly lists the nature of each diagnostic test in the ROMS.

4.3.2.1 Basic CPU Diagnostics

TEST 1 - SINGLE OPERAND TEST

This test executes all single operand instructions using destination mode 0. The basic objective is to verify that all single operand instructions operate; it also provides a cursory check on the operation of each instruction, while ensuring that the CPU decodes each instruction in the correct manner.

TEST 1 brings the test destination register through its three possible states: zero, negative, and positive. Each instruction operates on the register contents in one of four ways:

1. Data will be changed via a direct operation, i.e., increment, clear, decrement, etc.

2. Data will be changed via an indirect operation, i.e., arithmetic shifts, add carry, and subtract carry.

3. Data will be unchanged, but operated upon, via a direct operation, i.e., clear a register already containing zeros.

4. Data will be unchanged via a non-modifying instruction (TEST).

Note that when operating upon data in an indirect manner, the data is modified by the state of the appropriate condition code. Arithmetic shift will move the "C" bit into or out of the destination. This operation, when performed correctly, implies that the "C" bit was set correctly by the previous instruction. There are no checks on the data integrity prior to the end of the test. However, a check is made on end the result of the data manipulation. A correct result implies that all instructions manipulated (or, did not manipulate) the data in the correct way. If the data is incorrect, the program will hang in a program loop until the machine is halted.

TEST 2 - DOUBLE OPERAND, ALL SOURCE MODES.

DESTINATION MODE 0

This test verifies all double operand general and logical instruction--each in one of the seven modes (excludes mode 0). Thus, two operations are checked the correct decoding of each double operand instruction, and the correct operation of each addressing mode for the source operand.

Each instruction on the test must operate correctly in order for the next instruction to operate. This inter-dependence is carried through to the last instruction (bit test) where, only through the correct execution of all previous instructions is a data field examined for a specific bit configuration. Thus, each instruction prior to the last serves to set up the pointer to the test data.

Two checks on instruction operation are made in TEST 2. One check, a branch on condition, is made following the compare instruction, while the second is made as the last instruction in the test sequence.

Since the GO-NO GO test resides in a ROM memory, all data manipulation (modification) must be performed in destination mode 0 (register contains data). The data and addressing constants used by TEST 2, are contained within the ROM.

It is important to note that two different types of operations must execute correctly in order for this test to opeate:

1. Those instructions that paritcipate in computing the final address of the data mask for the final bit test instruction.

2. Those instructions that manipulate the test data within the register to generate the expected bit pattern.

Detection of an error within this test results in a program loop.

TEST 3 - JUMP TEST MODES 1, 2, AND 3

The purpose of this test is to ensure correct operation of the Jump instruction. This test is constructed such that only a Jump to the expected instruction will provide the correct pointer for the next instruction.

There are two possible failure modes that can occur in this test:

1. The Jump addressing circuitry will malfunction causing a transfer of execution to an incorrect instruction sequence or non-existent memory.

2. The Jump addressing circuitry will malfunction in such a way as to cause the CPU to loop.

The latter case is a logical error indicator. The former, however, may manifest itself as an after-the fact error. For example, if the Jump causes control to be given to other routines within the M9301, the inter-dependent instruction sequences would probably cause a

failure to eventually occur. In any case, the failing of the Jump instruction will eventually cause an out of sequence or "illogical event" to occur. This in itself is a meaningful indicator of a malfunctioning CPU.

This test contains a JUMP, MODE 2. This instruction is not compatible across the PDP-11 line. However, it will operate on any PDP-11, within this test, due to the unique programming of the instruction within TEST 3. Before illustrating the operation, it is important to understand the difference of the JUMP MODE 2 between machines.

On the PDP-11/20, 11/05, and 11/10 processor, for the Jump Mode 2 (JMP (R)+) the register (R) is incremented by 2 prior to execution of the Jump. On the PDP-11/40 and 11/35, (R) is used as the Jump address and incremented by 2 after execution of the Jump.

In order to avoid this incompatability, the Jump (R)+ is programmed with (R) pointing back on the Jump itself. On 11/20, 11/05, and 11/10 processors, execution of the instruction would cause (R) to be incremented to point to the following instruction, effectively continuing a normal execution sequence.

On the PDP-11/40 and 11/35 processors, the use of the initial value of (R) will cause the Jump to "loop" back on itself. However, correct operation of the auto-increment will move (R) to point to the next instruction following the initial Jump. The Jump will then be executed again. However, the destination address will be the next instruction in sequence.

TEST 4 - SINGLE OPEAND, NON-MODIFYING, BYTE TEST

This test focuses on then one unique single operand instruction, the TST. TST is a special case in the CPU execution flow since it is a non-modifying operation. TEST 4 also tests the byte operation of this instruction. The TSTB instruction will be executed in Mode 1 (register deferred) and Mode 2 (register deferred, auto increment).

The TSTB is programmed to operate on data which has a negative value most significant byte and a zero (not negative) least significant byte.

In order for this test to operate properly, the TSTB on the LSB must, first, be able to access the even addressed LSB, then set the proper condition codes. The TSTB is then re-executed with the auto-increment facility. After the auto-increment, the addressing register should be pointing to the MSB of the test data. Another TSTB is executed on what should be the MSB. The "N" bit of the condition codes should be set by this operation.

Correct execution of the last TSTB implies that the auto-increment recognized that a byte operation was request, thereby only incrementing the address in the register by one, rather than two. If the correct condition code was not set by the associated TSTB instruction, the program will loop.

TEST 5 - DOUBLE-OPERAND, NON-MODIFYING TEST

These are two non-modifying double-operand instructions - the compare (CMP) and bit test (BIT). These two instructions operate on test data in source modes 1 and 4, and destination modes 2 and 4.

The BIT and CMP instructions will operate on data consisting of all ones (177777). Two separate fields of ones are used in order to utilize the compare instructions, and to provide a field large enough to handle the auto-incrementing of the addressing register. Since the compare instruction is executed on two fields containing the same data, the expected result is a true "Z" bit, indicating equality.

The BIT instruction will use a mask argument of all ones against another field of all ones. The expected result is a non-zero condition (Z).

Most failures will result in a one instruction loop.

4.3.2.3 Register Display Routine - The register display routine prints out the octal contents of the CPU registers RO, R4, SP and old PC on the console terminal. This sequence will be followed by a prompt character ($) on the next line.

Example of a typical printout.

```
            XXXXXX     XXXXX     XXXXX     XXXXX
         $
         $
      Prompt  RØ         R4         R6         Old PC Program Counter
      Character                   (Stack
                                  Pointer)
```

1. Where X signifies an octal number (0-7).

2. Whenever there is a power up routine or the BOOT SWITCH is released on PDP11/04 and PDP11/34 machines, the PC at this time will be stored in R5. The contents of R5 are then printed as the OLD PC shown in the example.

    The prompting character string indicates that diagnostics have been run and the processor is operating.

4.3.2.3 Memory Modifying CPU Diagnostics

TEST 6 - DOUBLE OPERAND, MODIFYING, BYTE TEST

The objective of this test is to verify that the double-operand, modifying instructions will operate in the byte mode. TEST 6 contains three sub-tests:

1. Test source mode 2, destination mode 1, odd and even bytes.

2. Test souce mode 3, destination mode 2.

3. Test source mode 0, destination mode 3, even byte.

The move byte (MOVB), bit clear byte (BICB), and bit set byte (BISB) are used within TEST 6 to verify the opeation of the modifying double-operand functions.

Since modifying instructions are under test, memory must be used as a destination for the test data. TEST 6 uses location 500(8) as a destination address. Later, in TEST 7 and the Memory Test, location 500 is used as the first available storage for the stack.

Note that, since TEST 6 is a byte test, location 500(8) implies that both 500(8) and 501 are used for the bytes test (even and odd, respectively. Thus, in the word of data at 500 add and even bytes are caused to be all zeroes and all ones throughout the test. Each byte is modified independently of the other.

TEST 7 - JSR TEST

The JSR is the first test in the GO-NO GO sequence that utilizes the stack. The Jump Subroutine command (JSR is executed in modes 1 and 6. After the JSR is executed, the subroutine which was given control, will examine the stack to ensure that the correct data was placed in t correct stack location (500(8)). The routine will also ensure that the line back register points to the correct address. Any errors detected in this test will result in a Halt.

TEST 8 - MEMORY TEST

Although this test is intended to test both core and MOS memories, the data patterns used are designed to exhibit the most taxing operation for MOS. Before the details of the test are described, it would be appropriate to discuss the assumptions placed upon the failure modes of the MOS technology.

This test is intended to check for two types of problems that may arise in the memory.

1. Solid Element or Sense Amp failures.

2. Addressing Malfunctions external to the chip.

The simplest failure to detect is a solid read or write problem. If a cell fails to hold the appropriate data, it is expected that the Memory Test will easily detect this problem. In addition, the program attempts to saturate a chip in such a way as to cause marginal sense amp operation to manifest itself as a loss or pick-up of unexpected data. The 4K x 1 chip used in the memory consists of a 64 x 64 matrix of MOS storage elements. Each 64 bit section is tied to a common sense amplifier. The objective of the program is to saturate the section with, at first all zeroes and one "1" bit. This "1" bit is then floated through the chip. At the end, the data is complemented, and the test repeated.

For external addressing failures, it is assumed that if two or more

locations are selected at the same time, and a write occurs, it is likely that both locations will assume the correct state. Thus, prior to writing any test data, the background data is checked to ensure that there was no crosstalk between any two locations. All failures will result in a program halt as do failures in tests 6 and 7. After the halt, it is expected that the operator will depress the BOOT switch causing R0 (Expected Data), R4 (Received Data), SP (failing Address), and PC (PC indicating memory failure) to be displayed.

NOTE

If the expected and received data are the same, it is highly probable that an intermittent failure has been detected (i.e. timing or margin problem). The reason the expected and received data can be identical is that the test program re-reads the failing address after the initial non-compare is detected. Thus, a failure at CPU speed is deteted, and indicated by the reading of the failing address on a single reference (not at speed) operation.

4.3.2.4 Bootstrap Programs Supported by the M9301-YA and M9301-YB - Peripheral devices whose bootstraps are supported by the M9301-YA and M9301-YB are listed in TABLE 3 and TABLE 4. Each of these bootstraps is compatible with standard DEC boots and operate as follows.

4.3.2.4.1 RX11 DISKETTE - Loads the first 64 words (200 bytes) of data from track one, sector one into memory location 0 -177 beginning at location 0. Once loaded the contents of location 0 is checked. If it contains 240, operation is transferred to the routine beginning in location 0. If location 0 does not contain 240, the boot is restarted. Restarts will occur 2000 times before the machine is halted automatically.

4.3.2.4.2 TA11 CASSETTE - This bootstrap is identical to that of the RX11 except that data is loaded from the cassette beginning at the second block.

4.3.2.4.3 PC11 PAPER TAPE READER - Loads an Absolute Loader formatted tape into the upper memory locations XXX746 to XXX777 (XXX is dependent on memory size). Once loading is completed, the boot transfers operation to a routine beginning at location XXX752. In systems containing an M9301-YA which is set up not to run diagnostics

TEST 1 thru TEST 5, XXX will become 017 not the upper part of memory.

4.3.2.4.4 - DISKS (excluding RX11) - Load 1000 words (2000 bytes) of data from the disk into memory locations 0-1776.

4.3.2.4.5 MAGTAPE - TM11 - Loads second record (1000 bytes maximum size) from the magtape into memory location 0-777. TJU16 - Load second record (2000 bytes maximum size) from magtape into memory locations 0-1777.

4.3.2.4.6 CONSOLE EMULATOR - When this routine is used in conjunction with the user's terminal, functions quite similar to those found on the programmer's console of traditional PDP11 family computers are generated, as shown in the summary below. The description of the operation that follows assumes that the user's M9301 module is configurated to enter the console emulator routine (DIP switch settings for emulator are shown in TABLE(3) on POWER UP or whenever the BOOT switch is depressed.

                A SUMMARY OF THE CONSOLE EMULATOR FUNCTIONS

LOAD -   This function loads the address to be manipulated into
                the system

EXAMINE -   Allows the operator to examine the contents of the
                address that was loaded and or deposited.

DEPOSIT -   Allows the operator to write into the address that was
                loaded and/or examined

START -   Initializes the system and starts execution of the
                program at the address loaded

BOOT -   Allows the booting of a specified device by typing in a
                two character code and unit number.

Console Emulator Operation

The console emulator allows the user to perform load, examine, deposit, start, and boot operations by typing in appropriate code on the keyboard. The combination of the console emulator routine and the keyboard will be referred to as "The Console Emulator".

Discussion of the Simplified Operator's Flow Chart

Introduction

The simplified operator's flow chart of the console emulator routine (which will be referred to as the Operator's Flow Chart) is presented at this point in the text, to give the reader a unified picture of the console emulator routine.

Detailed discussions of each aspect of the chart are presented in Sections in the following paragraphs.

Symbols

Rectangle

Rectangles indicate automatic operations which are performed by the machine. There is only one entrance and one exit on a rectangle.
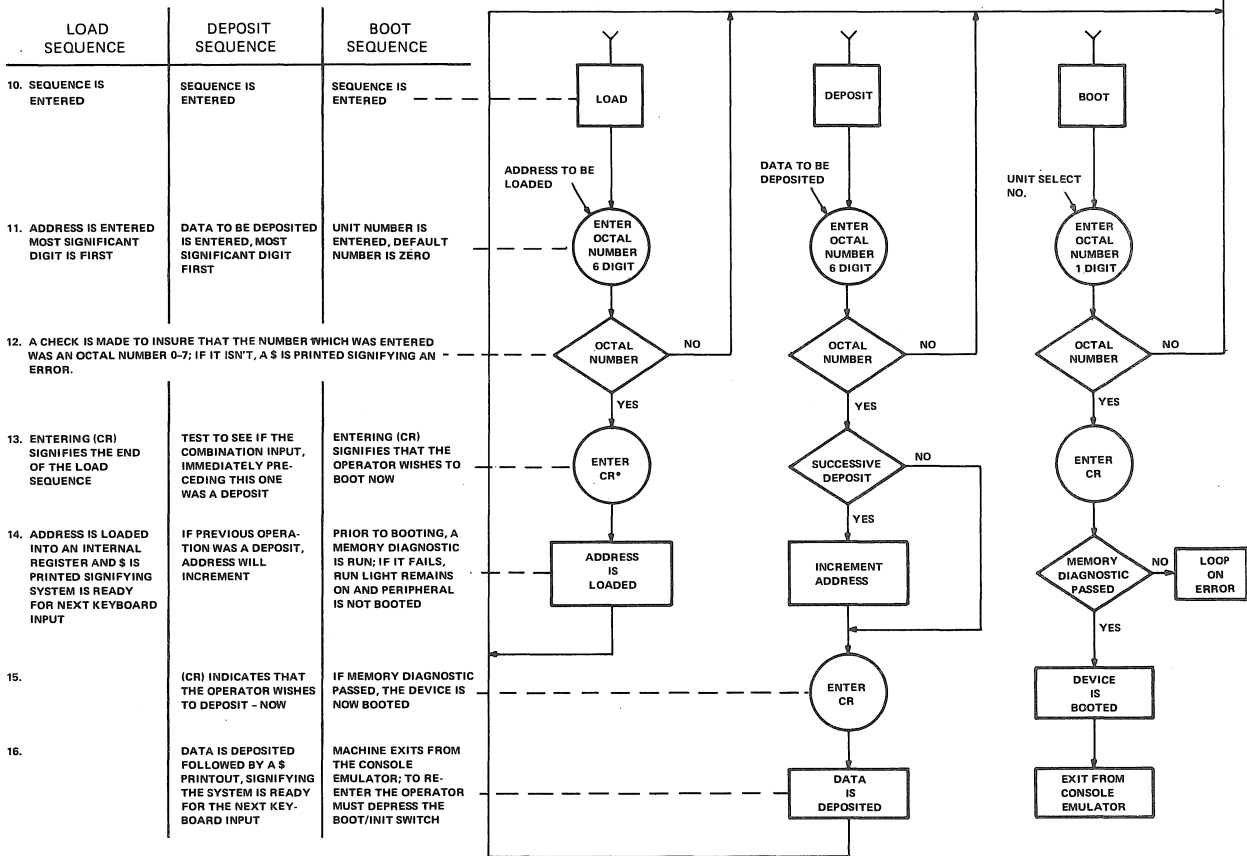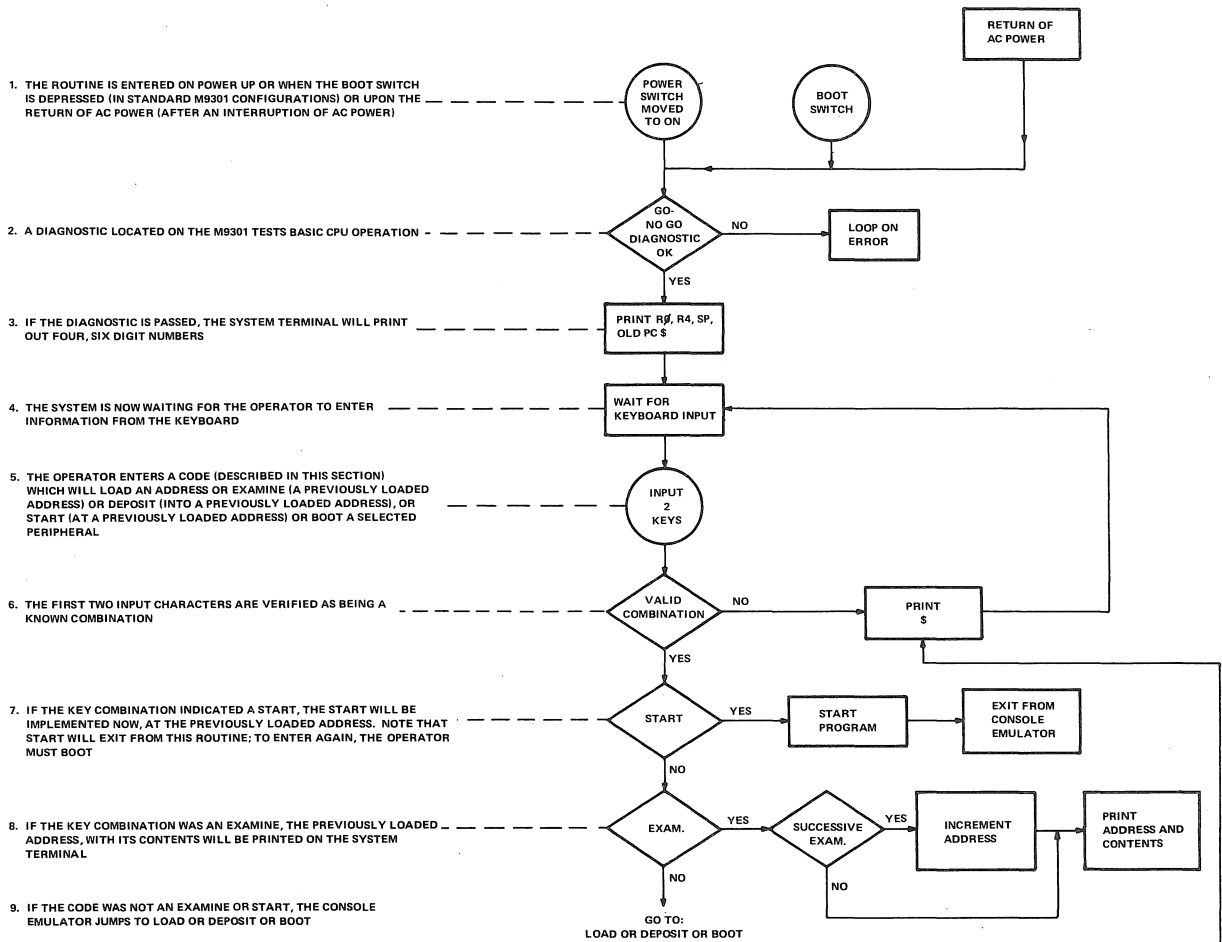
Diamond

A diamond indicates an automatic operation which can take either of two paths depending on how the question stated within the diamond is answered.

Circle

A circle indicates operator action, and the moving of a switch or the typing of keys.

SIMPLIFIED OPERATOR'S FLOWCHART OF THE CONSOLE EMULATOR ROUTINE

(FOR STANDARD M9301 CONFIGURATIONS)

RETURN OF
AC POWER

1. THE ROUTINE IS ENTERED ON POWER UP OR WHEN THE BOOT SWITCH IS DEPRESSED (IN STANDARD M9301 CONFIGURATIONS) OR UPON THE RETURN OF AC POWER (AFTER AN INTERRUPTION OF AC POWER)

POWER SWITCH MOVED TO ON

BOOT SWITCH

2. A DIAGNOSTIC LOCATED ON THE M9301 TESTS BASIC CPU OPERATION

GO-NO GO DIAGNOSTIC OK — NO → LOOP ON ERROR

YES

3. IF THE DIAGNOSTIC IS PASSED, THE SYSTEM TERMINAL WILL PRINT OUT FOUR, SIX DIGIT NUMBERS

PRINT RØ, R4, SP, OLD PC $

4. THE SYSTEM IS NOW WAITING FOR THE OPERATOR TO ENTER INFORMATION FROM THE KEYBOARD

WAIT FOR KEYBOARD INPUT

5. THE OPERATOR ENTERS A CODE (DESCRIBED IN THIS SECTION) WHICH WILL LOAD AN ADDRESS OR EXAMINE (A PREVIOUSLY LOADED ADDRESS) OR DEPOSIT (INTO A PREVIOUSLY LOADED ADDRESS), OR START (AT A PREVIOUSLY LOADED ADDRESS) OR BOOT A SELECTED PERIPHERAL

INPUT 2 KEYS

6. THE FIRST TWO INPUT CHARACTERS ARE VERIFIED AS BEING A KNOWN COMBINATION

VALID COMBINATION — NO → PRINT $

YES

7. IF THE KEY COMBINATION INDICATED A START, THE START WILL BE IMPLEMENTED NOW, AT THE PREVIOUSLY LOADED ADDRESS. NOTE THAT START WILL EXIT FROM THIS ROUTINE; TO ENTER AGAIN, THE OPERATOR MUST BOOT

START — YES → START PROGRAM → EXIT FROM CONSOLE EMULATOR

NO

8. IF THE KEY COMBINATION WAS AN EXAMINE, THE PREVIOUSLY LOADED ADDRESS, WITH ITS CONTENTS WILL BE PRINTED ON THE SYSTEM TERMINAL

EXAM. — YES → SUCCESSIVE EXAM. — YES → INCREMENT ADDRESS → PRINT ADDRESS AND CONTENTS

NO / NO

9. IF THE CODE WAS NOT AN EXAMINE OR START, THE CONSOLE EMULATOR JUMPS TO LOAD OR DEPOSIT OR BOOT

GO TO:
LOAD OR DEPOSIT OR BOOT

LOAD SEQUENCE	DEPOSIT SEQUENCE	BOOT SEQUENCE			
10. SEQUENCE IS ENTERED	SEQUENCE IS ENTERED	SEQUENCE IS ENTERED	LOAD	DEPOSIT	BOOT
			ADDRESS TO BE LOADED	DATA TO BE DEPOSITED	UNIT SELECT NO.
11. ADDRESS IS ENTERED MOST SIGNIFICANT DIGIT IS FIRST	DATA TO BE DEPOSITED IS ENTERED, MOST SIGNIFICANT DIGIT FIRST	UNIT NUMBER IS ENTERED, DEFAULT NUMBER IS ZERO	ENTER OCTAL NUMBER 6 DIGIT	ENTER OCTAL NUMBER 6 DIGIT	ENTER OCTAL NUMBER 1 DIGIT
12. A CHECK IS MADE TO INSURE THAT THE NUMBER WHICH WAS ENTERED WAS AN OCTAL NUMBER 0-7; IF IT ISN'T, A $ IS PRINTED SIGNIFYING AN ERROR.			OCTAL NUMBER — NO	OCTAL NUMBER — NO	OCTAL NUMBER — NO
			YES	YES	YES
13. ENTERING (CR) SIGNIFIES THE END OF THE LOAD SEQUENCE	TEST TO SEE IF THE COMBINATION INPUT, IMMEDIATELY PRECEDING THIS ONE WAS A DEPOSIT	ENTERING (CR) SIGNIFIES THAT THE OPERATOR WISHES TO BOOT NOW	ENTER CR*	SUCCESSIVE DEPOSIT — NO	ENTER CR
14. ADDRESS IS LOADED INTO AN INTERNAL REGISTER AND $ IS PRINTED SIGNIFYING SYSTEM IS READY FOR NEXT KEYBOARD INPUT	IF PREVIOUS OPERATION WAS A DEPOSIT, ADDRESS WILL INCREMENT	PRIOR TO BOOTING, A MEMORY DIAGNOSTIC IS RUN; IF IT FAILS, RUN LIGHT REMAINS ON AND PERIPHERAL IS NOT BOOTED	ADDRESS IS LOADED	YES → INCREMENT ADDRESS	MEMORY DIAGNOSTIC PASSED — NO → LOOP ON ERROR
					YES
15.	(CR) INDICATES THAT THE OPERATOR WISHES TO DEPOSIT – NOW	IF MEMORY DIAGNOSTIC PASSED, THE DEVICE IS NOW BOOTED		ENTER CR	DEVICE IS BOOTED
16.	DATA IS DEPOSITED FOLLOWED BY A $ PRINTOUT, SIGNIFYING THE SYSTEM IS READY FOR THE NEXT KEYBOARD INPUT	MACHINE EXITS FROM THE CONSOLE EMULATOR; TO RE-ENTER THE OPERATOR MUST DEPRESS THE BOOT/INIT SWITCH		DATA IS DEPOSITED	EXIT FROM CONSOLE EMULATOR

*CR = CARRIAGE RETURN KEY

11 - 3283

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CR

CR is the symbol for the carriage return key.

Using the Console Emulator

After The $ -

Once the system has been powered up or booted, and R0, R4, SP, PC and $ have been printed, the console emulator routine can be used.

Keyboard Input Symbols

The discussion of keyboard input format uses the following symbols:

        Space Bar   :   (SB)

        Carriage Return Key :   (CR)

        Any Number 0 - 7

        (Octal Number)key   :   (X)

Keyboard Input Format: Load - Examine deposit start.   All character keys shown in the following discussion represent themselves with the exception of those in parenthesis.

        FUNCTION   KEYBOARD STROKES

        Load Address   L (SB) (X) (X) (X) (X) (X) (X) (CR)

        Examine   E (SB)

        Deposit   D (SB) (X) (X) (X) (X) (X) (X) (CR)

        Start   S (SR)

Order of Significance of Input Keys

The first character that is typed will be the most significant character.   Conversely, the last character that is typed is the least significant character.

Leading Zeros

When an address or data word contains leading zeros, these zeros can be omitted when loading the address or depositing the data.

Example Using the Load, Examine, Deposit, and Start Functions

        Assume that a user wishes to:

1. Turn on power

2. Load address 700

3. Examine location 700

4. Deposit 777 into location 700

5. Examine location 700

6. Start at location 700

	USER	TERMINAL DISPLAY
1.	TURNS ON POWER	XXXXXX XXXXXX XXXXXX XXXXXX
2.	L(SB) 700 (CR)	$ L700
3.	E(SB)	$ E 000700 XXXXXX
4.	D(SB) 777(CR)	$ D 777
5.	E(SB)	$ E 000700 000777
6.	S(CR)	$ S

Even Addresses Only

The console emulator routine will not work with odd addresses.   Even
numbered addresses must always be used.

Successive Operations

Examine

Successive examine operations are permitted. The address is loaded
for the first examine only. Successive examines cause the address to
increment and will display consecutive addresses along with their
contents.

Example of Successive Examine Operation

Examine Addresses 500 - 506

Operator INPUT	Terminal DISPLAY
L(SB 500 CR	L 500
E(SB)	$E 000500 XXXXXX

```
        E(SB)                      $E 000502   XXXXX

        E(SB)                      $E 000504   XXXXX

        E(SB)                      $E 000506   XXXXX
```

Deposit

Successive deposit operations are permitted. The procedure is
identical to that used with examine.

Example of Successive Deposit Operations

Deposit 60 into Location 500
        2 into Location 502
        4 into Location 504

```
        Operator Input          Terminal Display

        L(SB 500 CR             $L 500

        D(SB) 60 CR             $D 60

        D(SB)  2 CR             $D 1
        D(SB)  4 CR             $D 4
```

Alternate Deposit - Examine Operations

This mode of operation will not increment the address.   The Address
will contain the last data which was deposited.

Example of Alternate Deposit - Examine Operations

Load address 500, deposit the following numbers with examines after
every deposit 1000,2000,5420.

```
        Operator Input          Terminal Display

        L(SB) 500 (CR)          $L 500

        D(SB) 1000 (CR)         $D L000

        E(SB)                   $E 000500    001000

        D(SB) 2000 (CR)         $D 2000

        E(SB)                   $E 000500    002000

        D(SB) 5420 (CR)         $D 5420

        E(SB)                   $E 000500    005420
```

Alternate Examine - Deposit Operations

If an examine is the first instruction after a load sequence, and is
alternately followed by deposits and examines, the address will not be
incremented, and the address will contain the last data which was
deposited. (The above example applies to this operation, with the
exception of the order of examine and deposit, the end result is the
same).

Limits of Operation

The M9301 console emulator routine can directly manipulate the lower
28K of memory and the 4K I/O page. See section 5, for an explanation
of techniques required to access addresses above the lower 28K.

Booting From The Keyboard

Once the $ symbol has been displayed in response to system power
coming up, or the boot switch being depressed, the system is ready to
load a bootstrap from the device which the operator selects.

Console Emulator Boot Procedures

1. Find the two character boot command code on either Table 3 or
   Table 4, that corresponds to the peripheral to be booted.

2. Load papertape, magtape, disc, etc, into the peripheral to
   be booted if required.

3. Verify that the peripheral indicators signify that the
   peripheral is ready (if applicable).

4. Type two character code obtained from the table.

5. If there is more than one unit of a given peripheral, type
   the unit number to be booted (0 - 7) if no number is typed,
   the default number will be 0.

6. Type (CR), this initiates the boot.

Before Booting...

Always Remember:

1. The medium (Paper tape, disc, magtape, cassette, etc,) must
   be placed in the peripheral to be booted prior to booting.

2. The machine will not be under the control of the console
   emulator routine after booting.

3. The program which is booted in must:

1) be self starting or 2) allow the user to load another program by using the CONT function or 3) be prestartable after the console emulator is recalled.

3. Actuating the boot switch will always abort the program being run. The contents of the general registers (R0-R7) will be destroyed. There is no way to continue with the program which was aborted. Some program are designed to be restartable.

Example: Booting the High Speed Reader Using The

Console Emulator

An operator wishes to load the CPU Diagnostic for an 11/39 computer system. The system has a high speed reader.

Procedure:

1. Place the HALT/CONT switch in the CONT position.

2. Obtain a $by:

   a. Turning on system power

   b. Actuating the boot.

      (R0, R4, SP, and PC will be printed prior to the $.)

3. Place the absolute loader paper tape (coded leader section) in the high speed reader.

4. Type: PR (CR)

   The absolute loader tape will be loaded, and the machine will halt.

5. Remove the absolute loader and place the leader of the program, in this case a CPU Diagnostic, in the reader.

6. Move the HALT/CONT switch to HALT and then return it to CONT. The diagnostic will be loaded and the machine will halt (normal for this programming, non-diagnostic programs could be self starting).

7. If program is not self starting activate the BOOT/INIT switch, this will restart the console emulator routine.

8. Using the console emulator, deposit desired functions into the Software Switch Register (a memory address) location. See the diagnostic for the software switch register's actual location and significance.)

9. Using the console emulator, load the starting address, and start the program as described earlier in this section.

Example of Booting A Disc Using the Console Emulator

A user wishes to boot the system's RK11 Disk, which contains the CPU Diagnostic which the user wants to run.

Procedure:

1. Verify the the HALT/CONT switch is in the CONT position and the write lock switch on the RK11 peripheral is in the ON position.

2. The user turns on system power. The system terminal displays R0, R4, SP and PC which are random binary numbers. Followed by a $ on the next line.

3. The user placed the disk pack into drive zero.

4. When the RK05 load light appears, the system is ready to be booted.

5. The user type in: DK (CR)

    This causes the loading of the bootstrap routine into memory and the execution of that routine.

6. The program should identify itself and initiate a dialogue (which won't be discussed here).

CONSOLE EMULATOR

The following discussion will describe the effects of entering information incorrectly to the console emulator routine.

Symbols

Space Bar   -   (SB)

Carriage Return Key   -   (CR)

Any Octal Number (0 - 7) Key (X)

Non-Octal Number (8 or 9) keys (9)

(Y) - Represents:

1. All Keys (other than numerics which are unknown.

2. Keys which are known but do not consitute a valid code in the
   context which they are entered.

Refer to previous sections for a discussion of the correct method
operating the console emulator routine.

ESCAPE ROUTE

If an entry has not been completed and the user realizes that an
incorrect or unwanted character has been entered, depress the rub out
or delete key. This action will void the entire entry and allow the
user to try again.

DEPOSIT   ERROR   USEFUL   EXAMPLES

ERROR	RESULT	REMEDY	OPERATOR	TERMINAL
L was followed by a key other than (SB)	Terminal display will immediately return a $ to signify an unknown code. No address is loaded.	Try again.	L(Y)	$L $ $
An illegal (non octal) number (8 or 9) is typed after the correct load entrance, within an otherwise valid number.	Upon receipt of the illegal number, the console will ignore the entire address and return a $.	Try again.	L(SB)XXX9	$LXXX $
An incorrect alpha key is typed after the correct load entrance within an otherwise valid number.	Same as illegal no.	Try again.	L(SB) XXXX	$L XXX $
The most significant octal number in a six bit address is greater than one.	An address will be loaded, however, the state of the most significant address bit will be determined by bit 15 only: 2 = 0 3 = 1 4 = 0 5 = 1 6 = 0 7 = 1	Try again if required.	S(SB) 6XXXXXX	$L 0XXX $
An unwanted byte legal octal number is loaded.	Address will be loaded, but unchanged.	Try again.		
An extra (seventh) octal number is typed.	The loaded number will be incorrect. The system will accept any size word but will only remember the last six characters typed in.	Try again.	L(SB) 1XXXXXX	$L 1XXX $ Actually Load 1XXXXXX
A memory location higher than the highest memory location available in the machine is loaded.	No errors will result unless a deposit, examine, or start is attempted.	Try again.	L(SB) 1XXXX (CR)	L 1XXXXX
Load entrance and number were entered correctly, (CR) wasn't entered.	Machine will wait indefinitely for (CR) $ will not be returned.	Type (CR)	L(SB) XXXXX (CR)	$L XXXXX $XXX(CR)
E or S is followed by a key other than space.	Terminal display will immediately return a $ to signify an unknown co	Try again.	E(Y) or S(X)	$E =$ or $S $

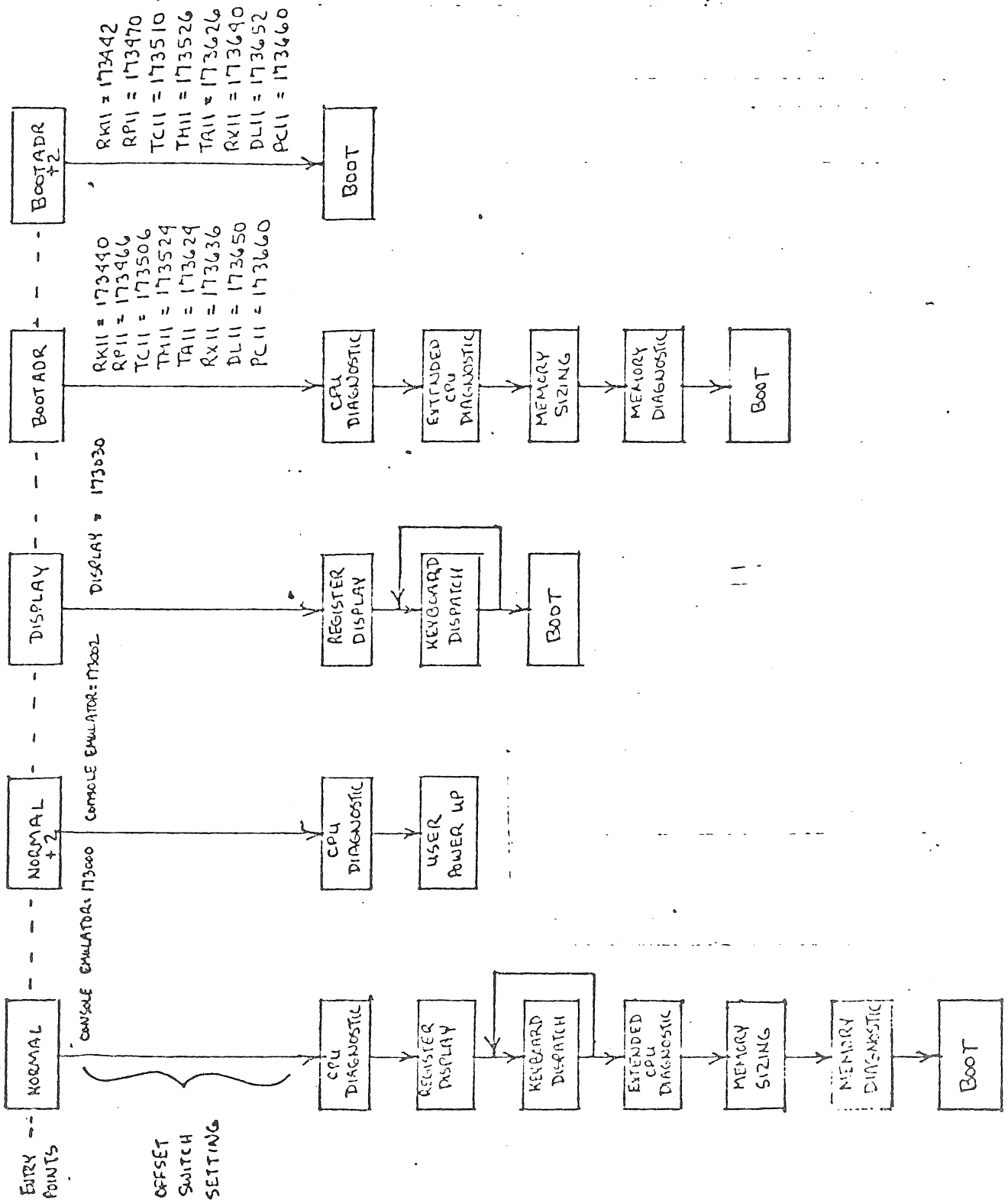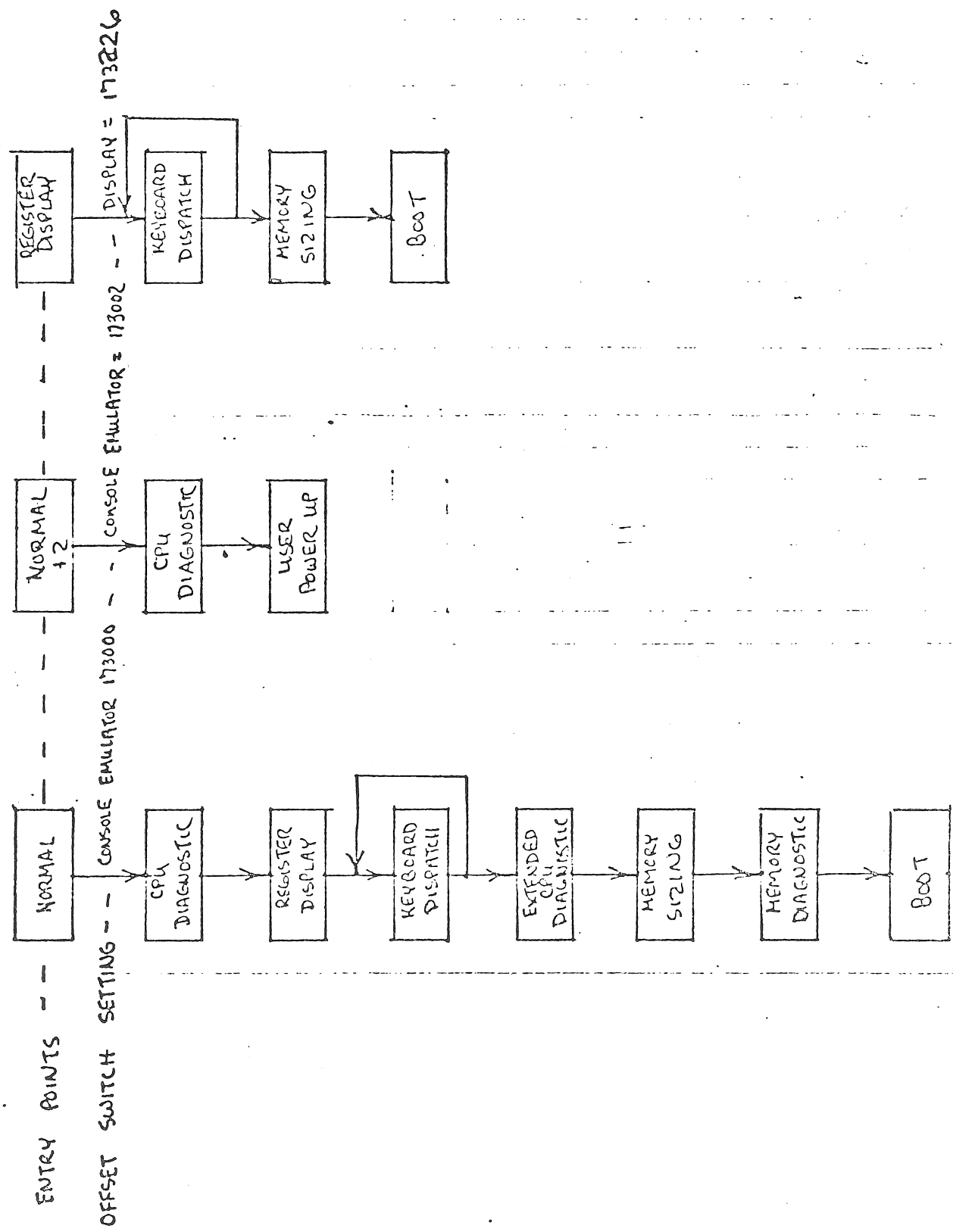|				
Examine or start is attempted to a memory location which is higher than the highest available memory location in the machine I/O page can be examined) or an odd memory location.	The system will hang up when (SB) is executed.	Depress the boot switch.	E(SB) or S(SB)	$E or $S
Examine is performed without loading an address prior to first examine.	Examine of an unknown address will be performed. It is possible to access an address which doesn't exist. The system may hangup in a program loop.	Try again or boot if system hangs up.		
Start is performed without loading an address prior to starting.	Start at an unknown location will occur.	Reload program and try again.		
D was followed by a key other than space.	Terminal display will immediately return a $ to signify an unknown code.	Try again.	D)Y)	$D $
Deposit is attempted to a memory location which is higher than the highest available memory location in the machine (with the exception of the I/O page).	The system will hang up when (SB) is executed.	Activate the boot switch to reboot the system.		
Deposit is performed without loading an address or knowing what address has been previously loaded.	a. Data will be written over and lost.	a. Immediately following the error, perform an examine to determine the access which was deposited into. Restore original contents if known.		
	b. Machine might hand up in a program loop.	b. Reboot machine.		
Deposit is attempted into an odd address.	The system will hang up when (CR) is executed.	Depress the boot switch.		

FIGURE 12
M9301 - YA PROGRAM FLOW

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ENTRY POINTS: NORMAL -- NORMAL +2 -- DISPLAY -- BOOT ADR -- BOOT ADR +2

CONSOLE EMULATOR: 173000

NORMAL:
CONSOLE EMULATOR: 173000
OFFSET SWITCH SETTING →
CPU DIAGNOSTIC → REGISTER DISPLAY → KEYBOARD DISPATCH → EXTENDED CPU DIAGNOSTIC → MEMORY SIZING → MEMORY DIAGNOSTIC → BOOT

NORMAL +2:
CONSOLE EMULATOR: 173002
CPU DIAGNOSTIC → USER POWER UP

DISPLAY:
DISPLAY = 173030
REGISTER DISPLAY → KEYBOARD DISPATCH → BOOT

BOOT ADR:
RKII = 173440
RPII = 173466
TCII = 173506
TMII = 173524
TAII = 173624
RXII = 173636
DLII = 173450
PCII = 173660
CPU DIAGNOSTIC → EXTENDED CPU DIAGNOSTIC → MEMORY SIZING → MEMORY DIAGNOSTIC → BOOT

BOOT ADR +2:
RKII = 173442
RPII = 173470
TCII = 173510
TMII = 173526
TAII = 173626
RXII = 173640
DLII = 173652
PCII = 173660
BOOT

FIGURE 13

M9301-YB - PROGRAM FLOW

ENTRY POINTS —

OFFSET SWITCH SETTING —

4.3.2.5 Program Flow of M9301-YA and M9301-YB - Figure 12 and Figure 13 show the program flows for the M9301-YA and M9301-YB respectively. Note that entry points are dependent on the switch settings S1-1 thru S1-10 on the M9301 module. Addresses which must be generated for the various devices are shown next to each entry.

4.3.3 Installation

As a universal bootstrap/terminator module, the M9301-YA and M9301-YB can be adapted by the user to meet a variety of boot requirements and system configurations. Major factors that must be considered during installation are as follows.

4.3.3.1 Power Up Reboot Enable - Automatic booting on all power ups can be enabled or disabled using the POWER UP REBOOT ENAB switch ((S1-2). If this DIP switch is set to the "OFF" position, the processor will power up normally obtaining a new PC from memory location 24(8) and a new PSW from location 26(8). When the switch is set the "ON" position, the processor will obtain its new PC from location 173024(8) which happens to be the address of the BOOT SELECT switches S1-3 thru S1-10.

The function performed by the REBOOT ENABLE switch (S1-2) can be remoted to an external switch using the FAST-ON tabs on the M9301 MODULE. THIS EXTERNAL SWITCH CLOSURE SHOULD BE MADE TO GROUND (ENABLING BOOT) USING FAST ON tab TP3 as a ground return. In the PDP 11/04, AND 34, when MOS memory is present with battery backup, a battery status indication signal is generated by the power supply. This signal should be attached to the POWER UP REBOOT ENAB input (TP2) on the M9301. If this status signal goes low, the contents of the MOS memory is no longer valid and must be reloaded, usually from some mass storage device. The M9301, sensing the status of the memory forces a boot on power up, allowing new data to be written into memory.

If the battery status input is high (logic "1"), the M9301 will not automatically boot on power up, and execution will begin at the address specified by location 24.

4.3.3.2 LOW ROM Enable - This DIP switch S1-1) when set to the "OFF" position prevents the M9301 from responding to the UNIBUS address range 76500 thru 756777. On both the M9301-YA and M9301-YB, this address space is occupied by the DISKETTE (RX11) and CASSETTE (TA11) bootstraps.

4.3.3.3 Boot Switch Selection - To select which device boot will be run on power-ups and external boot enables, eight DIP switches (S1-3 thru S1-10) are provided on both the M9301-YA and M9301-YB. Actual

ON-OFF selection of each switch for the various devices are shown in TABLE 3.

4.3.3.4 External Boot Switch - A device can be externally booted using the EXTERNAL BOOT input on FAST ON tab TP1. If this input is brought to ground, BUS AC LO L will be activated causing the processor to perform a POWER FAIL. Upon returning to a logic "1", this input will deactivate BUS AC LO L initiating a POWER UP sequence in the CPU and thus the boot select switches, FAST ON tab TP3 should be used as a ground return for the external boot switch.

4.4 M9301-YC

This version of the M9301 has been created specifically for the 11/70. If contains basic CPU, cache and Memory diagnostics in additon to booting from one of 9 devices. It also includes the capability of booting into other than the lowest bank of physical memory.

Physical Differences from M9301

The M9301-YC variation uses 4, Tri-State ROM'S which contain information used by the 11/70. The module also requires pull-up resister for the Bus Grant lines on the Unibus.

11/70 Bisic Diagnostics

4.4.1 Memory Map

See Fig. (14)

CACHE   MEMORY
DIAGNOSTICS

BOOTSTRAP

PROGRAM
                              17773000

CPU AND MEMORY

DIAGNOSTICS

                              17765000

FIGURE 14
M9301-YC PROGRAM MEMORY MAP

4.4.2 General Description

The diagnostic portion of the program will test the basic CPU, including: the branches, the registers, all addressing modes, and most of the instructions in the PDP-11 repertoire. It will then set the stack pointer to kernel D-space P.A.R. 7, check and turn on, if requested, memory management and the unibus map, and check memory from virtual address 100 to 157776. After main memory has been verified, with the cache off, the cache memory will be tested to verify that "hits" occur properly, then main memory will be scanned again to insure that the cache is working properly throughout the 28K of memory to be used in the "boot" operation.

If one of the cache memory tests fails, the operator can attempt to "boot" the system anyway by pressing "Continue". This will cause the program to force "Misses" in both groups of the cache before going to the bootstrap section of the program.

4.4.3 Diagnostic Test Descriptions

See fig. 15

TEST1   THIS TEST VERIFIES THE UNCONDITIONAL BRANCH

THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN THIS TEST IS ENTERED AND THEY SHOULD REMAIN THAT WAY UPON THE COMPLETION OF THIS TEST.

TEST2   TEST CLR, MODE "0", AND "BMI","BVS",BHI",BLOS"

THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN THE THIS TEST IS ENTERED. OPEN COMPLETION OF THIS TEST THE "SP" (R6) SHOULD BE ZERO AND ONLY THE "Z" FLOP-FLOP WILL BE SET.

TEST3   TEST "DEC", MODE "0", AND "BPL","BGE","BGT","BLE"

UPON ENTERING THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTER ARE: R0 = ?, R1 = ? R2 = ?
R3= ? R4 = ? R5 = ? SP = 000000
UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
N = 1, Z = 0, V = 0, AND C = 0
THE REGISTERS AFFECTED BY THE TEST ARE:
SP = 177777

```
TEST1     THIS TEST VERIFIES THE UNCONDITIONAL BRANCH
TEST2     TEST "CLR", MODE "0", AND "BMI","BVS","BHI",BLOS"
TEST3     TEST "DEC", MODE "0", AND "BPL", "BEQ",BGE",BGT",BLE"
TEST4     TEST "ROR", MODE "0", AND "BVC","BHIS",BHI",BNE"
TEST5     TEST "BHI", "BLT", AND "BLOS".
TEST6     TEST "BLE" AND "BGT"
TEST7     TEST REGISTER DATA PATH AND MODES "Z", "3", "6"
TEST10    TEST "ROL","BCC", "BLT", AND MODE "6"
TEST11    TEST "ADD", "INC", "COM", AND "BCS", "BLE"
TEST12    TEST "ROR", "BIS", "ADD", AND "BLO", "BGE"
TEST13    TEST "DEC" AND "BLOS", "BLT"
TEST14    TEST "COM", "BIC", AND "BGT", "BGE", "BLE"
TEST15    TEST "ADC", "CMP", "BIT", AND "BNE", "BGT", "BEQ"
TEST16    TEST "MOVB", "SOB", "CLR", "TST" AND "BPL", "BNE"
TEST17    TEST "ASR", "ASL"
TEST20    TEST ASH, AND SWAB
TEST21    TEST 16 KERNEL P.A.R.'S
TEST22    TEST AND LOAD KIPDR'S
TEST23    TEST "JSR", "RTS", "RTI", & "JMP"
TEST24    LOAD AND TURN ON MEMORY MANAGEMENT AND THE UNIBUS MAP
TEST25    TEST MAIN MEMORY FROM VIRTUAL 100 TO 28K
BOOTSTRAP ENTRY POINT IS AT 17773000
CODE TO WAIT FOR TU10 TO COME ON LINE
THIS IS THE CODE TO READ THE SWITCH REGISTER AND DECODE IT
THIS IS THE START OF THE TM11/TU10 BOOT STRAP (MAGNETIC TAPE, TM11)
THIS IS THE START OF THE TC11/TU56 BOOT STRAP (DECTAPE, TC11-G)
THIS IS THE START OF THE RK11/RK05 BOOT STRAP (DECPACK DISK CARTRIDGE
THIS IS THE START OF THE RP11/RP03 BOOT STRAP (DISK PACK, RP11-C)
THIS IS THE START OF THE COMMON READ CODE
THIS IS THE START OF THE RH70/TU16 BOOT STRAP (MAGNETIC TAPE SYSTEM,
THIS IS THE START OF THE RH70/RP04 BOOT STRAP (DISK PACK, RWP04)
THIS IS THE START OF THE RH70/RS04 BOOT STRAP (FIXED HEAD DISK, RWS04)
THIS IS THE START OF THE COMMON RH-70 CODE
THIS IS THE START OF THE RX11/RX01 BOOT STRAP (FLOPPY DISK)
THIS IS THE START RESERVED FOR A FUTURE DEVICE
FUNCTION CODES FOR THE ALL OF THE DEVICES
COMMAND AND STATUS REGISTER ADDRESS TABLE
FUNCTION POINTER TABLE
STARTING ADDRESS TABLE
CACHE MEMORY DIAGNOSTIC TESTS
TEST26    TEST CACHE DATA MEMORY
TEST27    TEST VIRTUAL 28K WITH CACHE ON
```

Figure (15)

TEST4   TEST "ROR", MODE "0", AND "BVC","BHIS","BHI","BNE",

UPON ENTERING THIS TEST THE CONDITION CODES ARE:
N = 1, Z = 0, V = 0, AND C = 0.
THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
R3 = ? R4 = ? R5 = ? SP = 177777
UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
N = 0, Z = 0, V = 1, AND C = 1
THE REGISTERS AFFECTED BY THE TEST ARE:
SP = 077777

TEST5   TEST "BH1", "BLT", AND "BLOS"

UPON ENTERING THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 0, V = 1, AND C = 1.
THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
R3 = ? R4 = ? R5 = ? SP = 077777
UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
N = 1, Z = 1, V = 1, AND C = 1
THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.

TEST6   TEST "BLE" AND "BGT"

UPON ENTERING THIS TEST THE CONDITION CODES ARE:
N = 1, Z = 1, V = 1, AND C = 1.
THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
R3 = ? R4 = ? R5 = ? SP = 077777
UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
N = 1, Z = 0, V = 1, AND C = 1
THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.

TEST7   TEST REGISTER DATA PATH AND MODES "2", "3", "6"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 1, Z = 0, V = 1, AND C = 1.
THE REGISTER REGISTER ARE: R0 = ?, R1 = ?, R2 = ?
RR3 = ?, R4 = ?, R5 =?, SP = 077777.
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE LEFT AS FOLLOWS:

R0 = 125252, R1 = 000000, R2 = 125252, R3 = 125252
R4 = 125252, R5 = 125252, SP = 125252, AND MAPL00 = 125252

TEST10 TEST "ROL", "BCC", "BLT", AND MODE "6"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252.
MAPL00 = 125252

UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 0, V = 1, AND C = 1.
THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
MAPL00 WHICH SHOULD NOW EQUAL 052524.

TEST11 TEST "ADD", "INC", "COM", AND "BCS", "BLE"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 0, Z = 0, V = 1, AND C = 1.
THE REGISTERS ARE: R0 = 125252, R1 = 00000, R2 = 125252
R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252,
MAPL00 = 052524.
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
R3 WHICH NOW EQUALS 000000, AND R1 WHICH IS ALSO 000000

TEST12 TEST "ROR", "BIS", "ADD", AND "BLO", "BGE"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
R3 = 030000, R4 = 125252, R5 = 125252, SP = 125252,
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
R3 WHICH SHOULD BE MODIFIED BACK TO 000000, AND
R4 WHICH SHOULD NOW EQUAL 052525

TEST13 TEST "DEC" AND "BLOS", "BLT"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 1, Z = 0, V = 0, AND C = 0.
THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
R1 WHICH SHOULD NOW EQUAL 177777

TEST14 TEST "COM , "BIC",AND "BGT", "BLE"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 1, Z = 0, V = 0, AND C = 0.
THE REGISTERS ARE: R0 = 125252, R1 = 177777, R2 = 125252
R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252,
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 0, V = 1, AND C = 1.
THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
R0 WHICH SHOULD NOW EQUAL 052525, AND
R1 WHICH SHOULD NOW EQUAL 052524

TEST15   TEST "ADC", "CMP", "BIT", AND "BNE", "BGT","BEQ"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 0, Z = 0, V = 1, AND C = 1.
THE REGISTERS ARE: R0 = 052525, R1 = 052524, R2 = 125252
R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE NOW:
R0 = 052525, R1 = 000000, R2 = 125252, R3 = 000000
R4 = 052525, R5 = 052525, SP = 125252,

TEST16   TEST "MOVB","SOB", "CLR", "TST" AND "BPL", "BNE"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE: R0 = 052525, R1 = 000000, R2 = 125252
R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252,
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
R0 IS DECREMENTED BY A SOB INSTRUCTION TO 000000
R1 IS CLEARED AND THEN INCREMENTED AROUND TO 000000

TEST17   TEST "ASR", "ASL"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0.
THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252,
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 0, V = 0, AND C = 0.
THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
R0 WHICH IS NOW EQUAL TO 000000.
R1 WHICH IS NOW 000001, AND
R2 WHICH IS NOW 000000.

TEST20   TEST ASH, AND SWAB

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 0, Z = 0, V = 0, AND C = 0,
THE REGISTERS ARE: R0 = 000000, R1 = 000001, R2 = 000000
R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252,
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 1,
THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
R1 WHICH SHOULD NOW EQUAL 000000

TEST21   TEST 16 KERNEL P.A.R.'S

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 1.

THE REGISTERS ARE: R0 = 000000, R1 = 000000, R2 = 000000
R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252,
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0,
THE REGISTERS NOW EQUAL:
R0 = 172400, R1 = 000000, R2 = 000000, R3 = 000000
R4 = 052525, R5 = 125252, SP = 125252,
ALL KERNEL P.A.R.'S = 125252,

TEST22   TEST AND LOAD KIPDR'S

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0,
THE REGISTERS ARE: R0 = 172400, R1 = 000000, R2 = 000000
R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252
UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
N = 0, Z = 1, V = 0, AND C = 0
THE REGISTERS THAT ARE MODIFIED ARE:
R0 = 172300, R1 = 000000, R2 = 077406
ALL KERNEL I-SPACE P.D.R.'S (172300 - 172316) = 077406

TEST23   TEST "JSR", "RTS", "RTI", "JMP"

THIS TEST FIRST SETS THE STACK POINTER TO "KDPAR7" (172376),
AND THEN VERIFIES THAT "JSR", "RTS", "RTI", AND "JMP"
ALL WORK PROPERLY.

ON ENTRY TO THIS TEST THE STACK POINTER "SP IS INITIALIZED
TO 172376 AND IS LEFT THAT WAY ON EXIT.

TEST24   LOAD AND TURN ON MEMORY MANAGEMENT AND THE UNIBUS MAP

THIS TEST IS ONLY EXECUTED IF THE UPPER 4 BITS <15:12> OF
THE SWITCH REGISTER ARE NON-ZERO. THE TEST WILL LOAD MEMORY
MANAGEMENT TO RELOCATE TO THE 32K BLOCK NUMBER SPECIFIED.
IT WILL ALSO SET UP THE UNIBUS MAP REGISTER 0 THRU 6 TO
RELOCATE THE UNIBUS ADDRESSES CORRECTLY. (IE. IF BITS <15:12>
SPECIFY BLOCK NUMBER 3, THEN YOU WANT TO BOOT INTO
MEMORY FROM 96K TO 128K. THE KIPAR'S WILL BE LOADED AS FOLLOWS:
KIPAR0 = 006000, KIPAR1 = 006200, KIPAR2 = 006400, KIPAR3 = 076600
KIPAR4 = 007000, KIPAR5 = 007200, KIPAR6 = 007400,)
KIPAR7 WILL ALWAYS EQUAL 177600,
THE UNIBUS MAP REGISTERS WILL THEN BE SET AS FOLLOWS:
MAPL0 = 000000, MAPH0 = 03, MAPL1 = 020000, MAPL1 = 03,
MAPL2 = 040000, MAPH2 = 03, MAPL3 = 060000, MAPH3 = 03,
MAPL4 = 100000, MAPH4 = 03, MAPL5 = 120000, MAPH5 = 03,
MAPL6 = 140000, MAPH6 = 03,

TEST25   TEST MAIN MEMORY FROM VIRTUAL 1000 TO 28K

THIS TEST WILL TEST MAIN MEMORY WITH THE CACHE DISABLED, FROM

VIRTUAL ADDRESS 001000 TO 157776 . IF THE DATA DIES NOT COMPARE
PROPERLY THE TEST WILL HALT AT EITHER 165740 OR 165756, IF A
PARPITY ERROR OCCURS THE TEST WILL HALT AT ADDRESS 165776, WITH
THE PC + 2 ON THE STACK WHICH IS IN THE KERNEL D-SPACE P.A.R.'S.

IN THIS TEST THE REGISTERS ARE INITIALIZED AS FOLLOWS:
R0 = 001000, R1 = DATA READ, R2 = 067400, R3 = 001000
R4 = 067400, R5 = 177746 (CONTROL REG.) SP = 172376

THE FOLLOWING TWO TESTS ARE CACHE MEMORY TESTS, IF EITHER OF
THEM FAILS TO RUN SUCCESSFULLY THEY WILL COME TO A HALT IN
THE M9301 ROM. IF YOU DESIRE TO TRY TO BOOT YOUR SYSTEM, OR
DIAGNOSTIC ANYWAY, YOU CAN PRESS "CONTINUE" AND THE PROGRAM
WILL FORCE MISSES IN BOTH GROUPS OF THE CACHE AND GO TO THE
BOOT STRAP THAT HAS BEEN SELECTED.

TEST26   TEST CACHE DATA MEMORY

THIS TEST WILL CHECK THE DATA MEMORY IN THE CACHE, FIRST GROUP
0 AND THEN GROUP 1. IT LOADS 052525 INTO AN ADDRESS COMPLEMENTS
IT TWICE AND THEN READS THE DATA, THEN IT CHECKS TO INSURE THAT
ADDRESS THE DATA WAS A HIT. THEN THE SEQUENCE IS REPEATED ON THE
SAME WITH 125252 AS THE DTA. ALL CACHE MEMORY DATA LOCATIONS
AE TESTED IN THIS WAY. IF EITHER GROUP FAILS AND THE OPERATOR
PRESSES CONTINUE THE PROGRAM WILL TRY TO BOOT WITH THE CACHE
DISABLED.

THE REGISTERS ARE INTIALIZED AS FOLLOWS FOR THIS TEST:
R0 = 1000 (ADDRESS) R1 = 2 (COUNT), R2 = 1000 (COUNT)
R3 = 1000 (COUNT), R4 = 125252 (PATTERN) R5 = 177746 (CONTROL REG)
SP = 172374 (FLAG OF ZERO PUSHED ON STACK)

TEST27   TEST VIRTUAL 28K WITH CACHE ON

THIS TEST CHECKS VIRTUAL MEMORY FROM 001000 THRU 157776
TO INSURE THAT YOU CAN GET HITS ALL THE WAY UP THROUGH MAIN
MEMORY, IT STARTS WITH GROUP 1 ENABLED, THEN TESTS GROUP 0, AND
FINALLY CHECKS MEMORY WITH BOTH GROUPS ENABLED. IF ANY OF
THE THREE PASSES FAIL THE TEST WILL HALT AT "CONT + 2", THEN
IF THE OPERATOR PRESSES "CONTINUE", THE PROGRAM WILL TRY TO
BOOT WITH THE CACHE DISABLED.

UPON ENTRY THE REGISTERS WILL BE SET UP AS FOLLOWS:
R0 = 001000 (ADDRESS), R1 = 3 (PASS COUNT), R2 = 67400 (MEMORY
COUNTER).
R3 = 1000 (FIRST ADDRESS), R4 = 67400 (MEMORY COUNTER).
R5 = 177746 (CONTROL REG.), SP = 172374 (POINTING TO CODE FOR CONTROL
RE.

UPON COMPLETION OF THIS TEST MAIN MEMORY FROM VIRTUAL ADDRESS
001000 THRU 157776 WILL CONTAIN ITS OWN VIRTUAL ADDRESS.

11/70 Bootstrap

The bootstap portion of the program looks at the lower byte of the
switch register to determine which one of 9 devices and which drive
number to attempt the "BOOT" from, switches <02 : 00> select the drive
number (0 - 7), and switches <06 :03> select the device code (1 -11).
if the lower byte of the switch register is zero, the program will
read the set of switches on the M9301-YC to determine the device and
drive number. These switches can be set by field service to select a
"DEFAULT BOOT" device.

THE DEVICE CODES AND DEVICE NAMES ARE AS FOLLOWS:

1.   TM11/TU10   MAGNETIC TAPE, TM11
2.   TC11/TU56   DECTAPE, TC11-G
3.   RK11/RK05   DECPACK DISK CARTRIDGE, RK11-D
4.   RP11/RP03   DISK PACK, RP11-C
5.   RESERVED
6.   RH70/TU16   MAGNETIC TA[E SYSTEM, TWU16
7.   RH70/RP04   DISK PACK, RWP04
10.   RH70/RS04   FIXED HEAD DISK, RWS04 (OR RWS03)
11.   RX11/RX01   DISKETTE

If the bootstrap operation fails as a result of a hardware error in
the peripheral device the program will do a "RESET" instruction and
jump back to the test that sets up and turns on memory management and
tests memory. Then the program will attempt to "BOOT" again.

4.4.5 Installation

The External Back Switch and Boot on Power-Up options are not
available on the M9301-YC. Therefore Power up REBOOT ENABLE switch on
the module (see schematics) should always be off.

Because it is required that the diagnostic portion of the Bootstrap
always be executed the LOW ROM ENABLE switch on the module (see
schematics) should always be on. The remaining 8 switches should be
set depending on the default device type and unit number desired.
(See starting procedure and schematics).

4.4.6 Starting Procedure

Switch Settings

The lower byte of the switch register should be set to have the drive
number (0 - 7) in switches <02 : 00>, and the device code (1 -11) in
switches <06 : 03>.

The upper byte of the switch register should be set to have the bank
number of the 32k block of memory to be used for the bootstrap

operation (0 - 17) in switches <15 : 12>.

THE DEVICE CODES ARE AS FOLLOW:

```
1.      TM11/TU10     MAGNETIC TAPE, TM11
2.      TC11/TU56     DECTAPE,TC11-G
3.      RK11/RK05     DECPACK DIS CARTRIDGE, RK11-D
4.      RP11/RP03     DISK PACK, RP11-C
5.      RESERVED FOR FUTURE DEVICE
6.      RH70/TU16     MAGNETIC TAPE SYSTEM, TWU16
7.      RH70/RP04     DISK PACK, RWP04
10.     RH70/RS04     FIXED HEAD DISK, RWS04 (OR RWS03)
11.     RX11/RX01     DISKETTE
```

THE MEMORY BLOCKS ARE AS FOLLOWS:

```
0.      PHYSICAL MEMORY 0 - 28K
1.      PHYSICAL MEMORY 32K - 60K
2.      PHYSICAL MEMORY 64K - 92K
3.      PHYSICAL MEMORY 96K - 124K
4.      PHYSICAL MEMORY 128K - 156K
.
.
10.     PHYSICAL MEMORY 256K - 284K
.
14.     PHYSICAL MEMORY 384K - 412K
15.     PHYSICAL MEMORY 416K - 444K
16.     PHYSICAL MEMORY 448K - 476K
17.     PHYSICAL MEMORY 480K - 508K
```

Starting Addresses

The normal starting address for this program is 177765000.

If the diagnostic portion of this program fails and the operator wants to attempt to "BOOT" anyway, he must follow these steps:

   1.   Set up memory management if "BOOTING" into other than the lower 28K of memory.

   2A. If device is on massbus:
        Set stack pointer to a valid address and load that address with the memory bank number he would put into switches <15:12>.

   2B. If device is on unibus:
        Set up unibus map registers 0 thru 6 to map to same memory as memory management.

3.   Deposit address 173000 into the PC.

4.   Set the device code and drive number in the lower byte of the switch register.

5.   Press continue.

Examples:

A.   RP04 --   SET STACK POINTER TO 40000
               LOAD 000000 INTO ADDRESS 40000
               LOAD 173000 INTO THE PC (177777707)
               SET 000070 INTO SWITCHES (RP04) DRIVE 0)
               PRESS "CONTINUE"

B.   RK05 --   LOAD 173000 INTO THE PC (177777707)
               SET 000030 INTO SWITCHES (RK05 DRIVE 0)
               PRESS "CONTINUE"

Operator Action

If the diagnostic portion of the ROM fails record the PC of the "HALT"
instruction and refer to the listing to find out what portion of the
machine failed.

4.4.7 errors

List of error hats indexed by the address displayed

ADDRESS DISPLAYED	TEST NUMBER AND SUBSYSTEM UNDER TEST
17765004	TEST 1 BRANCH TEST
17765020	TEST 2 BRANCH TEST
17765036	TEST 3 BRANCH TEST
17765052	TEST 4 BRANCH TEST
17765066	TEST 5 BRANCH TEST
17765076	TEST 6 BRANCH TEST
17765134	TEST 7 REGISTER DATA PATH TEST
17765146	TEST 10 BRANCH TEST
17765166	TEST 11 CPU INSTRUCTION TEST
17765204	TEST 12 CPU INSTRUCTION TEST
17765214	TEST 13 CPU INSTRUCTION TEST
17765222	TEST 14 "COM" INSTRUCTION TEST
17765236	TEST 14 CPU INSTRUCTION TEST
17765260	TEST 15 CPU INSTRUCTION TEST
17765270	TEST 16 BRANCH TEST
17765312	TEST 16 CPU INSTRUCTION TEST
17765346	TEST 17 CPU INSTRUCTION TEST
17765360	TEST 20 CPU INSTRUCTION TEST
17765374	TEST 20 CPU INSTRUCTION TEST
17765450	TEST 21 KERNEL P.A.R. TEST
17765474	TEST 22 KERNEL P.D.R. TEST
17765510	TEST 23 "JSR" TEST
17765520	TEST 23 "JSR" TEST
17765530	TEST 23 "RTS" TEST
17765542	TEST 23 "RTI" TEST
17765550	TEST 23 "JMP" TEST
17765760	TEST 25 MAIN MEMORY DATA COMPARE ERROR
17766000	TEST 25 MAIN MEMORY PARITY ERROR
	NO RECOVERY POSSIBLE FROM THIS ERROR
17773644	TEST 26 CACHE MEMORY DATA COMPARE ERROR
17773654	TEST 26 CACHE MEMORY NO "HLT"
	PRESSING "CONTINUE" HERE WILL CAUSE
	"BOOT" ATTEMPT FORCING "MISSES"
17773736	TEST 27 CACHE MEMORY DATA COMPARE ERROR
17773746	TEST 27 CACHE MEMORY NO "HIT"
	PRESSING "CONTINUE" HERE WILL CAUSE
	"BOOT" ATTEMPT FORCING "MISSES"
17773764	TEST 25 OR 26 CACHE MEMORY PARITY ERROR
	PRESSING "CONTINUE" HERE WILL CAUSE
	"BOOT" ATTEMPT FORCING "MISSES"

Error Recovery

Most of the above error halts are "HARD failures, which means that
there is no recovery from them. Especially the two (2) main memory
halts are not receiverable, your best bet is to try to "BOOT" into
another 32K bank of memory if it appears to be a main memory failure.

If the processor halts in one of the two cache tests the error can be recovered from. By pressing "CONTINUE" the program will either attempt to finish the test (if at eiter: 17773644 or 17773736) or force "misses" in both groups of the cache and attempt to "BOOT" the system monitor with the cache fully disabled (if at either: 17773654, 17773746, or 17773764).

If this program fails in an uncontrolled manner it might be due to an unexpected trap to location 000004. If this is suspected then load a "000006" into address 000004 and a "000000" into location 000006. This will cause all traps to location 000004 to halt with 000007010 in the address lights so that the operator can examine the CPU error register at location 17777766.

THE BITS IN THE CPU ERROR REGISTER ARE DEFINED AS FOLLOWS:

```
BIT03        = RED ZONE STACK LIMIT
BIT03        = YELLOW ZONE ATACK LIMIT
BIT04        = UNIBUS TIME-OUT
BIT05        = NON-EXISTANT MEMORY (CACHE)
BIT06        = ODD ADDRESS ERROR
BIT07        = ILLEGAL HALT
```

5.0   EXTENDED ADDRESSING

5.1   Extended Addressing (Defination)

The console emulator rouitne normally allows accesses to only the lower 28K of memory and the I/O page (160000(8) to 177776(8)). However, it is possible by use of memory management to use the console emulator to access beyond 28K for the examine and deposit functions. The reader should be familiar with the concepts of memory management in the KD11-E processor.

5.2   Definition of Virtual and Physical Addresses

The processor manipulates 16-bit numbers within general registers and memory locations which it often uses as addresses. These addresses are designated virtual addresses as opposed to physical addresses which are asserted on the Unibus to which devices are hardwired to respond.

5.3   Address Mapping without Memory Management

With memory management disabled (as is the case following depressing the boot switch), a simple hardware mapping scheme converts virtual addresses to physical addresses. Virtual addresses in the 0 to 28K

range are mapped directly into physical addresses in the range from 0 to 28K. Virtual addresses on the I/O age (160000-177776) are mapped into physical addresses in the range from 124K to 128K (360000(8)-377776(8)).

5.4 Address Mapping With Memory Management

With memory management enabled, a different mapping scheme is used. In this scheme, a relocation constant is added to the virtual address to create a physical or 'relocated' address.

Virtual address space consists of eight 4K banks where each bank can be relocated by the relocation constant associated with that bank. The procedure specified in this section allows the user to:

1. Create a virtual address to type into the Load Address command.

2. Determine the relocation constant to relocate the calculated virtual address into the desired physical address.

3. Enabe or disable the memory management hardware.

5.5 Creation of a Virtual Address

The easiest way to create a virtual address is to divide the 18 bit physical address into two separate fields - a virtual address and a physical bank number. The virtual/address is represented by the lower 13 bits and the physical bank by the upper five bits. This creates a virtual address in virtual bank 0. The calculated relocation constant is placed in the relocation register associated with virtual bank 0.

For example, assume a user wishes to access location 533720. The normal access capability of the console is 0 to 28K. This address (533720) is between the 28K limit and the I/O page (760000-777776), and consequently must be accessed as a relocated virtual address, with memory management enabled. The virtual address is 13720(8) in physical bank 25(8) and is derived as follows:

All locations in either bank #25 (520000-537776) or bank #37 (I/O page; 760000-777776) may be accessed through virtual address 000000-017776 and 160000-177776, respectively. The relocation and

descriptor registers in the KD11-E are still accessible since their addresses are within the I/O page.

The relocation constant for physical bank 25 is 005200. This constant is added in the relocation unit to the virtual address, as shown, yielding 533720.

    013720   Virtual address

    520000   Relocated Constant (Table A-1)

    533720   Physical Address

When memory management is enabled all CPU accesses are relocated. Instructions and data access to the console emulator routine will be relocated through virtual bank 7 since their virtual accesses exits in this bank (see Table 5.1 for the corresponding addresses of each of the eight virtual banks). Note that accesses to the I/O page (virtual bank 7) are not automatically relocated with memory management while accesses to the II/O page are automatically relocated when memory management is not utilized.

5.6   Memory Management Registers

The relocation constant that is added to the virutal address is stored in a relocation register. One such register exists for each of the eight virtual banks. In addition to the relocation registers, each bank has its own descriptor register which provides information regarding the types of accesses allowed (read only, read or write, or no access).

The memory management logic also provides various forms of protection against unauthorized access. The corresponding descriptor register must be set up along with the relocation register to allow access anywhere within the 4K bank.

5.7   Address Assignments

The Unibus addresses of the relocation registers and the descriptor registers are given in Table 5.1. The relocation constant to be loaded into the relocation register for each 4K bank is provided in Table 5.2. The data to be loaded in the descriptor register to provide read/write access to the full 4K is always 077406.

The Unibus address of the control register to enable memory management is 177572. This register is loaded with the value 000001 to enable memory management and 0 to disable it.

To complete the example previously described (location 533720), the console routine would be as follows:

```
$L    172340      /Setting relocation register for virtual bank 0
$D     5200       /To access extended memory
$L    172356      /Setting relocation register for virtual bank 7
$D     7600       /To access the I/O page
$L    172300      /Address of descriptor register, virtual
$D    77406       /bank 0
$L    172316      /Address of descriptor register, virtual
$D    77406       /bank 7
$L    177572      /Address of control register; enable
$D        1       /memory management
$L     13720      /Virtual address of location desired
$E   (examine)    /The data in location 533720
                  /will be typed,
```

Table 5.1

Unibus Address Assignments

Virtual Address	Virtual Bank	Relocation Register	Descriptor Register
160000-177776	7	172356	172316
140000-157776	6	172354	172314
120000-137776	5	172352	172312
100000-117776	4	172350	172310
060000-077776	3	172346	172306
040000-057776	2	172344	172304
020000-037776	1	172342	172302
000000-017776	0	172340	172300

Table 5.2

Relocation Constants

Physical Bank Number	Relocation Constant
37	007600
36	007400
35	007200
34	007000
33	006600
32	006400
31	006200
30	006000
27	005600
26	005400
25	005200
24	005000
23	004600
22	004400
21	004200
20	004000
17	003600
16	003400
15	003200
14	003000
13	002600
12	002400
11	002200
10	002000
7	001600
6	001400
5	001200
4	001000
3	000600
2	000400
1	000200
0	000000

Loading a new relocation constant into the relocation register for virtual bank 0 will cause virtual addresses 000000-177776 to access the new physical bank. A second bank can be made accessible by loading the relocation constant and descriptor data into the relocation and descriptor registers for virtual bank 1 and accessing the location through virtual address 020000-037776. Seven banks are accessible in this manner, by loading the proper constants, setting up the descriptor data, and selecting the proper virtual address. Bank 7 (I/O page) must remain relocated to physical bank 37 as it is accessed by the CPU to execute the console emulator routine.

Memory management is disabled by clearing (loading with 0s) the Control Register 177572. It should always be disabled prior to typing a 'boot' command.

The start command automatically disables memory management and the CPU begins executing at the physical address corresponding to the address specified by the previous Load Address command. Depressing the boot switch automatically disables memory management. The contents of the relocation registers are not modified.

The HALT/CONTINUE switch has no effect on memory management.

6.0   M9301-YD

6.1   Purpose

The M9301-YD is programmed to provide transparent pass-through of data between a terminal on a satellite computer and an asynchronous serial line on the same computer. It also contains all of the necessary instructions for requesting a secondary mode program load and for accepting a down-line load on its serial line from another machine using DDCMP protocol. These features enable a PDP-11 computer to be a satellite in a REMOTE-11 system.

6.2   Functionality

6.2.1   Normal Bootstrap (SA=173000)

Ordinarily, when the ROM code is initiated, the satellite comes up in pass-through mode. First, the memory size of the computer is ascertained. Then, necessary communications regions are set up, and the OSOP message "Enter terminal mode" is sent on the serial line. All further communication is in ASCII with the ROM program polling the ready flags in the four control and status registers to determine the next action. XON (^Q) and XOFF (^S) are supported within the satellite computer, and transmission is assumed to be full duplex.

The only way that terminal mode may be discontinued is the receipt of a DDCMP message. The ROM only accepts the messages, "Program load without transfer address", Program load with transfer address", and "Enter terminal mode."

6.2.2 Secondary mode bootstrap.

An alternate start address (173014) will cause the "Enter terminal mode" message to be replaced by "Request secondary mode program load." All other actions are identical to the normal bootstrap. The host machine should respond to this message with a program load so that terminal mode is only transiently activated. The bus addressed 177560-177566 will be addressed during this time. The secondary mode program load message may be used for loading programs in to satellites without terminals or for loading a scroller into a machine with a graphics terminal.

6.2.3 Sending DDCMP Messages

A callable subroutine within the ROM will send DDCMP "Boot" mode messages. Location 162 is loaded by the M9307 with the address of this subroutine. To use it, call by

        MOV   #MSG, R5
        JSR PC, @162

where MSG has the following format

        bytes 0 and 1 contain the number of bytes in the message

        byte 2 has an OSOP code

        bytes 3 through n have the data (if any)

The message is sent using interrupt driven code, but control is not returned to the user program until the message has been completely sent out.

6.2.4 Receiving DDCMP Messages

The boot will automatically receive DDCMP messages if properly initialized and the interrupt for the serial line receive register is enabled. A program to do this follows:

```
    MOV     @#154,R0        ; GET ADDRESS OF DESCRIPTOR BLOCK

    MOV     R0,R2           ; SETUP DESCRIPTON POINTER

    CMP     (R2)+,(R2)+     ; R2 R2 + 4

    MOV     R2,(R0)         ; RESET BUFFER POINTER

    MOV     #-10.,-(R2)     ; BYTE COUNT OF DDCMP HEADER

    CLR     -(R0)           ; INITIALIZE CRC AND FLAGS

    CLR     -(R0)

    CLR     -(R0)           ; ZERO FOR NO COMPLETION ROUTINE

    MOV     #164,-(SP)      ; GET DL ADDRESS INPUT

    ADD     #776,(SP)       ; STATUS REGISTER FROM BOOT

    BIS     #100,@(SP)+     ; ENABLE INTERRUPT

    TST     -4(R0)          ; WAIT UNTIL MESSAGE COMPLETE

    BEQ     .-4

    BMI     ERROR

    CMP     (R0)+,(R0)+     ; POINT TO OSOP CODE
```

To restart the Boot:

JMP @164

The M9301-YD uses locations 150-167 for communications and 172-171 for temporary data during program loads. It also loads location 54 with the high usable memory address. The address in 54 has been adjusted to leave room for buffers and a stack for use by the ROM.

6.3 Using the M9301-YD

The M9301-YD ROM will run of any PDP-11 computer. Two DL-11's are required with the following addresses and vectors:

FUNCTION	ADDRESS	VECTOR
Local terminal	177560	60
Interprocessor	1775610	400

The ROM may be activated by placing the address given for the desired junction in switch register and pressing LOAD ADDRESS, START or by utilizing the prower-up bootstrap feature of the Mm9301. The DIP switches should all be off for normal boot. Secondary mode requires the switches to be set to -----.

6.4 Program Listing.

7.0 APPENDIX

7.1. General description:

This fully decoded 2048 Bit Memory, is organized as 512 words of 4 Bits each. It has TTL compatible inputs and TTL compatible tri-state outputs. There is also one Chip Enable provided whose outputs are bussable to allow for memory expansion capability.

Memory Arrays are addressed in straight binary with full on-chip decoding. An overriding chip-select input is provided which when taken high, will inhibit the function causing all outputs to be in a high-impedance state that neither loads nor drives the bus lines. Data as specified by D.E.C. are permanently programmed into the 2048 Bit locations.

7.2. APPLICABLE DOCUMENTS (Latest revision on data of order):

Digital:

A-SP-7665212-0-0, "Process Compatibility Test Methods.".

A-PS-1900002-GS, "General   Requirements   DEC   Quality Assurance   Specification   for   Bipolar Integrated Circuits".

7.3. REQUIREMENTS:

This device shall meet the following requirements under all operating

conditions and over the full operating Free Air Temperature Range.

7.3.1 Mechanical:

7.3.1.1 Package Configuration: - 16 Pin dual in line shall meet the requirements of Digital Specification A-PS-1900002-GS, Section 1.2.5.

7.3. REQUIREMENTS (Continued)

7.3.1.2 Material (Packaging): - Shall be ceramic or plastic (Epoxy-B) or equivalent). Silicone package shall not be shipped without prior written approval from D.E.C.

7.3.1.3 Pin Configuration: - Shall meet the requirements of Digital, A-PS-1900002-GS, be of uniform high quality, delivered free from grease, oil and other contaminants.

7.3.1.4 Pin Connection Diagram: - Shall meet the requirements of Figure 1.

7.3.1.5 Thermal Resistance:

A. Junction to Ambient:
    $R\theta JA$=+75 C/W maximum (measured in free-air with the device soldered into a printed circuit board).

B. Junction to Case:
    $R\theta JC$=+20 C/W maximum (measured with the device immersed in freon bath).

7.3.2 Electrical:

7.3.2.1 Logic Diagram: - Shall meet requirements of Figure 2.

7.3.2.2 Absolute Maximum Ratings: - Reference Table 1.

7.3.2.3 Recommended Operating Conditions - Reference Table 11.

7.3.2.4 Electrical Characteristics: - Reference Table 111.

7.3.2.5 Test Load and Timing Diagram: - Shall meet the requirements of Figure 3.

7.3.3 Environmental:

7.3.3.1 Temperature:

A. Operating: 0 C to +75 C.
B. Storage: -60 C to +150 C

7.3.3.2 Altitude: - The device shall not be mechanically or electrically damaged at altitudes of 50,000 feet (90mm mercury).

7.3.3.3 Humidity:

A. Operating: 10% to 90% R.H. over the operating temperature range, (non-condensing).

B. Storage: 5% to 95% R.H. over the storage temperature range, (condensing allowed).

7.3 REQUIREMENTS (Continued)

7.3.4 Marking:

Shall contain vendor name or symbol, vendor part number, Pin 1 location and data code.

7.3.5 Process Compatibility Test Methods:

The device shall stay within the initial electrical/mechanical requirements and shall not show any evidence of degradation in cosmetics when subjected to the following methods.

7.3.5.1 Marking: - Digital, A-SP-7665212-0-0, Section 1, Test Method
100,

"Solvent Resistance".

7.3.5.2 Refer to Digital,   A-PS-1900002-GS   for   other   Process
Compatibility Requirements.

7.3.6 Shelf Life:

The device shall meet the intial Electrical/Mechanical requirements
after 1 year at storage requirements for temperature and relative
humidity.

7.3.7 Packaging and Shipping:

Marking on the packagaing shall contain as minimum information,
vendors name or symbol, vendors part number, Purchase Order Number and
quantity. It shall meet I.C.C. requirements for shipment by
airplane, rail and truck. Devices shall be packaged to meet the
requirements of Digital A-PS-1900002-GS.

7.3.8 Digital A-PS-1900002-GS:

General Requirements DEC Quality Assurance Specification for Bipolar
Integrated Circuits shall apply where no other document is
specifically referenced.

7.4. CONFLICT OF REQUIREMENTS:

The requirements of this document shall take precedent over all and
any documents when a conflict arises.

7.5. Approval:

The devices submitted under this specification shall have been
initially approved by Digital Equipment Corporation. Approval shall
be given only after samples representative of the vendors normal
production run have been examined, tested and found to meet the
requirements as specified.

7.6. Construction changes:

Approved vendors who desire at any time to make a change in the
design, materials, process, process control which impact any
requirement, shall submit a written request describing in detail the
changes requested. Also, evidence to justify such changes. The
cognizant engineer will them submit this request to the proper
Engineering Department(s) Component Engineering Group and all product
lines affected. No changes shall be incorporated until written
approval has been received from the above mentioned group or groups
authorized by the Cognizant Engineer.

Failure to comply shall be sufficient cause for removal as "Qualified
Source"; complete requalification may be required before the product
is deemed acceptable.

TABLE 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER NAME	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	VCC	+7.0	V
Input Voltage	VIN	-1.5 TO +5.5	V
Output Voltage	VOUT	-0.5 TO +5.5	V
Temperature: Storage Range	Tstg	-65 to +150	C

TABLE 11

RECOMMENDED OPERATING CONDITIONS

PARAMETER NAME	SYMBOL	VALUE MIN.	NOM.	MAX.	UNIT
Supply Voltage	VCC	4.75	5.0	5.25	V
Temperature: Operating Free-Air	TA	0		+70	$C

TABLE 111

ELECTRICAL CHARACTERISTICS

D.C.CHARACTERISTICS (VCC=5.0V +5%, TA =0 C+75 C

PARAMETER NAME	SYMBOL	TEST CONDITION	VALUE MIN.	MAX.	UNIT
High Level Input Voltage	VIH		2.0		V
Low Level Input Voltage	VIL			0.8	V
Input Clamp Voltage	VIC	(1)IN=-18mA		-1.5	V
High-Level Output Voltage	VOK	(1)H=-2.4mA	2.4		V
Low-Level Output Voltage	VOL	VCE=2.4V (1)OL=16mA		0.45	V
Input Breakdown Voltage	BVIN	(1)IN=1mA	5.5		V
Output Leakage Current	OLK	VO=5.5V,VCE=0.4V(1)		100	HA
	10 (High R State	VO=5.5V,VCE=2.4V		40	HA
	10 (High R STATE)	VO=0.4V,VCE=2.4V		40	HA
SUPPLY CURRENT	CC	Inputs either Open or at Ground(1)		140	mA
Ouput Short Circuit Current	OSC	VO=0V	-15	-60	mA
Address Input Load Current	FA	VA = 0.4V		-1.0	mA
Chip Enable Input Load Current	(1)FE	VCE=0.4V		-1.0	mA
Address Input Leakage Current	(1)RA	VA =4.5V		60	HA
Chip Enable Leakage Current	(1)RE	VCE=4.5V		60	HA
Capacitance IN	CIN	VIN=2.0V,VCC=0V		7	PF
Capacitance OUT	COUT	VO=2.0V,VCC=0V		8	PF

NOTE

The above characteristics are guaranteed to meet the output high level state when the chip is enabled CE=0.4V) and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.
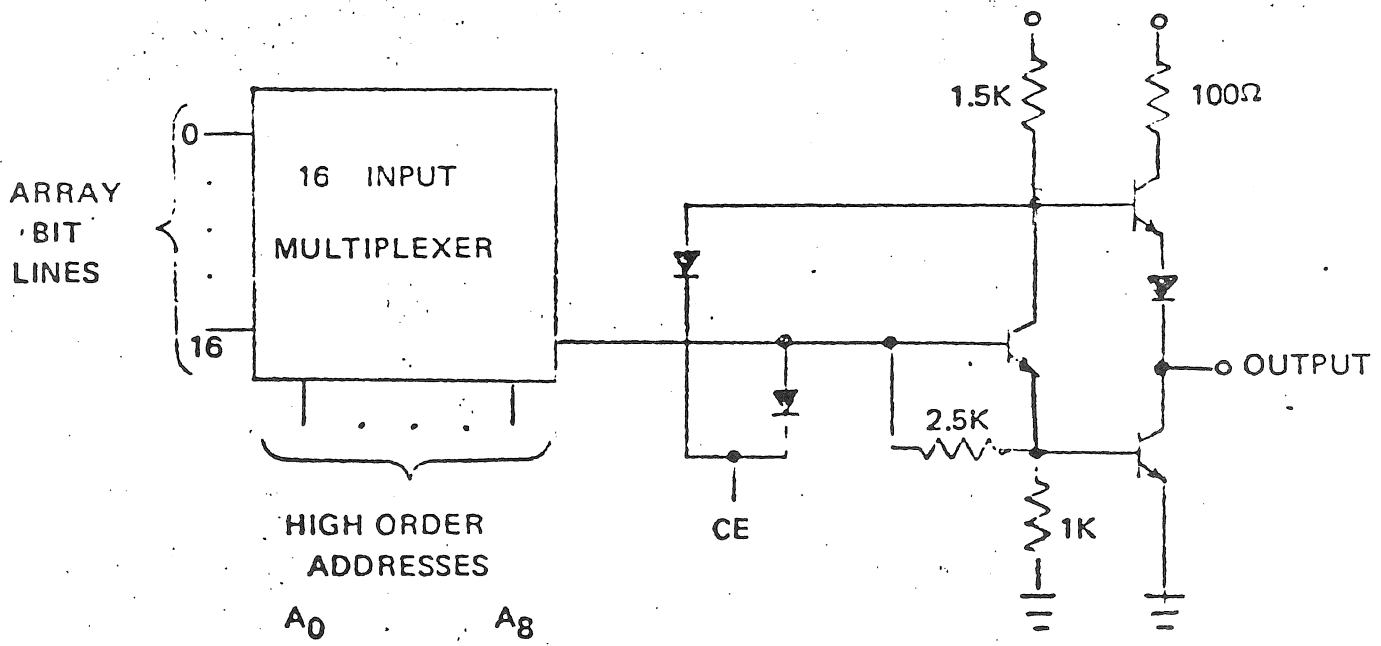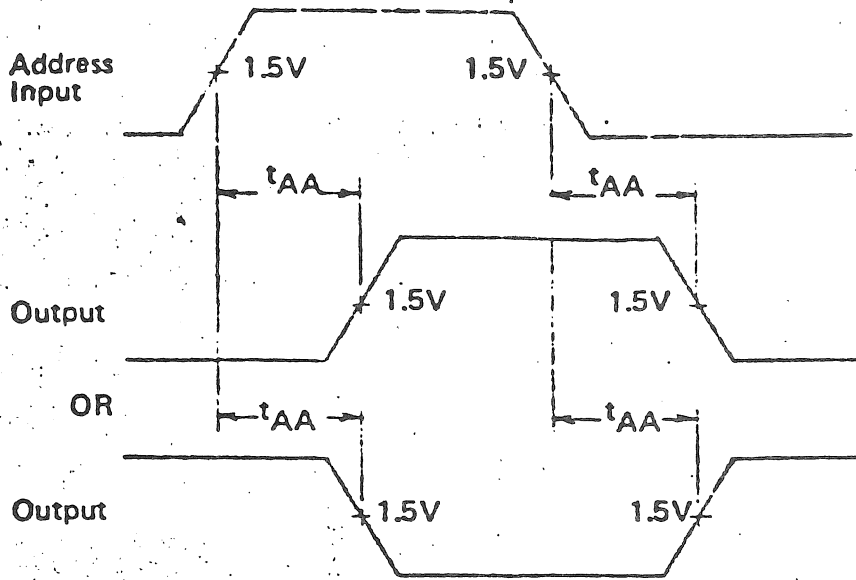

ELECTRICAL CHARACTERISTICS (Continued)

A.C SWITCHING CHARACTERISTICS (TA=25 C, VCC=5.0V)

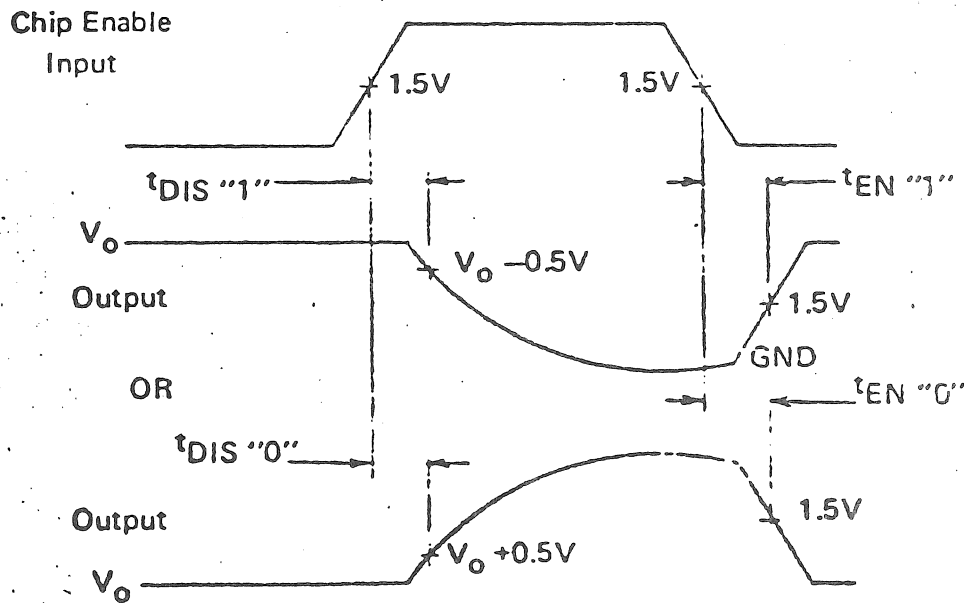| PARAMETER | | VALUE | | | | |
| | | | 25 C | | 0 C TO 75 C | |
NAME	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNIT
Access Time (Via Address Inputs)	tAA		70		80	ns
Output Disable Inputs	tDIS(2)		30		35	ns
Output Enable Time	tEN(2)		30	35		ns

NOTE

Output Disable Time is the time taken for the output to reach a high resistance state when either Chip Enable is taken high. Output Enable time is the time taken for the Output to become active when both Chip Enables are taken low. The high resistance state is defined as a point on the output waveform equal to a V of 0.5V from the active output level.

ACCESS TIME VIA ADDRESS INPUTS

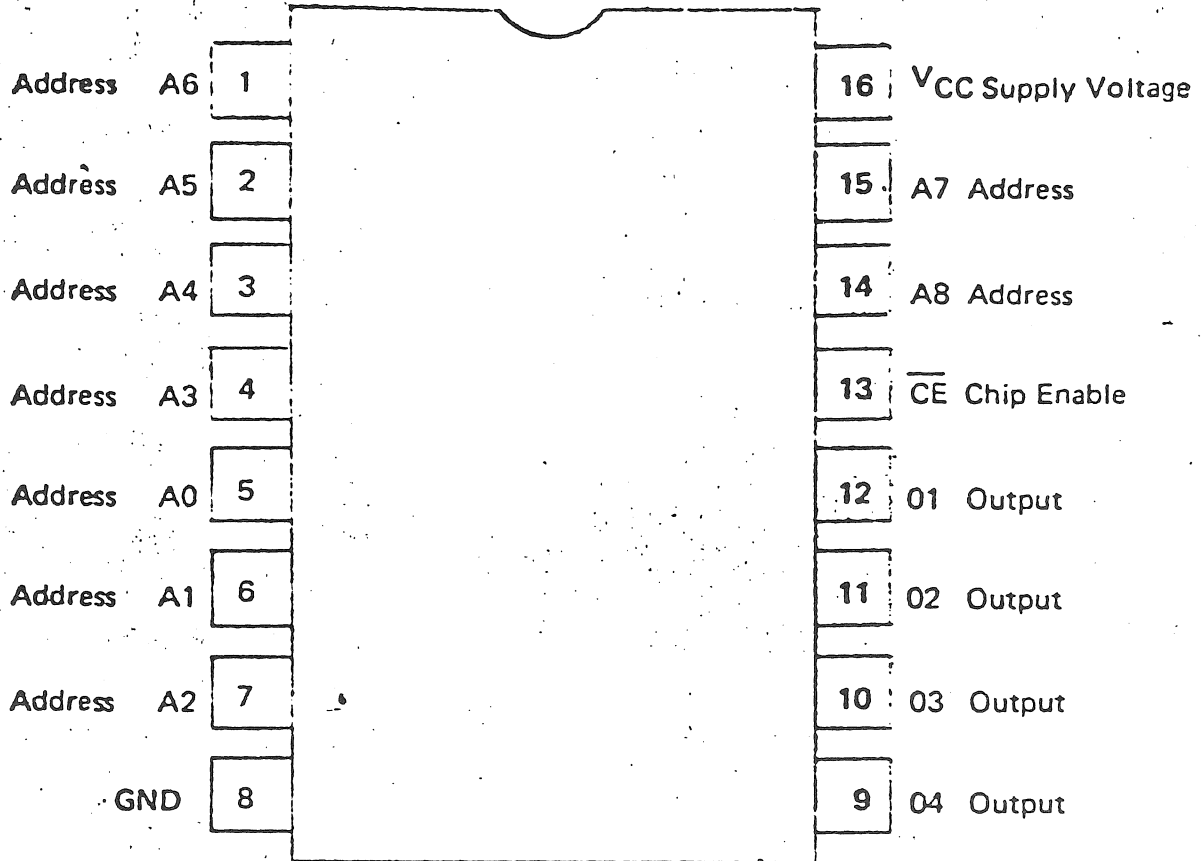OUTPUT ENABLE AND DISABLE TIMES

SWITCHING WAVEFORMS

TOP VIEW

Address A6	1	16	V_{CC} Supply Voltage
Address A5	2	15	A7 Address
Address A4	3	14	A8 Address
Address A3	4	13	$\overline{CE}$ Chip Enable
Address A0	5	12	01 Output
Address A1	6	11	02 Output
Address A2	7	10	03 Output
GND	8	9	04 Output

FIGURE 1

PIN CONNECTION DIAGRAM

01   02   03   04

(12)   (11)   (10)   (9)

13 CE

OUTPUT
BUFFER

MUX

ROM
MATRIX

ADDRESS
DECODER

(5)   (6)   (7)   (4)   (3)   (2)   (1)   (15)   (14)

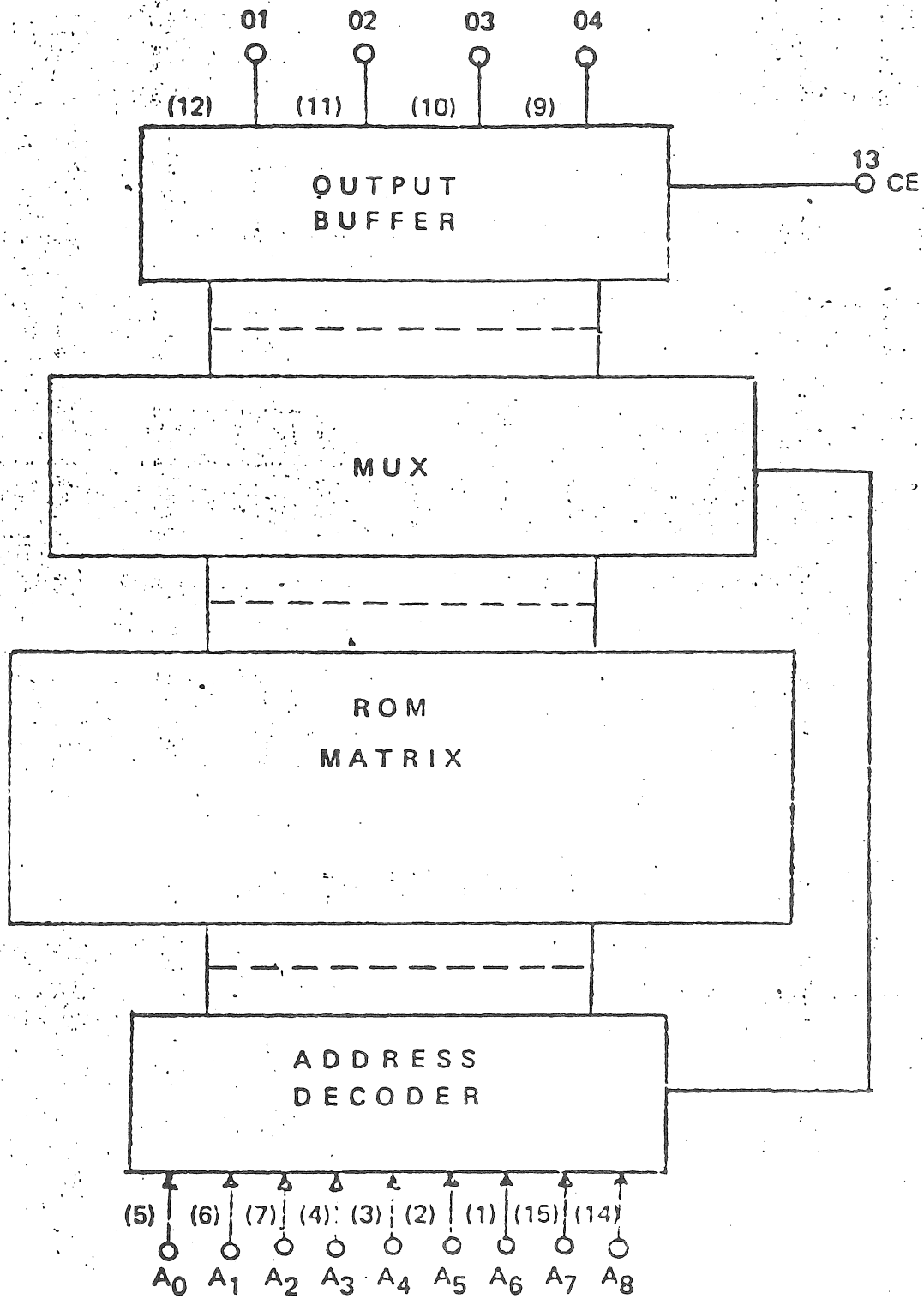A_0 A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8

FIGURE

LOGIC BLOCK DIAGRAM

PROGRAMMING PROCEDURE:

Device Description: This memory array is manufactured with logic level zeros in all storage locations. In order to program a logic level one at a specified bit, electrically alter a bit at logic level "0" to logic level "1". There are 2048 bits which are organized as 512 words of 4 bits each.

The device is programmed per the Digital Equipment Corporation pattern specification.

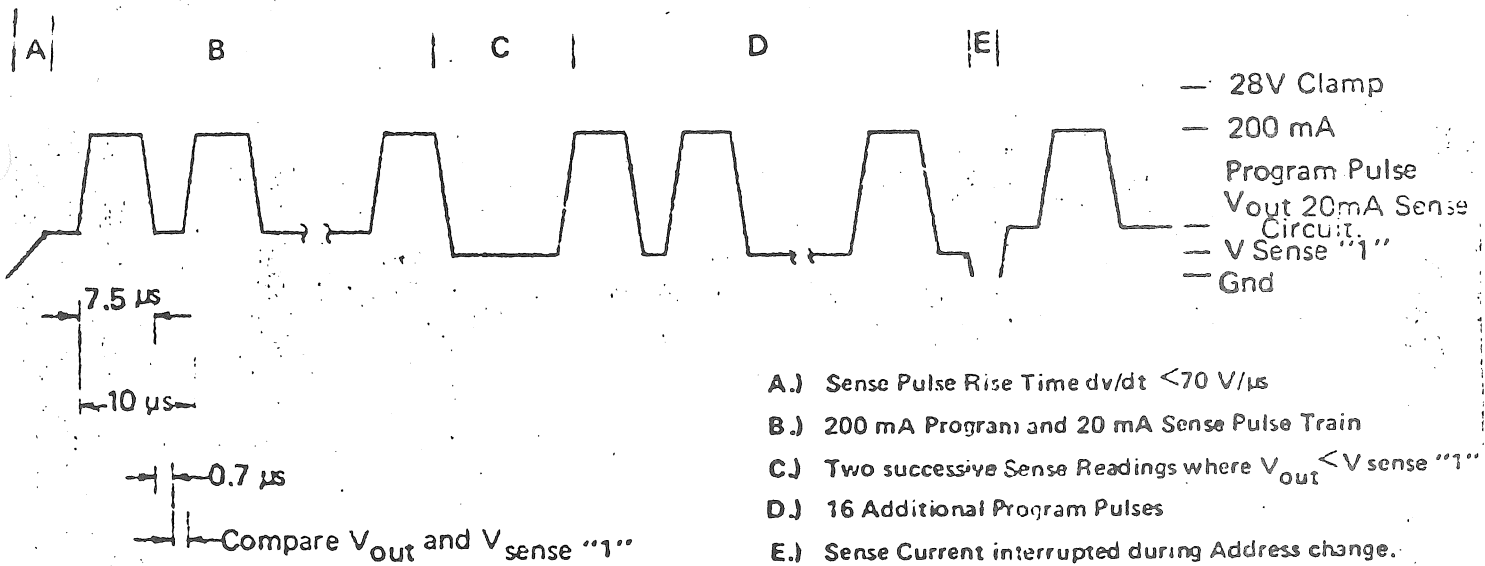| CHARACTERISTICS	LIMIT	UNITS	CONDITION
Programming Pulse:			
Amplitude	200 +5%	mA	Constant Current
Voltage (clamp)	28.0+0%-2%	V	Voltage limit of current source.
Ramp Rate dv/dt	70 max.	V/us	
Pulse Width	7.5+5%	us	15 V points, 150 load.
Duty Cycle	70% min.		
Sense Current	20.0+0.5	mA	The sense current must be interrupted after each address change for 10 us min. The sense current ramp rate dv/dt must be <70V/us, and clamped to 28.0V+0%-2%.
Programming Vcc	5.0+5%-0%	V	
Maximum Sensed Voltage for a programmed "1".	7.0+0.1	V	A bit programmed when two successive sense readings 1⁷ us apart with no intervening programming pulse, pass the limit. When this condition has been met, 16 additional program pulses are applied and the pulse train is then terminated.
Delay from trailing edge of program pulse before sensing output voltage	0.7 min.	us	
To Electrically Alter a Bit at Logic "0" to Logic "1".	200	us	

Input Conditions:

Amplitude ~0V to 3V

Rise & Fall Time ~5ns from 1V to 2V

Frequency ~ 1MHz
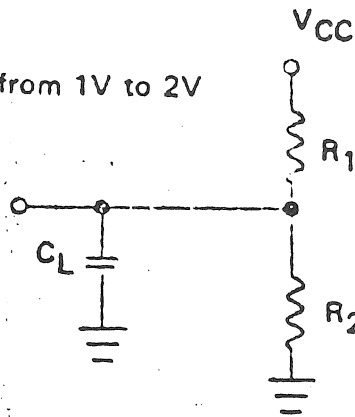
SWITCHING PARAMETER	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS} "1"	∞	600Ω	10 pF
t_{DIS} "0"	300Ω	600Ω	10 pF
t_{EN} "1"	∞	600Ω	30 pF
t_{EN} "0"	300Ω	600Ω	30 pF

SWITCHING TIME TEST CONDITION
OUTPUT LOAD CIRCUIT

7.5 µs

10 µs

0.7 µs

Compare V_{out} and V_{sense} "1"

— 28V Clamp
— 200 mA
Program Pulse
V_{out} 20mA Sense Circuit.
— V Sense "1"
— Gnd

A.) Sense Pulse Rise Time dv/dt <70 V/µs

B.) 200 mA Program and 20 mA Sense Pulse Train

C.) Two successive Sense Readings where V_{out} <V sense "1"

D.) 16 Additional Program Pulses

E.) Sense Current interrupted during Address change.

VOLTAGE WAVEFORM DURING PROGRAMMING