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digital

memories and peripherals

digital equipment corporation

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CHAPTER 1

INTRODUCTION

1.1 SCOPE

This handbook is a reference guide for the memory and peripheral hardware options that can be installed on the LSI-11 bus. It includes descriptions, specifications, configuration information, programming information as applicable to the options, and functional theory. The hardware options described in this handbook are designed to interface with a processor via the LSI-11 bus. Therefore, the user should be familiar with the contents of the appropriate processor handbook.

1.2 PERIPHERAL EQUIPMENT

Digital Equipment Corporation designs and manufactures the memory and peripheral options described in this handbook. The general design criterion was to provide maximum system throughput for peripherals when installed on the LSI-11 bus. LSI-11 bus-compatible processors and peripherals are designed to work together, providing a broad spectrum of system-compatible hardware options. The memory and peripheral devices can be used with any LSI-11 bus configuration; the system can later be expanded or modified to meet new system requirements. This hardware flexibility, when coupled with DIGITAL software and support, provides a single source for all present and future microcomputer processing needs.

1.3 LSI-11 FAMILY CHARACTERISTICS

LSI-11 bus systems include various processors, memory and peripheral device options, and software. Some of the characteristics of the LSI-11 bus systems are as follows:

- Low-cost, powerful processors for integration into any small- or medium-sized computer system.
- Direct addressing of all memory locations and peripheral device registers.
- Efficient processing of 8-bit bytes (characters) without the need to rotate, swap, or mask.
- Asynchronous bus operation that allows system components to run at their highest possible speed; replacement with faster devices means faster operation without other hardware or software changes.
- A module component design that provides ease and flexibility in configuring systems.

- Inherent direct memory access capabilities for high data rate devices.
- A bus structure that provides position-dependent priority for peripheral device interfaces connected to the I/O bus.
- Vectored interrupts that allow service routine entry without device polling.

1.4 PROCESSORS

The processor is connected to the LSI-11 bus (backplane) as a subsystem that executes programs and arbitrates usage of the LSI-11 bus for peripherals. It contains multiple, high-speed, general-purpose registers that can be used as accumulators, address pointers, index registers, and other specialized functions. The processor can perform data transfers directly between peripheral input/output (I/O) devices and memory without disturbing the processor registers. Data transfers include both 16-bit word and 8-bit byte data.

1.5 LSI-11 BUS

System components, including the processor, memory, and peripherals, are interconnected and communicate with each other via the LSI-11 bus. The form of communication is the same for all devices on the bus; instructions that communicate with memory can communicate with peripheral devices. Each device, including memory locations and peripheral device registers, is assigned an individual byte or word address on the LSI-11 bus.

The LSI-11 bus supports 18-bit addresses. However, processors and peripherals having a 16-bit addressing capability are completely PDP-11 hardware- and software-compatible within the 16-bit limitation. By PDP-11 convention, all peripheral device addresses are located within the upper 4K address space in the system, whether 16-bit or 18-bit addresses are used. This 4K address space is called the I/O page or "bank 7."

Whenever the I/O page is addressed, the processor must assert the BBS7 L bus signal. All peripheral devices use this signal line during addressing rather than decoding address bits (15:13) or (17:13). An active (asserted) BBS7 L signal will always indicate an address in the I/O page, enabling peripheral device addressing.

Peripheral device addresses within the I/O page are decoded by each peripheral device. Each peripheral device will include one or more "device register(s)." These registers can be accessed under program control in exactly the same manner as memory locations. Unique addresses within the I/O page are encoded on address bits (15:00).

NOTE

Address bits, for the purpose of this discussion, are logical states present on LSI-11 bus signal lines BDAL (17:00) L during the addressing portion of a bus cycle.

Refer to the appropriate processor handbook for a complete description of bus transactions, including bus cycles, addressing, etc.

1.6 DEVICE REGISTERS

All peripheral devices are defined by one or more device registers that are addressed as part of the main memory. These registers are generally designated control and status register(s).

Control and status registers (CSRs) contain all the necessary information to establish communications with the device. Some devices will require fewer than 16 status bits, while other devices could require more than 16 bits and, therefore, will require additional registers. The bits of the CSR have predetermined assigned functions. Typical bit functions include interrupt enable, error, done or ready, and enable.

Data buffer registers (DBRs) are for temporarily storing data to be transferred into and out of the processor. The number and type of data registers is a function of the individual peripheral device requirements.

1.7 INTERRUPTS

Interrupts allow devices to obtain processor service when they are "ready" for service, or "done" with a specific operation. The interrupt structure allows the processor to execute other programs while one or more peripherals are "busy." When a peripheral requires service, it requests an interrupt. The processor completes execution of the present instruction, saves PC and PS words on the stack, and acknowledges the interrupt. The highest priority peripheral device currently requesting interrupt service responds by inputting its interrupt vector address to the processor. The processor uses this vector address as a pointer to two memory locations containing the PC (starting address) and PS for the peripheral device interrupt service routine. Program control is transferred from the interrupted program to the routine associated with the requesting peripheral device. Note that no device polling is required since the interrupt vector is unique for that device. Once the device service routine execution has been completed, control is returned either to the previously interrupted program or to another peripheral device requesting interrupt service.

1.8 MEMORY ADDRESSES

Memory addresses are generally limited to the address space other than the I/O page. However, the I/O page can contain read-only memory (ROM) for disk bootstraps, paper tape loaders, diagnostics, etc. and/or read/write memory for DMA buffers. The system designer must use care in assigning memory addresses within the I/O page to avoid conflicts with peripheral device addresses used for actual system hardware, or addresses that system software may attempt to access for peripheral devices not actually installed in the system. See Appendix A for the standard assignments of the addresses in the I/O page.

CHAPTER 2

LSI-11 BUS PERIPHERALS AND OPTIONS

GENERAL

This chapter contains descriptions, features, specifications, configuration, and functional information for the LSI-11 bus peripherals and options. The data is arranged alphanumerically by option designation and is summarized by categories in Table 2-1. The option designation is printed on the top of each page to assist in locating any specific option. All the peripherals and options interface with the LSI-11 bus.

All the options include a module that connects to the bus backplane and provides the interface connections between the bus and the peripheral device. Some options provide only the interface module and will provide direct connections from the user's device to the bus. Other options include the device, such as line printers and disk drives. Some options have the capability to interface more than a single device, such as disk drives or terminals.

Table 2-1 Peripherals and Option Designations

Option	Name	Page
INTERFACE OPTIONS		
AAV11-A	4-Channel, 12-Bit D/A Converter	2-21
ADV11-A	Analog-to-Digital Converter	2-31
DRV11	Parallel Line Interface	2-173
DRV11-B	DMA Interface	2-193
DRV11-P	LSI-11 Bus Interface Foundation Module	2-217
IBV11-A	Instrument Bus Interface	2-295
KWV11-A	Programmable Real-Time Clock	2-339
COMMUNICATIONS OPTIONS		
DLV11	Asynchronous Serial Line Interface	2-81
DLV11-E	Asynchronous Line Interface	2-103
DLV11-F	Asynchronous Line Interface	2-125
DLV11-J	Four Asynchronous Serial Interfaces	2-147
DUV11	Synchronous Line Interface	2-245
DZV11	Asynchronous Multiplexer	2-269

Table 2-1 Peripherals and Option Designations (Cont)

Option	Name	Page
EXPANSION MEMORIES		
MMV11-A	4K by 16-Bit Core Memory	2-395
MRV11-AA	4K by 16-Bit Read-Only Memory	2-413
MRV11-BA	UV PROM/RAM Memory	2-425
MSV11-B	4K by 16-Bit MOS Read/Write Memory	2-441
MSV11-CD	16K by 16-Bit MOS Read/Write Memory	2-447
MSV11-D, -E	8K, 16K, or 32K Random Access Memory	2-471
PERIPHERALS		
LAV11	LA180 Printer Option	2-361
LPV11	LA180/LP05 Printer Option	2-375
RKV11-D	RK05 Disk Drive Option	2-509
RLV11	RL01 Disk Drive Option	2-545
RXV11	RX01 Floppy Disk Drive Option	2-575
MISCELLANEOUS OPTIONS		
BDV11	Diagnostic, Bootstrap, Terminator	2-51
KPV11-A, -B, -C	Power-Fail, Line-Time Clock, Terminator	2-317
REV11-A, -C	DMA Refresh, Bootstrap, Terminator	2-491
TEV11	Terminator	2-605

GENERAL SPECIFICATIONS

All the LSI-11 bus modules will operate under the following conditions:

Temperature	5° to 60° C (41° to 140° F)
Humidity	10 to 95% (no condensation)

When operating at the maximum outlet temperature (60° C or 140° F), adequate air flow must be maintained to control the inlet to outlet temperature rise across the modules to 5° C (9° F) maximum. The air flow should be directed to flow across the modules.

DETAILED SPECIFICATIONS

All the individual module specifications are included in the detailed description of the peripheral or option. A summary of the module characteristics is provided in Table 2-2; these characteristics are defined as follows.

1. The option designation is the alphanumerical code assigned to the option.

Table 2-2 Module Specifications

Option Desig.	Module No(s).	Description	Power Requirements +5 V ± 5%	+12 V ± 3 %	Bus Loads* AC (Max)	DC	Size	Page
AAV11-A	A6001	4-channel, 12-bit D/A converter	1.5 A	0.4 A	1.9	1	Quad	2-21
ADV11-A	A012	16-channel, 12-bit A/D converter	2.0 A	0.45 A	3.25	1	Quad	2-31
BDV11	M8012	Boot, term, diagnostic	1.6 A	0.07 A	2.0	1	Quad	2-51
DLV11	M7940	Asynchronous serial line interface	1.0 A	0.18A	2.5	1	Double	2-81
DLV11-E	M8017	Asynchronous line interface	1.0 A	0.18 A	1.6	1	Double	2-103
DLV11-F	M8028	Asynchronous line interface	1.0 A	0.18 A	2.2	1	Double	2-125
DLV11-J	M8043	4 asynchronous serial interfaces	1.0 A	0.25 A	1	1	Double	2-147

*These ac loads figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 2-2 Module Specifications (Cont)

Option Desig.	Module No(s).	Description	Power Requirements +5 V ± 5%	Power Requirements +12 V ± 3 %	Bus Loads* AC (Max)	Bus Loads* DC	Size	Page
DRV11	M7941	Parallel line unit interface	0.9 A	–	1.4	1	Double	2-173
DRV11-B	M7950	DMA interface	1.9A	–	3.3	1	Quad	2-193
DRV11-P	M7948	Foundation module	1.0A + user logic	–	2.1	1	Quad	2-217
DUV11	M7951	Synchronous serial line interface	0.86 A	0.32	1.00	1	Quad	2-245
DZV11-A	M7957	Asynchronous line interface	1 15 A	0 39 A	3.95	1	Quad	2 269
IBV11-A	M7954	Instrument bus interface	0.8 A	–	1.8	1	Double	2-295
KPV11-A	M8016	Power-fail/line-time clock	0.56 A	–	1.63	1	Double	2-317

*These ac loads figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 2-2 Module Specifications (Cont)

Option Desig.	Module No(s).	Description	Power Requirements +5 V ± 5%	Power Requirements +12 V ± 3 %	Bus Loads* AC (Max)	Bus Loads* DC	Size	Page
KPV11-B	M8016-YB	Power-fail/line-time clock/120 Ω bus terminator	0.56 A	–	1.63	1	Double	2-317
KPV11-C	M8016-YC	Power-fail/line-time clock/220 Ω bus terminator	0.56 A	–	1.63	1	Double	2-317
KWV11-A	M7952	Programmable real-time clock	1.75 A	0.01 A	3.4	1	Quad	2-339
LAV11	M7949	LA180 line printer interface	0.8 A	–	1.8	1	Double	2-361
LPV11	M8027	LA180/LP05 printer interface	0.8 A	–	1.4	1	Double	2-375
MMV11-A	H223 G653	4K × 16 core memory			1.91	1	2 quads	2-395
		(standby current)	3.0 A	0.2 A				
		(operating current)	7.0 A	0.6A				

*These ac loads figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 2-2 Module Specifications

Option Desig.	Module No(s).	Description	Power Requirements +5 V ± 5%	Power Requirements +12 V ± 3 %	Bus Loads* AC (Max)	Bus Loads* DC	Size	Page
MRV11-AA	M7942	4K × 16 read-only memory (less PROM integrated circuits	0.4 A	–	1.8	1	Double	2-413
		(with 32 512 × 4 PROM integrated circuits) (MRV11-AC)	2.8 A					
MRV11-BA	M8021	UV PROM-RAM (less PROM integrated circuits)	0.58 A	0.34 A	2.8	1	Double	2-425
		(with 8 1K × 8 PROM integrated circuits) (MRV11-BC)	0.62 A	0.5 A				

*These ac loads figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 2-2 Module Specifications (Cont)

Option Desig.	Module No(s).	Description	Power Requirements +5 V ± 5%	Power Requirements +12 V ± 3 %	Bus Loads* AC (Max)	Bus Loads* DC	Size	Page
MSV11-B	M7944	4K X 16 read/write MOS memory	0.6 A	0.54 A	1.9	1	Double	2-44
MSV11-CD	M7955-YD	16K X 16 read/write MOS memory	1.1 A	0.54 A	2.3	1	Quad	2-44
MSV11-D	M8044	4K/16K/32K MOS memory	1.7 A	0.34 A	2.0	1	Double	2-47
MSV11-E	M8045	4K/16K/32K MOS memory	2.0 A	0.41 A	2.0	1	Double	2-47
REV11-A	M9400-YA	120 Ω terminator, DMA refresh, bootstrap ROM	1.6 A	–	2.2	1	Double	2-49
REV11-C	M9400-YC	DMA refresh, bootstrap ROM	1.6 A	–	2.2	1	Double	2-49

*These ac loads figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Table 2-2 Module Specifications (Cont)

Option Desig.	Module No(s).	Description	Power Requirements +5 V ± 5%	Power Requirements +12 V ± 3 %	Bus Loads * AC (Max)	Bus Loads * DC	Size	Page
RKV11-D	M7269	LSI-11 bus control for RKV11-D	1.8 A	–	1.9	1	Double	2-509
RLV11	M8013 M8014	RL01 disk drive	6.5 A	1.0 A	3.2	1	2 quads	2-545
RXV11-A	M7946	RX01 interface	1.5 A	–	1.8	1	Double	2-575
TEV11	M9400-YB	120 Ω terminator	0.5 A	–	0	0	Double	2-605

*These ac loads figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/ac load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

2. The module number is the number assigned to the interface modules that are connected to the LSI-11 bus. This number is printed on the module handle and can be used as a quick reference to determine what specific options are installed in any system. The module numbers are listed numerically in Table 2-3 so that the user can identify the options installed by using the module numbers.

Table 2-3 Module Identification Numbers

Module	Option	Description
A012	ADV11-A	16-Channel, 12-Bit A/D Converter
A6001	AAV11-A	4-Channel, 12-Bit D/A Converter
G653	MMV11-A	4K X 16-Bit Core Memory
H223	MMV11-A	4K X 16-Bit Core Memory
M7269	RKV11-D	RK05 Disk Drive Option
M7940	DLV11	Serial Line Unit Interface
M7941	DRV11	Parallel Line Unit Interface
M7942	MRV11-AA	4K X 16-Bit Read-Only Memory (Less PROMs)
M7944	MSV11-B	4K X 16-Bit Read/Write MOS Memory
M7946	RXV11-A	Floppy Disk Drive Option
M7948	DRV11-P	Foundation Module
M7949	LAV11	LA180 Line Printer Option
M7950	DRV11-B	DMA Interface
M7951	DUV11-DA	Synchronous Serial Line Interface
M7952	KWV11-A	Programmable Real-Time Clock
M7954	IBV11-A	Instrument Bus Interface
M7955-YD	MSV11-CD	16K X 16-Bit Read/Write MOS Memory
M7957	DZV11-A	Asynchronous Line Interface
M8012	BDV11	Bootstrap, Diagnostic, and Terminator
M8013	RLV11	RL01 Disk Drive Option
M8014	RLV11	RL01 Disk Drive Option
M8016	KPV11-A	Power-Fail/Line-Time Clock
M8016-YB	KPV11-B	Power-Fail/Line-Time Clock/120-Ohm Terminator
M8016-YC	KPV11-C	Power-Fail/Line-Time Clock/220-Ohm Terminator
M8017	DLV11-E	Asynchronous Line Interface
M8021	MRV11-BA	UV PROM/RAM (Less PROMs)
M8027	LPV11	LA180/LP05 Printer Option
M8028	DLV11-F	Asynchronous Line Interface
M8043	DLV11-J	Four Asynchronous Line Interfaces

Table 2-3 Module Identification Numbers (Cont)

Module	Option	Description
M8044	MSV11-D	4K, 8K, 16K, 32K MOS Memory
M8045	MSV11-E	4K, 8K, 16K, 32K MOS Memory
M9400-YA	REV11-A	DMA Refresh/Bootstrap ROM/120-Ohm Terminator
M9400-YB	TEV11	120-Ohm Terminator
M9400-YC	REV11-C	DMA Refresh/Bootstrap ROM

3. The module description identifies the category of the option.

4. The power requirements specify the power used by the option when connected to the bus backplane. These requirements are used to determine the total power supply loading within a single system as described in Chapter 4.

5. The bus loads for ac and dc loading are provided so that the user can calculate the total ac and dc loading for any system. Complete details for the backplane requirements are contained in Chapter 4.

6. The interface modules are standardized as either a double or a quad and all are extended length. The double size module is 13.2 cm (5.2 in) high, 22.8 cm (8.9 in) long, and 1.27 cm (0.5 in) wide. The quad size module is 26.5 cm (10.5 in) high, 22.8 cm (8.9 in) long, and 1.27 cm (0.5 in) wide (Figure 2-1).

CONFIGURATION

The LSI-11 bus permits a unified addressing structure in which control/status and data registers for peripheral devices are directly addressed as memory locations. All operations on these registers, such as transferring information to or from them or manipulating data within them, are performed by normal memory address instructions. The use of memory address instructions on peripheral device registers greatly increases the flexibility of input/output communications.

Addresses

All the options except memories have at least one control and status register and may have several data registers. Each register is assigned an address through which the option can communicate with the processor. The upper 4K of memory address space is reserved for the processor and external input/output (I/O) registers. The user can select any address (Appendix A) in the range of 160000 through 177776 and assign it to the option interface module. The modules are configured to the desired address by selecting dip switches, connecting or disconnecting wire-wrap pins, or installing or removing wired jumpers on the module.

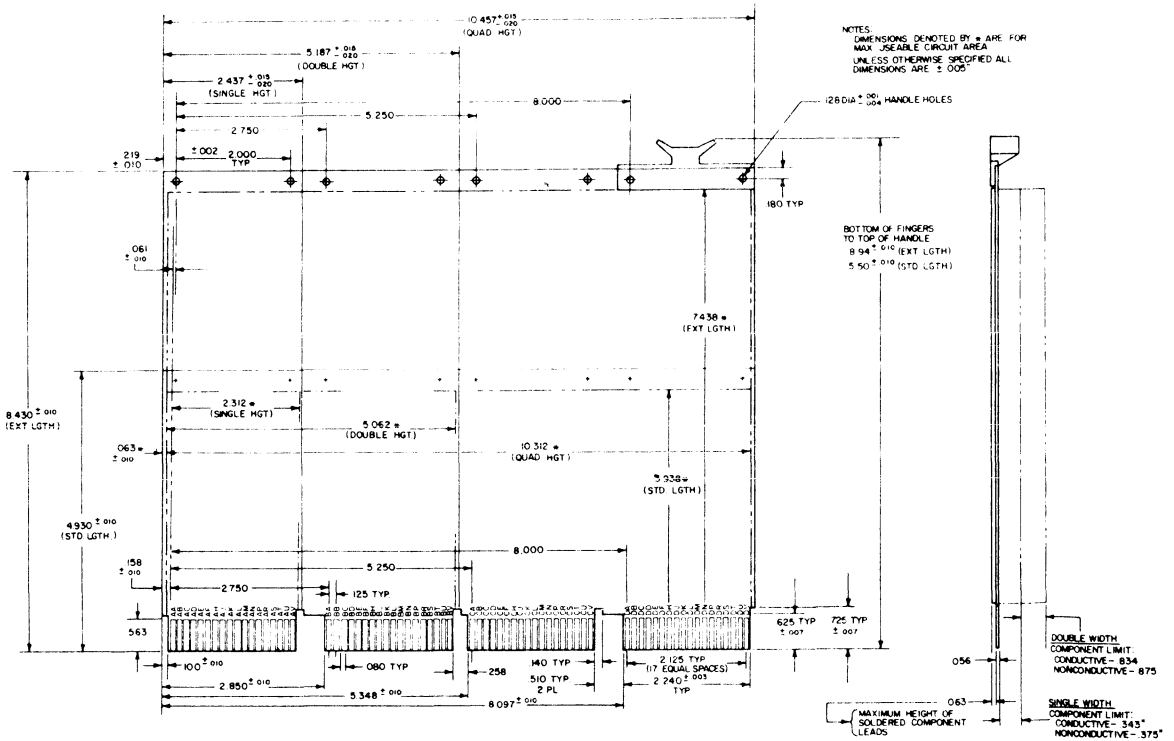


Figure 2-1 Module Dimensions

Control and Status Registers

The general form for the control and status registers, shown in Figure 2-2, does not necessarily apply to every device, but is presented as a guide

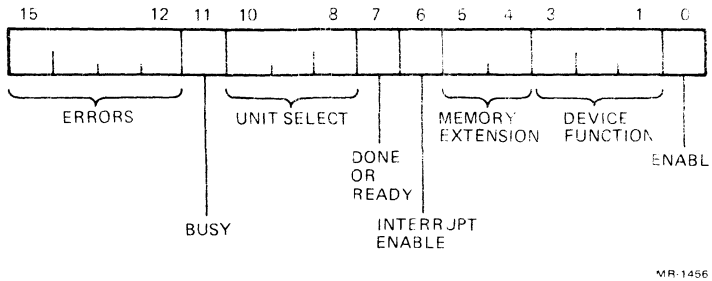


Figure 2-2 Controls and Status Register

Many devices require less than 16 status bits. Other devices will require more than 16 bits and therefore will require additional status and control registers.

The bits in the control and status registers are generally assigned as described in Table 2-4.

Table 2-4 Typical Control and Status Register

Bit	Name	Function
15–12	Errors	Generally there is an individual bit associated with a specific error. When more bits are required for errors, they can be obtained by expanding the error section in the word or by using another status word. Generally bit 15 is the inclusive-OR of all other error bits (if there is more than one). Most devices will have "hard" error conditions which will cause an interrupt if bit 6 is set. Some may also have "soft" errors (warning types) which do not cause immediate interrupts.

Table 2-4 Typical Control and Status Register (Cont)

Bit	Name	Function
11	Busy	Set to indicate that a device operation is being performed.
10–8	Unit Select	Some peripheral systems have more than one device per control. For example, a disk system can have multiple surfaces per control and an analog-to-digital converter can have multiple channels. The unit bits select the proper surface or channel.
7	Done or Ready	The register can contain a done bit, a ready bit or a done-busy pair of bits, depending on the device. These bits are set and cleared by the peripheral device, but may be queried by the program to determine the availability of the device.
6	Interrupt Enable	Set by the program to allow an interrupt to occur as a result of a function done or error condition.
5–4	Memory Extension	Allows devices to use a full 18 bits to specify addresses on the bus.
3–1	Device Function Bits	Specifies the operation that a device is to perform.
0	Enable	Set to enable the device to perform an operation.

Data Buffer Registers

The data buffer register is used for temporarily storing data to be transferred into or out of the computer. The number and type of data registers is a function of the device.

Interrupts

Interrupts are requests, made by peripheral devices, which cause the processor to temporarily suspend its present (background) program execution to service the requesting device. Each device that is capable of requesting an interrupt must have a user-supplied service routine that is automatically entered when the processor acknowledges the interrupt

request. After completing the service routine execution, program control is returned to the interrupted program. This type of operation is especially useful for the slower peripheral devices.

A device can interrupt the processor only when interrupts are enabled and services interrupts only when the appropriate PSW bits are cleared. Device priority is highest for devices electrically closest to the processor along the bus. Any device that can interrupt the processor can also interrupt the service routine execution of a lower priority device if the processor's priority is set during that execution; hence, interrupt nesting to any level is possible with this interrupt structure. Each device normally contains a control/status register (CSR), which includes an interrupt enable bit. A program must set this bit before an interrupt can be generated by the device.

Interrupt Vectors

An interrupt vector associated with each device is hard-wired into the device's interface/control logic. This vector is an address pointer that is transmitted to the processor during the interrupt acknowledge sequence, allowing automatic entry into the service routine without device polling. The user can select an interrupt vector from within the range of 000 to 777 for any interrupting options. The module can be configured to the desired interrupt vector by either selecting dip switches, connecting or disconnecting wire-wrap pins, or installing or removing wired jumpers on the module.

FUNCTIONAL DESCRIPTION

The functional description is provided for all the options in order to assist the user in understanding the theory of operation.

CATEGORIES

The LSI-11 bus peripherals and options are classified into general categories that pertain to their performance and function. This listing indicates the wide span of equipment capability available to the user.

Interface Options

AAV11-A — The AAV11-A is a 4-channel, 12-bit digital-to-analog converter module that includes control and interfacing circuits. It has four D/A converters, a dc-dc converter that provides power to the analog circuits, and a precision voltage reference. Each channel has its own holding register that can be addressed separately and provides 12 bits of resolution. Bits 0, 1, 2, and 3 of the fourth holding register are brought out to the I/O connector so that they can be used as a 4-bit digital output register.

ADV11-A

The ADV11-A is a 12-bit successive approximation analog-to-digital converter that samples analog data at specified rates and stores the digital equivalent value for processing. The multiplexer can accommodate up to 16 single-ended or 8 quasi-differential inputs. The converter uses a patented auto-zeroing design that measures the sampled data with respect to its own offset and therefore cancels out its own offset error.

External event inputs can originate at the user's equipment or from the Schmitt trigger output of the KWV11-A clock. Three reference signals are provided for self-testing any channel input. These signals consist of two dc levels and one bipolar triangular waveform. This output can be used with DIGITAL diagnostic software to produce a data base for extremely precise analog linearity testing.

DRV11

The DRV11 is a parallel interface module that is used to interconnect the LSI-11 bus with general-purpose, parallel line, TTL or DTL devices. It allows program-controlled data transfers at rates up to 40K words per second and uses LSI-11 bus interface and control logic to generate interrupts and process vector handling. The data is handled by 16 diode-clamped input lines and 16 latched output lines. There are two 40-pin connectors on the module for user interface applications.

DRV11-B

The DRV11-B is an interface module that uses direct memory access (DMA) to transfer data directly between the system memory and an I/O device. The interface is programmed by the processor to move variable length blocks of 8- or 16-bit data words to or from specified locations in the system memory. Once programmed, there is no processor intervention required. The module can transfer up to 250K 16-bit words per second in the single-cycle mode and up to 500K 16-bit words per second in the burst mode. It also allows read-modify-restore operations.

DRV11-P

The DRV11-P is a foundation wire-wrap interface module with a 40-pin I/O connector. Approximately 25 percent of the module is occupied by bus transceivers, interrupt vector generation logic, device comparator logic, protocol logic, and interrupt logic. The remaining 75 percent is for user applications; this portion has plated-through holes for securing ICs and wire-wrap pins for interconnecting the user's circuits. The plated-through holes can accept 6-, 8-, 14-, 16-, 18-, 20-, 22-, 24-, and 40-pin dual-in-line integrated circuits or discrete components.

IBV11-A The IBV11-A is an interface module that interconnects the LSI-11 bus with the instrument bus described in IEEE standard 488-1975, "Digital Interface for Programmable Instrumentation." The IBV11-A makes a processor-controlled programmable instrument system possible. The module can accommodate up to 15 IEEE-488 devices and is PDP-11 software-compatible.

KWV11-A The KWV11-A is a programmable real-time clock/counter that provides a means of determining time intervals or counting events. It can be used to generate interrupts to the processor at predetermined intervals or establish timing between input and output events. It can also initialize the ADV11-A analog-to-digital converter by a clock counter overflow or by firing a Schmitt trigger. The clock counter has a resolution of 16 bits and can be driven by any one of five crystal-controlled frequencies (100 Hz to 1 MHz), from a line frequency input, or from a Schmitt trigger fired by an external input. The module can operate in any of four programmable modes: single interval, repeated interval, external event timing, and external event timing from zero base.

Communications Options

DLV11 The DLV11 is a serial line unit (SLU) that interfaces with asynchronous serial I/O devices. The module has jumper-selectable baud rates (50–9600) and serial word format that includes the number of stop bits, number of data bits, and even, odd, or no parity bit. The DLV11 can support 20 mA current loop interfaces or EIA "data leads only" interfaces.

DLV11-E The DLV11-E is an asynchronous line interface module that interconnects the LSI-11 bus to standard serial communications lines. The module receives serial data, converts it to parallel data, and transfers it to the LSI-11 bus. Also, it accepts parallel data from the LSI-11 bus, converts it to serial data, and transmits it to the peripheral device. The module has jumper-selectable or software-selectable baud rates (50–19200), and jumper-selectable stop bit and data bit formats. The DLV11-E offers full modem control for EIA/CCITT interfaces.

DLV11-F The DLV11-F is an asynchronous line interface module that interconnects the LSI-11 bus to several types of standard serial communications lines. The module receives serial data, converts it to parallel data, and transfers it to the LSI-11 bus. It also accepts parallel data from the LSI-11 bus, converts it to serial data, and transmits it

to the peripheral device. The module has jumper-selectable or software-selectable baud rates (50–19200) and jumper-selectable stop bits and data bits. The DLV11-F supports either 20 mA current loop or EIA standard lines, but does not include modem control.

DLV11-J — The DLV11-J contains four independent asynchronous serial line channels used to interface peripheral devices to the LSI-11 bus. Each channel transmits and receives data from the peripheral device over EIA data leads (lines that do not use a control line). The module can be used with 20 mA current loop devices if a DUV11-KA adpater is used. The DLV11-J has jumper-selectable baud rates from 150 to 38.4K baud.

DUV11 — The DUV11 synchronous line interface module establishes a data communication line between the LSI-11 bus and a Bell 201 synchronous modem or equivalent. The module is fully programmable with respect to sync characters, character length (5 to 8 bits), and parity selection. The receiver logic accepts serial data from the modem and converts it to parallel data for the LSI-11 bus. The transmitter logic converts the parallel LSI-11 bus data into serial data for the transmission line. The interface logic converts the TTL logic levels to the EIA voltage levels required by the Bell 201 modems and also controls the modem for half-duplex or full-duplex.

DZV11 — The DZV11 is an asynchronous multiplexer interface module that interconnects the LSI-11 bus with up to four asynchronous serial data communications channels. The module provides EIA interface voltage levels and data set control to permit dial-up (auto-answer) operations with full-duplex modems such as Bell models 103, 113, 212, or equivalent. The DZV11 does not support half-duplex operations or the secondary transmit and receive operations available in some modems such as Bell 202. The DZV11 has applications in data concentration and collection systems where front-end systems interface to a host computer and for use in a cluster controller for terminal applications.

Expansion Memories

MMV11-A — The MMV11-A is a 4K by 16-bit core memory option that provides nonvolatile read/write storage. The memory can be configured by bank addressing switches. The module is limited to LSI-11 bus backplanes that contain the LSI-11 bus in both the A/B and the C/D slots.

MRV11-AA The MRV11-AA is a read-only memory module on which the user can install fusible link, programmable, read-only memory (PROM) chips or masked read-only memory (ROM) chips. The user selects the address space of the memory by configuring removable jumper wires.

MRV11-BA The MRV11-BA is a read-only memory module that uses ultraviolet (UV) erasable, programmable, read-only memory (PROM) integrated circuits. The module also contains a 256 by 16-bit random access memory (RAM) that can be used as a "scratchpad" or "stack" by the system software.

MSV11-B The MSV11-B is a 4K by 16-bit dynamic MOS read/write memory module. The user can select the memory addresses of the module by configuring removable jumpers. The memory refresh must be controlled by external bus signals.

MSV11-CD The MSV11-CD is a 16K by 16-bit dynamic MOS read/write memory module. Refresh is automatically performed by the module but it can be disabled if the user wishes to use the LSI-11 bus refresh signals. This memory module can be configured to operate in the battery backup mode. The user can configure the memory addresses by selecting switch settings.

MSV11-D, -E The MSV11-D module has either 8K, 16K, or 32K by 16 bits of MOS memory. The MSV11-E is the same as the MSV11-D except that it has an 18-bit word that generates and detects byte parity for each word. The modules have an on-board memory refresh and perform the necessary LSI-11 bus cycles. The memory addressing is selectable by the user by configuring switch settings. The module can use a battery backup system to preserve data when primary power is lost.

Peripherals

LAV11 The LAV11 option consists of an LA180 DECprinter, an interface module, and a BC11S-25 interface cable. The interface module provides interconnection between the LA180 DECprinter and the LSI-11 bus. The module outputs ASCII characters to the printer and monitors various printer operations that require operator control.

LPV11 The LPV11 printer option consists of an interface module, an interface cable, and either an LP05 or LA180 line printer. The interface module provides programmed control of data transfers and provides printer strobe signals

appropriate for either printer. The LA180 DECprinter is a high-speed printer that prints 180 characters per second and the LP05 printer can print 240 or 300 lines per minute, depending on which model is selected.

RKV11-D — The RKV11-D option consists of an RK05 disk drive controller, an LSI-11 bus interface module, and an RK05J disk drive. The RK05 disk drive controller can be used with up to eight RK05J disk drive units to form a mass memory storage system that contains up to 21M bytes of storage. The RKV11-D system is block-oriented but is capable of transferring from 1 to 2^{16} consecutive data words without reinitiation or processor intervention. The data transfers occur from the RKV11-D to the system memory by direct memory access (DMA) and operate at maximum bus bandwidth. The system can use either RK05J or RK05F disk drives and the controller can be mounted in a standard 48.3 cm (19 in) cabinet.

RLV11 — The RLV11 option interfaces the LSI-11 bus with an RL01 disk drive controller and an RL01 disk drive assembly. The controller can only be used in an H9273-A type backplane which incorporates on LSI-11 bus in slots A and B, with an interboard bus in slots C and D. The controller can interface up to four RL01 disk drives for a complete system of 21M bytes of storage. The RL01 disk drive is a random access, mass storage system that stores data in fixed length blocks on a preformatted disk cartridge. Each drive can store up to 5.24 million bytes and the complete system can store up to 21 million bytes. The RLV11 transfers data using direct memory access (DMA) techniques; this allows data transfers without processor intervention and at bus bandwidth speed.

RXV11 — The RXV11 option consists of an interface module, cable assembly, and either a single or dual drive RX01 floppy disk. This option is a random access mass storage device that stores data in fixed-length blocks on a preformatted flexible diskette. Each diskette can store and retrieve up to 256K, 8-bit bytes of data. The RXV11 system is rack-mountable in the standard 48.3 cm (19 in) cabinet.

Miscellaneous Options

BDV11 — The BDV11 module has 2K words of read-only memory (ROM) that contains diagnostic and bootstrap programs. These programs are user-selectable by setting dip switches. The diagnostic programs will test the processor, the memory, and the user's console. The bootstrap programs can boot LSI-11 peripheral devices. The module also has 120-ohm bus termination circuits.

The user can add up to 16K words of read-only memory (ROM) and up to 2K words of erasable programmable ROM (EPROM) on the module. This 18K words of additional memory can be used with no increase in the amount of I/O address space.

KPV11-A, -B, -C — The KPV11-A module generates power-up and power-down sequences, monitors for a power-fail condition, and generates the line-time clock (LTC) function. The KPV11-B is the same as the "A" except that it provides 120-ohm termination circuits. The KPV11-C is the same as the "A" except that it provides 220-ohm termination circuits. The module can be installed on any backplane or remotely installed via an optional cable.

REV11-A, -C — The REV11-C module has a bootstrap ROM and direct memory access (DMA) refresh circuits. The REV11-A is identical to the REV11-C except it has additional 120-ohm termination circuits.

TEV11 — The TEV11 is a bus terminator module that provides 120-ohm bus termination circuits.

AAV11-A 4-CHANNEL 12-BIT D/A CONVERTER

GENERAL

The AAV11-A is a 4-channel, digital-to-analog converter module that includes control and interfacing circuits. It has four D/A converters, a dc-dc converter that provides power to the analog circuits, and a precision voltage reference. Each channel has its own holding register that can be addressed separately and provides 12 bits of resolution. These registers can be written and read, using either word or byte format. In addition, bits 0, 1, 2 and 3 of the fourth holding register are brought out to the I/O connector so they can be used as a 4-bit digital output register.

FEATURES

- Four 12-bit digital input channels, binary encoded for either unipolar mode or bipolar mode
- Jumper-selected output ranges and modes:
  Bipolar mode ±2.56 V, ±5.12 V, ±10.24 V
  Unipolar mode 0 to +5.12 V, 0 to +10.24 V
- One part in 4096 resolution
- 5 V/μs slew rate
- ±5 mA drive capability per converter

SPECIFICATIONS

Identification	A6001
Size	Quad
Power	+5.0 Vdc ± 5% at 1.5 A +12.0 Vdc ± 3% at 0.4 A
Bus Loads	
AC	1.9
DC	1.0
Resolution	12-bits (1 part in 4096)
Number of D/A converters	4
Digital input	12-bits (binary encoded for unipolar mode; offset binary encoded for bipolar mode)

Digital storage	Read-write, word or byte operable, single buffered
Output voltage range (jumper selected)	±2.56 V, ±5.12 V, ±10.24 V bipolar, 0 V to +5.12 V, 0 V to +10.24 V unipolar
Gain accuracy	Adjustable (factory set for bipolar ±5.12 V)
Gain temperature coefficient	10 PPM per °C, max.
Offset temperature coefficient	20 PPM of full scale range per °C, max.
Linearity	±1/2 LSB max. non-linearity
Differential linearity	±1/2 LSB, monotonic
Output impedance	1 ohm max.
Drive capability	±6 mA max. per converter
Slewing speed	5 V/μs
Rise and settling time (to 0.1% of final value)	4 μs (8 μs with 5000 pF load in parallel with 1 kΩ)

CONFIGURATION

General

The following paragraphs describe how the user can configure the module so that it will function within his system by setting dip switches (Figure 1) to obtain the desired device address. The voltage range for each D/A converter (DAC 0 – DAC 3) can be independently configured by installing or removing the designated jumpers (Figure 1) associated with a specific D/A converter. Also described in this section is the method of connecting external devices to the module. The standard factory addresses for the registers are listed in Table 1.

Table 1 Standard Addresses

Register	Mnemonic	Address
Holding 0	DAC 0	170440
Holding 1	DAC 1	170442
Holding 2	DAC 2	170444
Holding 3	DAC 3	170446

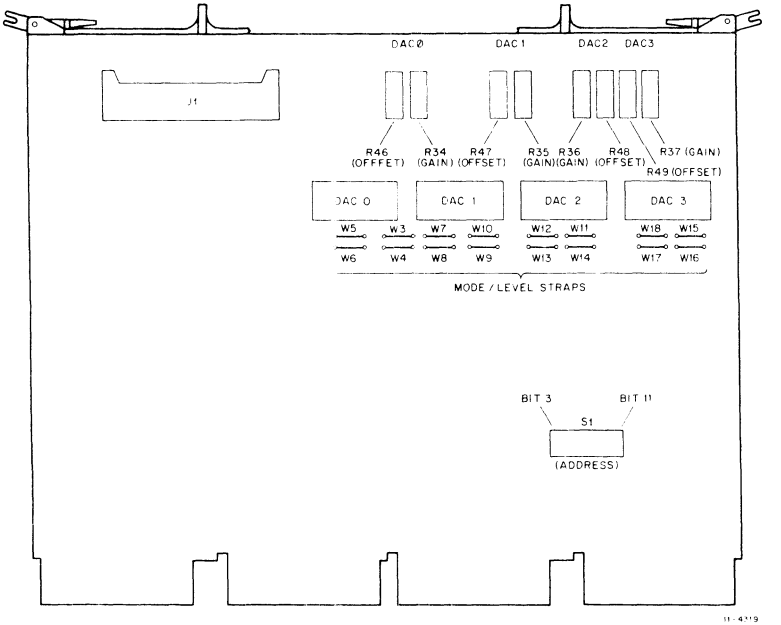


Figure 1 AAV11-A Connectors, Switches, and Jumpers

Device Registers

The device registers can be configured to respond to any address within the range 170000 to 177777. Each register address does not have to be individually set. The DAC 0 register address is selectable and the last digit will be zero. The remaining registers will use addresses 17XXX2, 17XXX4, and 17XXX6 for the DAC 1, DAC 2 and DAC 3 registers, respectively. The factory-configured device address is 170440 as shown in Figure 2. The word formats for the DAC registers are described in Table 2. Note that all device registers are always a sequence of four consecutive even locations. There is no vector used for this module.

D/A Converter Range and Mode

The range and mode (bipolar or unipolar) voltages can be selected by the user inserting or removing jumpers as shown in Figure 1. Four jumpers are associated with each D/A converter. The module is factory-configured for −5.12 to +5.12 V bipolar operation. The jumper configurations for the bipolar mode ranges are shown in Table 3; the unipolar ranges are shown in Table 4.

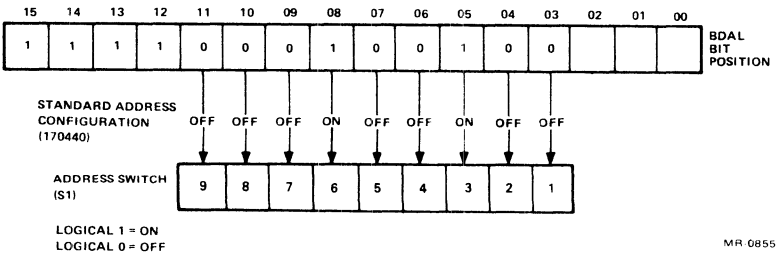


Figure 2 Address Selection

Table 2 DAC Word Formats

Bit	DAC 0, DAC 1, DAC 2	DAC 3
15–12	Not used	Not used
11	Binary 11	Binary 11
10	Binary 10	Binary 10
9	Binary 9	Binary 9
8	Binary 8	Binary 8
7	Binary 7	Binary 7
6	Binary 6	Binary 6
5	Binary 5	Binary 5
4	Binary 4	Binary 4
3	Binary 3	Binary 3/Control 3
2	Binary 2	Binary 2/Control 2
1	Binary 1	Binary 1/Control 1
0	Binary 0	Binary 0/Control 0

Table 3 Jumper Configurations for Bipolar Operation

	±2.56 V	±5.12 V	±10.24 V
DAC 1			
W3	IN	IN	OUT
W4	OUT	OUT	IN
W5	IN	OUT	OUT
W6	IN	IN	IN
DAC 2			
W7	IN	IN	OUT
W8	OUT	OUT	IN
W9	IN	OUT	OUT
W10	IN	IN	IN

Table 3 Jumper Configurations for Bipolar Operation (Cont)

	±2.56 V	±5.12 V	±10.24 V
DAC 3			
W11	IN	IN	OUT
W12	OUT	OUT	IN
W13	IN	OUT	OUT
W14	IN	IN	IN
DAC 4			
W15	IN	IN	OUT
W16	OUT	OUT	IN
W17	IN	OUT	OUT
W18	IN	IN	IN

Table 4 Jumper Configurations for Unipolar Operation

	0 V — +5.12 V	0 V — +10.24 V
DAC 1		
W3	IN	IN
W4	OUT	OUT
W5	IN	OUT
W6	OUT	OUT
DAC 2		
W7	IN	IN
W8	OUT	OUT
W9	IN	OUT
W10	OUT	OUT
DAC 3		
W11	IN	IN
W12	OUT	OUT
W13	IN	OUT
W14	OUT	OUT
DAC 4		
W15	IN	IN
W16	OUT	OUT
W17	IN	OUT
W18	OUT	OUT

J1 Output Connections

Analog output devices such as oscilloscopes may be either grounded or floating. If the oscilloscope is grounded, either through its power plug or through contact between its chassis and a grounded cabinet, the oscilloscope ground should not be connected to any of the AAV11-A ground pins. Doing so may result in a ground loop which will adversely affect oscilloscope control results as well as ADV11-A operation (if used). If the oscilloscope is floating, its ground should be connected to the AAV11-A logic ground, J1 pins L, N, R, or T. Note that the foregoing assumes that the LSI-11 power supply ground is connected to power line (earth) ground. If continuity checks reveal no such connection, attach a length of 12-gauge wire between the power supply ground and a convenient point associated with earth ground.

Oscilloscope X and Y inputs may be either differential or single-ended. Differential inputs should be driven as in Figure 3.

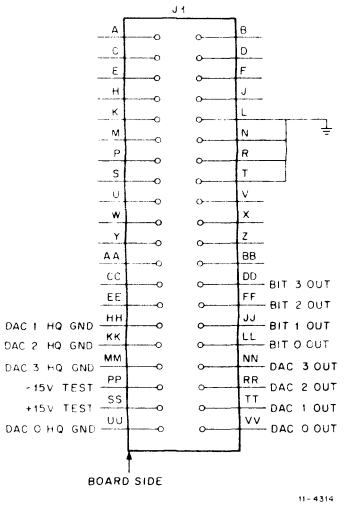


Figure 3 Connection to Oscilloscope with Differential Input

When oscilloscopes with single-ended inputs are involved, the AAV11-A analog grounds (pins UU and HH) are not used. Return path for X and Y signal currents is through ground for a grounded oscilloscope or through

logic ground (pins L, N, R, or T) for a floating oscilloscope. Since the grounded, single-ended oscilloscope receives an input voltage which is the sum of the AAV11-A output and the ground difference voltage between the oscilloscope and the AAV11-A, noise and line frequency errors may be minimized by plugging the oscilloscope into an ac socket as close as possible to the LSI-11 system. Running single-ended oscilloscopes in a floating configuration will eliminate noise and line frequency errors which are due to ground voltage differences.

The effect of magnetic coupling into the oscilloscope input lines can be minimized for a differential-input oscilloscope by running the AAV11-A output and its return line in a twisted pair. No benefit is derived from a twisted pair with a single-ended oscilloscope input.

The effect of electrostatic coupling into the oscilloscope input lines can be minimized by shielding the input lines from AAV11-A to the oscilloscope. The shield should be connected to ground at one end only. Grounding the shield at both ends may result in a ground loop which will adversely affect oscilloscope control results and any ADV11-A A/D operations (if used).

Careful selection of cabling is essential. The D/A outputs are capable of driving a maximum of 5000 pF. Output impedance is 1 ohm. Output current limit is 5 mA.

Optional Equipment

Figure 4 illustrates the H854 40-pin connector pin assignments for user outputs. These pins may be connected to the optional H322 distribution panel for convenient user access via an optional BC08R cable. The optional BC04Z is available for applications which require an unterminated cable. One end is terminated with an H856 connector that mates with the H854 connector on the AAV11-A module. The other end is an unterminated ribbon cable. The BC04Z cable is available in lengths of 3.05 m (10 ft), 4.5 m (15 ft), and 7.6 m (25 ft).

PROGRAMMING

All four DAC holding registers are automatically set to zero on system initialization. This produces −5.12 V at the DAC outputs when the mode/level jumpers are connected as delivered from the factory. Any holding register value remains in effect until changed by the processor in response to a program instruction. Coding to the D/A converters is offset binary for bipolar operation and straight binary for unipolar operation. Offset binary defines 0 as maximum negative voltage, mid-point (i.e., 4000_8 for the 12-bit AAV11-A) as 0 V, and all 1s (7777_8) as maximum positive voltage. These relationships are illustrated in Table 5.

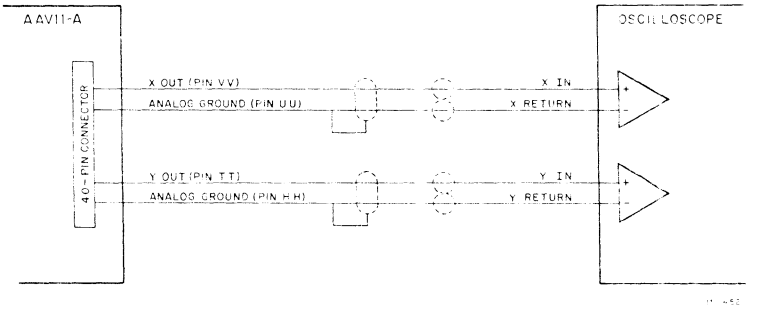


Figure 4 J1 Connector Pin Assignments

Table 5 AAV11-A Digital-to-Analog Conversions*

Input Code (octal)	Bipolar ±2.56 V (volts)	Bipolar ±5.12 V (volts)	Bipolar ±10.24 V (volts)	Unipolar 0 V to +5.12 V (volts)	Unipolar 0 V to +10.24 V (volts)
0000	−2.56	−5.12	−10.24	+0.0	+0.0
0001	−2.55875	−5.1175	−10.235	+0.00125	+0.025
3777†	−0.00125	−0.0025	−0.005	+2.55875	+5.1175
4000	0.0	0.0	0.0	+2.56	+5.12
4001	+0.00125	+0.0025	+0.005	+2.56125	+5.1225
7777	+2.55875	+5.1175	+10.235	+5.11875	+10.2375

* Offset binary for bipolar, straight binary for unipolar operating modes. Conversions may be made between 2's complement signed binary and offset binary numbers by subtracting 4000_8 from the 2's complement number (or adding 4000_8 to the offset binary number) and using only the low order 12 bits of the result.

† Note that in all ranges, actual maximum positive voltage output is 1 LSB less than nominal maximum positive output.

FUNCTIONAL DESCRIPTION

General

The function of the AAV11-A module is to convert digital data input to an analog dc voltage output that is representative of the input. This is accomplished by the bus interface, the control logic, and the D/A converter functions as shown in Figure 5.

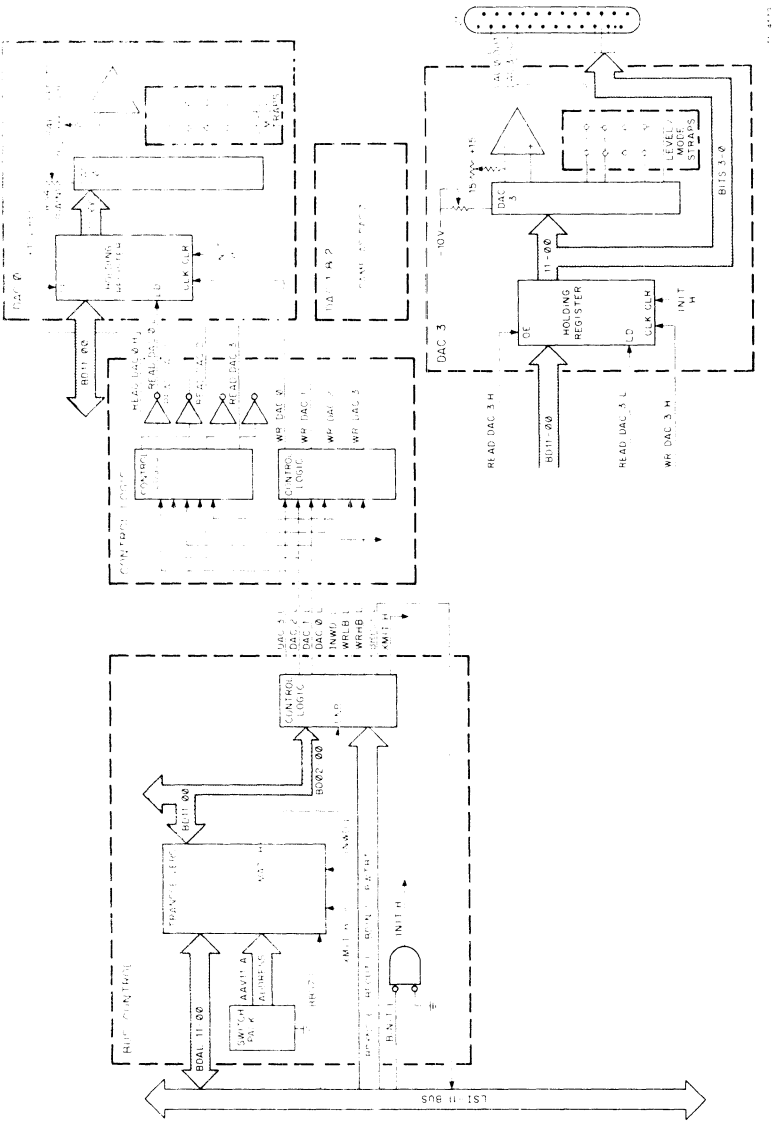


Figure 5 AAV11-A Block Diagram

Bus Interface
The logic associated with the bus interface section maintains proper communications protocol between the processor LSI-11 bus and the AAV11-A. This logic generates and monitors the bus signals involved during data transfers between the processor and the AAV11-A, permitting the AAV11-A to recognize when it is being addressed by the processor (address defined by setting on the address switch pack), to accept input data from the processor, and to output data to the processor.

Control Logic
The AAV11-A has no control/status register. The four digital-to-analog converters continually generate voltages at their outputs that reflect whatever digital values have most recently been written into their respective holding registers. The role of the control logic is to make the necessary discriminations between requests to change the state of the holding registers (i.e., to *write* into the holding registers), and requests to put the holding register contents onto the BD lines where they can be picked up through the transceivers by the processor.

DACs 0, 1, and 2
Digital-to-analog conversion functions are performed in each of the four AAV11-A channels by identical circuits:

- A holding register which stores the digital value output by the processor
- A digital-to-analog converter (DAC) proper which generates a current that is a function of the holding register value and of the mode/level jumper conditions
- An amplifier that translates the current into a proportional voltage, provides a low output impedance for the channel, and permits adjustment of signal offset.

DAC 3
DAC 3 is identical to DACs 0, 1, and 2 except that holding register bits 0–3 are routed to the I/O connector as well as to the DAC. This arrangement permits these bits to be routed to external equipment that requires binary control signals at programmable intervals. Control data in these bit positions affects any 12-bit D/A conversion that they coincide with, but since they involve the least significant bits of the word, the worst-case error is less than 0.5 percent. Consequently, DAC 3 can be used as a 12-bit DAC or as an 8-bit DAC plus four output bits for CRT Intensify, Store, Non-Store, Erase, etc.

ADV11-A ANALOG TO DIGITAL CONVERTER

GENERAL

The ADV11-A is a 12-bit successive approximation analog-to-digital converter that samples analog data at specified rates and stores the digital equivalent value for processing. A multiplexer section can accommodate up to 16 single-ended or 8 quasi-differential inputs. The converter section uses a patented auto-zeroing design that measures the sampled data with respect to its own circuitry offset and therefore cancels out its own offset error.

A/D conversions are initiated by program command, clock overflow, or external events. The program control is determined by the control and status register (CSR). The clock overflow command is supplied by the KWV11-A option. External event inputs can originate at the user's equipment or from the Schmitt trigger output on the KWV11-A clock. The digital data output is routed through a buffer register to the bus, from which it can be transferred into memory. This buffer optimizes the throughput rate of the converter.

Three reference signals are provided for self-testing on any channel input: two dc levels and one bipolar triangular waveform. This output can be used with DIGITAL diagnostic software to produce a data base for extremely thorough and precise analog linearity testing.

FEATURES

- 16-channel multiplexer
- Sample-and-hold functions
- Auto zeroing technique
- Buffered data output
- Self-testing features

SPECIFICATIONS

Identification	A012
Type	Quad
Power	+5 Vdc ± 5% at 2.0 A +12 Vdc ± 3% at 450 mA
Bus Loads	
AC	3.3
DC	1

ADV11-A

Inputs

Analog input protection	Fusible resistor guaranteed to open at ±85 V within 6.25 seconds. Guaranteed not to open from −25 V to +20 V at the input. Overload affects no components other than the fusible resistor on the overloaded channel; no other channels are affected.
Logic input protection	Fusible resistor guaranteed to open at ±25 V within 6.25 seconds. Guaranteed not to open from −4 V to +9 V at the input.
Analog input full scale range (FSR)	10.24 V bipolar (−5.12 V to +5.12 V)
Analog input dynamic resistance ($\lvert Vin \rvert \leq 5.12$ V)	100 MΩ, minimum
Analog input bias current ($\lvert Vin \rvert \leq 5.12$ V)	50 nA, maximum
Logic input voltages	Low = 0.0 to +0.7 V High = +2 V to +5 V
Logic input currents	Low = −6.8 mA at 0 V High = +1.3 mA at +5 V
Logic input rise/fall time	400 ns, maximum

Coding

A/D converter

Resolution	12 bits, binary weighted (2.5 mV nominal)
Format	Parallel offset binary, right justified

Input Voltage	Output Code
+FS-1 LSB	7777
0	4000
−FS	0
	(FS = 5.12 V; 1 LSB = 2.5 mV)

Vernier D/A	
Resolution	8 bits, binary weighted
Format	Offset binary encoded

Input Code	Approximate Offset Voltage
377	+2.5 A/D LSB (+6.4 mV)
200	0
0	−2.5 A/D LSB (−6.4 mV)

Performance

Gain error	Adjustable to zero
Offset error	Adjustable to zero
Differential linearity	No skipped states; no states wider than 2 LSB. 99% of state widths ±1/2 LSB
Integral linearity	±1 LSB, maximum non-linearity (referenced to end points)
Temperature coefficients	Gain = 6 PPM per °C Linearity = 2 PPM of full-scale range per °C Offset = 7.5 PPM of full scale range per °C
Noise	Module = 0.4 LSB rms; 2 LSB peak System = 0.5 LSB rms; 2 LSB peak
Warm-up time	5 minutes, maximum

Timing

External Start	Low level pulse, 50 ns minimum to 10 μs maximum; conversion starts on leading edge
Synchronization	0 to T
Conversion time	16 T (T = clock period = 2 μs)
Transition interval (reacquisition interval between end of conversion or channel change and start of new conversion)	9 μs

Test Signals

The ADV11-A provides three output voltages for test purposes:

1. Positive dc level, +4.4 V (±15%)
2. Negative dc level, −4.4 V (±15%)
3. Triangular wave, 15 Hz nominal (±15%).

CONFIGURATION

General

This section describes how the user can configure the module so that it will function within his system by setting dip switches S1 and S2 (Figure 1) to obtain the desired device address and interrupt vector as described in Table 1. When a jumper wire is inserted between the lugs, the single-ended inputs (16 channels) are selected. When the wire is removed, quasi-differential inputs are selected.

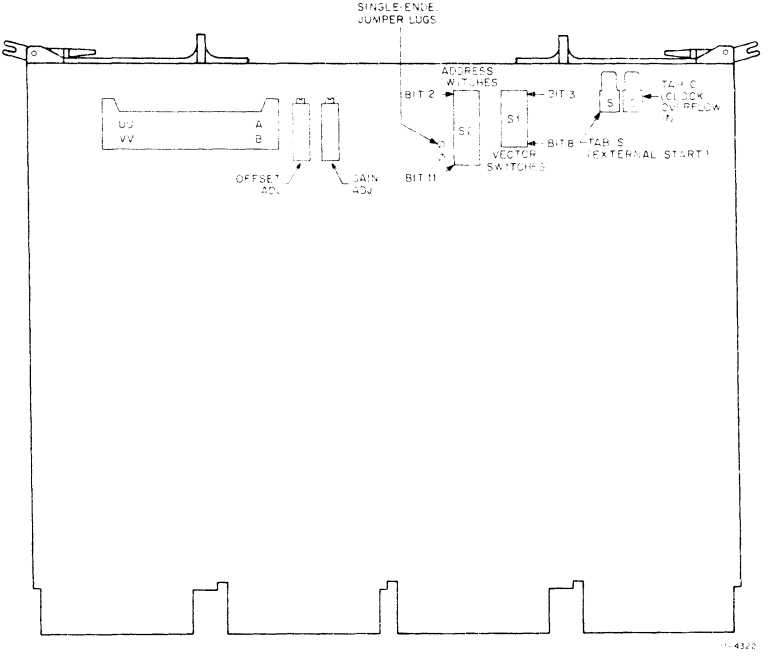


Figure 1 ADV11-A Connectors and Switches

Table 1 Standard Assignments

Description	Mnemonic	First Module Address	Second Module Address
Registers			
Control and Status	CSR	170400	170420
Data Buffer	DBR	170402	170422
Interrupt Vectors			
Conversion Complete		400	410
Error		404	414

Registers

The control and status register (CSR) address can be selected in the range of 170000 to 177774 by using the S2 dip switch as shown in Figure 2. Switch S2 is factory-set at 170400, which is the recommended address as illustrated in Figure 2. The functions of the CSR bits are shown in Figure 3 and detailed in Table 2.

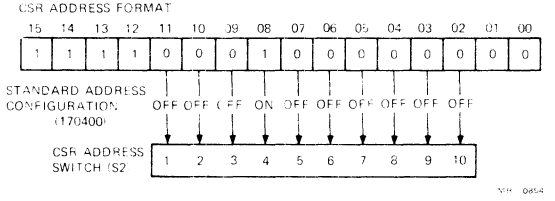


Figure 2 CSR Switch-Selectable Address

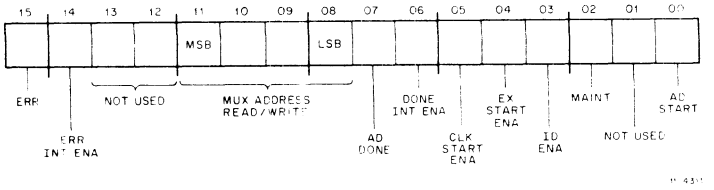


Figure 3 CSR Bit Format

Table 2 CSR Bit Functions

Bit	Description
15	A/D Error (Read/Write) – The A/D Error bit may be program set or cleared and is cleared by asserting BINIT L. It is set by any of the following conditions. 1. Attempting an external or clock start during the transition interval 2. Attempting any start during a conversion in progress 3. Failing to read the result of a previous conversion before the end of the current conversion.
14	Error Interrupt Enable (Read/Write) – When set, enables a program interrupt upon an error condition (A/D Error). Interrupt is generated whenever bits 14 and 15 are set, regardless of which was set first.
13–12	Not used.
11–8	Multiplexer Address (Read/Write) – Contain the number of the current analog input channel being addressed.
7	A/D Done (Read) – Set at the completion of a conversion when the data buffer is updated. Cleared when the data buffer is read and by asserting BINIT L. If enabled, interrupts are requested simultaneously by both bits 7 and 15; bit 7 has the higher priority.
6	Done Interrupt Enable (Read/Write) – When set, enables a program interrupt at the completion of a conversion (A/D Done). Interrupt is generated when bit 7 and bit 6 are both set, regardless of sequence.
5	Clock Start Enable (Read/Write) – When set, enables conversions to be initiated by an overflow from the clock option.
4	External Start Enable (Read/Write) – When set, enables conversions to be initiated by an external signal or through a Schmitt trigger from the clock option.
3	ID Enable (Read/Write) – When set, causes bit 12 of the data buffer register to be loaded to a 1 at the end of any conversion.

Table 2 CSR Bit Functions (Cont)

Bit	Description
2	Maintenance (Read/Write) – Loads, when set, all bits of the converted data output equal to multiplexer address LSB (bit 8) at the completion of the next conversion. Cleared by asserting BINIT L. Used for all 0s and all 1s = tests of A/D conversion logic.
1	Not used.
0	A/D Start (Read/Write) – Initiates a conversion when set. Cleared at the completion of the conversion and by asserting BINIT L.

The data buffer register (DBR) address will be the next even address following the selected CSR address. This address has two separate DBR registers: one read only and the other write only. The functions of the register bits are shown in Figure 4 and described in Table 3.

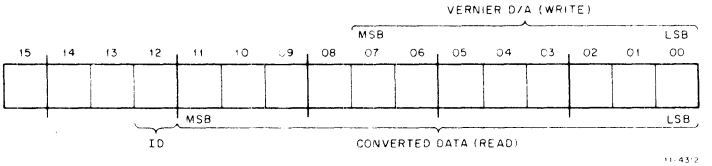


Figure 4 DBR Bit Format

Table 3 DBR Bit Functions

Bit	Function
Read Only	
15–13	Not used. Should read as 0.
12	ID – When ID Enable (bit 3) of the CSR has been set, DBR bit 12 will be set to a 1 at the end of conversion.
11–0	Converted Data – These bits contain the results of the last A/D conversion.

Table 3 DBR Bit Functions (Cont)

Bit	Function
Write Only	
15–8	Not used.
7–0	Vernier D/A – These bits provide a programmed offset to the converted value (scaled 1 D/A LSB = 1/50 A/D LSB). The hardware initializes this value to 200_8 (mid-range). Values greater than 200_8 make the input voltage appear more positive.

Vector Interrupt
The A/D conversion complete interrupt vector is set by dip switch S1 (Figure 1). Any address in the range of 000 to 777 can be selected by the user. The switch is factory-configured for 400, the recommended vector, as shown in Figure 5. The error interrupt vector will be four words higher than the A/D conversion complete interrupt vector.

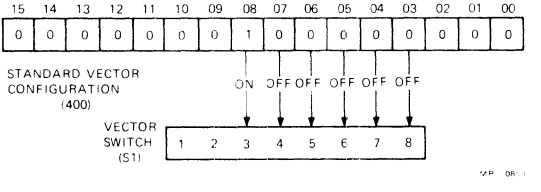


Figure 5 Interrupt Vector

Mode Control
The ADV11-A is equipped with the jumper lugs (Figure 1) that permit changing the operating mode from quasi-differential (no connection) to single-ended (jumper installed). The single-ended mode can also be selected by connecting H854 connector pin C to logic ground. This alternative is provided to permit convenient external mode selection in installations that require frequent alteration between one mode and the other.

Analog Input Interfacing

Single-Ended Mode – Single-ended analog input signals for the ADV11-A may be of two types, grounded and floating. A grounded input

is one whose level is referenced to the ground of the instrument that is producing it, as illustrated in Figure 6. Since the instrument may be located at a distance from the computer, there may be some voltage difference between the instrument ground and the computer ground. The voltage seen by the ADV11-A will be the sum of the undesired ground difference voltage and the desired instrument signal voltage. In cases where such differences are encountered, they can be minimized by plugging the instrument into an ac outlet as close as possible to that providing power to the computer. Do *not* run a wire from user's ground to the ADV11-A analog ground. Such a wire can cause ground loop currents which affect results not only on the input channel in question, but also on other channels.

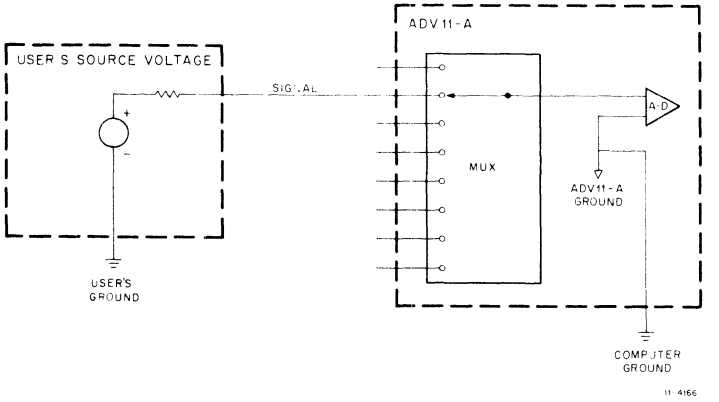


Figure 6 Single-Ended Input Referenced to User's Ground

A floating input is one whose signal voltage is developed with respect to a point not connected to ground, as illustrated in Figure 7. The identifying characteristic of a floating source is that connecting the signal return to the ADV11-A ground does not result in a current path between the ADV11-A ground and the instrument ground.

Note that the return of a floating input must be connected to one of the ADV11-A's analog ground terminals. Ground points may be shared among channels, as illustrated by the battery-powered sources in the figure.

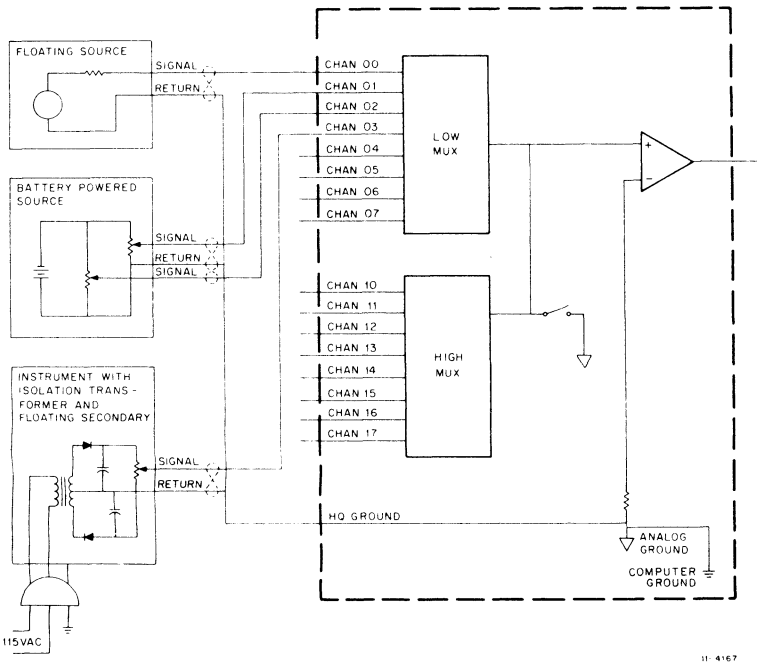


Figure 7 Floating ADV11-A Input Signals

Quasi-Differential Mode – The "quasi" prefix in "quasi-differential" can best be explained in the context of a preliminary review of true differential operation. A true differential input involves two signal lines connected to a differential amplifier in such a way that the output of the device is a function of the instantaneous *difference* between the voltages on the two signal lines. One advantage of such a configuration is illustrated in Figure 8.

Figure 8a assumes a single-ended generating device that produces a signal, V_S with respect to its ground and is situated sufficiently far from the receiving device for a significant noise voltage, V_n, to be developed in the power distribution ground lines. The result is that, at any given instant, the differential amplifier in the receiving device sees both the signal voltage and the noise voltage. Its output, V_O, is a function of $V_S + V_n$ and is in error with respect to V_S alone.

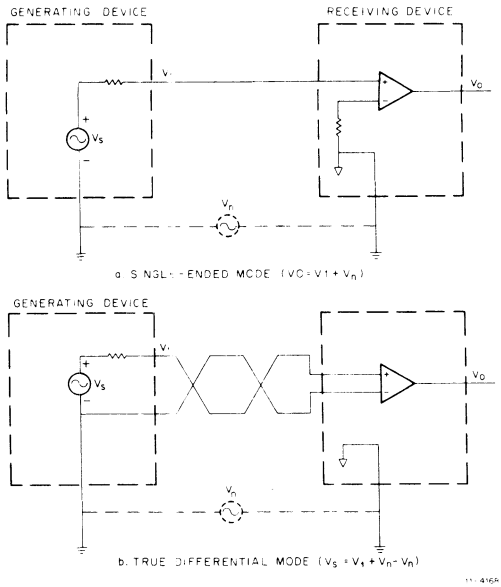


Figure 8 Single-Ended Versus True Differential Input Modes

Figure 8b illustrates the same device connected in true differential mode. The same noise voltage exists in the power distribution ground system, except the generating device ground is connected directly to the negative input of the receiving differential amplifier. Since the instantaneous noise voltage is common to both the + and – inputs, it is cancelled out of the final amplifier output. V_O now provides a valid representation of V_S alone.

Figure 9 illustrates the ADV11-A operating in the quasi-differential mode.

The major contrast between true differential operation as described above and the operation of the ADV11-A in differential mode is that in the latter, the two sides of the signal are not simultaneously input to a differential amplifier. Rather, their difference is established by a sequential operation that first samples the voltage at one of the two inputs and then, holding this value fixed, in effect subtracts from it the voltage at the second input. For near dc conditions, this procedure produces a result like that of true differential operation (i.e., the output is a function

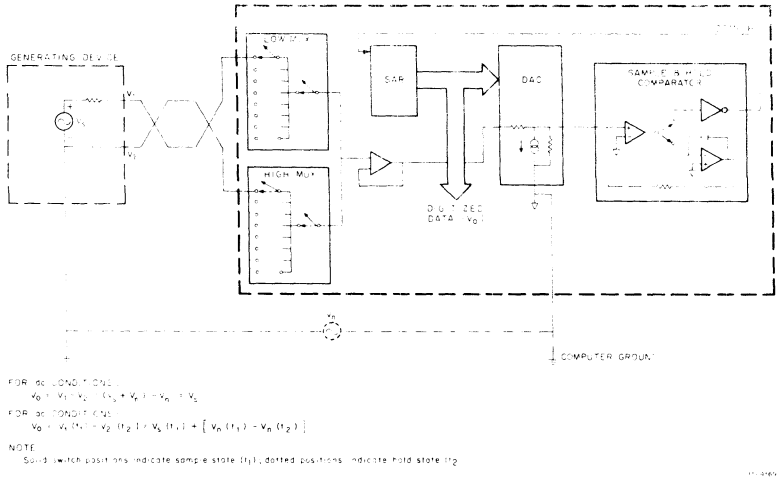


Figure 9 ADV11-A Quasi-Differential Mode

of the difference between the two input voltages, and common mode voltages are cancelled out). But, since there is a significant time lapse between taking the sample and completing the final approximation, a possibility for error is introduced by the ADV11-A that increases as a function of common mode signal frequency. The result is that the common mode rejection ratio, while essentially infinite at dc, rolls off for ac signals, and is about 40 dB at 60 Hz line frequency. In addition, since the holding action of the sample-and-hold circuit is only in effect on the first (non-inverting, signal) input but not on the second (inverting, return) input, the voltage rate of change on the second input should be kept below 25 mV/ms. This is the slope that results in a quarter-LSB change during the conversion interval. Such a rate of change corresponds to 125 mV peak-to-peak at 60 Hz line frequency. This dynamic response difference between the two inputs requires distinguishing the ADV11-A's differential mode from true differential operation. Hence the term "quasi-differential."

Installation Precautions

As a preliminary step, confirm that the computer power supply ground is connected to power line (earth) ground. If continuity checks reveal no such connection, attach a length of 12-gauge wire between the power supply ground and a convenient point associated with earth ground.

Twisted Pair Input Lines – The effects of magnetic coupling on the input signals may be reduced for floating single-ended or differential inputs by twisting the signal and return lines in the input cable. If the inductive pickup voltages of the two leads match, the net effect seen at the ADV11-A input is zero. Use of twisted pairs has no effect with a single-ended non-floating signal (referenced to ground at the instrument end).

Shielded Input Lines – The effects of electrostatic coupling on the input signals may be reduced by shielding the signal wires. This is especially important if the instrument or transducer has high source impedance. To prevent the shield from carrying current and thus developing ground loop voltages within the ADV11-A, connect it to ground at the instrument end only.

Allowing for Input Settling with High Source Impedance – All solid-state multiplexers inject a small amount of charge into their input lines when changing channels, causing a transient error voltage that is discharged by the input signal's source impedance. The ADV11-A shares this characteristic, and also injects a small charge into the selected input line at the end of each conversion when the auto-zero switch is turned off. After any channel change and after any conversion, the ADV11-A's control logic allows a 9 μs interval (identified as the transition interval) during which conversions cannot start without generating error conditions. Normally, this is sufficient time for the input transient to settle out. However, more time may be needed when the multiplexer is switching into an input channel with high source impedance, particularly when large amounts of shunt capacitance exist in the interconnecting cables. Source impedance/cable shunt capacitance products greater than 1 μs should be avoided whenever conversions are to be made at maximum rate with less than 1/2 LSB error. This means that cable shunt capacitance for a 1000 Ω source should not exceed 1000 pF ($10^3 \times 10^{-9} = 10^{-6}$), that shunt capacitance for a 100 Ω source should not exceed 0.01 μF ($10^2 \times 10^{-8} = 10^{-6}$), etc. Assuming twisted pair cable capacitance of 50 pF/foot, these constraints translate into a maximum run of 20 feet from a 1000 Ω source, 200 feet from a 100 Ω source, etc. Note that these values are consistent with good practice for avoiding noise pickup in long cable runs. Note also that settling errors can be eliminated by increasing the time between conversions or incorporating a software delay between channel changes and program start commands.

Connections

Figure 1 illustrates the location of user connectors and switches on the component side of the ADV11-A board.

ADV11-A

Analog input signals are input to the ADV11-A through the 40-pin connector. Pin assignments for the connector are shown in Figure 10. The proper H856-to-H856 cable is the BC08R; the proper H856 to prepared open-ended cable is the BC04Z.

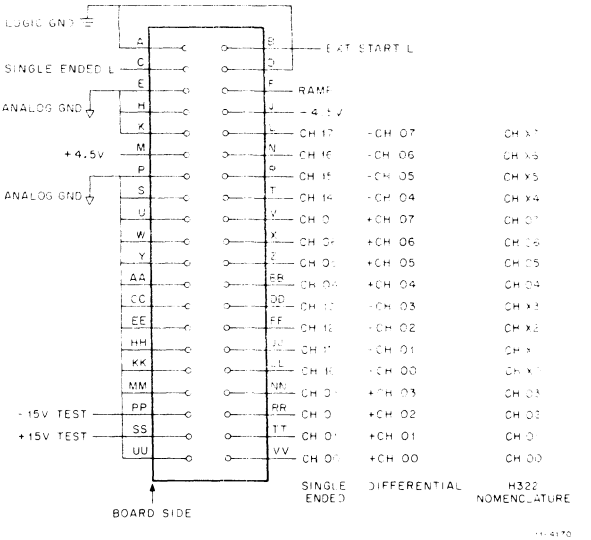


Figure 10 ADV11-A 40-Pin Connector Pin Assignments

Distribution Panel – Figure 11 shows a H322 distribution panel that is connected on the rear to the ADV11-A Berg connector and on the front provides easily identifiable and conveniently accessible barrier strip connections for user apparatus. Each H322 accommodates two ADV11-As or one ADV11-A and one other single-connector device. The ADV11-A is shipped with decal sets that specifically identify ADV11-A inputs and outputs. Note that the H323-B potentiometer box may *not* be used with the ADV11-A.

External and Clock Starts – The external start signal line, pin B of the 40-pin connector or TAB S (Figures 1 and 10), is a TTL-compatible input that presents five unit loads (8.0 mA) to any driving output. Conversions start on the high-to-low transitions of this signal.

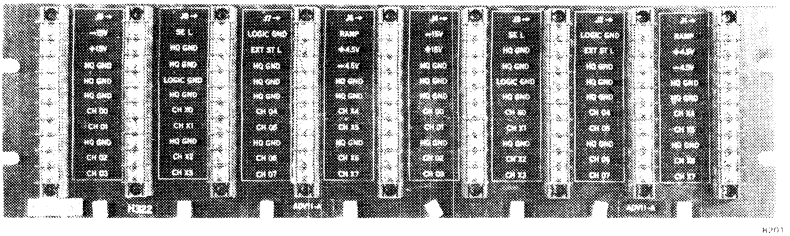


Figure 11 H322 Distribution Panel

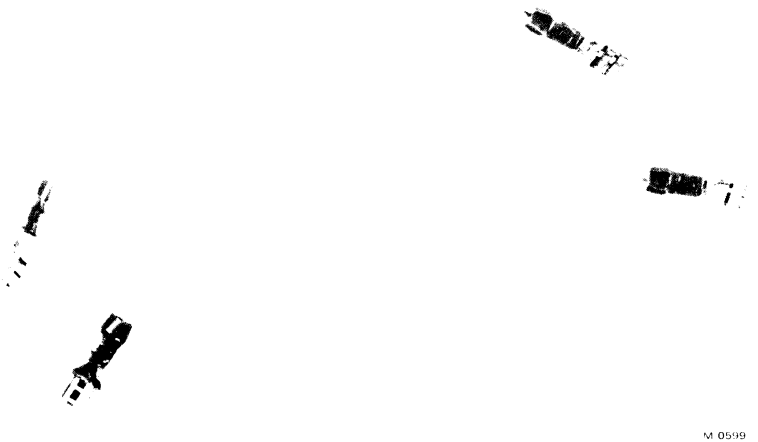


Figure 12 Module Jumpers

In most cases, the external start signal will be produced by a grounded (non-floating) pulse generator or logic circuitry located in a grounded instrument. The return path for the external start signal will be through the power line ground system. For this reason, ground differences between source and computer should be minimized to prevent spurious start pulses due to ground noise. In no case should a separate return line be run between grounded source and the computer ground. Only with floating devices should return lines be run between source logic ground and logic ground pins on the ADV11-A 40-pin connector. External

devices that require buffering can be interfaced to the ADV11-A through Schmitt trigger 1 of the KWV11-A clock (STI). Connection is made by means of a DEC 70-10771 type jumper (Figure 12) to TAB S (Figure 1) of the ADV11-A.

Conversions that must be initiated in consequence of time intervals or on every nth external event may be triggered from the KWV11-A through a DEC 70-10771 type jumper connected from the clock output tab (CLK) to the ADV11-A clock overflow tab (C).

PROGRAMMING

The following programming example reads 100_8 A/D conversions from channel 0 into locations 4000_8–4176_8 and halts.

```
START:  CLR     @ADSR           ;CLEAR A/D STATUS REGISTER
        MOV     #4000,R0        ;SET UP FIRST ADDRESS
        INC     @ADSR           ;START A/D CONVERSION
LOOP:   TSTB    @ADSR           ;CHECK DONE FLAG
        BPL     LOOP            ;WAIT UNTIL FLAG SET
        INC     @ADSR           ;START NEXT CONVERSION*
        MOV     @ADBR,(R0)+     ;PLACE CONVERTED VALUE
                                ;FROM A/D BUFFER INTO MEMORY
                                ;LOCATION AND SET UP NEXT
                                ;LOCATION FOR TRANSFER*
        CMP     R0,#4200        ;CHECK IF 100 CONVERSIONS
                                ;HAVE BEEN DONE
        BNE     LOOP            ;NO, GET NEXT CONVERSION
        HALT                    ;DONE
ADSR:   170400                  ;A/D STATUS REGISTER ADDRESS
ADBR:   170402                  ;A/D BUFFER REGISTER ADDRESS
        .END    START
```

*Starting a subsequent conversion before moving data from a previous conversion is recommended only with systems equipped with non-processor memory refresh. Without this capability, data will be lost occasionally by CPU memory refresh intervening between the INC and MOV commands. In general, non-processor memory refresh is essential to realizing the full potential of the ADV11-A.

FUNCTIONAL DESCRIPTION

General

The function of the ADV11-A module is to convert analog input data to a 12-bit digital word that is representative of the input. This is done by the channel selection, control logic, A/D converter, and bus interface functions as shown in Figure 13.

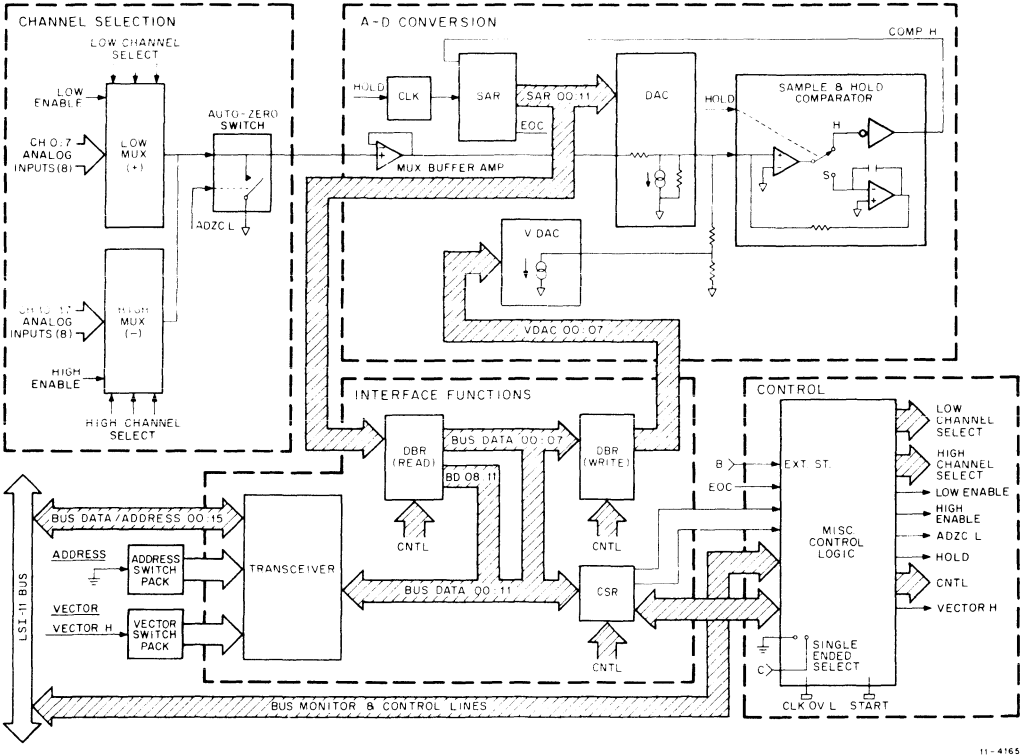


Figure 13 ADV11-A Functional Block Diagram

Channel Selection

Channel selection is accomplished under program control by two 8-channel multiplexers and is a function of the data asserted in bits 8 through 11 of the control/status register (CSR). Each of the 16 analog input channels is routed to the single output channel through a MOS field-effect transistor which acts as a normally open switch. During the sample interval, the data pattern in CSR bits 8 through 11 selects one of these transistors and causes it to change from a condition of nearly infinite resistance (1 GΩ or more) to one of very low resistance (1000 Ω or less). Since in the selected state the transistor conducts current within the ±5.12 V limits equally well in both directions, it now functions as a closed switch, effectively routing to the output line whatever analog signal is connected to its input.

A/D Conversion

A/D conversions can be initiated in three ways: under program control, on overflow from the KWV11-A real-time clock, or on external input. When a conversion is completed or the control program writes a multiplexer address into the CSR, the control logic initiates the transition interval, a delay of about 9 μs to allow the multiplexer adequate selection and settling time and to permit a valid representation of the signal level to be established in the sample circuit. If no A/D start signal has occurred by the time the transition interval has elapsed, the sample circuit merely follows the signal transmitted to it through the selected multiplexer channel and waits for an A/D start signal. When an A/D start signal occurs – or at the end of the transition interval if A/D start was previously generated by the writing of the CSR GO bit – the sample-and-hold circuits are switched to hold, sustaining the sampled level for the next step. The multiplexer output is then set to its hold condition, i.e., to ground if the single-ended (SE) input is set low for single-ended measurement, to the second differential input (return line) if the SE input is not set low. Note that if an external or clock start signal occurs during the transition interval, conversion starts immediately, without waiting for the transition interval to be completed. Bit 15 of the CSR (A/Error) is set, however, and an interrupt is generated if bit 14 (error interrupt enable) is set – alerting the program that conversions are occurring too fast and are consequently liable to be in error.

Under normal conditions, it is not until the transition interval is complete that the measurement process is begun. The successive approximation register (SAR) is cycled through 13 states by the clock. In the first state, its output code involves only the most significant bit (MSB) of the 12-bit SAR word. This output code causes the feedback digital-to-analog converter to generate an output equivalent to that produced by the hold circuits in response to a sample voltage of 0. The digital-to-analog converter output is summed with that produced by the hold circuits and with that coming from the grounded multiplexer output (single-ended mode)

or from the second differential input (quasi-differential mode). If the current from the summing mode is negative, the first approximation was too low, and the comparator signals the SAR to maintain the state of bit 11 and repeat the process with bit 10. If the current from the summing mode is positive, the first approximation was too high and the SAR changes the state of bit 11 before cycling into the second approximation. This process continues until all 12 bits in the word have been set, tested, and if necessary, changed. The 13th state (end of conversion, or EOC) indicates that the measurement is complete and that the SAR now contains an offset binary equivalent of the sampled voltage and may therefore be transferred to the processor. EOC causes the sample-and-hold circuits to return to the sample mode and to reset the SAR, preventing further SAR activity until the occurrence of the next hold condition.

Note that because the reference point against which the sample voltage is compared is at the output of the multiplexer itself rather than internal to the sample-and-hold circuits, all offset voltages generated by the intervening circuits are common to both sample-and-hold conditions and are therefore cancelled out of any measurement. In single-ended mode, grounding the multiplexer output (and thereby establishing this reference point) is identified as auto-zeroing the converter.

Bus Interface

In addition to stopping the SAR clock and reestablishing the sample mode, the end-of-conversion signal also initiates the process that causes the SAR data to be transferred to the processor. Since this operation takes a finite amount of time which would interfere with subsequent measuring operations, the SAR data is first transferred to a holding device, the data buffer register (DBR), where it will remain until the processor can be notified to read the conversion data for processing. In the meantime, the channel selection and A/D conversion circuits can begin the next measurement as dictated by control/status register (CSR) bit conditions controlled by the processor.

Included in the ADV11-A interface is an extension of the DBR designed to accept 8-bit write information from the bus data/address lines. This buffer permits programmed setting of the vernier DAC. Also included are transceivers that connect the bidirectional bus data lines to the LSI-11 bus data/address lines. Associated with these transceivers are switches that permit assigning device and vector addresses to any given ADV11-A.

Control Logic

As the above discussion suggests, a large number of signals must be precisely orchestrated each time the ADV11-A executes a conversion. The control logic contains an assortment of gates, latches, read-only

memories, and timing circuits designed to ensure that multiplexer channels are properly selected, sample durations are of adequate length, conversions are not initiated during uncompleted previous conversions, etc. In general, this logic precludes the need for the user to attend to any but the most elementary details of the conversion process, e.g., making necessary connections to the system and writing control programs that make appropriate use of the CSR.

BDV11 DIAGNOSTIC, BOOTSTRAP, TERMINATOR

GENERAL

The BDV11 module has 2K words of read-only memory (ROM) that contains both diagnostic programs and bootstrap programs. These programs are user-selectable by setting dip switches. The diagnostic programs test the processor, the memory, and the user's console. The bootstrap programs are used to boot a number of LSI-11-compatible peripherals. The module also contains 120-ohm bus terminator circuits.

Space is available on the module to allow the user to add up to 2K words of erasable programmable ROM (EPROM) and up to 16K words of read-only memory (ROM).

A HALT/ENABLE switch allows the user to start and stop the processor and a RESTART switch enables the user to reboot the system. The module also has four programmable light-emitting diodes (LEDs) that indicate a failure in a program and monitor the tests in progress. All the switches and indicators are edge-mounted on the module for easy access.

NOTE

There are two versions of the BDV11 module: revisions 0 and A. The revision 0 module was produced in limited quantities and does not incorporate all the characteristics of the revision A. The differences between these modules are listed at the end of this section.

FEATURES

- Programmed ROMs with bootstraps for RXV11, RXV21, RLV11, and RKV11 disk options
- DECnet bootstraps for DLV11-E, DLV11-F, and DUV11 serial line units
- Capable of boooting a system automatically with no operator intervention
- Can automatically load and start a 16K word program from ROM/EPROM to RAM
- 12-bit readable configuration register
- 16-bit read/write maintenance register
- Software-controllable line-time clock (LTC)
- Power OK monitor, green LED
- 4-bit LED programmable display
- RESTART and HALT switches
- 120-ohm bus terminator

BDV11

SPECIFICATIONS

Identification	M8012
Type	Quad
Power	+5 Vdc ± 5% at 1.6 A +12 Vdc ± 3% at 0 07 A
Bus Loads	
AC	2
DC	1

CONFIGURATION

General

The BDV11 is factory-configured (Group A in Table 2) by DIGITAL to allow the user the capability of expanding the diagnostic and bootstrap programs by adding 2K of EPROM and 16K of ROM/EPROM memory. The user is allowed to modify the configuration to allow the use of his own software requirements. There are 13 jumper wires located on the module as shown in Figure 1. Eight are used for selecting sockets and five are used to accommodate various types of memory chips used. The jumper wires are identified in Table 1. The switches used to select programs are listed in the section entitled "Programming."

Socket Selection

The socket selection logic is controlled by jumpers W1–W4 and W9–W12 and they can be configured in seven different ways as shown in Table 2. Group A assigns the PCR pages and socket selections. Groups B–G allow the user a choice of where the program execution begins, such as having the processor execute instructions directly from a system ROM or EPROM when power is turned ON, rather than from the diagnostic/bootstrap ROM.

Table 1 Selectable Jumpers

Jumper	Function
W1	Socket selection
W2	Socket selection
W3	Socket selection
W4	Socket selection
W5	Chip selection
W6	Chip selection
W7	Chip selection
W8	Chip selection
W9	Socket selection
W10	Socket selection
W11	Socket selection
W12	Socket selection
W13	Chip selection

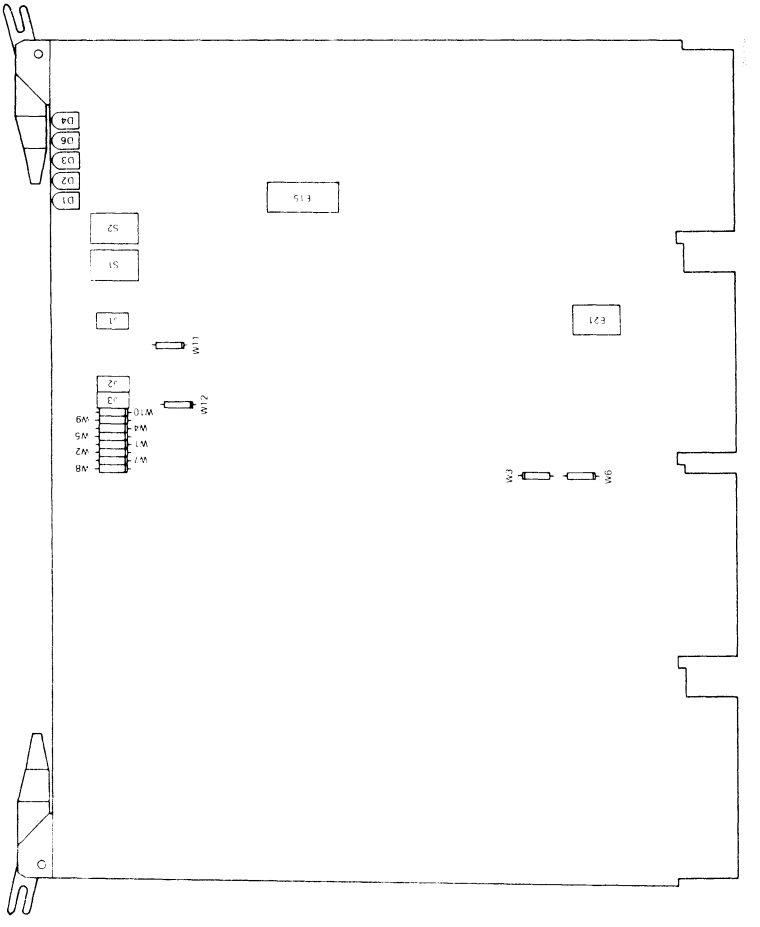


Figure 1 BDV11 Switch and Jumper Locations

Table 2 Memory Configuration

High Byte Socket	Low Byte Socket	Configuration Designation	ROM Address	PCR Page	Selection Signal
4K DIAGNOSTIC/BOOTSTRAP (DIGITAL)					
E53	E48	A	0–2K	0–17	SB1 L
(2)	(1)	B	4K–6K	40–57	SB1 L
		C	16K–18K	200–217	SB1 L
		D	20K–22K	240–257	SB1 L
E58	E44	A	2K–14K	20–37	SB2 L
(4)	(3)	B	6K–8K	60–77	SB2 L
		C	18K–20K	220–237	SB2 L
		D	22K–24K	260–277	SB2 L
2K USER EPROM					
E57	E40	A	4K–5K	40–47	SE1 L
(3)	(1)	B	0–1K	0–7	SE1 L
		C	20K–21K	240–247	SE1 L
		D	16K–17K	200–207	SE1 L
E52	E36	A	5K–6K	50–57	SE2 L
(4)	(2)	B	1K–2K	10–17	SE2 L
		C	21K–22K	250–257	SE2 L
		D	17K–18K	210–217	SE2 L

Table 2 Memory Configuration (Cont)

High Byte Socket	Low Byte Socket	Configuration Designation	ROM Address	PCR Page	Selection Signal
16K USER ROM					
E54	E49	A	16K–18K	200–217	SP8 L
(2)	(1)	E	16K–17K	200–207	SP8 L
		F	0–2K	0–17	SP8 L
		G	0–1K	0–7	SP8 L
E59	E45	A	18K–20K	220–237	SP7 L
(4)	(3)	E	18K–19K	220–227	SPP7 L
		F	2K–4K	20–37	SP7 L
		G	2K–3K	20–27	SP7 L
E60	E41	A	20K–22K	240–257	SP6 L
(6)	(5)	E	18K–19K	240–247	SP6 L
		F	4K–6K	40–57	SP6 L
		G	4K–5K	40–47	SP6 L
E55	E37	A	22K–24K	260–277	SP5 L
(8)	(7)	E	22K–23K	260–267	SP5 L
		F	6K–8K	60–77	SP5 L
		G	6K–7K	60–67	SP5 L

Table 2 Memory Configuration (Cont)

High Byte Socket	Low Byte Socket	Configuration Designation	ROM Address	PCR Page	Selection Signal
16K USER ROM (CONT)					
E51	E38	A	24K–26K	300–317	SP4 L
(10)	(9)	E	17K–18K	210–217	SP4 L
		F	8K–10K	100–117	SP4 L
		G	1K–2K	10–17	SP4 L
E47	E42	A	26K–28K	320–337	SP3 L
(12)	(11)	E	19K–20K	230–237	SP3 L
		F	10K–12K	120–137	SP3 L
		G	3K–4K	30–37	SP3 L
E43	E46	A	28K–30K	340–357	SP2 L
(14)	(13)	E	21K–22K	250–257	SP2 L
		F	12K–14K	140–157	SP2 L
		G	5K–6K	50–57	SP2 L
E39	E50	A	30K–32K	360–377	SP1 L
(16)	(15)	E	23K–24K	270–277	SP1 L
		F	14K–16K	160–177	SP1 L
		G	7K–8K	70–77	SP1 L

NOTE

The parenthetical numbers in the socket columns indicate the order in which each ROM is to be installed.

Memory Configuration

The user can change the configuration of the BDV11 memory structure by using socket selection jumpers W1–W4 and W9–W12; the standard configuration is designated "A" in Table 2. This table also indicates the installation order for the PROM/ROM chips. The B, C, D, E, F, and G configurations are shown as alternate ways the user can map the ROM memory. The details of how to select a configuration using the socket selection jumpers are shown below.

Configuration Designation	Socket Selection Jumpers*							
	W1	W2	W3	W4	W9	W10	W11	W12
A	R	I	I	R	I	R	R	I
B	X	X	X	X	I	R	I	R
C	X	X	X	X	R	I	R	I
D	X	X	X	X	R	I	I	R
E	I	R	I	R	X	X	X	X
F	R	I	R	I	X	X	X	X
G	I	R	R	I	X	X	X	X

*I = Installed, R = Removed, X = Don't care.

Chip Selection

The system ROM sockets can be occupied by either 2K ROMs or 1K ROMs. The ROM socket logic uses jumpers W5–W8 and W13 to select the type of ROM that can be used on the BDV11. The jumper configuration is detailed in Table 3, which also designates the type of ROM or PROM that is used with these configurations.

Control Registers

The BDV11 module has five hardware registers which are software addressable. These registers are assigned individual addresses that *cannot be changed or modified.* The registers are described in the following paragraphs; their designations and addresses are listed in Table 4.

Page Control Register (PCR) – This register is word- or byte-addressable and can be read or written. The PCR is a 16-bit register that consists of two 8-bit bytes. The low byte consists of bits 0–7 and the high byte consists of bits 8–15. When the low byte of the PCR is equal to page 6, then bus addresses 173000–173777 access the 128 ROM locations in the block 1400–1577. When a bus address falls in this range, the logic considers only the low byte of the PCR. However, if the bus address is in the range 173400–173777, only the high byte of the PCR is used to select the ROM location.

Table 3 Chip Selection Jumpers

ROM Type	Jumpers Inserted[1] W5	W6	W7	W8	W13
2708[2]	R	I	R	I	R
2716[3]	R	R	I	R	I
8316E[4]	I	R	I	R	R
8316E[5]	R	R	I	R	I

NOTES

1. I = inserted; R = removed
2. CB2 and DB2 must be supplied with external −5 V power.
3. Use only +5 Vdc type components.
4. Chip select signals must be programmed as follows:

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
LOW	LOW	LOW

5. Chip select signals must be programmed as follows:

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
LOW	LOW	HIGH

Table 4 Standard Assignments

Register	Read/ Write	Size	Address
Page Control	R/W	16 bits	177520
Read/Write	R/W	16 bits	177522
Configuration*	R	12 bits	177524
Display*	W	4 bits	177524
BEVNT*	W	1 bit	177546

* Dual-purpose register.

Table 5 relates the PCR contents to the PCR page for pages 0–17. As an example, if the PCR is loaded with data 000400, the PCR low byte contains data 000, while the high byte contains data 001. The PCR bytes can be loaded separately. To select ROM locations 1600–1777, for instance, one only needs to load the PCR high byte with page 7; thus, the high byte contains 007, while the low byte can contain anything. Table 6 lists the PCR contents for the remaining PCR pages.

Read/Write Register – This register is used as a maintenance register for the diagnostic programs. The register is cleared when power is turned on or when the RESTART switch is activated.

Configuration Register – This 12-bit register is read-only and is used for maintenance and system configuration by selecting diagnostics or bootstrap programs for execution. Bits 0–11 of the register are set by switches E15–1 through E15–8 and E21-1 through E21–4. These switches are associated with BDAL (0:11) L; when an individual switch is closed (on), the corresponding BDAL signal is low (1).

Display Register – This 4-bit register allows for program control of the diagnostic LED display. When bits 0–3 of the register are set, then the corresponding LEDs are off. The register is cleared by turning power on or activating the RESTART switch.

Table 5 PCR Contents/Page Relationship, Pages 0–17

PCR Page	PCR Contents	PCR High Byte (Bits 15–8)	PCR Low Byte (Bits 7–0)
0 1	000400	001	000
2 3	001402	003	002
4 5	002404	005	004
6 7	003406	007	006
10 11	004410	011	010
12 13	005412	013	012
14 15	006414	015	014
16 17	007416	017	016

Table 6 PCR Contents, Pages 20–57, 200–377

Page	Contents	Page	Contents
20, 21	010420	260, 261	130660
22, 23	011422	262, 263	131662
24, 25	012424	264, 265	132664
26, 27	013426	266, 267	133666
30, 31	014430	270, 271	134670
32, 33	015432	272, 273	135672
34, 35	016434	274, 275	136674
36, 37	017436	276, 277	137676
40, 41	020440	300, 301	140700
42, 43	021442	302, 303	141702
44, 45	022444	304, 305	142704
46, 47	023446	306, 307	143706
50, 51	024450	310, 311	144710
52, 53	025452	312, 313	145712
54, 55	026454	314, 315	146714
56, 57	027456	316, 317	147716
200, 201	100600	320, 321	150720
202, 203	101602	322, 323	151722
204, 205	102604	324, 325	152724
206, 207	103606	326, 327	153726
210, 211	104610	330, 331	154730
212, 213	105612	332, 333	155732
214, 215	106614	334, 335	156734
216, 217	107616	336, 337	157736
220, 221	110620	340, 341	160740
222, 223	111622	342, 343	161742
224, 225	112624	344, 345	162744
226, 227	113626	346, 347	163746
230, 231	114630	350, 351	164750
232, 233	115632	352, 353	165752
234, 235	116634	354, 355	166754
236, 237	117636	356, 357	167756
240, 241	120640	360, 361	170760
242, 243	121642	362, 363	171762
244, 245	122644	364, 365	172764
246, 247	123646	366, 367	173766
250, 251	124650	370, 371	174770
252, 253	125652	372, 373	175772
254, 255	126654	374, 375	176774
256, 257	127656	376, 377	177776

BEVNT Register – This single-bit register clamps the BEVNT signal low when the BEVNT switch is closed. This action permits program control of the processor line-time clock (LTC) function. The register is cleared when the power is turned on or when the RESTART switch is activated.

PROGRAMMING

General

The BDV11 contains dip switches that permit the user to select diagnostic and bootstrap programs for execution. These are monitored by the four LEDs that indicate when a program fails. A green LED monitors the +12 Vdc and +5 Vdc and is illuminated when power is ON. There is also a HALT/ENABLE switch and a RESTART switch for the user to start and stop the processor. The switches and LEDs are shown in Figure 2.

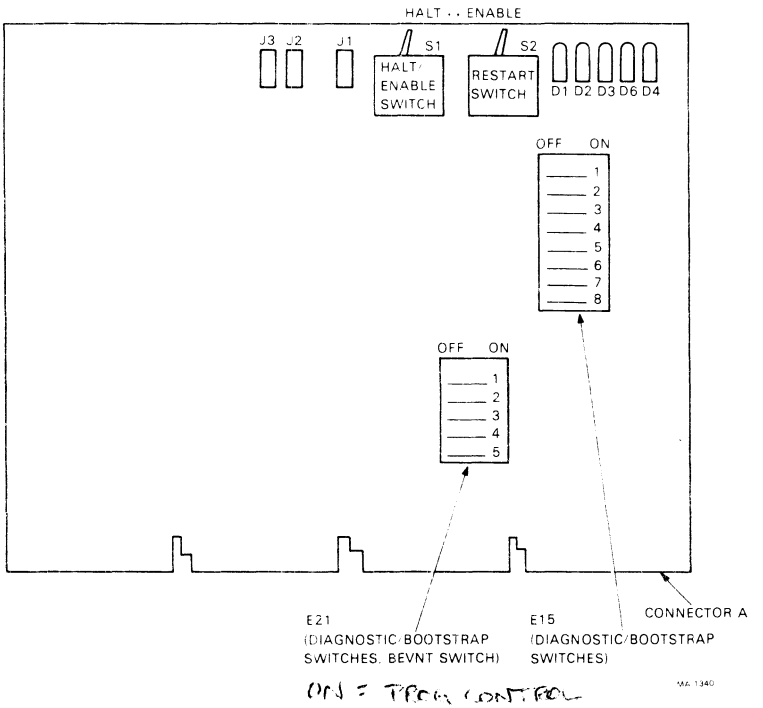


Figure 2 BDV11 Switches and Indicators

Diagnostic/Bootstrap Switches

Dip switch units E15 and E21 allow the user to select diagnostic programs and/or a bootstrap program. The switches are designated as A1–A8, representing switches 1–8 of E15, and B1–B4, representing switches 1–4 of E21. The programs selected by these switches are listed below. These 12 switches comprise the configuration register that can be read at address 177524.

Switches A1–A4 are defined as follows.

A1	ON	Execute CPU test upon power-up or restart.
A2	ON	Execute memory test upon power-up or restart.
A3	ON	DECnet boot – A4, 5, 6, and 7 are arguments.
A4	ON	Console test and dialog (A3 OFF).
A4	OFF	Turnkey boot dispatched by switch setting (A3 OFF).

DECnet boot arguments are:

Boot*	A4	A5	A6	A7
DUV11	ON	OFF	OFF	OFF
DLV11-E	OFF	ON	OFF	OFF
DLV11-F	OFF	ON	OFF	ON

All boots other than the above DECnet boots are controlled by the bit patterns in switches A5 through A8 and B1 (shown in Table 7) or, if the console test is selected, by mnemonic and unit number. The console test prompts with

```
xx
START?
```

where xx is the decimal multiple of 1024 words of RAM found in the system when sized from 0 up in 1024-word increments. The first word of each 1024-word segment is read and then written back into itself.

Allowed responses are a 2-character mnemonic with a 1-digit octal unit number or one of two special single character mnemonics. The response must be followed by a RETURN. The special single character mnemonics are:

Y	Use switch settings to determine boot device
N	Halt – enter microcode ODT

*DLV11-E CSR = 175610; DLV11-F CSR = 176500;DUV11 CSR = 160040 if no devices from 160010 to 160036.

Table 7 Diagnostic/Bootstrap Switch Selection

Mnemonic	A5	A6	A7	A8	B1	Program Selected[1]
	0	0	0	0	0	Unused
	0	0	0	0	1	Loop on test
DKn n < 8	0	0	0	1	0	RKV11 Boot
	0	0	0	1	1	Unused
DLn n < 4	0	0	1	0	0	RLV11 Boot
	0	0	1	0	1	Unused
	0	0	1	1	0	Unused
	0	0	1	1	1	Unused
DXn n < 2	0	1	0	0	0	RXV11 Boot
	0	1	0	0	1	Unused
	0	1	0	1	0	Unused
	0	1	0	1	1	Unused
DYn n < 2	0	1	1	0	0	RXV21 Boot
	0	1	1	0	1	Unused
	0	1	1	1	0	Unused
	0	1	1	1	1	Unused
	1	0	0	0	0	ROM Boot[2]
	1	0	0	0	1	Unused
	1	0	0	1	0	Unused
	1	0	0	1	1	Unused
	1	0	1	0	0	Unused
	1	0	1	0	1	Unused
	1	0	1	1	0	Unused
	1	0	1	1	1	Unused
	1	1	0	0	0	Unused
	1	1	0	0	1	Unused
	1	1	0	1	0	Unused
	1	1	0	1	1	Unused
	1	1	1	0	0	Unused
	1	1	1	0	1	Unused
	1	1	1	1	0	Unused
	1	1	1	1	1	Unused

NOTES

1. All unused patterns or mnemonics will default to ROM boot if switch B2, B3, or B4 is on.
2. The ROM boot uses switches B2, B3, and B4 to dispatch as follows:

B2	B3	B4	ROM
1	X	X	Extended diagnostic
0	1	X	2708
0	0	1	Program ROM

where X = don't care.

If an unrecognized mnemonic or switch setting (A5 through B1) is encountered, the presence of additional ROM is checked (by checking B2, 3, 4) and, if present, the ROM boot is invoked. The mnemonic's first character is placed in the high byte of location 2. Both characters are converted to upper-case with bit 7 cleared. Location 0 is loaded with the binary unit number. If an unrecognized switch setting is encountered instead, a copy of the switches is placed in location 2 with bit 15 set.

If no additional ROM exists, the switch checking routine will halt or the mnemonic routine will reprompt.

The above features allow the user to implement additional features or boots in additional ROMs without change to the base ROMs. If the additional ROM encounters an unrecognized mnemonic, it should load address 173000 into the PC, which will restart the BDV11 base ROM and reprompt.

Diagnostic Lights

When a failure occurs in a diagnostic test or in a bootstrap program, the diagnostic light display indicates the area of the failure as shown in Table 8. A failure causes the error to be indicated by the display and an error halt instruction is carried out by the processor. When entering the halt mode, the processor outputs the PC address at the time of the error on the console terminal. (The actual error address is one word less than the terminal printout.) In the halt mode, the processor responds to console ODT commands and the operator can troubleshoot the error. Table 9 lists the possible address and the cause of some errors.

BEVNT L Switch

Contact 5 of dip-socket switch E21 is the BEVNT L switch. When the switch is off (open), the LSI-11 bus BEVNT L signal can be controlled by the power supply-generated LTC signal. When the switch is on (closed), the LTC function is program-controlled, i.e., a single-bit, write-only register in the logic (address 177546, bit 6) clamps BEVNT L low when the register is cleared. (The register is automatically cleared when the power is turned on or when the RESTART switch is cycled.)

Power OK LED

This green LED is lighted when the +12 Vdc supply voltage is greater than +10 V and the +5 Vdc supply voltage is greater than +4 V for normal operating conditions. The +12 Vdc voltage and the +5 Vdc voltage can be measured at the tip jacks as indicated below. (Both J2 and J3 have a 560-ohm resistor in series to prevent damage from a short circuit; use at least a 20,000 ohm/V meter to measure the voltage.)

Jack	Color	Voltage
J1	Black	Ground
J2	Red	+5 Vdc
J3	Purple	+12 Vdc

HALT/ENABLE Switch

When this switch is in the ENABLE position, the processor can operate under program control. If the switch is placed in the HALT position, the processor enters the halt mode and responds to console ODT commands. While in the halt mode, the processor can execute single instructions, facilitating maintenance of the system. Program control is reestablished by returning the switch to the ENABLE position and entering a "P" command at the console terminal (providing the contents of register R7 were not changed). Refer to the appropriate processor handbook for a description of console ODT command usage.

Table 8 Diagnostic LED Error Display (D1–D4)*

D4 Bit 3	D3 Bit 2	D2 Bit 1	D1 Bit 0	Comments* (Type of Error)
On	On	On	On	System hung; halt switch on or power-up mode wrong.
Off	Off	Off	On	CPU, fault, or configuration error.
Off	Off	On	Off	Memory error; R1 points to bad location.
Off	Off	On	On	Console SLU will not transmit.
Off	On	Off	Off	Waiting for response from operator.
Off	On	Off	On	Load device fault.
Off	On	On	Off	Secondary boot incorrect (location 0 not a NOP).
Off	On	On	On	DECnet waiting for response from host.
On	Off	Off	Off	DECnet; received done flag set.
On	Off	Off	On	DECnet; message received.
On	Off	On	Off	ROM bootstrap error.

*The light combination indicates the corresponding test is in progress or failed. Some tests retry (DECnet) and others will halt the CPU (CPU, memory, non-DECnet boots).

Table 9 List of Error Halts

Address of Error	Cause of Error
173 022	Memory error 1. Write address into itself.
173 040	SLU switch selection incorrect. Error in switches.
173 046	SLU error. SCR address for selected device. Check CSR for selected device in floating CSR address area.
173 050	CP1 error. R0 contains address of error.
173 052	Memory error 2. Data test failed.
173 106	Memory error 3. Write and read bytes failed.
173 202	ROM loader error. Checksum on data block.
173 240	CP4 error. R0 contains address of error.
173 366	ROM loader error. Checksum on address block.
173 402	ROM loader error. Jump address is odd.
173 532	RL device error.
173 634	CPU error 3. R0 points to cause of error.
173 642	In console terminal test a "no" typed.
173 656	RK device error.
173 656	Switch mode halt. Match was not made with switches.
173 670	Console terminal test. No done flag.
173 706	CPU error 2. R0 points to cause of error.
173 712	RX device error.

RESTART Switch

When the RESTART switch is cycled, i.e., moved from one side to the other and back, the CPU automatically carries out a power-up sequence. Thus, the system can be rebooted at any time for maintenance purposes.

Addressing ROM on the BDV11 module

A block of 256 LSI-11 bus addresses is reserved to address the ROM locations on the BDV11 module. This block resides in the upper 4K address bank (28K–32K), which is normally used for peripheral-device addressing, and consists of byte addresses 173000–173776.

The BDV11 logic enables all 2048 locations in a selected 2K ROM (or 1024 locations in a 1K ROM) to be addressed by just these 256 bus addresses. The logic includes a page control register (PCR) at bus address 177520; the contents of this read/write register determine the specific ROM location that is accessed when 1 of the 256 bus addresses is placed on the BDAL lines. The PCR is loaded with "page" information, i.e., the PCR contents point to 1 of 16 (or 1 of 8) 128-word pages in the selected ROM (16 pages × 128 words = 2048 words). To illustrate, if the PCR contents represent pages 0 and 1, bus addresses 173000–173776 access ROM locations 0000–0377; if the PCR contents represent pages 10 and 11, bus addresses 173000–173776 access ROM locations 2000–2377. Table 10 relates bus addresses, PCR pages, and ROM locations.

At the top of each column of PCR pages in Table 10 appear two circuit component designations; column 1, for example, is headed by E53/E48. These designations represent the ROMs and EPROMs that one might find on a BDV11 module. For instance, the BDV11 is supplied with 2K words of diagnostic ROM. The ROM inserted in socket XE53 supplies the high byte (bits 8–15) of these 2K words, while the ROM inserted in socket XE48 supplies the low byte (bits 0–7). To access the BDV11 diagnostic ROM locations, the user must load the PCR with the pages in column 1; thus, when 12 and 13, for example, are loaded in the PCR, diagnostic ROM locations 2400–2777 can be addressed by the LSI-11 BDAL signals. Another variation of the BDV11 could have 1K-word EPROMs inserted in sockets XE57–XE40 (E57 supplies the high byte, while E40 supplies the low byte). To access these EPROM locations, the user would load the PCR with pages in column 3; thus, with 44 and 45 in the PCR, EPROM locations 1000–1377 are accessible.

Table 10 BDV11 Bus Addresses/PCR Pages

ROM Bus Address	PCR Pages E53/ E48	E58/ E44	E57/ E40	E52/ E36	E54/ E49	E59/ E45	E60/ E41	E55/ E37	E51/ E38	E47/ E42	E43/ E46	E39/ E50	Location Accessed
173000–173376	0	20	40	50	200	220	240	260	300	320	340	360	0000–0177
173400–173777	1	21	41	51	201	221	241	261	301	321	341	361	0200–0377
173000–173376	2	22	42	52	202	222	242	262	302	322	342	362	0400–0577
173400–173777	3	23	43	53	203	223	243	263	303	323	343	363	0600–0777
173000–173376	4	24	44	54	204	224	244	264	304	324	344	364	1000–1177
173400–173777	5	25	45	55	205	225	245	265	305	325	345	365	1200–1377
173000–173376	6	26	46	56	206	226	246	266	306	326	346	366	1400–1577
173400–173777	7	27	47	57	207	227	247	267	307	327	347	367	1600–1777
173000–173376	10	30			210	230	250	270	310	330	350	370	2000–2177
173400–173777	11	31			211	231	251	271	311	331	351	371	2200–2377
173000–173376	12	32			212	232	252	272	312	332	352	372	2400–2577
173400–173777	13	33			213	233	253	273	313	333	353	373	2600–2777
173000–173376	14	34			214	234	254	274	314	334	354	374	3000–3177
173400–173777	15	35			215	235	255	275	315	335	355	375	3200–3377
173000–173376	16	36			216	236	256	276	316	336	356	376	3400–3577
173400–173777	17	37			217	237	257	277	317	337	357	377	3600–3777

As Table 10 implies, the PCR pages are assigned to specific module ROM sockets. Furthermore, the sockets are assigned specific kinds of ROMs, as indicated in Table 11, e.g., the diagnostic/bootstrap ROM can occupy only sockets XE53 and XE48. Thus, a specific ROM can be addressed only when the PCR contains the page or pages assigned to the socket that the ROM occupies. To illustrate, if 2K ROMs are inserted in sockets E39 and E50, they can be addressed only when the PCR contains pages 360–377. The page/socket assignments indicated in Table 10 apply to the BDV11 module shipped by DIGITAL. There are eight locations on the BDV11 printed circuit board in which jumpers are inserted selectively to achieve these assignments. It is possible to change the factory arrangement of these jumpers; by doing so, the user can cause the CPU to execute instructions directly from a ROM or EPROM of the user's choice when power is turned on, rather than from the diagnostic ROMs.

Table 11 Functions of ROM Sockets

Sockets	ROM Function	Sockets	ROM Function
XE53/XE48	2K Diagnostic/Bootstrap	XE47/XE42	2K System ROM
XE58/XE44	2K Diagnotic/Bootstrap (reserved for DIGITAL)	XE51/XE38	2K System ROM
XE57/XE40	1K EPROM	XE55/XE37	2K System ROM
XE52/XE36	1K EPROM	XE60/XE41	2K System ROM
XE39/XE50	2K System ROM	XE59/XE45	2K System ROM
XE43/XE46	2K System ROM	XE54/XE49	2K System ROM

Loading ROM into RAM

A utility is provided in the BDV11 firmware which will load user programs from ROM to RAM at specified (and possibly scattered) addresses and transfer control to a specified address. This feature allows a programmer to write a program (to be stored in ROM) without knowledge of the BDV11 mapping hardware or the necessity to "ROMize" the program. This utility will load either the DIGITAL-reserved space, the 2K EPROM, or the 16K ROM/EPROM areas. This utility uses the four highest words of RAM (<30K) as scratch space.

The format used is a modified version of absolute loader paper tape format. The standard format consists of sequential data blocks, byte organized, as follows:

1 BYTE	This indicates start of block.
0 BYTE	Required
BCL	Low-order eight bits of byte count.
BCH	High-order eight bits of byte count.
ADL	Low-order eight bits of load address.
ADH	High-order eight bits of load address.
DATA	Sequential bytes of data.
CKB	Checksum byte.

These frames are repeated as required until a starting address block is encountered. This is indicated by a byte count of six, which is too short to allow a data field. The load address of this block is used as the starting address.

The format skips every 255th and 256th location in the ROM pattern. These locations are filled with checking information which allows DIGITAL diagnostics to determine that the ROMs are good and inserted in the correct socket.

An RT11 FORTRAN program follows which will generate ROM patterns from RT11 LDA files of paper tape programs. This program generates a data base only since blasting hardware is very installation specific. It should be noted that the RT11 linker generates relatively short data blocks and that this leads to significant waste due to the overhead in each block. A user may customize the pattern generation program or linker to reduce this problem.

The ROMs should be inserted as indicated in the ROM address chart. The user program may be patched by changing only the last ROM of a set and by adding a new data block(s) before the starting address block. This block will overlay previously loaded data.

```
FORTRAN IV      V02.04

0001            PROGRAM     RPAT2
      C         THIS PROGRAM CONVERTS ABSOLUTE LOADER IMAGE FILES (.LDA)
      C         INTO THE REQUIRED NUMBER OF SEQUENTIAL ROM PATTERNS
      C         FOR USE WITH THE BDV11-AA'S ROM LOADER.
      C
      C         TO USE THIS PROGRAM CREATE A .LDA FILE EITHER WITH THE
      C         RT11 LINKER OR PIP FROM A PAPER TAPE.
      C         LIST THE DIRECTORY TO GET THE NUMBER OF BLOCKS IN THE
      C         INPUT FILE THEN RUN THIS PROGRAM.
      C
      C         THIS PROGRAM WILL REQUEST THE NAME OF THE INPUT FILE
      C         AND ITS LENGTH. THEN IT WILL REQUEST  A SERIES OF
      C         OUTPUT FILE NAMES, ONE FOR EACH ROM REQUIRED.
      C
      C         THE PROGRAM PROCESSES THE INPUT FILE ONE BYTE AT A TIME
      C         RECORDING THE BYTES IN THE OUTPUT FILE. EVERY 255 TH
      C         BYTE OF THE OUTPUT FILE IS SET >0 AND EVERY 256 TH BYTE
      C         CONTAINS A CHECKSUM OF THE PREVIOUS 255 LOCATIONS.
      C         NO INPUT BYTES ARE RECORDED IN THE 255 TH OR 256 TH BYTE.
      C         THESE LOCATIONS ARE USED BY DEC SUPPLIED DIAGNOSTICS
      C         AND ARE SKIPPED BY THE BDV11'S ROM LOADER.
      C
      C         THE OUTPUT OF THIS PROGRAM CONSISTS OF ONE SEQUENTIAL
      C         FORMATTED FILE PER ROM PATTERN, EACH FILE CONSISTS OF
      C         SEQUENTIAL BYTES OF THE ROM WRITTEN IN O6 FORMAT, ONE
      C         BYTE PER RECORD (LINE).
      C
0002            COMMON /DAT/IB,IEND,ILONG,INBLK,IBLK,IA(256),IBN,IL,
     C       ISUM,IROM(2048),IRN,KMARK,I255
0003            LOGICAL*1 L(2),LA(512)
0004            EQUIVALENCE (L(1),IL),(LA(1),IA(1))
0005            DATA KMARK/'52525/
0006            IRN=0       ! INDEX VARIABLE FOR ROM ARRAY
0007            I255=0      ! MOD 256 COUNTER
0008            ISUM=0      ! CHECKSUM OF ROM BYTES
0009            IBN=525     ! CURRENT BYTE IN INPUT (INITIALIZED TO >512)
      C                 TO FORCE READING OF THE FIRST INPUT BLOCK
0010            INBLK=0         ! NUMBER OF BLOCKS IN INPUT FILE
0011            ILONG=0     ! LENGTH OF ROM
0012            IEND=0      ! FLAG THAT INDICATES LAST FRAME BEING PROCESSED
0013            IBLK=0      ! INDEX VARIABLE, CURRENT BLOCK OF INPUT FILE
0014            IB=0            ! THE CURRENT BYTE BEING PROCESSED
      C         IROM(2048) IS AN ARRAY USED TO STORE THE ROM IMAGE
      C         LA(512) IS A LOGICAL*1 ARRAY HOLDING IMAGE OF INPUT FILE BLOCK
      C         LA(512) EQUIVALENCED TO IA(256) FOR I/O
      C         L(1) AND IL EQUIVALENCED FOR WORD/BYTE CONVERSIONS
      C
0015            WRITE(5,5)
0016      5     FORMAT(1H ,'PROGRAM RPAT2 VERSION 2.1 RT11')
0017            WRITE(5,10)
0018      10    FORMAT(1H ,'ENTER LENGTH OF ROM ',$)
0019            READ(5,15)ILONG
0020      15    FORMAT(I5)
0021            WRITE(5,20)
```

```
0022  20    FORMAT(1H ,'ENTER INPUT FILE SPEC ',$)
0023        CALL ASSIGN(11,'DUM',-1,'OLD','NC',1)
0024        WRITE(5,25)
0025  25    FORMAT(1H ,'ENTER LENGTH OF FILE IN BLOCKS ',$)
0026        READ(5,15)INBLK
0027        DEFINE FILE 11(INBLK,256,U,IWHERE)
      C
      C     START PATTERN PROCESSING
      C     GET THE FIRST BYTE OF THE ABS LOADER FRAME
      C
0028  100   CALL NEXTB
      C     IF IT ISN'T A 1 WE HAVEN'T FOUND THE BEGINNING YET
0029        IF(IB.NE.1)GO TO 100
0031        CALL OUTB
0032        CALL NEXTB
0033        IF(IB.NE.0)STOP 'INPUT FORMAT ERROR'
0035        CALL OUTB
      C     GET THE BYTE COUNT AND MAKE INTO A INTEGER
0036        CALL NEXTB
0037        L(1)=IB
0038        CALL OUTB
0039        CALL NEXTB
0040        CALL OUTB
0041        L(2)=IB
0042        INUM=IL
      C     IF THE LENGTH IS 6, THIS IS A STARTING ADDRESS BLOCK
      C     WHICH IS THE LAST ONE TO PROCESS
0043        IF(INUM.EQ.6)IEND=1
      C     COMPUTE THE NUMBER OF BYTES LEFT IN THIS FRAME
      C    = NUMBER OF BYTES IN FRAME - THE NUMBER ALREADY PROCESSED(4)
      C     PLUS THE CHECK BYTE, THEN PROCESS THE REMAINING BYTES OF THE
      C     FRAME.
0045        INUM=INUM-3
0046        DO 120 J=1,INUM
0047        CALL NEXTB
0048        CALL OUTB
0049  120   CONTINUE
      C     IF IT WASN'T THE LAST FRAME DO THE NEXT ONE
0050        IF(IEND.EQ.0)GO TO 100
      C     IEND=2 TELLS THE OUTPUT ROUTINE TO FINISH UP
0052        IEND=2
      C     SET BYTE TO ZERO AND OUTPUT TO END OF ROM
      C     THE OUTPUT ROUTINE WILL TERMINATE THE PROGRAM
0053  200   IB=0
0054        CALL OUTB
0055        GO TO 200
0056  1000  STOP
0057        END
```

```
FORTRAN IV      V02.04

0001        SUBROUTINE NEXTB
      C     THIS ROUTINE GETS SEQUENTIAL BYTES FROM THE INPUT FILE
0002        COMMON /DAT/IB,IEND,ILONG,INBLK,IBLK,IA(256),IBN,IL,
           C    ISUM,IROM(2048),IRN,KMARK,I255
0003        LOGICAL*1 L(2),LA(512)
0004        EQUIVALENCE (L(1),IL),(LA(1),IA(1))
      C     IF IBN IS 512 OR GREATER READ A NEW BLOCK
0005        IF(IBN.LT.512)GO TO 200
0007  100   IBLK=IBLK+1
0008        IF(IBLK.GT.INBLK)STOP 'NUMBER OF BLOCKS EXCEEDED'
0010        READ(11'IBLK)IA
0011        IBN=0
0012  200   IBN=IBN+1
0013        IB=LA(IBN).AND.255
0014        RETURN
0015        END
```

Executing ROMs in the I/O Page

ROMs may be executed in the I/O page provided their starting address is between 173016 and 173376. The next page lists a program which executes in the I/O page. It uses the ROM loader but only supplies a starting address block. It must start in the window between 173000 and 173376 since the ROM boot is executing out of the other window. It is the programmer's responsibility to properly map the upper window and then manage all remapping.

A RT11 FORTRAN program follows (RPAT1B) which will convert save image (SAV) files linked at 173000 and generate correct ROM patterns. This program inserts checking information every 255th and 256th ROM location as did the previous program.

One assembly is required for every 256 words of ROM and they must be input in order of ascending page number (two 128-word pages at a time).

```
FORTRAN IV      V02.04

0001            SUBROUTINE OUTB
      C         THIS ROUTINE WRITES SEQUENTIAL BYTES TO THE OUTPUT FILE
      C         AND ADDS CHECKING INFORMATION EVERY 255'TH AND 256'TH
      C         LOCATION. THIS INFORMATION IS SKIPPED BY THE BDV11-AA
      C         ROM LOADER BUT USED BY DEC SUPPLIED DIAGNOSTICS TO INSURE
      C         THAT THE ROMS ARE GOOD AND IN THE CORRECT SOCKETS.
0002            COMMON /DAT/IB,IEND,ILONG,INBLK,IBLK,IA(256),IBN,IL,
     C             ISUM,IROM(2048),IRN,KMARK,I255
0003            LOGICAL*1 L(2),LA(512)
0004            EQUIVALENCE (L(1),IL),(LA(1),IA(1))
0005  10        IRN=IRN+1
0006            IB=IB.AND.255
0007            I255=I255+1
      C         IF THIS IS THE 255 TH ADD 2 CHECK BYTES
0008            IF(I255.NE.255)GO TO 150
      C         SET NON ZERO NON -1 IN 255'TH BYTE AND RESET MOD 256 COUNTER
0010            IROM(IRN)=KMARK.AND.255
0011            I255=0
0012            ISUM=(ISUM+KMARK).AND.255
0013            IRN=IRN+1
      C         CALCULATE CHECKSUM FOR BDV11 DIAGNOSTIC
0014            ISUM=(-ISUM.AND.255)
0015            IROM(IRN)=ISUM
0016            ISUM=0
      C         IF THIS IS THE END OF A ROM WRITE PATTERN TO OUTPUT FILE
0017            IF(IRN.EQ.ILONG)GO TO 200
      C         IF WE JUST ADDED CHECK INFO OUTPUT THE CURRENT BYTE
0019            GO TO 10
      C         PUT BYTE IN ARRAY AND ADD TO ISUM
0020  150       IROM(IRN)=IB
0021            ISUM=(ISUM+IB).AND.255
0022            RETURN
0023  200       WRITE(5,201)
0024  201       FORMAT(1H ,'ENTER OUTPUT FILE SPECIFICATION ',$)
0025            CALL ASSIGN(12,'DUM',-1,'NEW','CC',1)
0026            WRITE(12,220)(IROM(J),J=1,ILONG)
0027  220       FORMAT(1H ,O6)
0028            CALL CLOSE(12)
      C         RESET ROM IRN AND IF END OF INPUT STOP PROGRAM
0029            IRN=0
0030            IF(IEND.EQ.2)STOP
      C         OUTPUT THE CURRENT BYTE
0032            GO TO 10
0033            END
```

```
0030          CALL CLOSE(10)
0031          IFILE=IFILE+1
0032          IF(IFILE.NE.INUM)GO TO 100
      C
      C       THE FOLLOWING LOOP SETS EVERY 255 TH LOCATION >0
      C       AND INSERTS BYTE CHECKSUMS IN EVERY 256 TH LOCATION
      C
0034          DO 125 J=1,8
0035          ISUM1=0
0036          ISUM2=0
0037          DO 125,JJ=1,256
0038          J1=(256*J)+JJ-256
0039          IF(JJ.EQ.255)I(J1)=KMARK
0041          IL=I(J1)
0042          IF(JJ.EQ.256)GO TO 122
0044          ISUM1=(ISUM1+L(1)).AND.255
0045          ISUM2=(ISUM2+L(2)).AND.255
0046          GO TO 125
0047    122   ISUM1=(-ISUM1).AND.255
0048          L(1)=ISUM1
0049          ISUM2=(-ISUM2).AND.255
0050          L(2)=ISUM2
0051          I(J1)=IL
0052    125   CONTINUE
0053    128   IBYTE=IBYTE+1
0054          IF(IBYTE.EQ.2)GO TO 14D5
0056          WRITE(7,130)
0057    130   FORMAT(1H ,'ENTER LOW BYTE OUTPUT SPECIFICATION ',$)
0058          GO TO 140
0059    135   WRITE(7,136)
0060    136   FORMAT(1H ,'ENTER HIGH BYTE OUTPUT SPECIFICATION ',$)
0061    140   CALL ASSIGN(11,'DUM',-1,'NEW','CC',1)
0062          DO 150 J=1,ILONG
0063          IL=I(J)
0064          IOUTB=L(IBYTE)
0065          IOUTB=IOUTB.AND.255
0066          WRITE(11,141)IOUTB
0067    141   FORMAT(1H ,O6)
0068    150   CONTINUE
0069          CALL CLOSE(11)
0070          IF(IBYTE.LT.2)GO TO 128
0072          END
```

```
FORTRAN IV      V02.04

0001          PROGRAM RPAT1B
      C       THIS PROGRAM ACCEPTS SAVE IMAGE FILES AND GENERATES
      C       ROM PATTERNS SUITED FOR EXECUTION
      C       ON A BDV11-AA.
      C
      C       THIS PROGRAM USES ONLY THE 124 TH BLOCK OF THE INPUT FILE
      C       WHICH CONTAINS ADDRESSES 173000 TO 173776
      C
      C       THE PROGRAM USES A DIRECT IMAGE OF THE CODE BETWEEN 173000
      C       AND 173776 AND INSERTS CHECKING INFO IN EVERY 255 TH AND 256 TH
      C       LOCATION OF THE ROM PATTERN OVER-WRITING LOCATIONS 173774
      C       AND 173776
      C
      C       EACH PAIR OF 2K X 8 ROMS CAN HOLD 8 ASSEMBLIES EACH LINKED
      C       AT 173000 AND NOT MORE THAN 256 WORDS LONG. THE FILE NAMES
      C       OF THE LINKED ASSEMBLIES MUST BE INPUTTED SEQUENTIALLY
      C       BY PAGE NUMBER. (EG. FIRST PAGE 200/201 THEN 202/203 ECT.)
      C       RERUN THE PROGRAM FOR EACH GROUP OF 8 ASSEMBLIES.
      C
      C       THE PROGRAM WILL OUTPUT 2 FORMATTED SEQUENTIAL FILES, ONE
      C       FOR THE LOW BYTE ROM, THEN ONE FOR THE HIGH BYTE ROM . EACH
      C       OUTPUT FILE CONSISTS OF SEQUENTIAL BYTES OF EITHER THE LOW
      C       OR BYTE ROM OR HIGH BYTE ROM. THE BYTES ARE WRITTEN IN O6
      C       FORMAT WITH ONE BYTE PER RECORD (LINE).
      C
```

```
0002          COMMON /ROMDAT/I(2048),ID(256)
0003          DATA KMARK/'52525/
0004          LOGICAL*1 L(2)
      C       L AND IL ARE USED TO PICK OFF BYTES OF INTEGERS
0005          EQUIVALENCE (L(1),IL)
0006          WRITE(7,1)
0007    1     FORMAT(1H ,'PROGRAM RT11 RPAT1 VERSION 3.0')
0008          IBYTE=0                 !FLAG SET TO INDICATE LOW BYTE, THEN HIGH
0009          IFILE=0                 !FLAG SET TO INDICATE FIRST OF INUM FILES
0010          INUM=0                  !ZERO THE NUMBER OF INPUT FILES
0011          DO 5 J=1,2048
0012          I(J)=0
0013    5     CONTINUE
0014          WRITE(7,10)
0015   10     FORMAT(1H ,'ENTER LENGTH OF ROM ',$)
0016          READ(5,11)ILONG
0017   11     FORMAT(I6)
0018          WRITE(7,16)
0019   16     FORMAT(1H ,'ENTER NUMBER OF INPUT FILES ',$)
0020          READ(5,11)INUM
0021   100    WRITE(7,101)
0022   101    FORMAT(1H ,'ENTER INPUT FILE SPECIFICATION ',$)
0023          CALL ASSIGN(10,'DUM',-1,'OLD','CC',1)
0024          DEFINE FILE 10(124,256,U,IV)
0025          READ(10'124)ID
0026          DO 120 J=1,256
0027          J1=J+(256*IFILE)
0028          I(J1)=ID(J)
0029   120    CONTINUE
```

FUNCTIONAL DESCRIPTION

General

The functions of the BDV11 are shown in Figure 3. The transceiver and control functions control the transfer of data between the bus and the BDV11. The ROM address function decodes the address data from the bus and uses the socket selection and ROM address functions to access the memory located on the BDV11. The ROM address function is also used to transfer data into the data selection function. Then data is placed on the LSI-11 bus by the control and transceiver functions. The data for the read/write registers is also transferred in and out by using the transceiver and control functions. The BDV11 uses power-up, BVENT, and display functions for monitoring program operations.

Transceiver

The transceiver logic monitors the LSI-11 bus BDAL lines for the address of a BDV11 register or the address of a ROM location. When a register or a ROM has been addressed, the transceiver logic gates the address onto the BDV11 DAL lines. If a register was addressed, the transceiver logic generates the address match signal that activates the control logic. If a ROM address was generated, then the DAL lines transfer the address to the ROM address selection logic. The transceiver logic is also used to transfer data from the DAL lines to the LSI-11 bus BDAL lines. This data can be from either a register or ROM address when the transceiver receives XMIT H. For the detailed operation of the transceiver logic (DC005 bidirectional buffer), refer to Chapter 5.

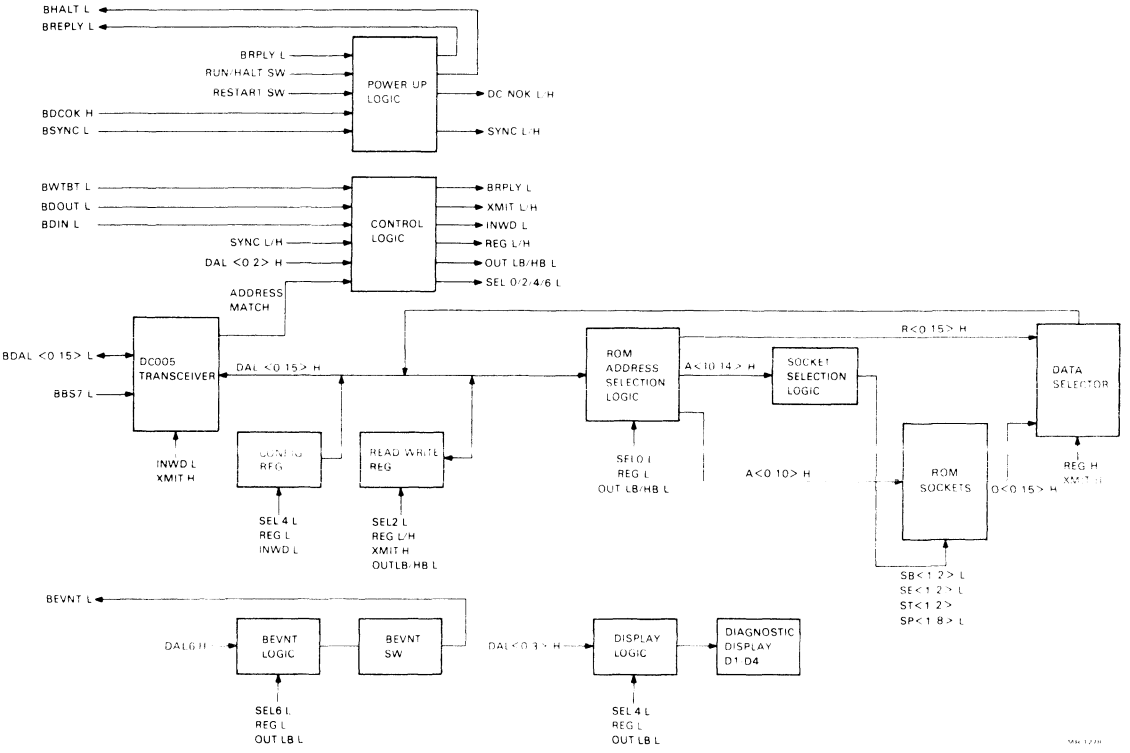


Figure 3 BDV11 Block Diagram

Control

The control logic consists of a DC004 protocol chip (Chapter 5) and an 82523 PROM. The control logic is enabled by the address match signal from the transceiver logic. The PROM monitors some of the DAL lines and the address match signal and generates an enable signal for the DC004 chip whenever any of the assigned bus addresses (173000 to 173777) is placed on the BDAL lines. The DC004 chip generates all the protocol signals used with the LSI-11 bus to permit data transfers. The control logic also generates the control signals for the read/write register's ROM address selection and the ROM socket selection logic. The bus control signals are defined in the appropriate processor handbook.

Read/Write Registers

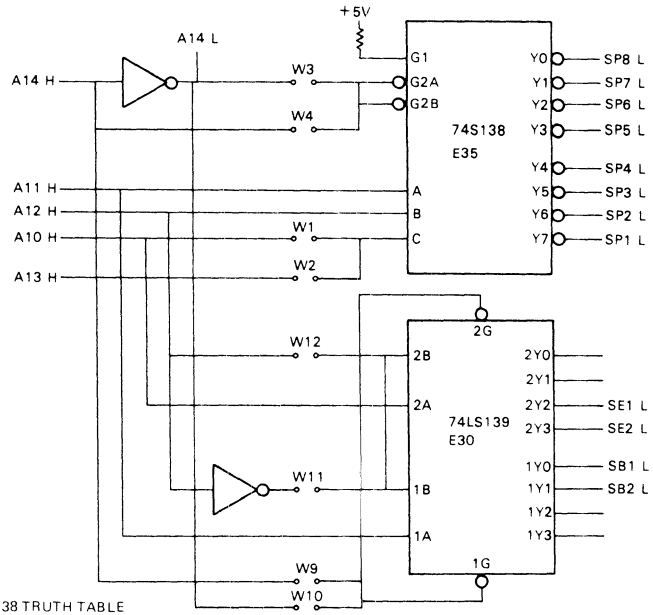
The read/write register logic consists of two 8-bit universal shift registers. When the registers are being read, the control logic asserts XMIT H and the information on the DAL lines is the data within the shift registers. When the registers are to be written into, the XMIT signal is negated and the registers are placed into a load condition. The registers are clocked and the information on the DAL lines is loaded into the registers as data. The registers are cleared when power is turned on or when the system is booted.

ROM Address Selection

The ROM address selection logic uses the contents of the PCK register and the LSI-11 bus address to determine the address of the BDV11 ROM locations. Each ROM has 2048_{10} addresses available. The logic selects the high byte of the PCR register if bit 8 of the LSI-11 bus is a one and selects the low byte when bit 8 is a zero. The selected byte is shifted to the right one bit and used as the high byte of the BDV11 address. The low byte of the LSI-11 bus address is shifted one bit to the right and used as the low byte of the BDV11 address. The complete BDV11 ROM address is formatted by using the combination of the high and low bytes generated. Table 10 is a listing of how the PCR contents and the LSI-11 bus addresses are used to generate ROM addresses.

Socket Selection

The socket (or ROM) selection logic (Figure 4) consists of two decoders (E30 and E35) that provide the outputs used to select the high byte and low byte sockets. The A10 H to A14 H inputs to these decoders are programmable by the user selecting jumper wires W1–W4 and W9–W12 to determine the configuration designation described in Table 2. The SB1 L and SB2 L outputs are used to select the 4K of diagnostic/bootstrap DIGITAL programs. The SE1 L and SE2 L outputs are used to select the 2K of user PROM. The SP1 L to SP8 L outputs are used to select the additional 16K of user ROM.



74S138 TRUTH TABLE

G1	G2	C	B	A	OUT LOW
H	L	L	L	L	Y0 (SP8 L)
		L	L	H	Y1 (SP7 L)
		L	H	L	Y2 (SP6 L)
		L	H	H	Y3 (SP5 L)
		H	L	L	Y4 (SP4 L)
		H	L	H	Y5 (SP3 L)
		H	H	L	Y6 (SP2 L)
		H	H	H	Y7 (SP1 L)

74LS139 TRUTH TABLE (EACH HALF)

G	B	A	OUT LOW
L	L	L	Y0(SB1 L)
	L	H	Y1 (SB2 L)
	H	L	Y2 (SE1 L)
	H	H	Y3 (SE2 L)

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Figure 4 Socket Selection Logic

ROM Address

The ROM address logic uses the socket select logic outputs and address lines A0 to A10 to select the desired address. The diagnostic/bootstrap ROMs are enabled by SB1 L and SB2 L and are addressed by A0 to A10. The user EPROMs are enabled by SE1 L and SE2 L and are addressed by A0 to A9. The user ROM sockets are enabled by SP1 L to SP8 L and addressed by A0 to A9. The output data from the ROMs is sent to the data selector logic.

Data Selector

The data selector receives data from the ROMs and the registers of the BDV11. This data is stored until the outputs are enabled by XMIT. The data is then gated to the DAL0–15 bus lines where it is transferred to the LSI-11 bus by the transceiver and control logic.

Display

The display logic consists of four flip-flops and four LEDs. The contents of the display register (address 177524) are gated into the flip-flops and the outputs illuminate the display LED indicators. The display is used to indicate to the user the type of program error when a failure occurs.

Power-Up

The power-up logic includes the ENABLE/HALT switch and the RESTART switch. In normal operation, the ENABLE/HALT switch is in the ENABLE position. When the switch is placed in the HALT position, the bus signal BHALT L is asserted. The processor enters the halt mode and responds to the console ODT commands. To resume processor operation, the user must set the switch to ENABLE and enter a "P" command from the console.

The RESTART switch must be cycled to reboot the system. When the switch is cycled, a capacitor is charged to disable the bus BDCOK H signal and the DCNOK L is asserted in order to initialize the BDV11 registers. When the capacitor discharges, the BDCOK H signal is enabled, the processor carries out a power-up sequence, and normal operation is resumed.

BVENT

The BVENT logic uses a switch located in E21 that allows the user to control the LTC function. When the switch is open, the bus BVENT L signal can be controlled by the LTC signal that is generated in the LSI-11 bus power supply. When the switch is closed, the BVENT L signal can be controlled by the program.

DIFFERENCES BETWEEN REVISIONS 0 AND A

1. The following part numbers distinguish revision 0 from A.

Socket	Rev 0	Rev A
E48	23-010E2	23-045E2
E53	23-011E2	23-046E2

2. Revision 0 does not support auto-loading of more than 3K words of ROM.

3. Revision 0 does not support DECnet bootstrap for the DLV11-F and does not have the RXV21 boot.

4. Revision 0 will test only 28K and print "??" for size if console test is enabled.

5. Revision 0 will only accept "Y" or "N" for mnemonics and unit numbers.

6. Revision 0 does not default to ROM boot when it encounters an unrecognized switch pattern.

7. Revision 0 uses switches B1, B2, and B3 for the ROM boot and is enabled by having switch B4 "ON." Revision A uses switches B2, B3, and B4 only.

DLV11 SERIAL LINE UNIT

GENERAL

The DLV11 serial line unit (SLU) interfaces asynchronous serial line I/O devices with a 20 mA current loop or EIA interface to the LSI-11 bus.

FEATURES

- Either an optically isolated 20 mA current loop or an EIA interface selected by using the appropriate interface cable option
- Selectable crystal-controlled baud rates: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, and an externally supplied rate
- Jumper-selectable stop bit and data bit formats
- LSI-11 bus interface and control logic for interrupt processing and vector generation
- Control/status register (CSR) and data registers compatible with PDP-11 software routines. CSRs and data buffer registers directly accessed via processor instructions.

SPECIFICATIONS

Identification	M7940
Size	Double
Power	+5.0 Vdc ± 5% at 1.0 A (1.6 A max) +12.0 Vdc ± 3% at 0.18 A (0.25 A max)
Bus Loads	
AC	2.5
DC	1.0

CONFIGURATION

General

The following paragraphs describe how the user can configure the module so that it will function within his system. The user can select the register address, parity, number of data bits, number of stop bits, baud rate, and type of serial interface. The descriptions of the registers and their standard factory addresses are listed in Table 1. Available jumpers are shown in Figure 1 and their applications are listed in Table 2.

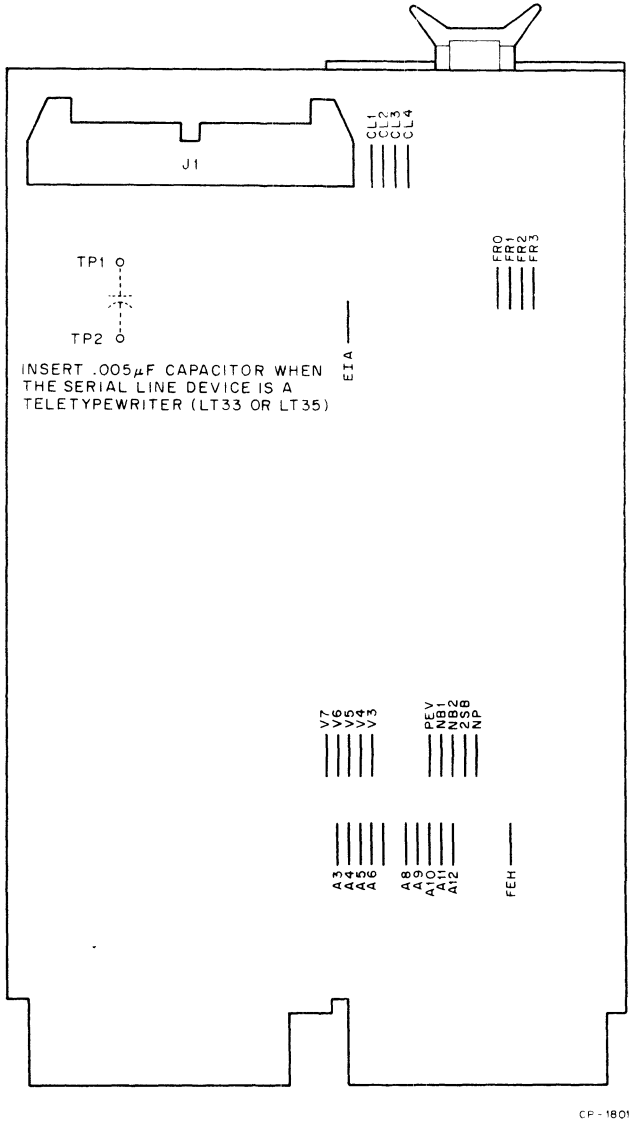

Figure 1 DLV11 Jumper Locations

Table 1 Standard Addresses

Register	Mnemonic	First Module	Second Module
Receiver control status	RCSR	177560	175610
Receiver data buffer	RBUF	177562	175612
Transmit control/status	XCSR	177564	175614
Transmit data buffer	XBUF	177566	175616
Standard vectors	KCSR	060	330
	XCSR	064	304

Table 2 DLV11 SLU Factory Jumper Configuration

Jumper Designation	Jumper State*	Function Implemented
A3	I	This arrangement of jumpers A3 through A12
A4	R	implements the octal device address 17756X,
A5	R	which is the assigned address for the console
A6	R	device SLU. The least significant digit is hard-
A7	I	wired on the module to address the four SLU
A8	R	device registers as follows:
A9	R	X=0, RCSR address
A11	R	X=2, Receive data register address
A10	R	X=4, XCSR address
A12	R	X=6, Transmit data register address
V3	I	This jumper arrangement implements the inter-
V4	R	rupt vector: 60 for received data and 64 for
V5	R	transmitted data.
V6	I	
V7	I	
NP	R	No parity
2SB	R	Two stop bits
NB2	R	Eight data bits
NB1	R	
PEV	R	Even parity if NP installed
FEH	I	Halt on framing error
EIA	I	12 V EIA operation enabled

*R = removed, I = installed

Table 2 DLV11 SLU Factory Jumper Configuration (Cont)

Jumper Designation	Jumper State*	Function Implemented
FR0	R	
FR1	R	110 baud rate selected
FR2	R	
FR3	R	
CL1	I	20 mA current loop active receiver and transmitter selected
CL2	I	Jumpered with 180 ohm resistors
CL3	I	
CL4	I	

*R = removed, I = installed

Addresses

Addresses for the DLV11 can range from 160000 through $17777X_8$. The least significant three bits (only bits 1 and 2 are used; bit 0 is ignored) address the desired register in the DLV11, as described in Table 1.

Address bits 3 through 12 are jumper-selected as shown in Figure 2.

Since each DLV11 module has four registers, each requires four addresses. Addresses 177560–177566 are reserved for the DLV11 used with the console peripheral device. Additional DLV11 modules should be assigned addresses from 175610 through 176176, allowing up to 30 additional DLV11 modules to be addressed.

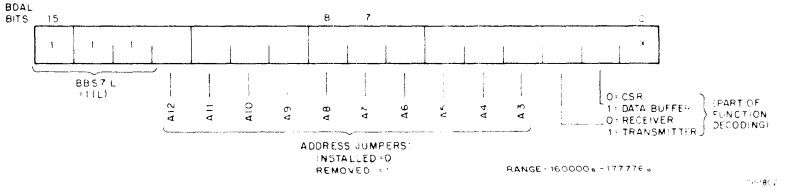

Figure 2 CSR Address Selection

Word Format

The word format for the RCSR register is detailed in Figure 3 and the functions are described in Table 3.

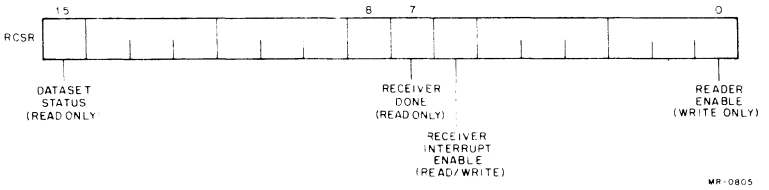

Figure 3 RCSR Word Format

Table 3 RCSR Word Format

Bit	Function
15	Dataset Status – Set when CARRIER or CLEAR TO SEND and DATA SET READY signals are asserted by an EIA device. Read-only bit.
14–8	Not used. Read as 0.
7	Receiver Done – Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF is addressed or when the BDCOK H signal goes false (low). A receiver interrupt is enabled by the DLV11 when this bit is set and receiver interrupt is enabled (bit 6 is also set). Read-only bit.
6	Interrupt Enable – Set under program control when it is desired to generate a receiver interrupt request when a character is ready for input to the processor (bit 7 is set). Cleared under program control or by the BINIT signal. Read/write bit.
5–1	Not used. Read as 0.
0	Reader Enable – Set by program control to advance the paper tape reader on a teletypewriter device to input a new character. Automatically cleared by the new character's start bit. Write-only bit.

The receiver data buffer register (RBUF) word format is shown in Figure 4 and described in Table 4.

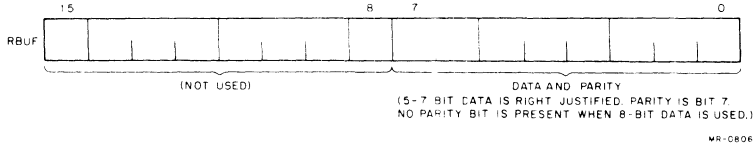

Figure 4 Receiver Data Buffer (RBUF)

Table 4 RBUF Word Format

Bit	Function
15–8	Not used. Read as 0.
7–0	Contains five to eight data bits in a right-justified format. MSB is the optional parity bit. Read-only bits.

The transmit control/status register (XCSR) word format is shown in Figure 5 and described in Table 5.

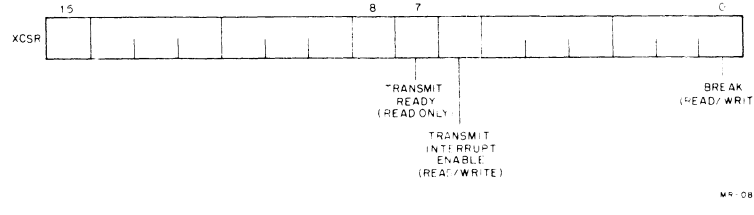

Figure 5 Transmit Control Status (XCSR)

Table 5 XCSR Word Format

Bit	Function
15–8	Not used. Read as 0.
7	Transmit Ready – Set when XBUF is empty and can accept another character for transmission. It is also set during the power-up sequence by the BDCOK H signal. Automatically cleared when XBUF is loaded. When transmitter interrupt is enabled (bit 6 also set), an interrupt request is asserted by the DLV11 when this bit is set. Read-only bit.
6	Interrupt Enable – Set under program control when it is desired to generate a transmitter interrupt request when the DLV11 is ready to accept a character for transmission. Reset under program control or by the BINIT signal. Read/write bit.
5–1	Not used. Read as 0.
0	Break – Set or reset under program control. When set, a continuous space level is transmitted. BINIT resets this bit. Read/write bit.

The transmit data buffer register (XBUF) word format is shown in Figure 6 and described in Table 6.

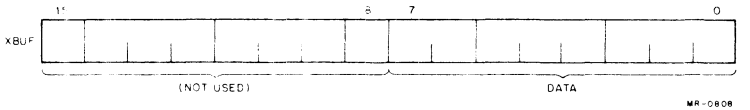

Figure 6 Transmitter Data Buffer (XBUF)

Table 6 XBUF Word Format

Bit	Function
15–8	Not used.
7–0	Contains five to eight right-justified data bits. Loaded under program control for serial transmission to a device. Write-only bits.

Interrupt Vectors

Vectors can range from 0 through $37X_8$. Vectors 60 and 64 are reserved for the console peripheral device. Additional DLV11 modules should be assigned vectors following any DRV11 modules installed in the system starting at 300. Vector bits 3 through 7 are selectable by the user to form the address as described in Figure 7. The factory configuration will set the receiver interrupt vector for 060 and the transmitter interrupt vector will be set at 064.

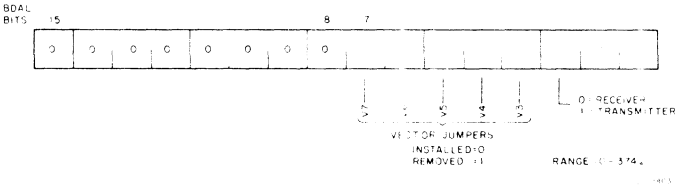

Figure 7 Interrupt Vector

UART Operation

The UART operation is programmed by using jumpers NP, 2SB, NB1, NB2, and PEV as shown below.

Number of Data Bits

	NB1	NB2
5	Installed	Installed
6	Removed	Installed
7	Installed	Removed
8	Removed	Removed

Number of Stop Bits Transmitted

2SB installed = One stop bit
2SB removed = Two stop bits

Parity Transmitted

NP removed = No parity bit
NP and PEV installed = Odd parity
NP installed and PEV removed = Even parity

Baud Rate Selection

Baud rate is programmed via jumpers FR0 through FR3 as shown in Table 7.

Table 7 Baud Rate Selection

Baud Rate	FR3	FR2	FR1	FR0
50	I	I	R	I
75	I	I	R	R
110	R	R	R	R
134.5	I	R	I	I
150	R	R	R	I
200	I	R	I	R
300	R	R	I	R
600	I	R	R	I
1200	R	I	R	R
1800	R	I	R	I
2400	I	R	R	R
2400	R	R	I	I
4800	R	I	I	R
9600	R	I	I	I
External (via pin BH1)	I	I	I	X

NOTE:
I = installed
R = removed
X = don't care

EIA Interface

EIA drivers are enabled when jumper EIA is installed. This jumper applies −12 V to the EIA driver chip. It should be removed during 20 mA current loop operation.

20 mA Current Loop Interface

Jumpers CL1 through CL4 are associated with 20 mA current loop interface operation. Remove EIA and remove or install CL1 and CL4 jumpers and CL2 and CL3 180 ohm resistors for the desired function as described below.

The active current loop jumper configuration is shown in Figures 8 and 9.

Transmit:
CL4 jumper installed
CL3 resistor installed

Receive:
CL1 jumper installed
CL2 resistor installed

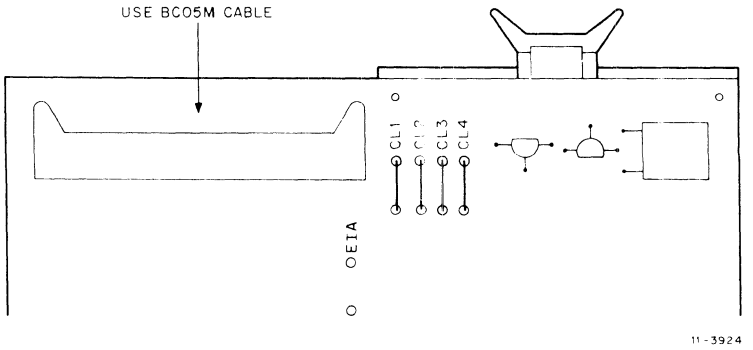

Figure 8 20 mA Active Current Loop Jumper Configuration

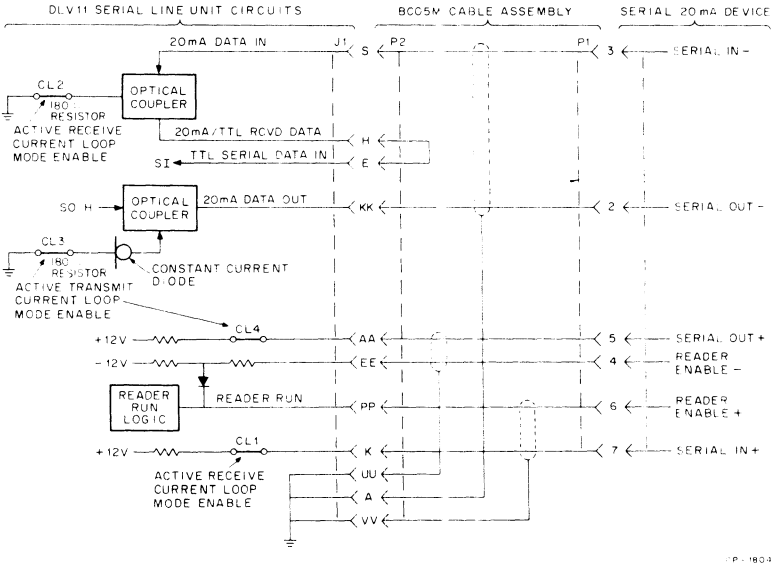

Figure 9 Active 20 mA Current Loop Interface

The passive current loop jumper configuration is shown in Figures 10 and 11.

Transmit:	CL4 jumper removed CL3 resistor removed
Receive:	CL1 jumper removed CL2 resistor removed

The DLV11 is supplied with jumpers CL1 through CL4 wired for the active transmit, active receive mode (Figure 9). When in this mode, serial current limiting to 23 mA is provided by resistors (one each for transmit and receive functions) connected to the +12 V source. Note that when module power is removed, the 20 mA transmit optical coupler closes the serial loop (active or passive mode). When the DLV11 is used in the passive 20 mA mode (Figure 11), the serial device must produce the 20 mA current. Current limiting must be provided for transmit and receive currents in the serial device.

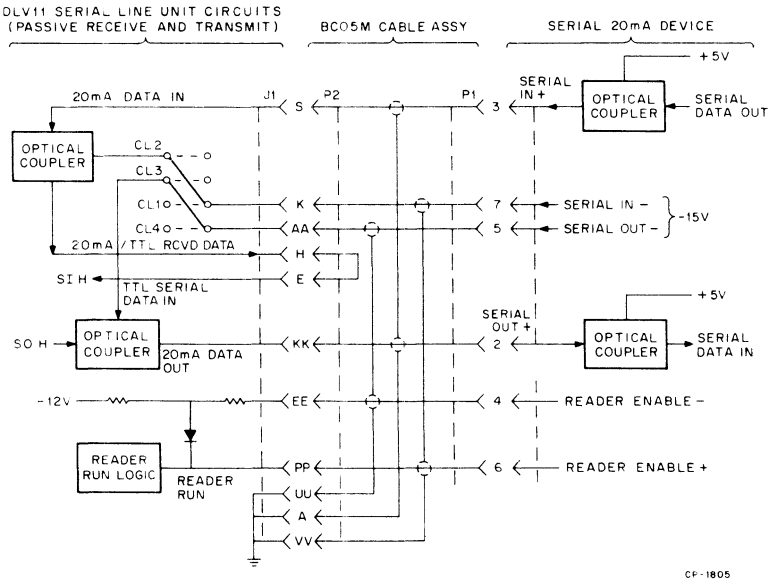

Figure 10 Passive 20 mA Current Loop Interface

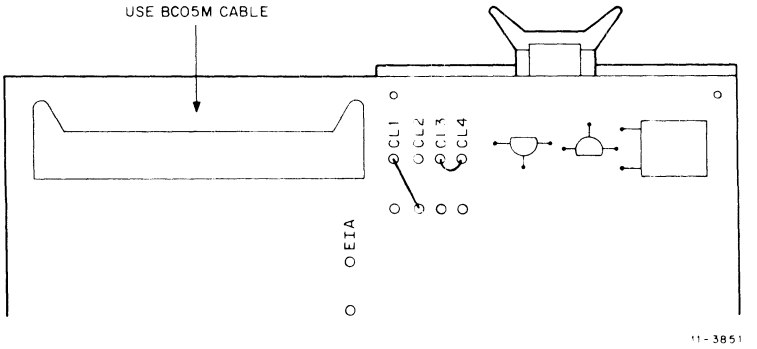

Figure 11 20 mA Passive Current Loop Jumper Configuration

Framing Error Halt

A framing error halt allows entry to console microcode directly from the console device by pressing the BREAK key, producing a framing error. A framing error occurs when the received character has no valid stop bit. This error condition is detected by the UART. FEH is factory-installed, causing the assertion of BHALT L when the framing error is detected. The processor then executes console microcode.

Installation

Prior to installing the DLV11 on the backplane, first establish the desired priority level to determine the backplane slot in which the module will be installed. Then, check that jumpers are removed or installed as described for your application. Connection to the peripheral device is via an optional data interface cable. Cables are listed below.

Application	Cable Type*
EIA Interface	BC01V-X or BC05C-X Modem Cable
20 mA Current Loop	BC05M-X Cable Assembly

*The -X in the cable number denotes length in feet, as follows: -1, -6, -10, -20, -25. For example, a 10-ft EIA interface cable would be ordered as BC05C-10.

Interfacing with 20 mA Current Loop Devices

When interfacing with 20 mA current loop devices, the BC05M cable assembly provides the correct connections to the 40-pin connector on the DLV11. The peripheral device end of the cable is terminated with a Mate-N-Lok connector that is pin-compatible with the following peripheral options:

LA36 DECwriter
LT33 Teletypewriter
LT35 Teletypewrier
VT05B Alphanumeric Terminal
VT50 DECscope
VT52 DECscope
RT02 Alphanumeric Terminals
DF01-A Acoustic Telephone Coupler

The complete interface circuit provided by the BC05M cable and the associated DLV11 jumpers is shown in Figure 10.

NOTE

When the DLV11 is used with teletypewriter devices, a 0.005 μF capacitor must be installed between split lugs TP1 and TP2.

After configuring the module jumpers and installing the proper interface cable, the DLV11 can be installed in the backplane.

Interfacing with EIA-Compatible Devices

When interfacing with EIA devices, the BC01V or BC05C modem cable provides the correct connection to the 40-pin connector on the DLV11. The peripheral device end of the cable is terminated with a Cinch DB25P connector that is pin-compatible with Bell 103, 113 modems. Connector pinning and signal levels conform to EIA specification RS232C. The complete EIA interface circuit is shown in Figure 12; jumpers are shown in Figure 13

OPTIONAL HARDWARE

Cables

BC05M	20 mA; H856 to Mate-N-Lok female
BC05C	EIA; H856 to Cinch 25-pin male.

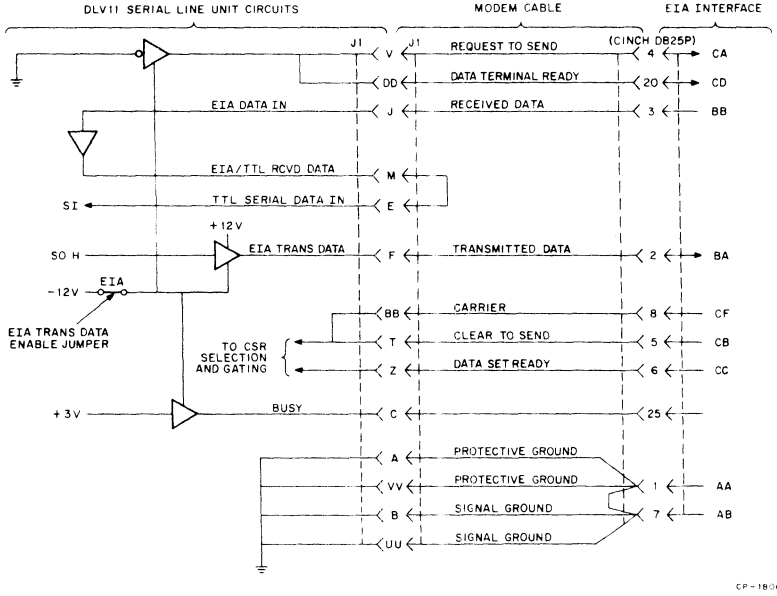

Figure 12 EIA Interface

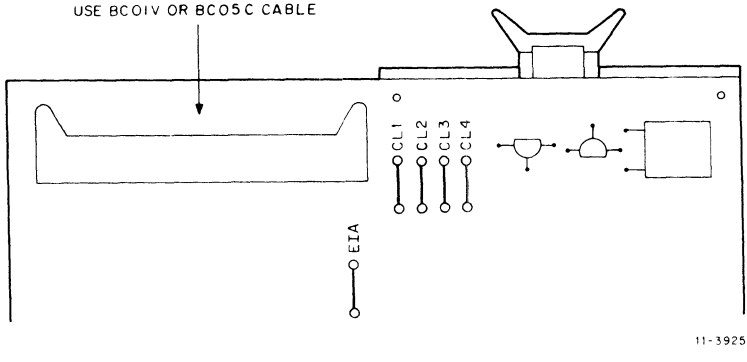

Figure 13 EIA Jumper Configuration

Connectors

H856	To module
Cinch DB25S	To BC05C
Mate-N-Lok (male)	12-09340-01 connector
Mate-N-Lok (male)	12-09378-01 contacts
Mate-N-Lok (female)	12-09340-00 connector
Mate-N-Lok (female)	12-09379-01 contacts

Miscellaneous

BC05F	20 mA extension cable (Mate-N-Lok to Mate-N-Lok)
BC03P	Null modem cable (female Cinch to female Cinch)
H312A	Null modem

FUNCTIONAL DESCRIPTION

General

The DLV11 functions as an interface between an asynchronous serial communication channel and the LSI-11 bus. It performs serial-to-parallel and parallel-to-serial data conversion with the universal asynchronous receiver/transmitter (UART). The UART includes the receiver functions and the transmitter functions. The receiver performs serial-to-parallel conversion of 5-, 6-, 7- or 8-level codes. The character length is selectable and the characters appear right justified in the data buffer register stripped of start, stop, and parity bits. The transmitter section performs parallel-to-serial conversion of data provided by the LSI-11 bus. The character length and stop code are the same as used in the receiver section. This section adds the start, stop, and parity bits to the data being transmitted. A function diagram of the module is shown in Figure 14.

UART Operation

The main function on the DLV11 module is the universal asynchronous receiver/transmitter (UART) chip. This is a 40-pin LSI chip that is capable of parallel I/O with the computer bus and asynchronous serial I/O with an external device. Jumpers allow the user to select parity functions, number of stop bits, and number of data bits. Both transmit and receive functions are totally asynchronous in operation. The transmit clock is always driven by the baud rate generator's CLK L signal. CLK L is applied to one MSPAREB backplane pin (BK1), where it is connected to MSPAREB pin BL1; this is the receive function UART clock input (RCLK L) signal.

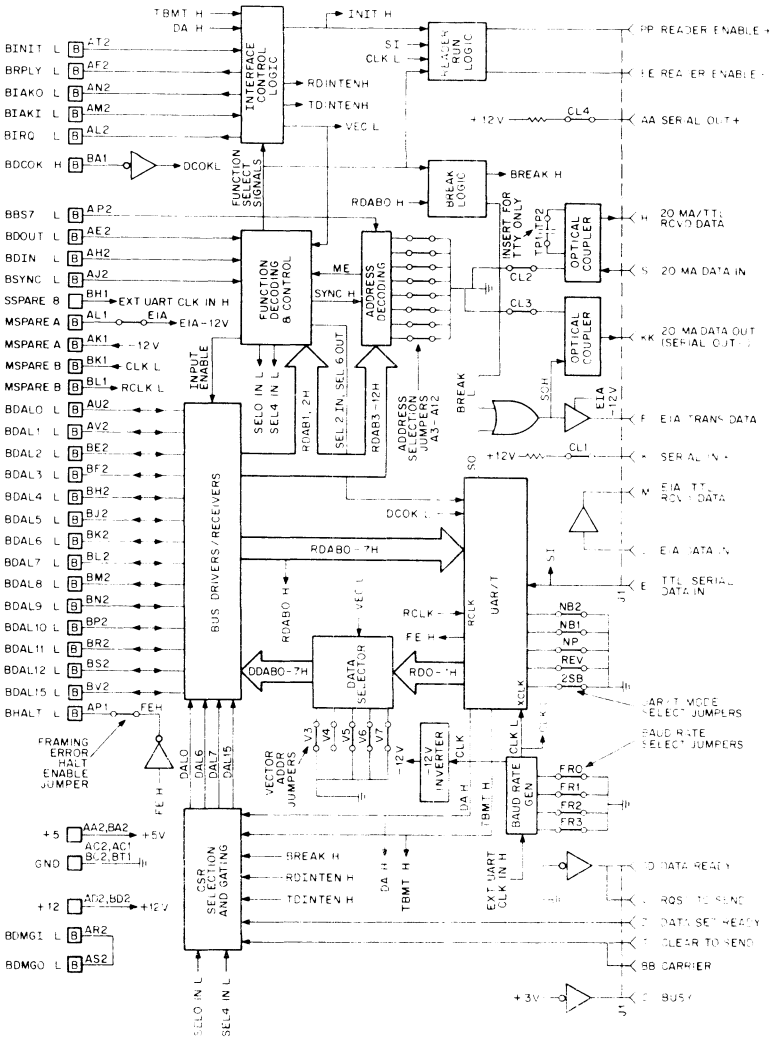

Figure 14 DLV11 Logic Block Diagram

When a user application requires split transmit and eceive baud rates, the MSPARE jumper can be broken from pins BK1 and BL1 and an external receive baud rate signal can be applied to BL1 (the drive frequency should be 16 times the desired baud rate).

Baud Rate Generator
The baud rate generator produces the desired UART clock and a fixed 2.4576 MHz clock for the -12 V inverter circuit. A crystal-controlled oscillator produces the basic 2.4576 MHz frequency for the baud rate generator. A single baud rate generator chip divides this frequency to produce the available baud rates. Jumpers select the desired baud rate for the CLK L output signal.

Bus Drivers and Receivers
Bus drivers and receivers interface directly with the LSI-11 bus. Line receivers produce RDAB0–12 H signals in response to BDAL0–12 L bus signals. When an input data or vector transfer is desired, function decoding and control logic generates an active INPUT ENABLE signal, which enables the bus drivers. When a data input operation is selected, the UART receiver data buffer contents (RD0–7 H) are routed through the data selector (DDAB0–7 H) to the BDAL bus. When responding to an interrupt acknowledge signal, interface control logic generates VEC L, which selects the vector address produced by jumpers W6–W10. In addition, DAL0, 6, 7, and 15 are driven by CSR selection and gating circuits when a data input transfer from either the receiver (RCSR) or transmitter (XCSF) control/status register is performed.

Address Decoding
Address decoding logic responds to the address present on the bus when BSYNC L is asserted. The DLV11 device address is contained on RDAB3–12 H, along with address bits RDAB0, 1, and 2 H, which are decoded by function decoding logic. Address bits are not required for bank selection since all devices, such as any DLV11, reside in the upper 4K bank (addresses ranging from 28–32K). The processor generates an active BBS7L signal, indicating an I/O device addressing operation. Address selection jumpers A3–A12 allow the user to configure address bits 3–12. When the DLV11 is addressed, device selection is indicated by an active ME signal. This signal remains active throughout the entire I/O cycle (while BSYNC L remains active), enabling function decoding.

Function Decoding and Control
Function decoding and control logic decodes DLV11 internal gating functions based on address selection, address bits RDAB0, 1, and 2 H, bus signals BDIN L, BDOUT L, and BSYNC L, and the VEC L signal generated by the interface control logic. In addition to generating function select signals, this circuit inverts BSYNC L to produce SYNC H whose leading edge clocks the address decoding logic. A truth table of function select signals is provided in Table 8.

Table 8 DLV11 Function Decoding

Address Inputs		Control Inputs			Function Select Signals (low-active)						
A1	A2	BDIN L	BDOUT L	ME L	SEL 0IN L	SEL 2IN L	SEL 4IN L	SEL 0OUT L	SEL 6IN L	SEL 4OUT L	SEL 6OUT L
X	X	X	X	H	H	H	H	H	H	H	H
L	L	L	X	L	L	H	H	H	H	H	H
H	L	L	X	L	H	L	H	H	H	H	H
L	H	L	X	L	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	L	H	H	H
L	H	H	L	L	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	L
H	H	L	H	L	H	H	H	H	L	H	H

Interface Control Logic

Interface control logic produces the BRPLY L signal in response to I/O operations, contains the interrupt control logic, and receives and distributes the BINIT L initialize signal. This function also contains the transmit data interrupt enable (TDINTEN H) flip-flop and receiver data interrupt enable (RDINTEN H) flip-flop; both flip-flops can be read or written by the LSI-11 bus. RDINTEN is set or reset by BDAL6 L; the flip-flop is clocked on the leading edge of SEL0OUT L. Similarly, TDINTEN is set or reset by BDAL6 L; this flip-flop is clocked on the leading edge of SEL4OUT L.

Receiver-generated interrupts occur as a result of the RDINTEN flip-flop being set (interrupts enabled) and an active receiver data available (DA H) UART status signal. When this condition occurs, the receiver data interrupt request flip-flop sets and generates an active BIRQ L signal. The LSI-11 bus responds (if its PS bit 7 is not set) by asserting BDIN L; this enables the device requesting the interrupt to place its vector on the BDAL bus when the interrupt request is acknowledged. The processor then asserts BIAKO L, acknowledging the interrupt request. The interface control logic receives BIAKI L and responds by generating active VEC L and BRPLY L signals, placing its interrupt vector on the LSI-11 bus and clearing the BIRQ L signal. The stored BIAK signal is cleared when the next BIAKI L signal is received and the DLV11 is not requesting an interrupt.

Transmitter-generated interrupts occur in a manner similar to the receiver-generated interrupts. However, they occur as a result of the TDINTEN flip-flop being set (interrupts enabled) and when the transmitter buffer empty (TBMT H) UART signal is active (high). Note that if the transmitter and receiver functions request interrupts simultaneously, the receiver interrupt vector will be transmitted on the first interrupt cycle, and the transmitter interrupt vector will be transmitted on a subsequent (separate) interrupt sequence. If BIAKI L is received and the DLV11 is not requesting an interrupt, it passes BIAKO L to the next device in the priority chain.

The interface control logic also generates the DLV11's BRPLY L signal. It generates this signal when any function select signal is asserted or VEC L is generated.

The system initialize signal (BINIT L) is generated by the processor to reset all peripheral device registers. Interface control logic responds by clearing all control flip-flops, including the interrupt request, interrupt acknowledge, and break flip-flops. The UART's RBUF and XBUF data registers are not cleared by BINIT L; however, the initialize signal does clear the DAH signal and set the TBMT H signal.

CSR Selection and Gating
CSR selection and gating logic enables the LSI-11 bus to read receiver and transmitter control/status bits. Functions are summarized below.

Read RCSR (SEL0IN L asserted)
CARRIER or CLR TO SEND or DATA SET READY → BDAL15
DAH → BDAL7
RDINTEN H → BDAL6

Read XCSR (SEL4IN L asserted)
TBMTH → BDAL7
TDINTEN H → BDAL6
BREAK H → BDAL0

Break Logic
Break logic comprises the break status flip-flop. It is set or cleared by the LSI-11 bus by BDAL0 while executing a bus output cycle with the XCSR. Thus, the duration of the break signal is program controlled. The break flip-flop is clocked on the leading edge of the SEL4OUT H signal. When set, the serial output line is continuously negated (space) or open circuit. The status of the break flip-flop can be read in XCSR bit 0.

Reader Run Logic
The reader run logic enables DLV11 generation of a READER RUN pulse for 20 mA current loop teletypewriter devices. It is enabled by loading RCSR bit 0; the LSI-11 bus asserts BDAL0 and causes generation of the SEL0OUT H signal (load RCSR). READER RUN is asserted and remains active until the received serial data has been in a mark condition for the duration of eight consecutive clock pulses. The start bit of the serial input (SI) from the low-speed reader initiates a 4-bit binary counter. When eight CLK L pulses have been counted (equivalent to one-half of the start bit), READER RUN is negated.

EIA Interface Circuits
An EIA interface is provided by EIA drivers and receivers. EIA signal drivers are provided for EIA TRANS DATA, RQST TO SEND, DATA TERMINAL READY (always an active high), and BUSY (always an active low). Jumper EIA applies −12 V to the EIA driver chip when the DLV11 is used with EIA-compatible devices. EIA signal receivers are provided for EIA DATA IN, CARRIER or CLEAR TO SEND, and DATA SET READY. The optional BC05C modem cable connects the output signal of the EIA DATA IN driver (EIA/TTL RCVD DATA) to the TTL SERIAL DATA IN input to the UART.

20 mA Loop Current Interface

The 20 mA loop current interface is provided by optical isolation. An active 20 mA current loop is provided when jumpers CL1 through CL4 are installed. If the jumpers are removed, 20 mA passive current loop operation is selected. The optional BC05M cable assembly connects the 20 mA/TTL RCVD DATA optical coupler signal output to the TTL SERIAL DATA IN input of the UART. When the DLV11 is used with a 110 baud teletypewriter device, a 0.005 μF, 100 V filter capacitor should be installed between terminals TP1 and TP2.

−12 V Inverter

The −12 V inverter generates −12 V for use by the UART chip and EIA driver and receiver chips. Input to the circuit is the CLK signal (2.4576 MHz) and +12 V. The output is zener regulated to −12 V.

DLV11-E ASYNCHRONOUS LINE INTERFACE

GENERAL

The DLV11-E is an asynchronous line interface module that interfaces the LSI-11 bus to any of several standard types of serial communications lines. The module receives serial data from peripheral devices, assembles it into parallel data, and transfers it to the LSI-11 bus. It accepts data from the LSI-11 bus, converts it into serial data, and transmits it to the peripheral devices. The DLV11-E offers full modem control and EIA type interface.

FEATURES

- Jumper- or program-selectable, crystal-controlled baud rates: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, and 19,200. Split transmit and receive baud rates are possible.
- Provisions for user-supplied external clock inputs for baud rate control
- Jumper-selectable stop bit and data bit formats
- LSI-11 bus interface and control logic for interrupt processing and vectored addressing of interrupt service routines
- Control, status, and data buffer registers directly accessible via processor instructions
- Full modem control (Bell 103, 113, 202C, 202D, and 212-compatible)

SPECIFICATIONS

Identification	M8017
Size	Double
Power	+5.0 Vdc ± 5% at 1.0 A +12.0 Vdc ± 3% at 0.18 A
Bus Loads	
AC	1.6
DC	1.0

CONFIGURATION

General

The following paragraphs describe how the user can configure the module so that it will function within his system. The user can select the register addresses, interrupt vectors, data format, baud rate, and interface mode. The descriptions of the registers and their standard factory addresses are listed in Table 1. The jumpers used on this module consist of wire-wrap pins to which the connections are made; their locations are shown in Figures 1 and 2. A complete listing of the jumpers and a description of their functions are contained in Table 2.

Addresses for the DLV11-E can range from 160000 through 177770_8. The least significant three bits (only bits 1 and 2 are used; bit 0 is ignored) address the desired register in the module, as described in Table 1. Address bits 3 through 12 are jumper-selected as illustrated in Figure 2.

Since each module has four registers, each requires four addresses. Addresses 177560–177566 are reserved for the module used with the console peripheral device. Additional modules should be assigned addresses from 175610 through 176176, allowing up to 30 additional DLV11-E modules to be addressed.

Table 1 Standard Assignments

Description	Mnemonic	Console Module	Second Module
Register			
Receiver Control/Status	RCSR	177560	175610
Receiver Data Buffer	RBUF	177562	175612
Transmit Control/Status	XCSR	177564	175614
Transmit Data Buffer	XBUF	177566	175616
Interrupts			
Receiver		60	300
Transmitter		64	304

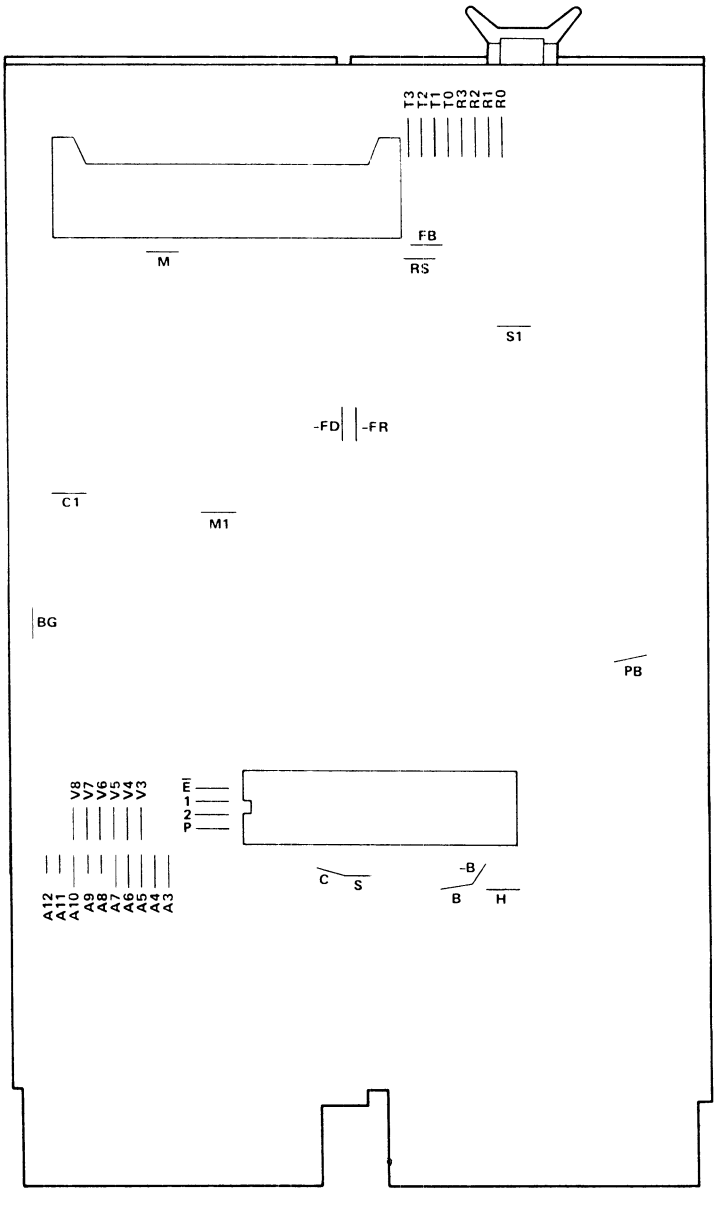

Figure 1 DLV11-E Jumper Locations

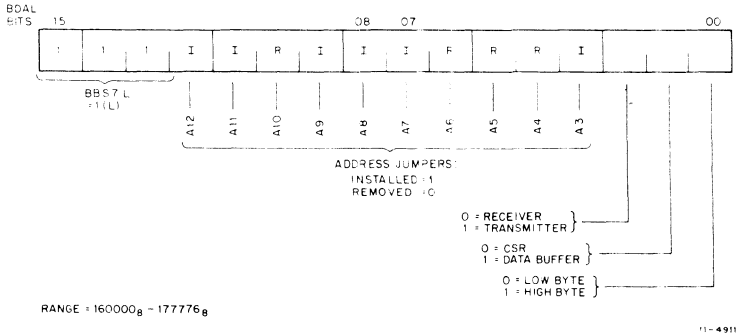

Figure 2 DLV11-E Addressing

Table 2 DLV11-E Jumper Definitions

NOTE

Jumpers are inserted to enable the function they control except for those jumpers which indicate negation (such as "-B" and "$\overline{E}$"). Negated jumpers are removed to enable the functions they control.

Jumper	Function
A3–A12	These jumpers correspond to bits 3 through 12 of the address word. When inserted, they will cause the bus interface to check for a true condition on the corresponding address bit.
V3–V8	Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector bit on the LSI-11 bus.
R0–R3	Receiver and transmitter baud rate select jumpers during common speed operation. Receiver-only baud rate select jumpers during split speed operation as defined in Table 3.
T0–T3	Transmitter baud rate select jumpers during split speed operation. Both receiver and transmitter baud rate if maintenance mode is entered during split speed operation as defined in Table 3.

Table 2 DLV11-E Jumper Definitions (Cont)

Jumper	Function
BG	Jumper is inserted to enable break generation.
P	Jumper is inserted for operation with parity.
$\overline{E}$	Removed for even parity; inserted for odd parity.
1, 2	These jumpers select the desired number of data bits, as defined in Table 4.
PB	Jumper is inserted to enable the programmable baud rate capability.
C, C1	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted.)
S, S1	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.)
H	This jumper is inserted to assert BHALT L when a framing error is received, except when the maintenance bit is set. This places the processor in the halt mode.
B, -B	Jumper B is inserted to negate BDCOK H when a break signal or framing error is received, except when the maintenance bit is set. This causes the processor to reboot. (Jumper -B must be removed when B is inserted.)
-FD	Jumper is removed to force data terminal ready signal on.
-FR	Jumper is removed to force request to send signal on.
RS	This jumper is inserted to enable normal transmission of the request to send signal.
FB	Inserted to enable transmission of the force busy signal (for Bell model 103E data sets).
M, M1	These are test jumpers used during the manufacture of the module. They are not defined for field use.

Interrupt Vectors

The interrupt vectors are selected by using jumpers V3 to V8. The standard configuration is shown in Figure 3 and Table 1. The vectors can range from 001 through 774. Note that vectors 60 and 64 are reserved for the console device. Additional DLV11-E modules should be assigned vectors following any DRV11 parallel interface modules installed in the system that start at address 300.

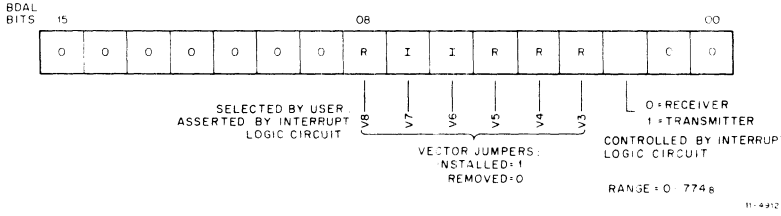

Figure 3 DLV11-E Interrupt Vectors

Baud Rate Selection

The DLV11-E allows the user to configure jumpers T0–T3 and R0–R3 for the transmit baud rate and the receiver baud rate as shown in Table 3.

Data Bit Selection

The number of data bits being transmitted or received by the DLV11-E is user-selectable by installing or removing jumpers 1 and 2. The specific number of data bits as controlled by the configuration of jumpers 1 and 2 is shown in Table 4.

Factory Configuration

The user can reconfigure any of the jumpers so that the module will meet his requirements. The factory configuration as shipped is shown in Table 5 to assist the user in determining what changes are required.

Registers

The word format for the DLV11-E CSR is shown in Figure 4 and functionally described in Table 6.

Table 3 DLV11-E Baud Rate Selection

Program Control Receive Jumpers Transmit Jumpers	Bit 15 R3 T3	Bit 14 R2 T2	Bit 13 R1 T1	Bit 12 R0 T0	Bit 11*	Baud Rate
	I	I	I	I		50
	I	I	I	R		75
	I	I	R	I		110
	I	I	R	R		134.5
	I	R	I	I		150
	I	R	I	R		300
	I	R	R	I		600
	I	R	R	R		1200
	R	I	I	I		1800
	R	I	I	R		2000
	R	I	R	I		2400
	R	I	R	R		3600
	R	R	I	I		4800
	R	R	I	R		7200
	R	R	R	I		9600
	R	R	R	R		19200

I = Jumper inserted = program bit cleared.
R = Jumper removed = program bit set.

*Bit 11 of the XCSR (write-only bit) must be set in order to select a new baud rate under program control. Also, jumper PB must be inserted to enable baud rate selection under program control.

Table 4 DLV11-E Data Bit Selection

Jumpers		Number of Data Bits
2	1	
I	I	5
I	R	6
R	I	7
R	R	8

Table 5 DLV11-E Factory Jumper Configuration

Jumper Designation	Jumper State	Function Implemented
A3	I	Jumpers A3 through A12 implement device address 17561X. The least significant octal digit is hardwired on the module to address the four device registers as follows: X = 0 RCSR X = 2 RBUF X = 4 XCSR X = 6 XBUF
A4	R	
A5	R	
A6	R	
A7	I	
A8	I	
A9	I	
A10	R	
A11	I	
A12	I	
V3	R	This jumper selection implements interrupt vector address 300_8 for receiver interrupts and 304_8 for transmitter interrupts.
V4	R	
V5	R	
V6	I	
V7	I	
V8	R	
R0	I	The module is configured to receive at 110 baud.
R1	R	
R2	I	
R3	I	
T0	I	The transmitter is configured for 9600 baud if split speed operation is used.
T1	R	
T2	R	
T3	R	
BG	I	Break generation is enabled.
P	R	Parity bit is disabled.
E	R	Parity type is not applicable when P is removed
1	R	Operation with 8 data bits per character.
2	R	
PB	R	Programmable baud rate function disabled.
C	I	Common speed operation enabled.
C1	I	

Table 5 DLV11-E Factory Jumper Configuration (Cont)

Jumper Designation	Jumper State	Function Implemented
S S1	R R	Split speed operation disabled.
H	R	Halt on framing error disabled.
B	R	Boot on framing error disabled.
FD	I	The data terminal ready signal is not forced continuously true.
RS	I	The circuitry controlling the request to send signal is enabled.
FB	R	The force busy signal is disabled.
EF	R	Error flags are enabled.
MT	R	Maintenance bit disabled.
M M1	R R	Factory test jumpers. Not defined for field use.

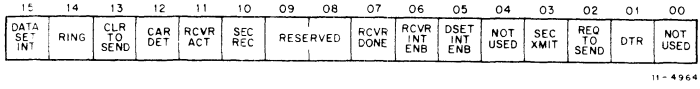

Figure 4 DLV11-E RCSR Word Format

Table 6 DLV11-E RCSR Bit Assignments

Bit	Name	Description
15	DATA SET INT (Data Set Interrupt)	This bit initiates an interrupt sequence provided the DSET INT ENB (bit 5) is also set.

Table 6 DLV11-E RCSR Bit Assignments (Cont)

Bit	Name	Description
		This bit is set whenever CAR DET, CLR TO SEND, or SEC REC changes state, i.e., on a 0 to 1 or 1 to 0 transition of any one of these bits. It is also set when RING changes from 0 to 1. Cleared by INIT or by reading the RCSR. Because reading the register clears the bit, it is, in effect, a "read-once" bit.
14	RING	When set, indicates that a ringing signal is being received from the data set. Note that the ringing signal is not a level but an EIA control with a duty cycle of 2 seconds ON and 4 seconds OFF. Read-only bit.
13	CLR TO SEND (Clear to Send)	The state of this bit is dependent on the state of the clear to send signal from the data set. When set, this bit indicates an ON condition; when clear, it indicates an OFF condition. Read-only bit.
12	CAR DET (Carrier Detect)	This bit is set when the data carrier is received. When clear, it indicates either the end of the current transmission activity or an error condition. Read-only bit.
11	RCVR ACT (Receiver Active)	When set, this bit indicates that the DLV11-E's receiver is active. The bit is set at the center of the start bit, which is the beginning of the input serial data from the device, and is cleared by the leading edge of R DONE H.

Table 6 DLV11-E RCSR Bit Assignments (Cont)

Bit	Name	Description
		Read-only bit; cleared by INIT or by RDONE H (bit 7).
10	SEC REC (Secondary Received or Supervisory Received Data)	This bit provides a receive capability for the reverse channel of a remote station. A space (+6 V) is read as a 1. (A transmit capability is provided by bit 3.) Read-only bit.
9–8	Not Used	Reserved for future use.
7	RCVR DONE (Receiver Done)	This bit is set when an entire character has been received and is ready for transfer to the processor. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 6) is also set. Cleared whenever the receiver buffer (RBUF) is addressed. Also cleared by INIT. Read-only bit.
6	RCVR INT ENB (Receiver Interrupt Enable)	When set, allows an interrupt sequence to start when RCVR DONE (bit 7) sets. Read/write bit; cleared by INIT. (See Note 1.)
5	DSET INT ENB (Data Set Interrupt Enable)	When set, allows an interrupt sequence to start when DATA SET INT (bit 15) sets. Read/write bit; cleared by INIT. (See Note 1.)
4	Not Used	Reserved for future use.

Table 6 DLV11-E RCSR Bit Assignments (Cont)

Bit	Name	Description
3	SEC XMIT (Secondary Transmitted or Supervisory Transmitted Data)	This bit provides a transmit capability for a reverse channel of a remote station. When set, transmits a space (≈+11.5 V). (A receive capability is provided by bit 10.) Read/write bit; cleared by INIT.
2	REQ TO SEND (Request to Send)	A control lead to the data set which is required for transmission. A jumper on the DLV11-E ties this bit to REQ TO SEND or force busy in the data set. Read/write bit; cleared by INIT.
1	DTR (Data Terminal Ready)	A control lead for the data set communication channel. When set, permits connection to the channel. When clear, disconnects the interface from the channel. Read/write bit; must be cleared by the program; is not cleared by INIT. (See Note 2.)

NOTES

1. When clearing an interrupt enable bit, first set the appropriate processor status bit = 1. After the interrupt enable bit at the module is cleared, the processor may be returned to its normal priority.

2. The state of this bit is not defined after power-up.

3. INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-E RBUF register is shown in Figure 5 and functionally described in Table 7.

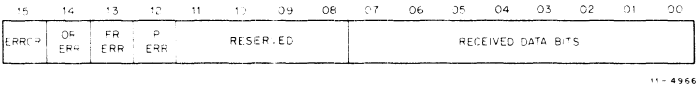

Figure 5 DLV11-E RBUF Word Format

Table 7 DLV11-E RBUF Bit Assignments

Bit	Name	Description
15	ERROR (Error)	Used to indicate that an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes error to set. This bit is not connected to the interrupt logic. Read-only bit; cleared by removing the error-producing condition.
		NOTE Error indications remain present until the next character is received, at which time the error bits are updated. INIT clears the error bits.
14	OR ERR (Overrun Error)	When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Read-only bit. Cleared by INIT.
13	FR ERR (Framing Error)	When set, indicates that the character that was read had no valid stop bit. Read-only bit. Cleared by INIT.

Table 7 DLV11-E RBUF Bit Assignments (Cont)

Bit	Name	Description
12	P ERR (Parity Error)	When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected. Read-only bit. Cleared by INIT.
11–8	Not Used	Reserved for future use.
7–0	RECEIVED DATA BITS	Holds the character just read. If less than eight bits are selected, then the buffer is right-justified into the least significant bit positions. In this case, the higher unused bit or bits are read as 0s. Read-only bits; not cleared by INIT.

NOTE
INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-E XCSR register is shown in Figure 6 and functionally described in Table 8.

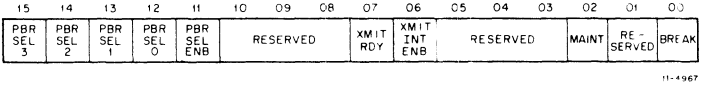

Figure 6 DLV11-E XCSR Word Format

Table 8 DLV11-E XCSR Bit Assignments

Bit	Name	Description
15–12	PBR SEL (Programmable Baud Rate Select)	When set, these bits choose a baud rate from 50–9600 baud. See Table 3. Write-only bits.

Table 8 DLV11-E XCSR Bit Assignments (Cont)

Bit	Name	Description
11	PBR ENB (Programmable Baud Rate Enable)	This bit must be set in order to select a new baud rate indicated by bits 12 to 15. Write-only bits.
10–8	Not Used	Reserved for future use.
7	XMIT RDY (Transmitter Ready)	This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 6) is also set.
6	XMIT INT ENB (Transmitter Interrupt Enable)	When set, allows an interrupt sequence to start when XMIT RDY (bit 7) is set. Read/write bits; cleared by INIT. (See Note.)
5–3	Not Used	Reserved for future use.
2	MAINT	Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed when common speed operation is enabled. Read/write bit; cleared by INIT.
1	Not Used	Reserved for future use.

Table 8 DLV11-E XCSR Bit Assignments (Cont)

Bit	Name	Description
0	BREAK	When set, transmits a continuous space to the external device. Read/write bit; cleared by INIT.
		NOTE When clearing an interrupt enable bit, first set the appropriate processor status word bit = 1. After the interrupt enable bit at the module is cleared, the processor may be returned to its normal priority.

The word format for the DLV11-E XBUF register is shown in Figure 7 and functionally described in Table 9.

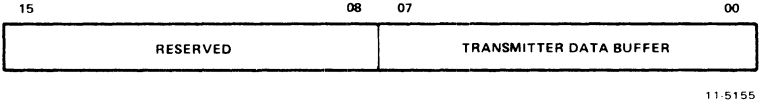

Figure 7 DLV11-E XBUF Word Format

Table 9 DLV11-E XBUF Bit Assignments

Bit	Name	Description
15–8	Not Used	Not defined. Not necessarily read as 0s.
7–0	TRANSMITTER DATA BUFFER	Holds the character to be transferred to the external device. If less than eight bits are used, the character must be loaded so that it is right-justified into the least significant bits. Write-only bits. Not necessarily read as 0s.

Installation

Prior to installing the DLV11-E on the backplane, first establish the desired priority level to determine the backplane slot in which the module will be installed. Then, check that module configuration jumpers are configured as required for your application. Connection to the peripheral device is via an optional BC05C-X* modem cable for EIA interface applications.

The BC05C modem cable provides the correct connection to the 40-pin connector on the DLV11-E. The peripheral device end of the cable is terminated with a Cinch DB25P connector that is pin-compatible with Bell 103, 113, 202C, 202D, and 212 modems. Connector pinning and signal levels conform to EIA specification RS232C. The EIA interface circuit is shown in Figure 8; jumpers are shown in Figure 1.

FUNCTIONAL DESCRIPTION

General

Major functions contained on the DLV11-E are shown in Figure 9. Communications between the processor and the DLV11-E are executed via programmed I/O operations or interrupt-driven routines.

Bus Interface

The bus interface circuit signal levels consist of data moving between the LSI-11 bus and the module's internal tri-state bus. It decodes the device address and produces an address match (MATCH H) signal and it places interrupt vectors on the LSI-11 bus. The bus interface receives from the LSI-11 bus unless it is switched to transmit to the LSI-11 bus. The interrupt logic can cause the bus interface to transmit either a transmitter or receiver interrupt vector and the I/O control logic can cause the bus interface to transmit or receive data to or from the LSI-11 bus.

The bus interface receives LSI-11 bus lines BDAL00 L through BDAL15 L and places them on the module's tri-state bus. If BBS7 L is asserted, the circuit decodes BDAL03 L through BDAL12 L and asserts MATCH H. Jumpers A3–A12 are configured to allow the option to respond to specific device register addresses. Jumpers V3–V8 select the options' interrupt vector.

I/O Control Logic

When the I/O control logic receives MATCH H from the bus interface, it decodes tri-state bus lines DAT00 H through DAT02 H and selects the addressed device register. The I/O control logic exchanges bus control signals with the processor to perform input and output data transfers.

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*X = Length in feet. Standard length is 25 feet.

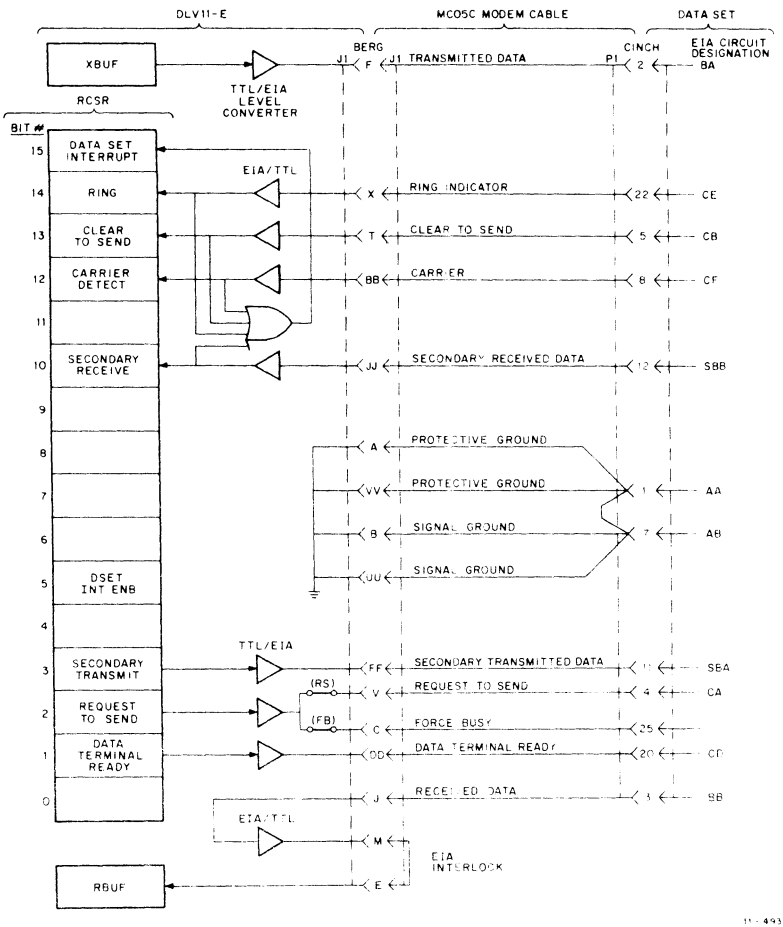

Figure 8 DLV11-E Peripheral Interface Signal Flow

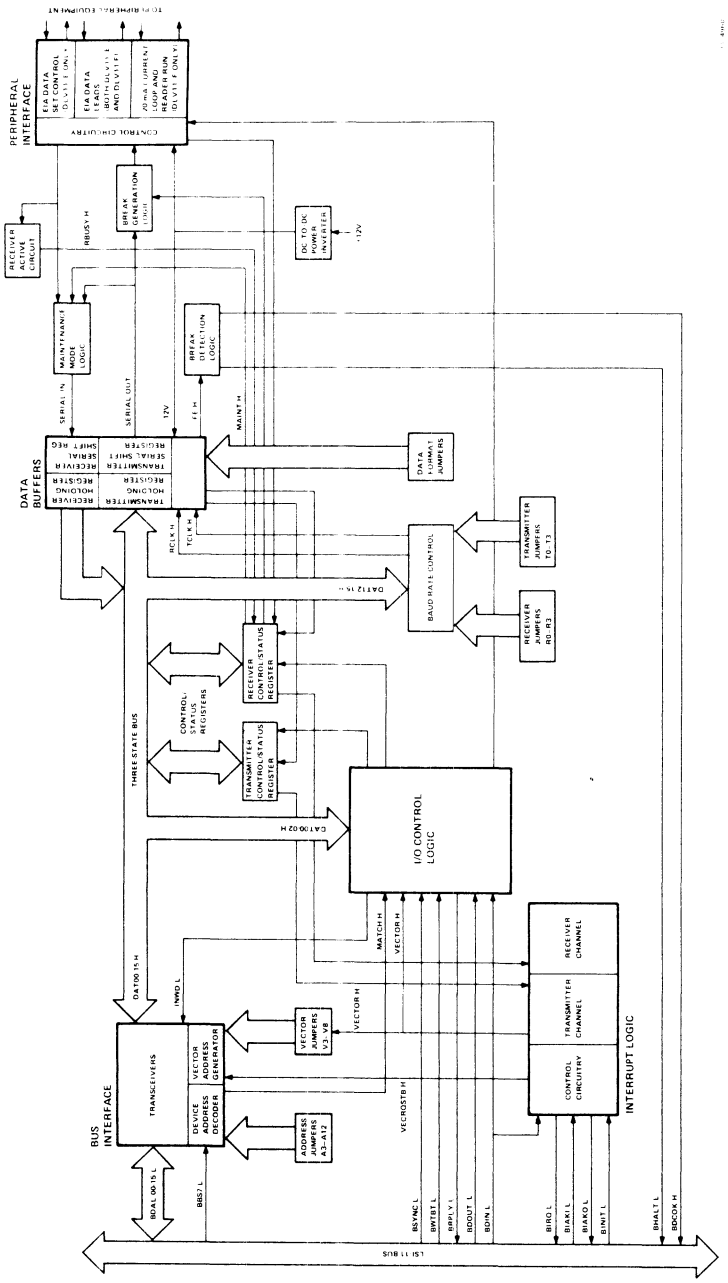

Figure 9 DLV11-E Asynchronous Line Interface Logic Block Diagram

During an interrupt transaction, VECTOR H from the interrupt logic causes the circuit to assert BRPLY L in response to BDIN L. During data transactions, the I/O control logic asserts INWD L to switch the bus interface transceivers from receiving to transmitting.

Control/Status Registers
The receiver control/status register (RCSR) and the transmitter control/status register (XCSR) are enabled by selection signals from the I/O control logic. The CSRs are byte addressable for reading status bits or writing control bits.

Data Buffers
The receiver buffer (RBUF) and transmitter buffer (XBUF) provide double-buffering in that one byte of data can be held while another byte is entering or exiting. This allows asynchronous, full-duplex operation. Data is handled in the low byte of the registers. The buffer control circuitry places receiver buffer error flag bits in the high byte of the RBUF. It also sends a status bit to the RCSR and a framing error bit (FE H) to the break logic.

Receiver Active Circuit
This circuit monitors the received serial data line and sets a status bit (RCVR ACT) as soon as the RBUF begins receiving data. It clears the bit when a full character of data has been received.

Interrupt Logic
The DLV11-E can generate transmitter interrupts. If the XBUF is ready to serialize another character of data and the transmitter interrupt enable bit is set in the XCSR, the interrupt logic requests to interrupt the processor (by asserting BIRQ L). If the processor acknowledges via the BIAKI/BIAKO daisy-chain, the interrupt logic asserts VECTOR H and VECRQSTB H. These signals cause the bus interface to place the transmitter function interrupt vector address on the LSI-11 bus.

The module also can request a receiver interrupt if the RBUF has received a character and the receiver interrupt bit is set in the RCSR. When the interrupt request is acknowledged, the interrupt logic asserts VECTOR H. VECTOR H causes the bus interface circuit to place the receiver function interrupt vector on the LSI-11 bus. (VECRQSTB H is used only for a transmitter interrupt.)

The DLV11-E also generates a receiver interrupt as a result of data set status. If the data set interrupt enable bit is set in the RCSR, a receiver interrupt will result from a change of state on any of the modem control lines (ring, clear to send, carrier, or secondary received data).

The interrupt acknowledge daisy-chain (BIAKI/BIAKO) passes through both the receiver and transmitter sections of the interrupt logic. It goes through the receiver section first, thereby giving the receiver channel priority over the transmitter channel.

Baud Rate Control

The baud rate control establishes the speed at which the data buffers handle serial data. It produces clock signals by dividing a crystal oscillator frequency by an amount selected by jumpers or the program. The circuit can be jumpered to generate either independent transmitter and receiver clocks (split speed operation) or a common clock (common speed operation).

When the programmable baud rate enable bit is set in the XCSR, the baud rate control decodes tri-state bus lines DAT12 H through DAT15 H. These bits control the receive baud rate in split speed operation and both transmit and receive baud rate in common speed operation. When programmable baud rate is not enabled, the baud rates are controlled by jumpers. In split speed operation, jumpers R0–R3 control the receive baud rate and jumpers T0–T3 control the transmit baud rate. In common speed operation, R0–R3 control both baud rates.

The circuit also has provisions for a user-supplied external clock.

Break Logic

A break signal is a continuous spacing condition on the serial data line. If the break bit is set in the XCSR, the module will transmit a break signal to the peripheral device (normally another processor). If the module receives a break signal from the peripheral device (normally a console device), the RBUF control circuitry interprets the absence of stop bits as a framing error. The circuit can be jumpered to ignore the framing error, to place the processor in the halt mode, or to cause the processor to reboot. The break logic asserts BHALT L to halt the processor. It negates BDCOK H to reboot.

Maintenance Mode Logic

The modules can check out their data paths up to (but not including) the peripheral interface circuit by looping the XBUF's serial output back to the RBUF's serial input. Data from the LSI-11 bus still goes to the peripheral device, but no data is received from the peripheral in this maintenance mode. The program can compare received (looped) data with transmitted data to check for errors. The maintenance mode is entered by setting the maintenance bit in the XCSR.

Signal Peripheral Interface

This circuit converts the module's TTL levels to EIA standard levels for modem control. It receives ring, carrier, clear to send, and secondary received data from the data set. It transmits data terminal ready, request to send, force busy, and secondary transmitted data to the data set. (Request to send and force busy are jumper-selectable.) If data set interrupts are enabled, a change in state on any of the received control lines initiates a receiver interrupt. Data is received on the received data line and transmitted on the transmitted data line. Handshake sequences are under program control.

DC-to-DC Power Inverter

The power inverter uses the +12 V from the backplane to produce −12 V for the peripheral interface and data buffer circuitry. It consists of an oscillator, rectifier, inductive charge pump, and a zener regulator.

DLV11-F ASYNCHRONOUS LINE INTERFACE

GENERAL

The DLV11-F asynchronous line interface module interfaces the LSI-11 bus to any of several standard types of serial communications lines. The module receives serial data from peripheral devices, assembles it into parallel data, and transfers it to the LSI-11 bus. It accepts data from the LSI-11 bus, converts it into serial data, and transmits it to the peripheral devices. The DLV11-F supports either 20 mA current loop or EIA-standard lines, but does not include modem control.

FEATURES

- Jumper- or program-selectable, crystal-controlled baud rates: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, and 19,200. Split transmit and receive baud rates are possible.
- Provisions for user-supplied external clock inputs for baud rate control
- Jumper-selectable stop bit and data bit formats
- LSI-11 bus interface and control logic for interrupt processing and vectored addressing of interrupt service routines
- Control, status, and data buffer registers directly accessible via processor instructions
- Support for "data leads only" modem (Bell type 103, 113)
- Generation of reader run signal for use with ASR type terminals (when equipped with reader run relay)

SPECIFICATIONS

Identification	M8028
Size	Double
Power	+5.0 Vdc ± 5% at 1.0 A +12.0 Vdc ± 3% at 0.18 A
Bus Loads	
AC	2.2
DC	1.0

CONFIGURATION

General

The following paragraphs describe how the user can configure the module so that it will function within his system. The user can select the register addresses, interrupt vectors, data format, baud rate, and interface mode. The registers and their standard factory addresses are listed in Table 1. The jumpers used on this module consist of wire-wrap pins to which the connections are made; their locations are shown in Figure 1. A complete listing of the jumpers and a description of their functions are listed in Table 2.

Addresses

Addresses for the DLV11-F can range from 160000 through 177770_8. The least significant three bits (only bits 1 and 2 are used; bit 0 is ignored) address the desired register in the module, as described in Table 1. Address bits 3 through 12 are jumper-selected as illustrated in Figure 2.

Since each module has four registers, each requires four addresses. Addresses 177560–177566 are reserved for the module used with the console peripheral device. Additional modules should be assigned addresses from 175610 through 176176, allowing up to 30 additional DLV11-F modules to be addressed.

Interrupt Vectors

The interrupt vectors are selected by using jumpers V3 to V8. The standard configuration is shown in Figure 3 and Table 1. The vectors can range from 001 through 774. Note that vectors 60 and 64 are reserved for the console device. Additional DLV11-F modules should be assigned vectors following any DRV11 peripheral interface module installed in the system that starts at address 300.

Table 1 Standard Assignments

Description	Mnemonic	Console Module	Second Module
Register			
Receiver Control/Status	RCSR	177560	175610
Receiver Data Buffer	RBUF	177562	175612
Transmit Control/Status	XCSR	177564	175614
Transmit Data Buffer	XBUF	177566	175616
Interrupts			
Receiver		60	300
Transmitter		64	304

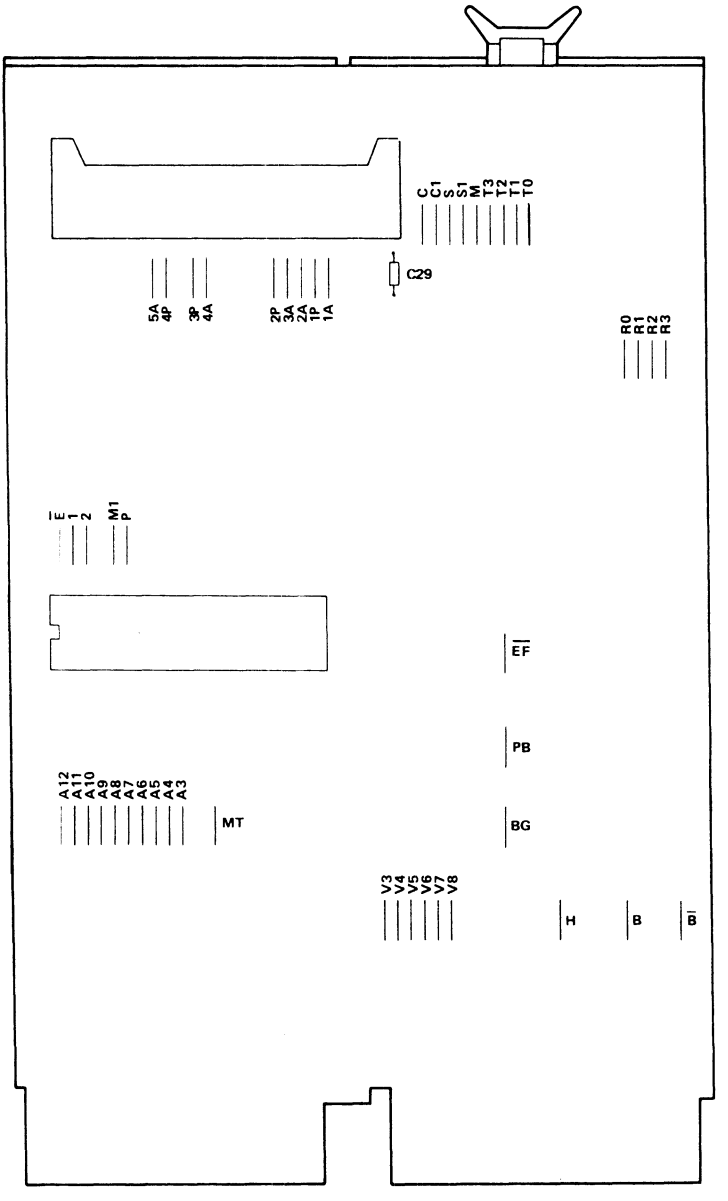

Figure 1 DLV11-F Jumper Locations

Table 2 DLV11-F Jumper Definitions

NOTE

Jumpers are inserted to enable the function they control except for those jumpers which indicate negation (such as "-B" and "$\overline{E}$"). Negated jumpers are removed to enable the functions they control.

Jumper	Function
A3–A12	These jumpers correspond to bits 3 through 12 of the address word. When inserted, they will cause the bus interface to check for a true condition on the corresponding address bit.
V3–V8	Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector bit on the LSI-11 bus.
R0–R3	Receiver and transmitter baud rate select jumpers during common speed operation.
	Receiver-only baud rate select jumpers during split speed operation as defined in Table 3.
T0–T3	Transmitter baud rate select jumpers during split speed operation.
	Both receiver and transmitter baud rate if maintenance mode is entered during split speed operation as defined in Table 3.
BG	Jumper is inserted to enable break generation.
P	Jumper is inserted for operation with parity.
$\overline{E}$	Receiver checks for appropriate parity and transmitter inserts appropriate parity.
1, 2	These jumpers select the desired number of data bits, as defined in Table 4.

Table 2 DLV11-F Jumper Definitions (Cont)

Jumper	Function
PB	Jumper is inserted to enable the programmable baud rate capability.
C, C1	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted.)
S, S1	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.)
H	This jumper is inserted to assert BHALT L when a framing error is received, except when the maintenance bit is set. This places the processor in the halt mode.
B, -B	Jumper B is inserted to negate BDCOK H when a break signal or framing error is received, except when the maintenance bit is set. This causes the processor to reboot. (Jumper -B must be removed when B is inserted.)
1A, 2A, 3A	These three jumpers are inserted to make the 20 mA current loop receiver active. (Jumpers 1P and 2P must be removed when 1A, 2A, and 3A are inserted.)
1P, 2P	These jumpers are inserted to make the 20 mA current loop receiver passive. (Jumpers 1A, 2A, and 3A must be removed when 1P and 2P are installed.)
4A, 5A	Inserted to make the 20 mA current loop transmitter active. (Jumpers 3P and 4P must be removed when 4A and 5A are inserted.)
3P, 4P	Inserted to make the 20 mA current loop transmitter passive. (Jumpers 4A and 5A must be removed when 3P and 4P are inserted.)
$\overline{EF}$	Jumper is removed to enable the error flags to be read in the high byte of the receiver buffer.
M, M1	These are test jumpers used during the manufacture of the module. They are not defined for field use.

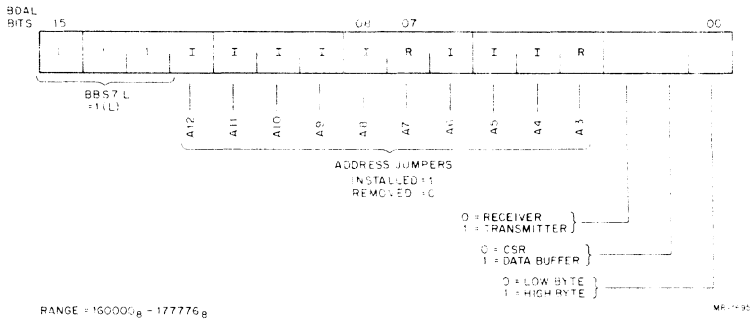

Figure 2 DLV11-F Addressing

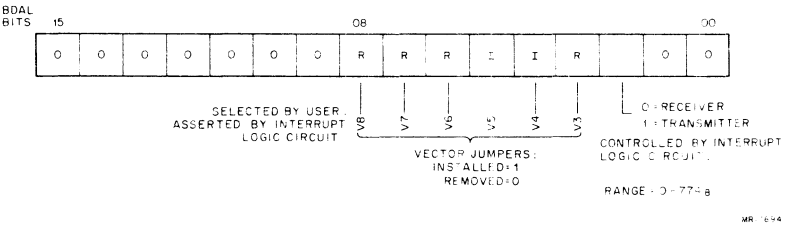

Figure 3 DLV11-F Interrupt Vectors

Baud Rate Selection

The DLV11-F allows the user to configure jumpers T0–T3 and R0–R3 for the transmit baud rate and the receiver baud rate as shown in Table 3.

Data Bit Selection

The number of data bits being transmitted or received by the DLV11-F is user-selectable by installing or removing jumpers 1 and 2. The specific number of data bits as controlled by the configuration of jumpers 1 and 2 is shown in Table 4.

Table 3 DLV11-F Baud Rate Selection

Program Control Receive Jumpers Transmit Jumpers	Bit 15 R3 T3	Bit 14 R2 T2	Bit 13 R1 T1	Bit 12 R0 T0	Bit 11*	Baud Rate
	I	I	I	I		50
	I	I	I	R		75
	I	I	R	I		110
	I	I	R	R		134.5
	I	R	I	I		150
	I	R	I	R		300
	I	R	R	I		600
	I	R	R	R		1200
	R	I	I	I		1800
	R	I	I	R		2000
	R	I	R	I		2400
	R	I	R	R		3600
	R	R	I	I		4800
	R	R	I	R		7200
	R	R	R	I		9600
	R	R	R	R		19200

I = Jumper inserted = program bit cleared
R = Jumper removed = program bit set

*Bit 11 of the XCSR (write-only bit) must be set in order to select a new baud rate under program control. Also, jumper PB must be inserted to enable baud rate selection under program control.

Table 4 DLV11-F Data Bit Selection

Jumpers		Number of Data Bits
2	1	
I	I	5
I	R	6
R	I	7
R	R	8

Factory Configuration

The user has the option to reconfigure any of the jumpers so that the module will meet his requirements. Therefore, the factory-configuration as shipped is shown in Table 5 to assist the user in determining what changes are required.

Table 5 DLV11-F Factory Jumper Configuration

Jumper Designation	Jumper State	Function Implemented
A3	R	Jumpers A3 through A12 implement device address 17756X. The least significant octal digit is hardwired on the module to address the four device registers as follows: X = 0 RCSR X = 2 RBUF X = 4 XCSR X = 6 XBUF
A4	I	
A5	I	
A6	I	
A7	R	
A8	I	
A9	I	
A10	I	
A11	I	
A12	I	
V3	R	This jumper selection implements interrupt vector 60_8 for receiver interrupts and 64_8 for transmitter interrupts.
V4	I	
V5	I	
V6	R	
V7	R	
V8	R	
R0	R	The module is configured to receive at 110 baud.
R1	R	
R2	I	
R3	I	
T0	I	The transmitter is configured for 9600 baud if split speed operation is used.
T1	R	
T2	R	
T3	R	
BG	I	Break generation is enabled.
P	R	Parity bit is disabled.
$\overline{E}$	R	Parity type is not applicable when P is removed

Table 5 DLV11-F Factory Jumper Configuration (Cont)

Jumper Designation	Jumper State	Function Implemented
1	R	Operation with 8 data bits per character.
2	R	
PB	R	Programmable baud rate function disabled.
C	I	Common speed operation enabled.
C1	I	
S	R	Split speed operation disabled.
S1	R	
H	I	Halt on framing error enabled.
B	R	Boot on framing error disabled.
1A	I	The 20 mA current loop receiver is configured as an active receiver.
2A	I	
3A	I	
1P	R	
2P	R	
4A	I	The 20 mA current loop transmitter is configured for active operation.
5A	I	
3P	R	
4P	R	
$\overline{EF}$	I	Error flags are disabled.
MT	R	Maintenance bit disabled.
M	R	Factory test jumpers. Not defined for field use.
M1	R	

Registers

The word format for the DLV11-F RCSR is shown in Figure 4 and functionally described in Table 6.

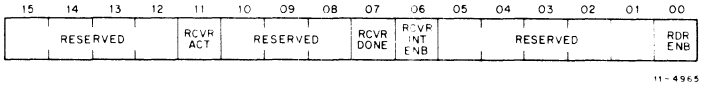

Figure 4 DLV11-F RCSR Word Format

Table 6 DLV11-F RCSR Bit Assignments

Bit	Name	Description
15–12	Not Used	Reserved for future use.
11	RCVR ACT (Receiver Active)	When set, this bit indicates that the DLV11-F interface receiver is active. The bit is set at the center of the start bit, which is the beginning of the input serial data from the device and is cleared by the leading edge of RDONE H. Read-only bit; cleared by INIT or by RCVR DONE (bit 7).
10–8	Not Used	Reserved for future use.
7	RCVR DONE (Receiver Done)	This bit is set when an entire character has been received and is ready for transfer to the processor. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 6) is also set. Read-only bit.
6	RCVR INT ENB (Receiver Interrupt Enable)	When set, allows an interrupt sequence to start when RCVR DONE (bit 7) sets. Read/write bit; cleared by INIT.
5–1	Not Used	Reserved for future use.

Table 6 DLV11-F RCSR Bit Assignments (Cont)

Bit	Name	Description
0	RDR ENB (Reader Enable)	When set, this bit advances the paper tape reader in DIGITAL-modified TTY units (LT33-C, LT35-A, C) and clears the RCVR DONE bit (bit 7). This bit is cleared at the middle of the start bit, which is the beginning of the serial input from an external device. Also cleared by INIT. Write-only bit.

NOTE
INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-F RBUF register is shown in Figure 5 and functionally described in Table 7.

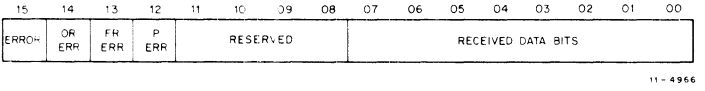

Figure 5 DLV11-F RBUF Word Format

Table 7 DLV11-F RBUF Bit Assignments

Bit	Name	Description
15	ERROR	Used to indicate that an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes error to set. This bit is not connected to the interrupt logic.

Table 7 DLV11-F RBUF Bit Assignments (Cont)

Bit	Name	Description
		Read-only bit; cleared by removing the error-producing condition.
		NOTE Error indications remain present until the next character is received, at which time the error bits are updated. INIT clears the error bits.
14	OR ERR (Overrun Error)	When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Read-only bit. Cleared by INIT.
13	FR ERR (Framing Error)	When set, indicates that the character that was read had no valid stop bit. Read-only bit. Cleared by INIT.
12	P ERR (Parity Error)	When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected. Read-only bit. Cleared by INIT.
11–8	Not Used	Reserved for future use.
7–0	RECEIVED DATA BITS	Holds the character just read. If less than eight bits are selected, then the buffer is right-justified into the least significant bit positions. In this case, the higher unused bit or bits are read as 0s. Read-only bits; not cleared by INIT.
		NOTE INIT = LSI-11 bus BINIT signal assertion.

The word format for the DLV11-F XCSR register is shown in Figure 6 and functionally described in Table 8.

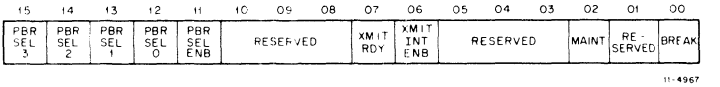

Figure 6 DLV11-F XCSR Word Format

Table 8 DLV11-F XCSR Bit Assignments

Bit	Name	Description
15–12	PBR SEL (Programmable Baud Rate Select)	When set, these bits choose a baud rate from 50–9600 baud. See Table 3. Write-only bits.
11	PBR ENB (Programmable Baud Rate Enable)	This bit must be set in order to select a new baud rate indicated by bits 12 to 15. Write-only bits.
10–8	Not Used	Reserved for future use.
7	XMIT RDY (Transmitter Ready)	This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 6) is also set.
6	XMIT INT ENB (Transmitter Interrupt Enable)	When set, allows an interrupt sequence to start when XMIT RDY (bit 7) is set. Read/write bits; cleared by INIT. (See Note.)
5–3	Not Used	Reserved for future use.

Table 8 DLV11-F XCSR Bit Assignments (Cont)

Bit	Name	Description
2	MAINT	Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed when common speed operation is enabled. Read/write bit; cleared by INIT.
1	Not Used	Reserved for future use.
0	BREAK	When set, transmits a continuous space to the external device. Read/write bit; cleared by INIT.

NOTE

When clearing an interrupt enable bit, first set the appropriate processor status word bit = 1. After the interrupt enable bit at the module is cleared, the processor may be returned to its normal priority.

The word format for the DLV11-F XBUF register is shown in Figure 7 and functionally described in Table 9.

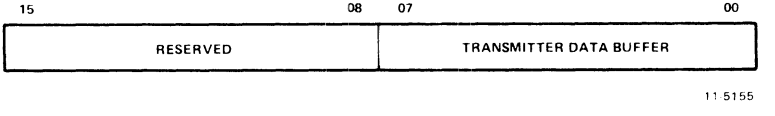

Figure 7 DLV11-F XBUF Word Format

Table 9 DLV11-F XBUF Bit Assignments

Bit	Name	Description
15–8	Not Used	Not defined. Not necessarily read as 0s.
7–0	TRANSMITTER DATA BUFFER	Holds the character to be transferred to the external device. If less than eight bits are used, the character must be loaded so that it is right-justified into the least significant bits. Write-only bits. Not necessarily read as 0s.

Installation

Prior to installing the DLV11-F on the backplane, first establish the desired priority level to determine the backplane slot in which the module will be installed. Then, check that module configuration jumpers are configured as required for your application. Connection to the peripheral device is via an optional data interface cable. Cables are listed below.

Application	Cable Type*
EIA Interface	BC01V-X or BC05C-X Modem Cable
20 mA Current Loop	BC05M-X Cable Assembly

Interfacing EIA-Compatible Devices

The DLV11-F supports only the data leads of EIA-compatible devices. It uses a BC05C modem cable to interface devices such as the Teletype® Model 37 Teletypewriter and the Bell Data Set Model 103 (in auto mode). The DLV11-F's EIA "data leads only" interface circuit is shown in Figure 8 and the jumpers are shown in Figure 1.

*X = Length in feet. Standard length is 25 feet.

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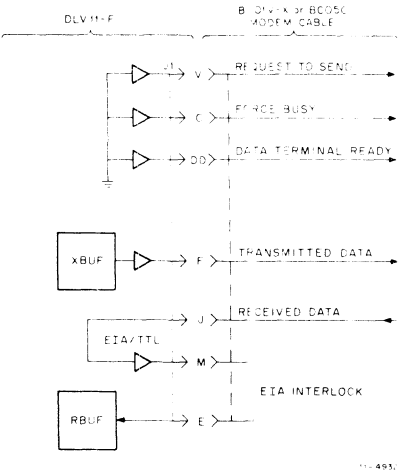


Figure 8 Data Leads Only Interface

Interfacing 20 mA Current Loop Devices with the DLV11-F
When interfacing with 20 mA current loop devices, the BC05M cable assembly provides the correct connections to the 40-pin connector on the DLV11-F. The peripheral device end of the cable is terminated with a Mate-N-Lok connector that is pin-compatible with all DIGITAL 20 mA serial interface terminals.

The interface circuits provided by the BC05M cable and the associated DLV11-F jumpers are shown in Figures 9, 10, and 11.

NOTE
When the DLV11-F is used with teletypewriter devices, a 0.005 μF capacitor must be installed. (See Figure 1.)

FUNCTIONAL DESCRIPTION

General
Major functions contained on the DLV11-F are shown in Figure 12. Communications between the processor and the DLV11 are executed via programmed I/O operations or interrupt-driven routines.

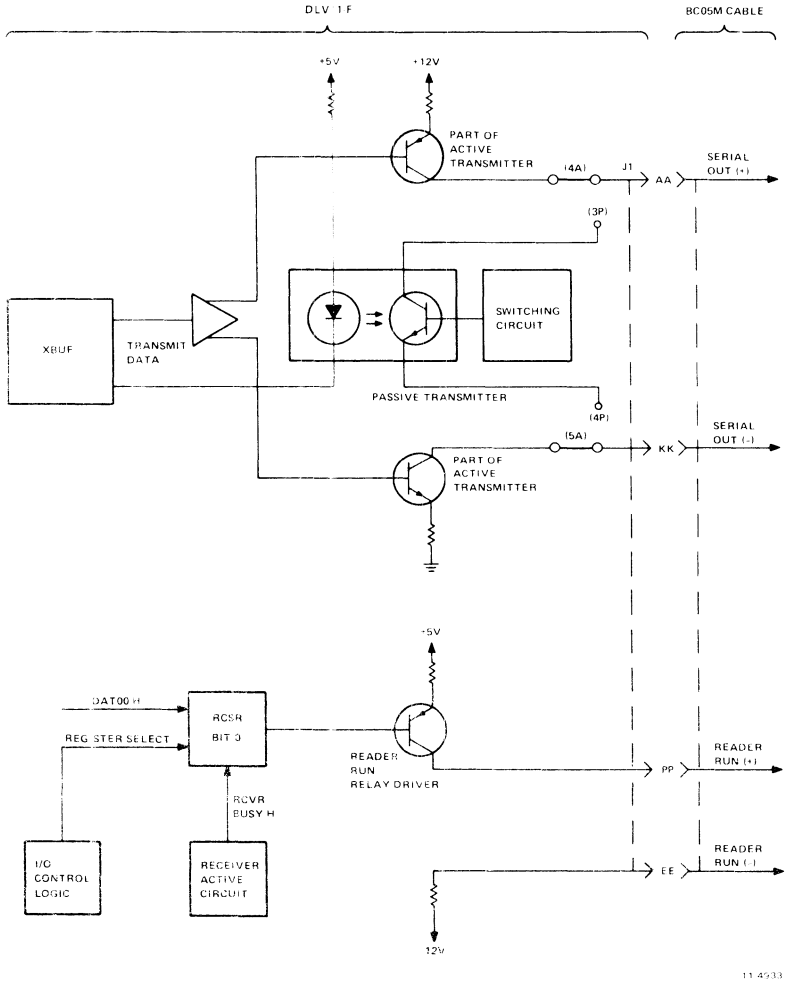


Figure 9 20 mA Transmitter and Reader Run Circuits

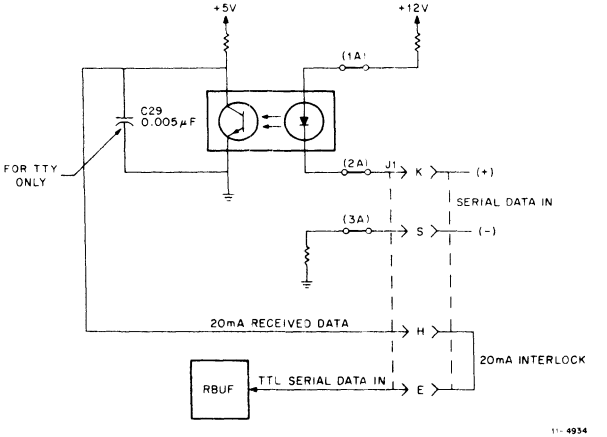


Figure 10 Active Receive 20 mA Current Loop

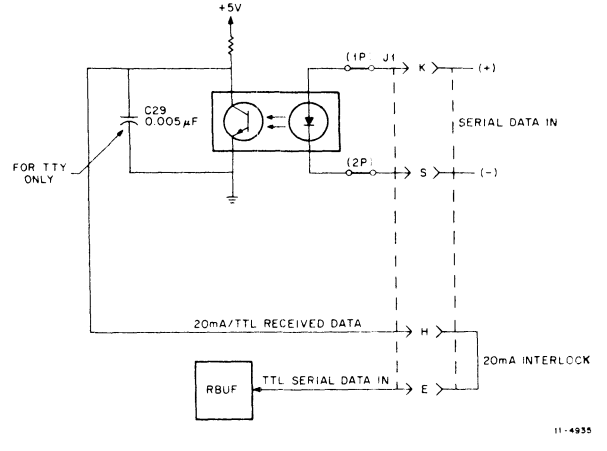


Figure 11 Passive Receive 20 mA Current Loop

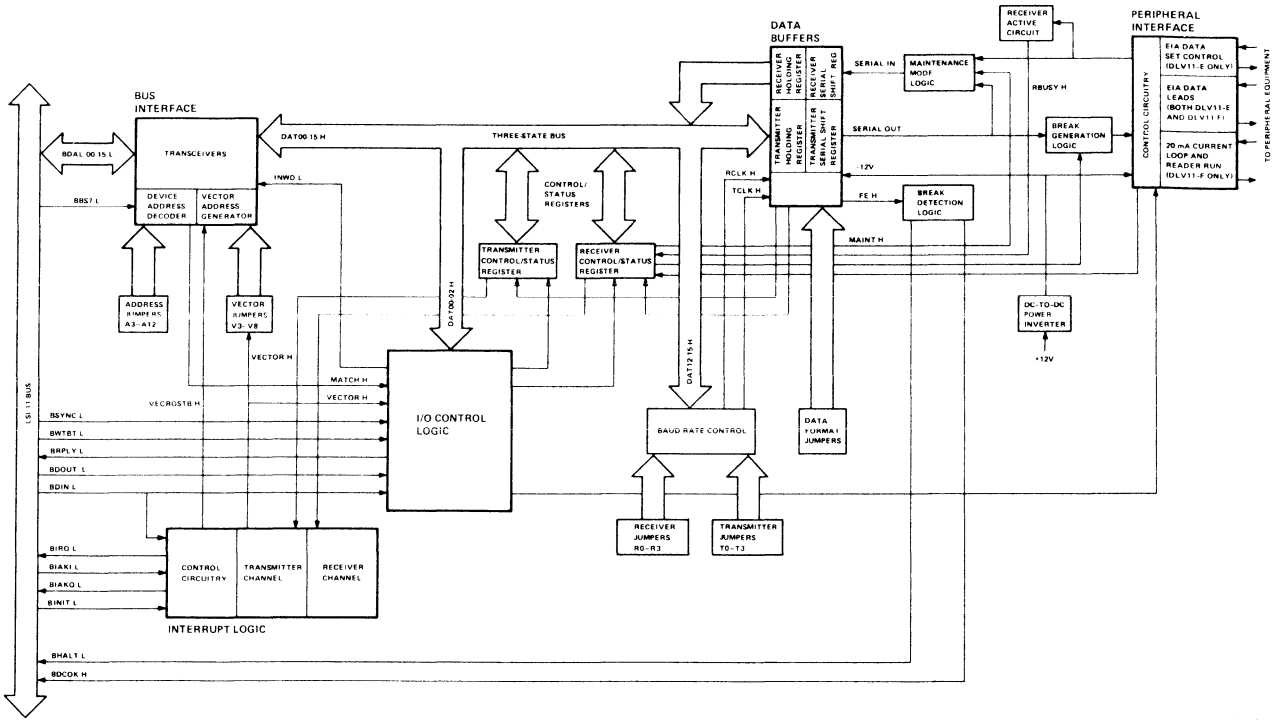


Figure 12 DLV11-F Asynchronous Line Interface Logic Block Diagram

Bus Interface

The bus interface circuit signal levels consist of data moving between the LSI-11 bus and the module's internal tri-state bus. It decodes the device address and produces an address match (MATCH H) signal, and it places interrupt vectors on the LSI-11 bus. The bus interface receives from the LSI-11 bus unless it is switched to transmit to the LSI-11 bus. The interrupt logic can cause the bus interface to transmit either a transmitter or receiver interrupt vector and the I/O control logic can cause the bus interface to transmit or receive data to or from the LSI-11 bus.

The bus interface receives LSI-11 bus lines BDAL00 L through BDAL15 L and places them on the module's tri-state bus. If BBS7 L is asserted, the circuit decodes BDAL03 L through BDAL12 L and asserts MATCH H. Jumpers A3–A12 are configured to allow the option to respond to specific device register addresses. Jumpers V3–V8 select the options' interrupt vector.

I/O Control Logic

When the I/O control logic receives MATCH H from the bus interface, it decodes tri-state bus lines DAT00 H through DAT02 H and selects the addressed device register. The I/O control logic exchanges bus control signals with the processor to perform input and output data transfers. During an interrupt transaction, VECTOR H from the interrupt logic causes the circuit to assert BRPLY L in response to BDIN L. During data transactions, the I/O control logic asserts INWD L to switch the bus interface transceivers from receiving to transmitting.

Control/Status Registers

The receiver control/status register (RCSR) and the transmitter control/status register (XCSR) are enabled by selection signals from the I/O control logic. The CSRs are byte addressable for reading status bits or writing control bits.

Data Buffers

The receiver buffer (RBUF) and transmitter buffer (XBUF) provide double-buffering in that one byte of data can be held while another byte is entering or exiting. This allows asynchronous, full-duplex operation. Data is handled in the low byte of the registers. The buffer control circuitry places receiver buffer error flag bits in the high byte of the RBUF. It also sends a status bit to the RCSR and a framing error bit (FE H) to the break logic.

Receiver Active Circuit

This circuit monitors the received serial data line and sets a status bit (RCVR ACT) as soon as the RBUF begins receiving data. It clears the bit when a full character of data has been received.

Interrupt Logic
The DLV11-F can generate transmitter interrupts. If the XBUF is ready to serialize another character of data and the transmitter interrupt enable bit is set in the XCSR, the interrupt logic requests to interrupt the processor (by asserting BIRQ L) If the processor acknowledges via the BIAKI/BIAKO daisy-chain, the interrupt logic asserts VECTOR H and VECRQSTB H. These signals cause the bus interface to place the transmitter function interrupt vector address on the LSI-11 bus.

The module also can request a receiver interrupt if the RBUF has received a character and the receiver interrupt bit is set in the RCSR. When the interrupt request is acknowledged, the interrupt logic asserts VECTOR H. VECTOR H causes the bus interface circuit to place the receiver function interrupt vector address on the LSI-11 bus. (VECRQSTB H is used only for a transmitter interrupt.)

The interrupt acknowledge daisy-chain (BIAKI/BIAKO) passes through both the receiver and transmitter sections of the interrupt logic. It goes through the receiver section first, thereby giving the receiver channel priority over the transmitter channel.

Baud Rate Control
The baud rate control establishes the speed at which the data buffers handle serial data. It produces clock signals by dividing a crystal oscillator frequency by an amount selected by jumpers or the program. The circuit can be jumpered to generate either independent transmitter and receiver clocks (split speed operation) or a common clock (common speed operation).

When the programmable baud rate enable bit is set in the XCSR, the baud rate control decodes tri-state bus lines DAT12 H through DAT15 H. These bits control the receive baud rate in split speed operation and both transmit and receive baud rate in common speed operation. When programmable baud rate is not enabled, the baud rates are controlled by jumpers. In split speed operation, jumpers R0–R3 control the receive baud rate and jumpers T0–T3 control the transmit baud rate. In common speed operation, R0–R3 control both baud rates.

The circuit also has provisions for a user-supplied external clock.

Break Logic
A break signal is a continuous spacing condition on the serial data line. If the break bit is set in the XCSR, the module will transmit a break signal to the peripheral device (normally another processor). If the module receives a break signal from the peripheral device (normally a console device), the RBUF control circuitry interprets the absence of stop bits as

a framing error. The circuit can be jumpered to ignore the framing error, to place the processor in the halt mode, or to cause the processor to reboot. The break logic asserts BHALT L to halt the processor. It negates BDCOK H to reboot.

Maintenance Mode Logic
The modules can check out their data paths up to (but not including) the peripheral interface circuit by looping the XBUF's serial output back to the RBUF's serial input. Data from the LSI-11 bus still goes to the peripheral device, but no data is received from the peripheral in this maintenance mode. The program can compare received (looped) data with transmitted data to check for errors. The maintenance mode is entered by setting the maintenance bit in the XCSR.

Peripheral Interface
This circuit can be jumpered to support either EIA-level data leads (no modem control) or 20 mA current loop modes. When interfacing EIA-level data leads ("data leads only" operation), request to send, force busy, and data terminal ready are held continuously true by separate EIA drivers. No modem control signals are received.

In the current loop mode of operation, the circuit uses optical isolators to interface TTL to 20 mA current loops. Operation is jumper-selectable for either active or passive operation of the transmitter and receiver circuitry.

The peripheral interface also produces a reader run current to advance the paper tape reader on a peripheral equipped with a reader run relay. This is controlled by the reader enable bit in the DLV11-F's RCSR.

DC-to-DC Power Inverter
The power inverter uses the +12 V from the backplane to produce -12 V for the peripheral interface and data buffer circuitry. It consists of an oscillator, rectifier, inductive charge pump, and a zener regulator.

DLV11-J FOUR ASYNCHRONOUS SERIAL INTERFACES

GENERAL

The DLV11-J is a 4-channel asynchronous serial line unit used to interface peripheral equipment to an LSI-11 bus. The interface transmits and receives data from the peripheral device over Electronics Industry Association (EIA) "data leads only" lines which do not use control lines. The module can be used with 20 mA current loop devices (with "reader-run" capabilities) when the DLV11-KA option is installed. With a DLV11-J interface, the processor can communicate with a local terminal such as a console teleprinter, a remote terminal via data sets and private line, public switched telephone facilities, or another local or remote processor.

FEATURES

- Four independent serial line channels with unique bus device and vector address assignments.
- Serial line compatibility with EIA RS-232C and RS-423, AS-422 or 20 mA current loop (depending on channel configuration and cable selection).
- All channels may be configured for independent:

  Crystal-controlled baud rates: 150, 300, 600, 1200, 2400, 4800, 9600, 19,200 or 38,400 bits per second. When using the DLV11-KA option, 110 bit/s rate is available.

  Character formats: 7 or 8 data bits, 1 or 2 stop bits, parity or no parity, and even or odd parity.
- Channel 3 may be configured as a dedicated console device interface.
- Channel 3 break condition response of bootstrap, halt (console emulator mode) or no response.
- Hardware and software equivalent to four DLV11s.

SPECIFICATIONS

Identification	M8043
Size	Double

Power	+5 V ± 5% at 1.0 A +12 V ± 3% at 0.25 A
Bus Loading	
AC	1
DC	1

CONFIGURATION

General

The DLV11-J device and vector addressing, serial word formats, baud rates, interface type, etc. are selected by installing and/or removing jumpers. Wire-wrap posts are provided on the module for this purpose. The module is factory-configured and ready to use in most user applications. However, as a system requires different device register addresses and interrupt vectors or operations, the module may be reconfigured. The DLV11-J module is factory-configured for the following operations:

- Base address = 176500
- Base vector address = 300
- Channel 3 enabled as the console device (device addresses 177560–177566 and vector addresses 60 and 64).
- Channel 3 halt on break enabled
- Baud rates (transmit and receive are identical):

  Channels 0, 1 and 2 = 9.6K baud

  Channel 3 = 300 baud

- Data/parity/stop bit format (all channels):

  Eight data bits
  One stop bit
  No parity

- Serial line signal interface levels (all channels) compatible with both EIA RS-232C and RS-423, simultaneously (slew rate = 2 μs)

Figure 1 gives jumper and pad locations on the DLV11-J module and Table 1 gives a summary of the module's factory configuration.

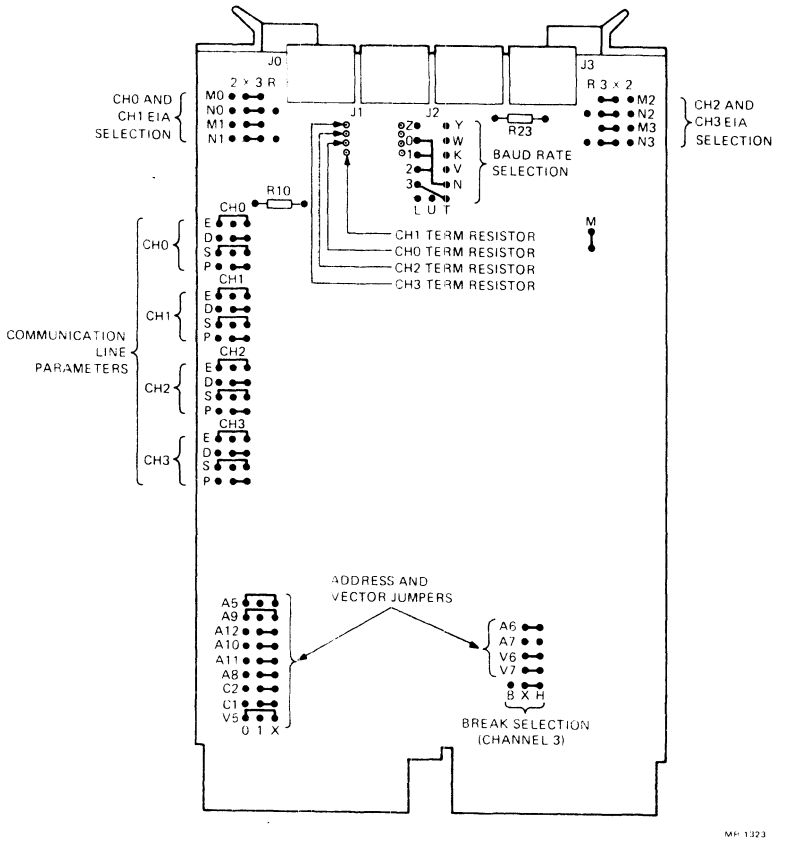


Figure 1 DLV11-J Jumper Locations

Table 1 Factory Jumper Configuration

Label	Standard Configuration	Function Implemented	
A12 A11 A10 A9 A8 A7 A6 A5	X to 1 X to 1 X to 1 X to 1 X to 0 R I X to 0	This arrangement of jumpers A5–A12 implements the octal base device address 1765XX, which is the assigned address for channel 0 RCSR. The least significant digit is decoded on the module during operation to address one of four SLU device registers as follows X = 0, RCSR X = 2, RBUF X = 4, XCSR X = 6, XBUF	
C1 C2	X to 1 X to 1	These jumpers are used to enable channel 3 for console operation. Base address must be 176500 (factory-configured), 176540, or 177500 for the console.	
(Break response)	X to H	This jumper determines channel 3 break response. The board is configured for halt (console emulator mode) on break condition.	
V7 V6 V5	I I X to 0	This arrangement of jumpers V5–V7 implements the octal "base" vector of 300 with channel 3 at 60 and 64.	
E D S P	X to 0 X to 1 X to 0 X to 1	Odd parity 8 data bits 1 stop bit Parity inhibited	These jumpers determine the word format used by the channel. All channels are configured the same at the factory.
0 1 2 3	0 to N 1 to N 2 to N 3 to T	9.6K baud 9.6K baud 9.6K baud 300 baud	These jumpers determine the baud rate of the serial line channel for same baud rate daisy-chain wire-wraps.

Table 1 Factory Jumper Configuration (Cont)

Label	Standard Configuration	Function Implemented
N0–3 M0–3	X to 3 X to 3	These jumpers determine the EIA standard compatibility of the channel. All channels are set at the factory to be compatible to both EIA RS-423 and RS-232C simultaneously.
R10	22 kΩ	Channels 0 and 1, slew rate of 2 μs (used when configured for EIA RS-423/RS-232C)
R23	22 kΩ	Channels 2 and 3, slew rate of 2 μs (used when configured for EIA RS-423/RS-232C)

Device Registers

The DLV11-J contains 16 device registers that can be individually addressed by the program. The four device registers provided for each of the SLU channels (0 through 3) are:

Receive Control/Status Register (RCSR)
Receive Buffer (RBUF)
Transmit Control/Status Register (XCSR)
Transmit Buffer (XBUF)

Wire-wrap jumpers are configured to establish a "base" address (BA) for the module. This base address is the channel 0 RCSR address. The device address format is shown in Figure 2. The remaining device addresses follow through 16 (total) contiguous word addresses; however, it is possible to independently dedicate the last four addresses (channel 3) to a console device. When configured for console device operation, the channel's device register addresses will be 177560–177566. For console operation, the board's base address must be one of the following:

176500 (factory-configured)
176540
177500

The floating address configurations are listed in Table 2 and the factory or standard configuration addresses are listed in Table 3.

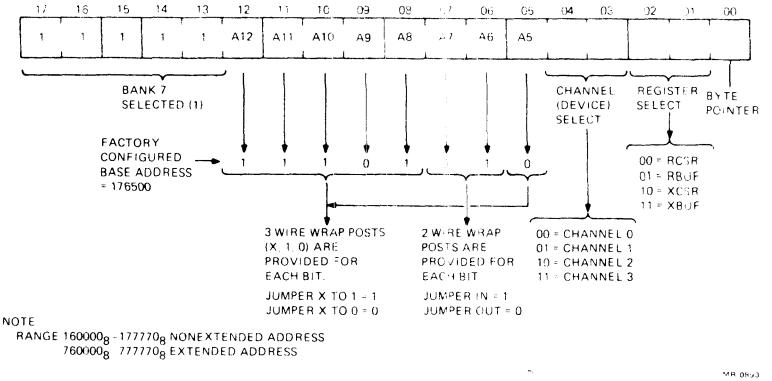


Figure 2 Channel 0 RCSR Address Format

Table 2 Address Assignments (with Console Selected)

Address	Device Register	Associated Vector
	Channel 0	
Module Base Address (BA)	RCSR	Module Base Vector (BV)
BA+2	RBUF	
BA+4	XCSR	BV+4
BA+6	XBUF	
	Channel 1	
BA+10	RCSR	BV+10
BA+12	RBUF	
BA+14	XCSR	BV+14
BA+16	XBUF	
	Channel 2	
BA+20	RCSR	BV+20
BA+22	RBUF	
BA+24	XCSR	BV+24
BA+26	XBUF	

Table 2 Address Assignments (with Console Selected) (Cont)

Address	Device Register	Associated Vector	
	Channel 3*		
177560	RCSR	60	Console Selected
177562	RBUF		
177564	XCSR		
177566	XBUF	64	

*Channel 3 is used as a console device.

Table 3 Factory or Standard Addresses

Address	Register	Vector	
176500	RCSR		
176502	RBUF	300	Channel 0
176504	XCSR		
176506	XBUF	304	
176510	RCSR		
176512	RBUF	310	Channel 1
176514	XCSR		
176516	XBUF	314	
176520	RCSR		
176522	RBUF	320	Channel 2
176524	XCSR		
176526	XBUF	324	
176560	RCSR		
176562	RBUF	60	Channel 3
176564	XCSR		
176566	XBUF	64	

Four word formats, one for each device register within a channel, are shown in Figure 3 and described in Table 4. These word formats are typical of all channels on the DLV11-J module.

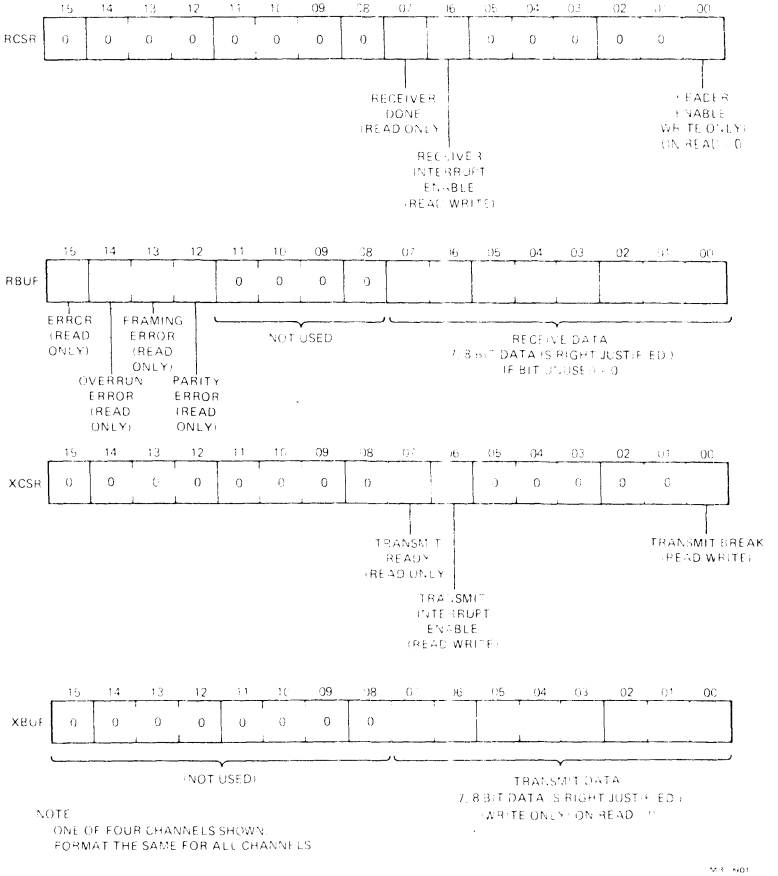


Figure 3 DLV11-J Device Register Formats

Table 4 DLV11-J Word Formats

Bit	Description
	Receive Control/Status Register
8/15	Not used. On read = 0.
7	Receiver Done. Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF is read, when BINIT L signal goes true (low), or when reader enable bit is set. Read-only bit. If receiver interrupt enable (bit 6) is set, the setting of receiver done starts an interrupt sequence.
6	Receive Interrupt Enable. Set under program control when it is desired to generate a receiver interrupt request (when a character is ready for input to the processor signified by bit 7 being set). Cleared under program control or by the BINIT signal. Read/write bit.
1–5	Not used. On read = 0.
0	Reader Enable. Setting this bit advances the paper tape reader on an LT33 terminal one character at a time. Setting of this bit clears receiver done (bit 7). Write-only bit. The DLV11-KA 20 mA current loop option is required for operation of this bit.
	Receive Buffer
15	Channel Error Status. Logical OR of bits 14, 13, and 12. Read-only bit.
14	Overrun Error. When set, indicates that the reading of the previously received character was not completed (receiver done not cleared) prior to receiving a new character. Cleared by BINIT signal. Read-only bit. **NOTE** When "back-to-back" characters are received, one full character time is allowed from the time instant receiver done (bit 7) is set to the occurrence of an overrun error.

Table 4 DLV11-J Word Formats (Cont)

Bit	Description
13	Framing Error. When set, indicates that the character read had no valid stop bit. Cleared by BINIT signal. Read-only bit.
12	Parity Error. When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no-parity operation is configured for the channel. Read-only bit. **NOTE** Error bits remain valid until the next character is received, at which time the error bits are updated.
8–11	Not used. On read = 0.
0–7	Data bits. Contains seven or eight data bits in a right-justified format. Bit 7 = 0 when 7 data bits are enabled. Read-only bits.
	Transmit Control/Status Register
8–15	Not used. On read = 0.
7	Transmit Ready. Set when XBUF is empty and can accept another character for transmission. It is also set by INIT during the power-up sequence or during a reset instruction. Read-only bit. If transmitter interrupt enable (bit 6) is set, the setting of transmit ready will start on interrupt sequence.
6	Transmit Interrupt Enable. Set under program control when it is desired to generate a transmitter interrupt request (when transmitter is ready to accept a character for transmission). The bit is cleared under program control, during power-up sequence, or reset instruction. Read/write bit.
1–5	Not used. On read = 0.

Table 4 DLV11-J Word Formats (Cont)

Bit	Description
0	Transmit Break. Set or reset under program control. When set, a continuous space level is transmitted. However, transmit done and transmit interrupt can still operate, allowing software timing of break. When not set, normal character transmission can occur. Cleared by BINIT. Read/write bit.
	Transmit Buffer
8–15	Not used. On read = 0.
0–7	Data bits. Contains seven or eight right-justified data bits. Loaded under program control for serial transmission.

Interrupt Vectors

Two interrupt vectors are provided for each of the four SLU channels (eight vectors total). The procedure for configuring the vectors is similar to that used when configuring the base device register address; the configured base vector is the channel 0 receiver interrupt vector. Each interrupt vector references two word locations in memory (the program counter address and the processor status word). Hence, sequential vectors appear in increments of four.

The module is factory-configured with an interrupt vector base of 300. However, it is also configured for channel 3 operation as the console device; thus, channel 3 will automatically have interrupt vectors of 60 and 64. The vector format is shown in Figure 4 and a summary of vector jumper configurations is provided in Table 5. Table 6 gives a list of the factory-configured vector assignments.

Interrupt priority within the DLV11-J module is structured as follows:

Interrupt Priority	Requesting Function
1 (highest)	Channel 0, receiver
2	Channel 1, receiver
3	Channel 2, receiver
4	Channel 3, receiver
5	Channel 0, transmitter
6	Channel 1, transmitter
7	Channel 2, transmitter
8 (lowest)	Channel 3, transmitter

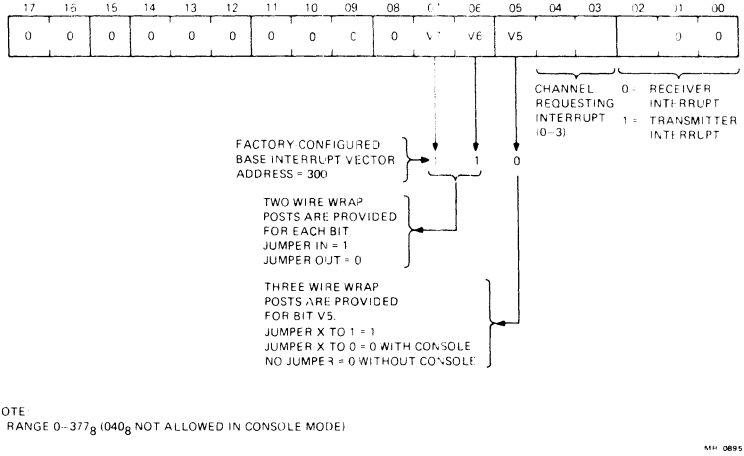


Figure 4 Interrupt Vector Format

Table 5 Summary of Vector Jumper Configurations

Label	Logical 1	Logical 0
V7	Jumper installed.	Jumper removed.
V6	Jumper installed.	Jumper removed.
V5	Jumper installed from wire-wrap post X to 1.	Console not selected: jumper removed. Console selected: jumper installed from wire-wrap post X to 0.

Table 6 Vector Assignments (with Console Selected) (Factory Configured)

Standard Address		Interrupt Vector
300 [Module Base Vector (BV)]		Channel 0, Receiver
304 (BV+4)		Channel 0, Transmitter
310 (BV+10)		Channel 1, Receiver
314 (BV+14)		Channel 1, Transmitter
320 (BV+20)		Channel 2, Receiver
324 (BV+24)		Channel 2, Transmitter
60	Console Selected	Channel 3, Receiver
64		Channel 3, Transmitter

NOTES

1. Module is factory-configured for channel 3 as a console device.
2. All addresses are in octal notation.

Character Formats

Each of the four channels may be independently configured for various character formats. When a character format is configured (by wire-wrap jumpers) for a channel, both the transmitter and receiver will use the same format. The character may contain:

7 or 8 data bits
1 or 2 stop bits
Parity or no parity
Even or odd parity

Configuration instructions for determining the character formats of each channel are shown in Table 7.

Baud Rates

Each channel can be configured for baud rates ranging from 150 to 38400 bits per second. One baud rate clock input wire-wrap pin is provided for each channel (0 through 3). Both the transmitter and receiver for a given channel must operate at the same baud rate; split baud rate operation cannot be configured. Configure baud rates by connecting a jumper from the appropriate baud rate generator output wire-wrap pin to the clock input pin of the channel. One jumper is required for each channel. When configuring the same baud rate for more than one channel, the wire-wrap pins may be daisy-chained. Table 8 lists the possible baud rates for each channel and their associated labels.

Table 7 Character Format Jumpers

Label	Channel Parameter	Wire-wrap Connection X to 0	X to 1	Comments
D	No. of data bits	7 bits	8 bits	LSB transmitted first
S	No. of stop bits	1 bit	2 bits	
P	Parity inhibit	Parity generation and detection enabled	Parity bit deleted; parity error = 0	
E*	Even parity enabled	Odd parity expected	Even parity expected	Only when P=0

* Jumper must be installed to 0 or 1 even if no parity is selected.

Table 8 Baud Rate Generator Outputs

Wire-Wrap Pin Label	Baud Rate (Bits/Second)
U	150
T	300
V	600
W	1,200
Y	2,400
L	4,800
N	9,600
K	19,200
Z	38,400

When using the DLV11-KA option, 110 bits/s operation is possible. A 110 baud rate clock generator circuit on the option will supply the DLV11-J module with the proper clock; no baud rate jumper is configured on the module for the desired channel.

Console Device Selection

Channel 3 of the DLV11-J module may be independently dedicated for console device operation. To accomplish this, the console select jumpers must be properly configured. Table 9 gives channel 3 configuration instructions. When configured for console operation, the device addresses are 177560–177566 and the interrupt vectors are 60 and 64.

Table 9 Summary of Console Selection Jumper Configurations

Label	Console Selected	Console Not Selected
C1	Install jumper from wire-wrap pins X to 1.	Install jumper from wire-wrap pins X to 0.
C2	Install jumper from wire-wrap pins X to 1.	Install jumper from wire-wrap pins X to 0.

Break Response

Channel 3 may be configured to either bootstrap, halt (console emulator mode), or have no response to a receive break condition. A bootstrap operation upon a receive break condition will cause the processor to execute the bootstrap program starting at the memory location defined

by the power-up mode jumpers of the processor. A halt operation upon a receive break condition will cause the processor to halt and the console octal debugging technique (ODT) microcode to be invoked. Configuration instructions are given on Table 10.

Table 10 Channel 3 Break Operation Jumper Summary

Break Operation Response	Jumper Connection
Boot*	Install jumper between wire wraps X to B.
Halt	Install jumper between wire wrap pins X to H.
No Response	No jumper installed.

*Do not send continual breaks to a system so configured, as it will cause continued reinitializing of any device on the bus.

Peripheral Interface Configuration

Each of the channels can be independently configured for serial line signal compatibility with EIA RS-423 (simultaneously RS-232C), RS-422, or 20 mA current loop devices. When using 20 mA current loop devices, the DLV11-KA option is required. Configuration instructions for each of the standards are listed in Table 11. Table 12 is used when configuring EIA RS-423 (RS-232C compatible) slew rates. Use this table in conjunction with Table 11.

FUNCTIONAL DESCRIPTION

General

The DLV11-J module is designed to interface peripheral devices that transmit and receive asynchronous serial data over EIA-compatible data lines or 20 mA current loops to the parallel LSI-11 bus. When configured, the module transmits and receives the specified EIA signal levels on the receive and transmit data lines of the cable. Also the module constantly asserts the data terminal ready signal.

When configured for 20 mA current loop operation (DLV11-KA option installed), the DLV11-J can support devices which contain program-controlled paper tape readers (such as DIGITAL's LT33 Teletypewriters or the ASR33 Teletypewriter with the LT33 modification kit.)

Table 11 Summary of Serial Channel Signal Level Configurations

Serial Channel Signal Level Modifiers	EIA RS-422	EIA RS-232C and RS-423	20 mA Current Loop (Using DLV11-KA)
M0–3 Jumper	Connect wire-wrap pins X and 2.	Connect wire-wrap pins X and 3.	Connect wire-wrap pins X and 3.
N0–3 Jumper	Connect wire-wrap pins X and 2.	Connect wire-wrap pins X and 3.	Connect wire wrap pins X and R for program-controlled paper tape reader.
Termination Resistor (one per channel)	Install a 100 Ω, 1/4 W, non-wire wound, fusible resistor.		
Wave-Shaping Resistor (one per channel pair; channel pairs 0 and 1; 2 and 3)		Install resistor from Table 12 (1/4 W non-wire wound).	
Fuse F1			Install 1.0 A Pico fuse

Table 12 EIA RS-423 and RS-232C Slew Rate Resistor Values

Baud Rate	R10 or R23
38.4 KB	22 kΩ
19.2 KB	51 kΩ
9.6 KB	120 kΩ
4.8 KB	200 kΩ
2.4 KB	430 kΩ
1.2 KB	820 kΩ
600	1 MΩ
300	1 MΩ
150	1 MΩ
110	1 MΩ

During operation, the module is required to convert data from parallel to serial and serial to parallel. To accomplish this, a universal asynchronous receiver/transmitter (UART) is employed. When performing this conversion, the UART must also alter the speed and character format for the data (to meet user-selected parameters). In addition, the UART creates error bits to allow the programmer to check data transmission for errors. A block diagram of the DLV11-J module is shown in Figure 5.

UART Operation

The DLV11-J module is equipped with four universal asynchronous receiver/transmitters, one for each channel. The UART chip is capable of parallel data transfers with the computer and serial data transfers with the peripheral device. User-selectable jumpers determine the character format used during transmission. The jumpers select:

7 or 8 data bits
1 or 2 stop bits
Parity or no parity
Even or odd parity

The receiver section performs serial-to-parallel conversion of data which will always appear right-justified in the receive data buffer. The start, stop, and parity bits are removed and error flags appended to the transmission as it enters the receive buffer. The error flags, when set, will not interrupt operation, but they are available to the programmer when reading the RBUF.

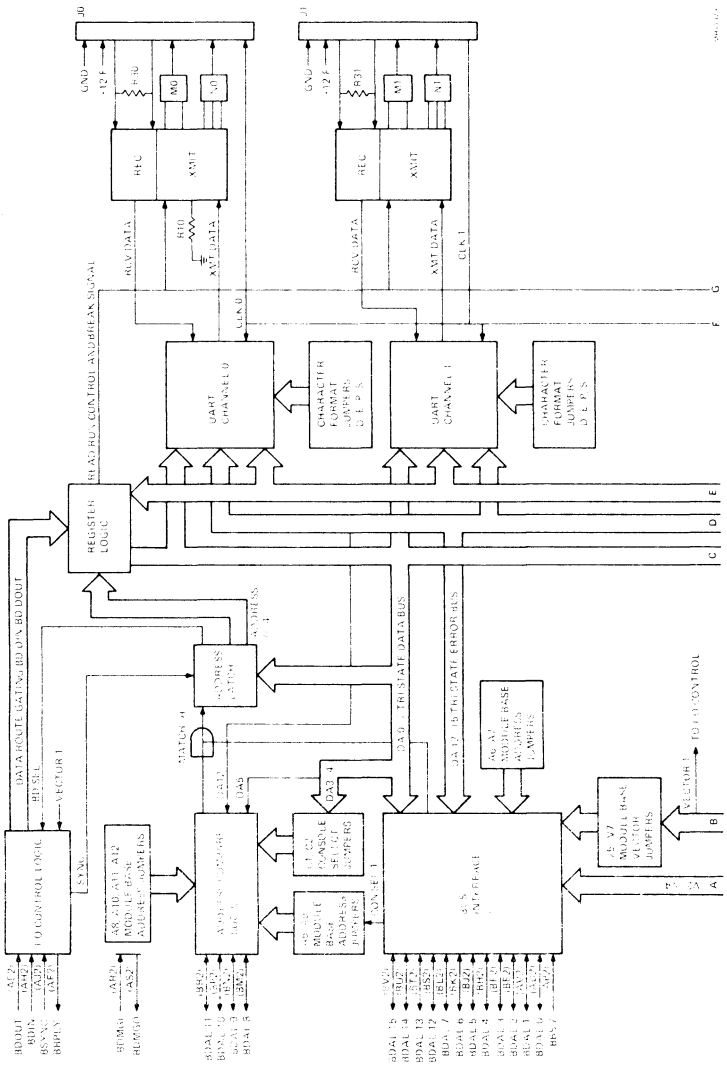


Figure 5 DLV11-J Block Diagram (Sheet 1 of 2)

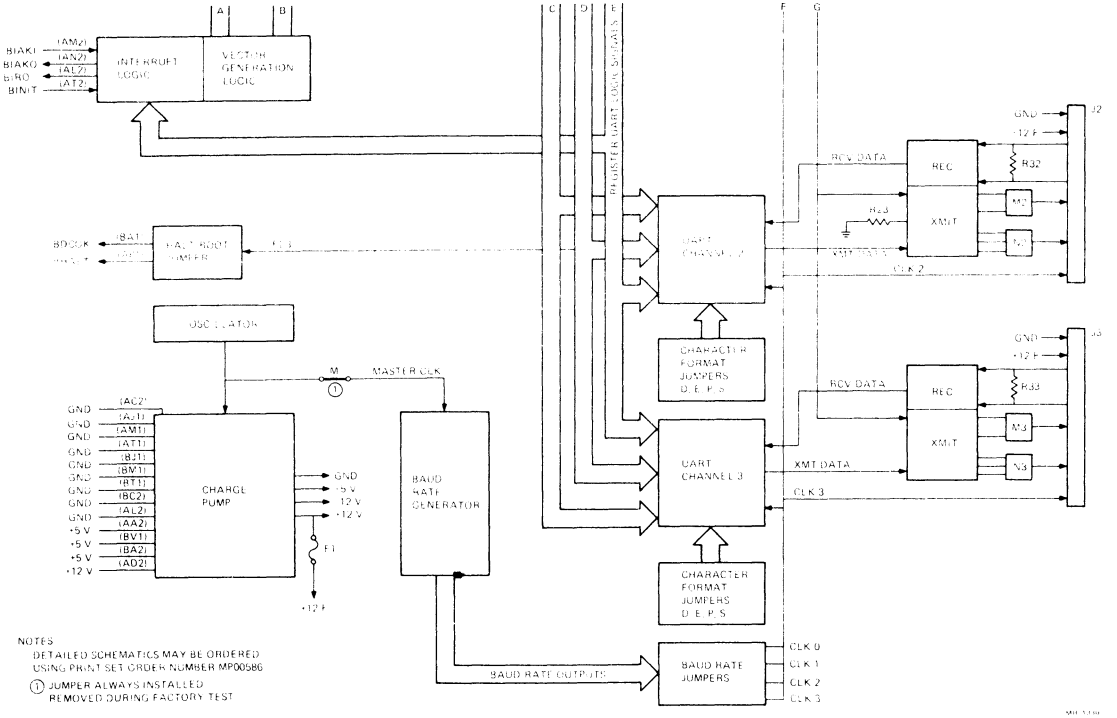


Figure 5 DLV11-J Block Diagram (Sheet 2 of 2)

The transmitter performs parallel to serial conversion of data provided by the LSI-11 bus. The character length, stop bit code, parity, and baud rate are identical to the receiver section of the SLU channel. The transmitter, however, appends the proper start, stop, and parity bits to the data before transmission.

Baud Rate Generator

The baud rate control circuit generates clock signals that control the speed at which the receive buffer (RBUF) and the transmit buffer (XBUF) move serial data. The circuit provides a common clock to both buffers of the channel.

The speed at which a channel will operate is configured by the selection of wire-wrap jumpers which supply the desired baud rate clock. The clock is developed by a crystal-controlled oscillator driving a frequency division chip. The outputs of the frequency division chip are connected to wire-wrap posts which may be selected when configuring the channel(s). If more than one channel is used for a particular baud rate, the clock may be daisy-chained between channels.

When 110 baud operation is desired, the DLV11-KA option must be used. This option provides the 110 clock to the channel via the peripheral device cable; no baud rate jumper may be configured on the module for the 110 baud channel.

I/O Control Logic

The I/O control logic directs data transfers between the computer and the DLV11-J module. The logic monitors the LSI-11 bus control lines to determine the type of data transfer to be executed (from the LSI-11 bus to the register logic for an output operation or from the register logic to the LSI-11 bus for an input operation). The following LSI-11 bus control lines are monitored by the I/O control logic during operation:

BSYNC	Bus Synchronized. Set when valid address has been placed on LSI-11 bus.
BDIN	Bus Data Input. Set when processor is ready to receive input data.
BDOUT	Bus Data Output. Set when processor is ready to transmit output data.

The module asserts the BRPLY (reply from module) bus control line when the data transfer has been completed.

During operation, the module receives the BSYNC signal indicating an address has been placed onto the LSI-11 bus. The I/O control logic gates this address into the address latch of the module with a SYNC H gating signal. If the address received is a bus device address on the DLV11-J, the address latch sends a BD SEL signal to the I/O control logic (indicating a valid address has been received). The control logic may now develop the proper gating signals (BDOUT/BDIN) to move the data to its proper destination. When the data transfer is complete, the module signals the processor via the BRPLY control line.

Address Latch

The address latch is used to hold the channel address (0–3), the device register address (RCSR, RBUF, XCSR, or XBUF), and the high-low byte indicator of the pending operation. When the program addresses the DLV11-J module, address bits 0–4 are presented to the address latch by the bus interface circuit over the internal tri-state data bus. Simultaneously, the address compare circuit and the bus interface circuit supply the address latch with the MATCH H signal (if the board address is correct). The address and the MATCH H signal are gated into the latch under the control of the I/O control logic circuit (SYNC H signal). The address latch now holds the address and a board select signal (BD SEL 1) to be used by the I/O control/register logic during the completion of the desired operation.

Address Compare Circuit

The address compare circuit tests the user-configured base address of the module (wire-wrap jumpers A5, A8–12) against the LSI-11 bus input (BDAL 5, 8–12 L). If the addresses are the same, the address compare circuit generates a portion of the MATCH H signal. (The remainder of MATCH H is supplied by the bus interface.) The MATCH H signal is used by the address latch circuit when creating the BD SEL H signal required by the I/O control logic during data transfers.

When channel 3 is configured as a console device interface, the bus interface logic tests for a proper console device address on the LSI-11 bus. If the address received by the bus interface is a proper console address, the CON SEL 1 H signal is generated. This signal is transmitted from the bus interface to the address compare circuit to force console address recognition.

Bus Interface

The module contains bus drivers and receivers which interfere directly with the LSI-11 bus. This allows data movement between the LSI-11 bus and the module's internal tri-state bus. These drivers also have the ability to transmit vector addresses received from the interrupt vector generation logic onto the LSI-11 bus.

If the LSI-11 bus holds an address within the I/O page, the BBS7 L signal line is asserted. This will cause the bus interface circuit of the DLV11-J to test the BDAL 6–7 L lines against the user-configured wire-wrap pins (A6–7) when the addresses and the same MATCH H signal are allowed to be asserted to the address latch. Since this is a "wired-AND," the MATCH H signal from the address compare signal must also be asserted. The MATCH H signal is required by the address latch to allow I/O data transfers. If channel 3 has been selected as a console device interface (jumpers C1 and C2 installed between wire-wrap posts X and 1), the bus interface performs a match operation between the LSI-11 bus lines (BDAL 3–5) and an internal address which is enabled by console select jumper C1. If the addresses agree, a CON SEL 1 H signal is produced for the address compare circuit which will force a console address recognition.

Interrupt and Vector Generation Logic

When a peripheral device interfaced to a DLV11-J needs service, the module can, if enabled, interrupt the computer program and vector to a service routine. The interrupt logic can initiate two types of interrupts: a receiver interrupt and a transmitter interrupt. These interrupts are handled through separate receiver and transmitter channels.

For an interrupt transaction to occur, the program must set the interrupt enable bit (bit 6) in the control/status register (CSR). Next, the interrupt logic must recognize a condition requiring service (indicated by the setting of bit 7 within the CSR) and then assert the interrupt request line (BIRQ L) on the LSI-11 bus. When the interrupt is acknowledged by the processor, the interrupt logic creates an input to the module's vector generation circuit which reflects the channel needing service (0, 1, 2, or 3) and the type of service needed (receive or transmit). The vector generation logic creates a vector function address which may be modified by the user-configured "base vector" address jumpers (V5–7). This modified address is output to the LSI-11 bus by the bus interface circuit, thus causing the processor to jump to the proper peripheral device service routine.

A receiver interrupt request is initiated when the receive buffer (RBUF) has received and assembled a character of data and is ready to transfer it to the processor. A transmitter interrupt is initiated when the transmitter buffer holding register (XBUF) is empty and is ready for another data input from the processor. The interrupt logic is also used to initialize the DLV11-J module. On a system power-up sequence, the processor creates BINIT L on the LSI-11 bus which is converted by the interrupt logic into INITO H. This signal is distributed on the module to initialize the four UARTs and the interrupt status registers (held within the interrupt logic).

Control/Status Registers

The control/status registers (CSRs) consist of a series of latches, data selectors, and gating circuitry. During data transactions, the I/O control logic enables the XCSR or RCSR to either latch in control bits or gate out status bits.

The RCSR uses only three bits during operation:

Receiver done (bit 7), set by RBUF
Receiver interrupt enable (bit 6), set by program
Reader enable (bit 0), set by program

All bits except the reader enable bit may be read by the program.

The XCSR uses three bits during operation:

Transmitter ready (bit 7), set by XBUF

Transmitter interrupt enable (bit 6), set by program

Break (bit 0), set by program and used only with the DLV11-KA option.

All bits may be read by the program.

Break Logic

During normal operation, the UART checks each received character for the proper number of stop bits. It does this by testing for a marking condition at the appropriate bit time. If it finds a spacing condition instead, it sets the framing error (FE) flag. The BREAK signal is a continuous spacing condition, and is interpreted by the UART as a data character that is missing its stop bit(s). The UART, therefore, responds to the BREAK signal by asserting FE H. If the channel 3 break response jumper is installed from X to B, FE H will negate control line BDCOK H; BDCOK H indicates to the processor that dc power is "OK." When FE H negates this signal, it causes the computer to restart at the bootstrap (provided proper processor power-up mode is selected).

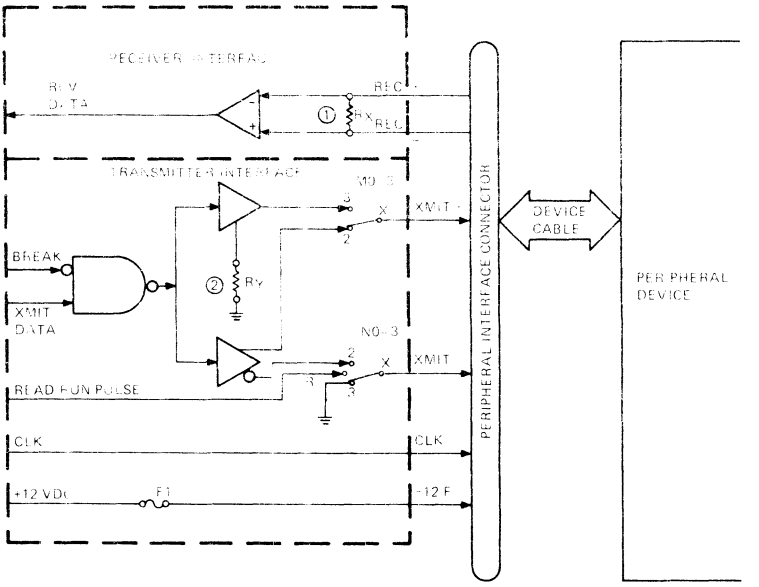
If the break jumper is installed from X to H, the computer will not "boot" on a framing error, but FE H will negate control line BHALT L. This causes the computer to halt when a framing error is received.

CAUTION

If the system is using MOS memory, data may be lost when BDCOK H is negated because this action interrupts the memory refresh cycle. If the jumper is not installed, the module will not take action.

Peripheral Interface

Each SLU channel of the DLV11-J module can be independently configured for line signal compatibility with EIA RS-232C and RS-423, RS-422, or 20 mA current loop operation (Figure 6). Each of the four interfaces may be configured to support 20 mA current loop devices with the addition of the DLV11-KA option. When installed, the peripheral interface supplies all power supply voltages needed by this option. If the 20 mA device contains a paper tape reader that can be program-controlled



NOTES

① R_X IS INSTALLED WHEN CHANNEL IS CONFIGURED FOR EIA RS-422 OPERATION (100 Ω, 1/4 W NON WIRE WOUND)
R30 CHANNEL 0
R31 CHANNEL 1
R32 CHANNEL 2
R33 CHANNEL 3

② R_Y IS CHOSEN FOR PROPER SLEW RATE WHEN CHANNEL IS CONFIGURED FOR EIA RS-232C/RS-423 OPERATION
R10 SETS SLEW RATE FOR CHANNELS 0 AND 1
R23 SETS SLEW RATE FOR CHANNELS 2 AND 3

MR-1207

Figure 6 Typical Peripheral Interface

(such as DIGITAL's LT33 or an ASR33 Teletypewriter with LT33 modification kit), the interface can be configured to advance the reader one character at a time.

DC-to-DC Power Converter

The power converter produces −12 Vdc and +5 Vdc from the LSI-11 power supply voltage of +12 Vdc. These voltages are produced to power all chips on the DLV11-J module and to supply the DLV11-KA 20 mA option. The power converter circuit consists of a crystal-controlled oscillator which drives a charge pump. The charge pump during operation supplies the desired power supply output voltage.

DRV11 PARALLEL LINE UNIT

GENERAL

The DRV11 is a general-purpose interface unit used for connecting parallel line TTL or DTL devices to the LSI-11 bus over up to 7.6 m (25 ft) of cable. It permits program-controlled data transfers at rates up to 40K words per second and provides LSI-11 bus interface and control logic for interrupt processing and vector generation. Data is handled by 16 diode-clamped input lines and 16 latched output lines. Device address is user-assigned and control/status registers (CSR) and data registers are compatible with PDP-11 software routines.

FEATURES

- 16 diode-clamped data input lines
- 16 latched output lines
- 16-bit word or 8-bit byte programmed data transfers
- User-assigned device address decoding
- LSI-11 bus interface and control logic for interrupt processing and vector generation
- Interrupt priority determined by electrical position along the LSI-11 bus
- Control/status registers (CSR) and data registers that are compatible with PDP-11 software routines
- Four control lines to the peripheral device for NEW DATA RDY, DATA TRANS, REQ A, and REQ B
- Logic-compatible with TTL and DTL devices
- Program-controlled data transfer rate of 40K words per second (maximum)

SPECIFICATIONS

Identification	M7941
Size	Double

Power	5.0 Vdc ± 5% at 0.9 A
Bus Loads	
AC	1.4
DC	1.0

CONFIGURATION

The following paragraphs describe how the user can configure the module by inserting or removing jumpers (Figure 1) so that it will function within his system. The jumpers, listed in Table 1, indicate the factory configuration when shipped.

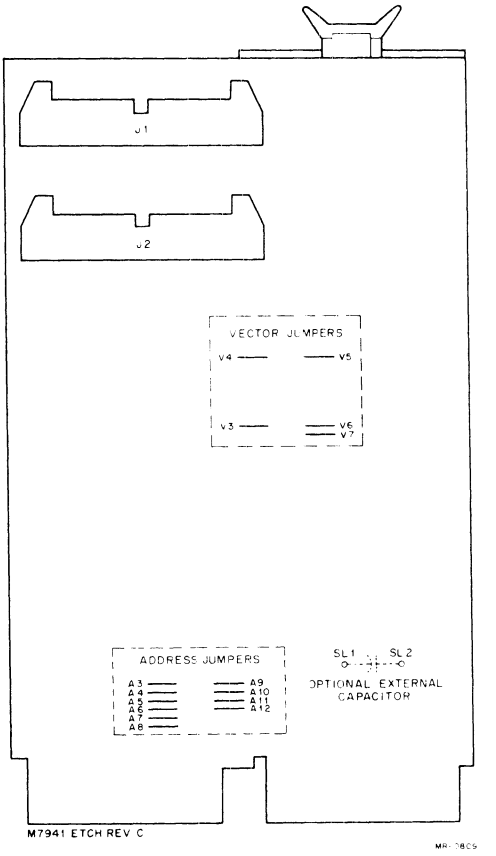


Figure 1 DRV11 Jumper Locations

Table 1 DRV11 PLU Factory Jumper Configuration

Jumper Designation	Jumper State*	Function Implemented
A3	R	This arrangement of jumpers A3 through A12 assigns the device address 16777X to the PLU. This address is the starting address of a reserved block in memory bank 7 which is recommended for user device address assignments. The least significant digit X is hardwired on the module to implement the three PLU device addresses as follows: X = 0 DRCSR address X = 2 Output buffer address X = 4 Input buffer address
A4	R	
A5	R	
A6	R	
A7	R	
A8	R	
A9	R	
A10	R	
A11	R	
A12	I	
V3	I	This factory-installed jumper configuration implements the two interrupt vector addresses 300 and 304 for use as defined by application requirements.
V4	I	
V5	I	
V6	R	
V7	R	

*R = Removed, I = Installed

Device Address

Addresses for the DRV11 can range from 16000X through 17777X. The three least significant bits are predetermined for the other DRV11 registers as shown in Table 2 and Figure 2. Addresses within 177560 to 177566 are reserved for the console device and should not be used for the DRV11

Table 2 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Registers				
Control and Status	DRCSR	R/W	167770	167760
Output Buffer	DROUTBUF	R/W	167772	167762
Input Buffer	DRINBUF	R	167774	167764
Interrupt				
Request A	REQ A	–	300	310
Request B	REQ B	–	304	314

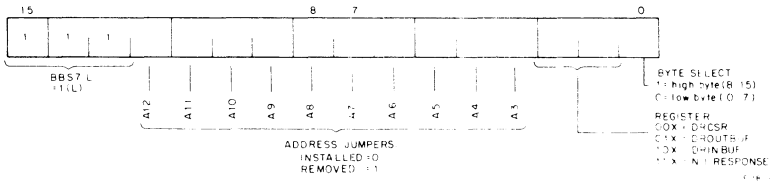


Figure 2 DRV11 Device Address Selection

Jumpers for bits 3 through 12 are installed or removed to produce the 16-bit address word shown in Figure 2. The appropriate jumpers are removed to produce logical 1 bits, and the appropriate jumpers are installed to produce logical 0 bits.

Vectors

The two vectors are selected within the range of 000 to 374 by using jumpers V3 to V7. Vector bits 3 through 7 are selected by the user to form the vector as described in Figure 3. The factory configuration sets the interrupt vector for 300 as shown in Table 2 and Figure 3.

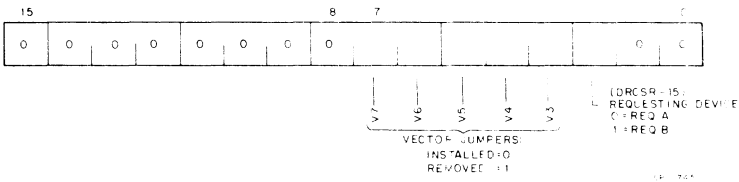


Figure 3 DRV11 Interrupt Vector

Registers

The word format for the control and status register (DRCSR) is shown in Figure 4 and described in Table 3.

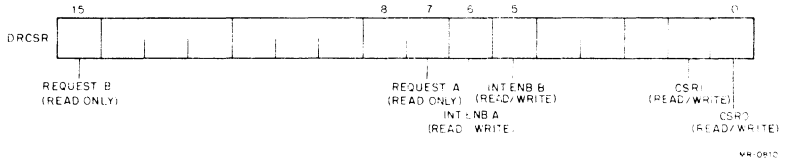


Figure 4 DRCSR Word Format

Table 3 DRCSR Word Formats

Bit	Description
15	Request B. This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program. When used as an interrupt request, it is asserted by the external device and initiates an interrupt provided the INT ENB B bit (bit 5) is also set. When used as a flag, this bit can be read by the program to monitor external device status. When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 1). This permits checking interface operation by loading a 0 or 1 into CSR1 and then verifying that Request B is the same value. Read-only bit. Cleared by INIT when in maintenance mode.
14–8	Not used. Read as 0.
7	Request A. Performs the same function as Request B (bit 15) except that an interrupt is generated only if INT ENB A (bit 6) is also set. When the maintenance cable is used, the state of Request A is identical to that of CSR0 (bit 0). Read-only bit. Cleared by INIT when in maintenance mode.
6	INT ENB A. Interrupt enable bit. When set, allows an interrupt request to be generated, provided Request A (bit 7) becomes set.
5	INT ENB B. Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided Request B (bit 15) becomes set.
4–2	Not used. Read as 0.
1	CSR1. This bit can be loaded or read (under program control) and can be used for a user-defined command to the device (appears only on connector no. 1).

Table 3 DRCSR Word Formats (Cont)

Bit	Description
	When the maintenance cable is used, setting or clearing this bit causes an identical state in bit 15 (Request B). This permits checking operation of bit 15 which cannot be loaded by the program. Can be loaded or read by the program (read/write bit). Cleared by INIT.
0	CSR0. Performs the same functions as CSR1 (bit 1) but appears only on connector no. 2 When the maintenance cable is used, the state of this bit controls the state of bit 7 (Request A). Read/write bit; cleared by INIT.

The word format for the transmit output buffer (DROUTBUF) is shown in Figure 5 and defined in Table 4.

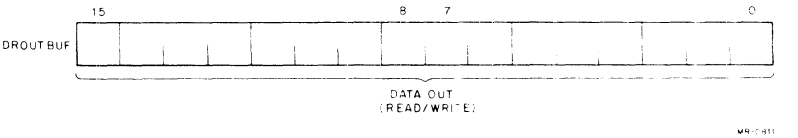


Figure 5 DROUTBUF Word Format

Table 4 DROUTBUF Word Format

Bit	Description
15–0	Output Data Buffer. Contains a full 16-bit word or one or two 8-bit bytes; high byte = 15–8; low byte = 7–0. Loading is accomplished under a program-controlled DATO or DATOB bus cycle. It can be read under a program-controlled DATI cycle.

The word format for the receiver input buffer (DRINBUF) is shown in Figure 6 and defined in Table 5.

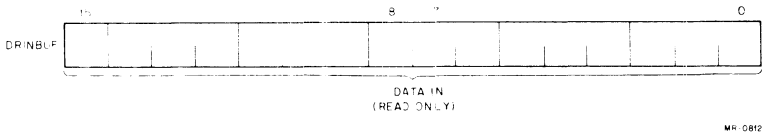


Figure 6 DRINBUF Word Format

Table 5 DRINBUF Word Format

Bit	Description
15–0	Input Data Buffer. Contains a full 16-bit word or one or two 8-bit bytes. The entire 16-bit word is read under a program-controlled DATI bus cycle.

Installation

Prior to installing the DRV11 on the backplane, first establish the desired priority level for the backplane slot installation. Check that proper device address vector jumpers are installed. The DRV11 can then be installed on the backplane. Connection to the user's device is via optional cables.

Interfacing to the User's Device

Interfacing the DRV11 to the user's device is via the two board-mounted H854 40-pin male connectors. Pins are located as shown in Figure 7. Signal pin assignments for input interface J2 (connector no. 2) and output interface J1 (connector no. 1) are listed in Table 6. Optional cables and connectors for use with the DRV11 include:

BC08R-01 – Maintenance cable; 40-conductor flat with H856 connectors on each end.

*BC07D-X** – Signal cable; two 20-conductor ribbon cables with a single H856 connector on one end; remaining end is terminated by the user. Available in lengths of 3, 4.6, and 7.6 m (10, 15, and 25 ft).

*The -X in the cable number denotes length in feet, -10, -12, -20. For example, a 10-ft BC07D cable would be ordered as BC07D-10.

*BC04Z-X** – Flat 40-conductor signal cable with a single H856 connector on one end; remaining end is terminated by the user. Available in lengths of 3, 4.6, and 7.6 m (10, 15, and 25 ft)

*BCV11-X** – Flat, 40-conductor, twisted pair cable with a single H856 connector on one end. The remaining end is connected by the user. Available in lengths of 1.5, 3, 4.6 6.1, and 7.6 m (5, 10, 15, 20, and 25 ft).

H856 – Socket, 40-pin female, for user-fabricated cables.

When using the BC07D cable, connect the free end of the ribbon cables using the wiring data contained in Table 7. Refer to the *Hardware/Accessories Catalog* for additional optional interface accessories.

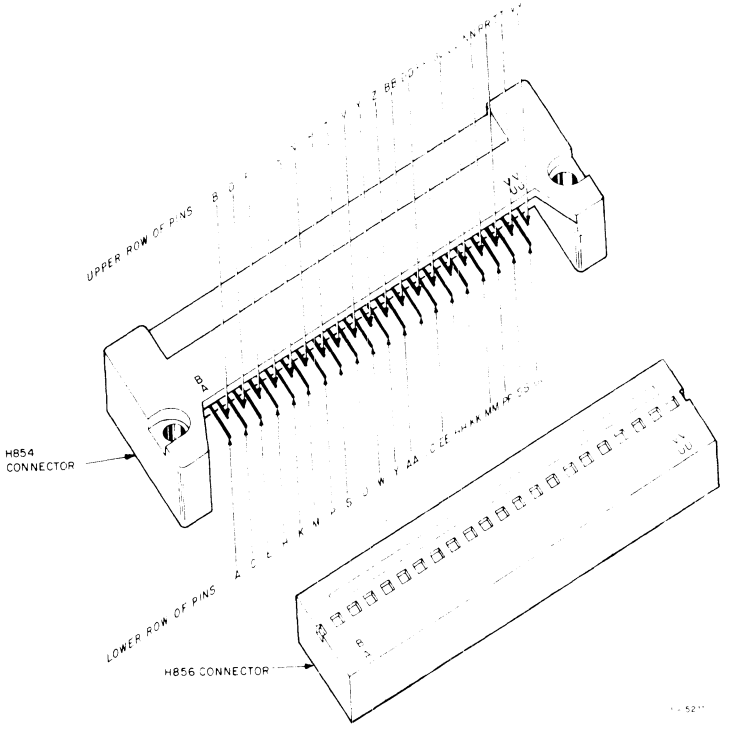


Figure 7 J1 or J2 Connector Pin Locations

*The -X in the cable number denotes length in feet, -10, -12, -20. For example, a 10-ft BC07D cable would be ordered as BC07D-10.

Table 6 DRV11 Input and Output Signal Pins

Inputs			Outputs		
Signal	Connector	Pin	Signal	Connector	Pin
IN00	J2	TT	OUT00	J1	C
IN01	J2	LL	OUT01	J1	K
IN02	J2	H, E	OUT02	J1	NN
IN03	J2	BB	OUT03	J1	U
IN04	J2	KK	OUT04	J1	L
IN05	J2	HH	OUT05	J1	N
IN06	J2	EE	OUT06	J1	R
IN07	J2	CC	OUT07	J1	T
IN08	J2	Z	OUT08	J1	W
IN09	J2	Y	OUT09	J1	X
IN10	J2	W	OUT10	J1	Z
IN11	J2	V	OUT11	J1	AA
IN12	J2	U	OUT12	J1	BB
IN13	J2	P	OUT13	J1	FF
IN14	J2	N	OUT14	J1	HH
IN15	J2	M	OUT15	J1	JJ
REQ B	J2	S	REQ A	J1	LL
DATA TRANS	J2	C	NEW DATA RDY	J1	VV
CSR0	J2	K	CSR1	J1	DD
INIT	J2	RR, NN	INIT	J1	P

Table 7 BC07D Signal Cable Connections

Wire Color	Cable 1 (connector pins B-VV)			Cable 2 (connector pins A-UU)		
	Pins	J1 Signal	J2 Signal	Pins	J1 Signal	J2 Signal
blk	B	open	open	A	open	open
brn	D	open	open	C	OUT00	DATA TRANS
red	F	open	open	E	open	IN02
orn	J	GND	GND	H	open	IN02
yel	L	OUT04	GND	K	OUT01	CSR0
grn	N	OUT05	IN14	M	GND	IN15
blu	R	OUT06	GND	P	INIT	IN13
vio	T	OUT07	GND	S	GND	REQ B
gry	V	GND	IN11	U	OUT03	IN12

Table 7 BC07D Signal Cable Connections (Cont)

Wire Color	Cable 1 (connector pins B-VV)			Cable 2 (connector pins A-UU)		
	Pins	J1 Signal	J2 Signal	Pins	J1 Signal	J2 Signal
wht	X	OUT09	GND	W	OUT08	IN10
blk	Z	OUT10	IN08	Y	GND	IN09
brn	BB	OUT12	IN03	AA	OUT11	GND
red	DD	CSR1	GND	CC	GND	IN07
orn	FF	OUT13	open	EE	GND	IN06
yel	JJ	OUT15	GND	HH	OUT14	IN05
grn	LL	REQ A	IN01	KK	GND	IN04
blu	NN	OUT02	INIT	MM	GND	GND
vio	RR	OUT02	INIT	PP	GND	GND
gry	TT	open	IN00	SS	GND	GND
wht	VV	New DATA RDY	open	UU	GND	GND

Output Data Interface

The output interface is the 16-bit buffer (DROUTBUF). It can be either loaded or read under program control. When loaded by a DATO or DATOB bus cycle, the NEW DATA RDY H pulse is generated to inform the user's device of the data transfer. The trailing edge of this positive-going pulse should be used to strobe the data into the user's device in order to allow data to settle on the interface cable. The system initialize signal (BINIT L) will clear DROUTBUF.

All output signals are TTL levels capable of driving eight unit loads except for the following:

New Data Ready = 10 unit loads
Data Transmitted = 30 unit loads
INIT (Initialize) = 10 units per connector

Input Data Interface

The input interface is the 16-bit DRINBUF read-only register, comprising gated bus drivers that transfer data from the user's device onto the LSI-11 bus under program control. DRINBUF is not capable of storing data; hence the user must keep input data on the IN lines until read by the processor. When read, the DRV11 generates a positive-going DATA TRANS H pulse which informs the user's device that the data has been accepted. The trailing edge of the pulse indicates that the input transfer has been completed.

All input signals are one standard TTL unit loads; inputs are protected by diode clamps to ground and +5 V.

Request Flags

Two signal lines (REQ A H and REQ B H) can be asserted by the user's device as flags in the DRCSR word. REQ B is available via connector no. 2, and it can be read in DRCSR bit 15. REQ A is available via connector no. 1, and it can be read in DRCSR bit 7. Two DRCSR interrupt enable bits, INT ENB A (bit 6) and INT ENB B (bit 5), allow automatic generation of an interrupt request when their respective REQ A or REQ B signals are asserted. Interrupt enable bits can be set or reset under program control.

In a typical application, REQ A and REQ B are generated by request flip-flops in the user's device. The user's request flip-flop must be set when servicing is required and must be cleared by the trailing edge of NEW DATA RDY or DATA TRANS when the appropriate data transaction has been completed.

This timing is shown in Figure 8. The logic required by the user to implement this is shown in Figure 9. The logic consists of a flip-flop that is set by the User Request pulse, which indicates that the user's device is

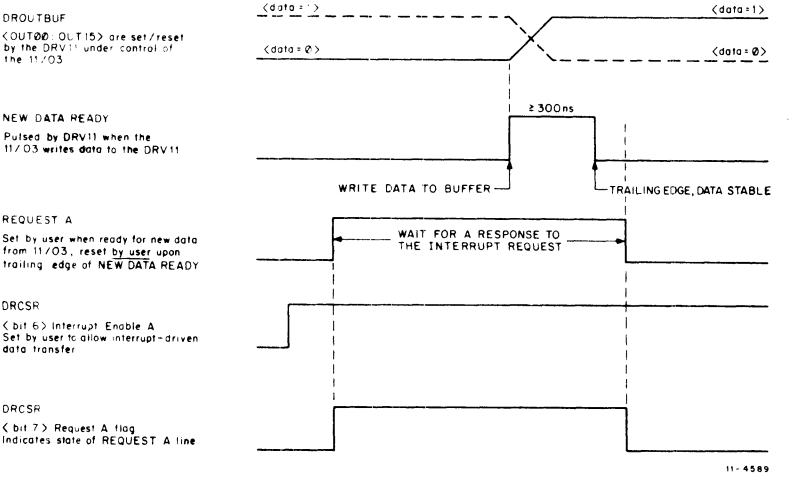


Figure 8 DRV11 Interface Signal Sequence

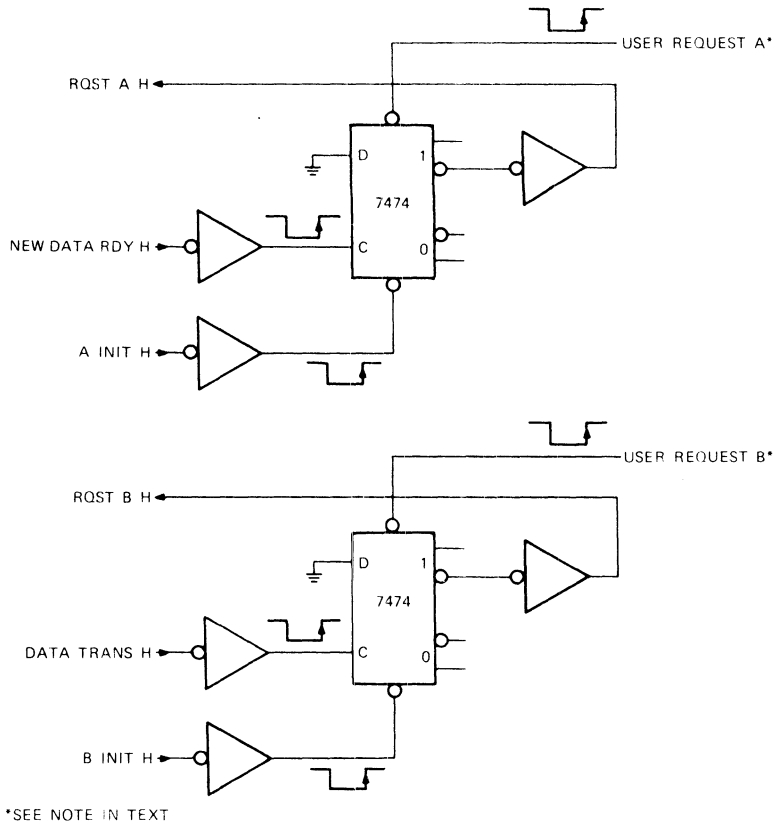


Figure 9 User Request Logic

requesting a transfer. The flip-flop is reset by the trailing edge of the NEW DATA RDY signal or the DATA TRANS signal.

NOTE

The User Request signal must return to the "high" state prior to the occurrence of the trailing edge of NEW DATA RDY or DATA TRANS. The leading edge of NEW DATA RDY or DATA TRANS can be used for this purpose. In most applications, a pulse on the User Request line of less than 10 μs is adequate.

Initialization

The BINIT L processor-generated initialize signal is applied to DRV11 circuits for interface logic initialization. It is also available to the user's circuits via connectors J1 and J2 as follows:

Connector/Pin	Signal
J1/P	AINIT H
J2/RR	BINIT H
J2/NN	BINIT H

An active BINIT L signal will clear: DROUTBUF data; DRCSR bits 6, 5, 1, 0; bits 16 and 7 (when the maintenance cable is connected); and interrupt request and interrupt acknowledge flip-flops.

NEW DATA RDY and DATA TRANS Pulse Width Modification

An optional capacitor can be added by the user to the DRV11 module to extend the pulse width of both the NEW DATA RDY and DATA TRANS pulse widths. The capacitor can be added in the location shown in Figure 1 to produce the approximate pulse widths listed below.

Optional External Capacitance (μF)	Approximate Pulse Width (ns) NEW DATA RDY	DATA TRANS
None	350	1150
0.0047	750	1550
0.01	1550	2400
0.02	2330	3200
0.03	3150	3900

BC08R Maintenance Cable

When using the optional BC08R maintenance cable, the connections listed in Table 8 are provided. Cable connectors P1 and P2 are connected to DRV11 connectors J1 and J2, respectively. Note that CSR0 (J2-K), which can be set or reset under program control, is routed to the REQ A input (J1-LL); similarly, CSR1 (J1-DD) is routed to REQ B (J2-S). Hence, a maintenance program can output data to DROUTBUF and read the same data via the cable and DRINBUF. DRCSR bits 0 (CSR0) and 1 (CSR1) can be used to simulate REQ A and REQ B signals, respectively. If the appropriate INT ENB bit (DRCSR bits 5 or 6) is set, the simulated signal will generate an interrupt request. Note that the BC08R cable must incorporate a half-twist when connected to J1 and J2.

Table 8 BC08R Maintenance Cable Signal Connection

J2		J1	
Pin	Name	Pin	Name
VV	OPEN	A	OPEN
UU	GND	B	OPEN
TT	IN00	C	OUT00
SS	GND	D	OPEN
RR	INIT H	E	OPEN
PP	GND	F	OPEN
NN	INIT H	H	OPEN
MM	GND	J	GND
LL	IN01	K	OUT01
KK	IN04	L	OUT04
JJ	GND	M	GND
HH	IN05	N	OUT05
FF	OPEN	P	INIT H
EE	IN06	R	OUT06
DD	GND	S	GND
CC	IN07	T	OUT07
BB	IN03	U	OUT03
AA	GND	V	GND
Z	IN08	W	OUT08
Y	IN09	X	OUT09
X	GND	Y	GND
W	IN10	Z	OUT10
V	IN11	AA	OUT11
U	IN12	BB	OUT12
T	GND	CC	GND
S	REQ B	DD	CSR1
R	GND	EE	GND
P	IN13	FF	OUT13
N	IN14	HH	OUT14
M	IN15	JJ	OUT15
L	GND	KK	GND
K	CSR0	LL	REQ A
J	GND	MM	GND
H	IN02	NN	OUT02
F	OPEN	PP	GND
E	IN02	RR	OUT02
D	OPEN	SS	GND
C	DATA TRANS	TT	OPEN
B	OPEN	UU	GND
A	OPEN	VV	NEW DATA RDY

FUNCTIONAL DESCRIPTION

General

Major functions contained on the DRV11 module are shown in Figure 10. Communications between the processor and the DRV11 are executed via programmed I/O operations or interrupt-driven routines.

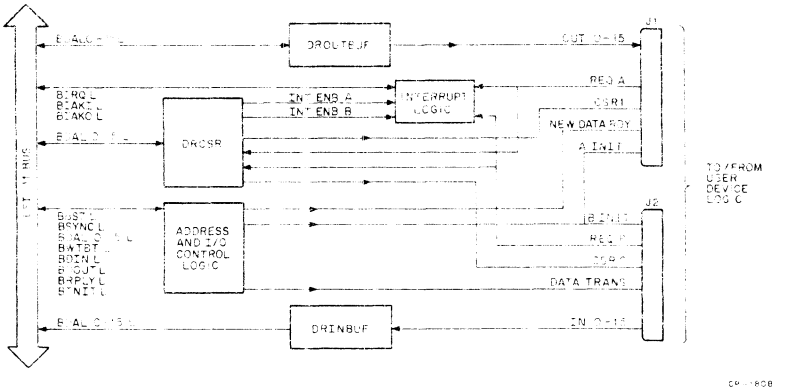


Figure 10 DRV11 Parallel Line Unit

The DRV11 is capable of storing one 16-bit output word or two 8-bit output bytes in DROUTBUF. The stored data (OUT0–15 H) is routed to the user's device via an optional I/O cable connected to J1. Any programmed operation that loads either a byte or a word in DROUTBUF causes a NEW DATA RDY H signal to be generated, informing the user's device of the operation.

Input data (DRINBUF) is gated onto the BDAL bus during a DATI bus cycle. All 16 bits are placed on the bus simultaneously; however, when the processor is involved in an 8-bit byte operation, it uses only the high or low byte. When the data is taken by the processor, a DATA TRANS H pulse is sent to the user's device to inform the device of the data transfer.

Addressing

When addressing a peripheral device interface such as the DRV11, the processor places an address on BDAL0–15 L, which is received and

distributed as BRD0–15 H in the DRV11. The address is in the upper 4K (28–32K) address space. On the leading edge of BSYNC L, the address decoder decodes the address selected by jumpers A3–A12 and sets the device selected flip-flop (not shown); the active flip-flop output is the ME signal, which enables function selection and I/O control logic operation. At the same time, function selection logic stores address bits BRD0–2.

NOTE

When addressed, the DRV11 always responds to either BDIN L or BDOUT L by asserting BRPLY L (L = assertion).

Function Selection

Function selection and I/O control logic monitors the ME signal and bus signals BDIN L, BDOUT L, and BWTBT L. It responds by generating appropriate select signals which control internal data gating. NEW DATA RDY H or DATA TRANS H output signals for the user's device, and the BRPLY L bus signal which informs the processor that the DRV11 has responded to the programmed I/O operation. Since the DRV11 appears to the processor as three addressable registers (DRCSR, DROUTBUF, and DRINBUF) that can be involved in either word or byte transfers, the three low-order address bits stored during the addressing portion of the bus cycle are used for function selection. The select signals relative to I/O bus control signals and address bits 0–2 are listed in Table 9.

Function selection is performed by a ROM located at E15 on the DRV11. The inputs to this ROM consist of the address bits and other LSI-11 bus signals as shown at the top of Table 9. This table shows the functions performed by the ROM outputs for a specific input condition. For example, when the output buffer is addressed by the processor, the last octal digit is decoded by the ROM to provide the SEL2IN L and the RPLY L signals. The RPLY L signal is delayed and becomes the BRPLY L signal. The SEL2IN L signal is used by the DRV11 logic to enable the contents of the output buffer register to be placed on the data lines of the LSI-11 bus so that the processor can read the data.

NEW DATA READY H is active for the duration of BDOUT L when in a DROUTBUF write operation. This signal is normally active for 350 ns. However, by adding an optional capacitor in the BRPLY L portion of the circuit, the leading edge of BRPLY is delayed, effectively increasing the duration of the NEW DATA RDY H pulse; adding the capacitor also increases the DATA TRANS H pulse width by approximately the same amount.

DATA TRANS H is active for the duration of BDIN L when in a DRINBUF read operation. This signal is normally active for 1150 ns. The time, however, can be extended by adding the optional capacitor to the BRPLY L portion of the circuit as previously described.

Table 9 DRV11 Device Function Decoding

Programmed Operation	Stored Device Addr. Bits 0-2	BWTBT L During Data Transfer	BDIN L	BDOUT L	Bus Cycle Type	Select Signals
Write DRCSR	0	0	H	L	DATO	SEL0OUT L
	0	1	H	L	DATOB	
Read DRCSR	0	0	L	H	DATI or DATIO	SEL0IN L
Write DROUTBUF Word	2	0	H	L	DATO	SEL2OUT (W + HB) L, SEL2OUT (W + LB) L, and NEW DATA READY H
Low Byte	2	1	H	L	DATOB	SEL2OUT (W + LB) L and NEW DATA READY H
High Byte	3	1	H	L	DATOB	SEL2OUT (W + HB) L and NEW DATA READY H
Read DROUTBUF	2	0	L	H	DATI or DATIO	SEL2IN L
Read DRINBUF	4	0	L	H	DATI	SEL4IN L and DATA TRANS H

Read Data Multiplexer

The read data multiplexer selects the proper data and places it on the BDAL bus when the processor inputs DRCSR, DROUTBUF or interrupt vectors; DRINBUF contents are gated onto the bus separately. The select signals (previously described) and VECTOR H, produced by the interrupt logic, control read data selection.

DRCSR Functions

The control/status register (DRCSR) is comprised of separate functions. Four of the six significant DRCSR bits can be involved in either write or read operations. The remaining two bits, 7 and 15, are read-only bits that are controlled by the external device via the REQ A H and REQ B H signals, respectively. The four read/write bits are stored in the 4-bit CSR latch. They represent CSR0 and CSR1 (DRCSR bits 0 and 1, respectively), which can be used to simulate interrupt requests when used with an optional maintenance cable. INT ENB A and INT ENB B (bits 6 and 5, respectively) enable interrupt logic operation. Note that CSR0 and CSR1 are available to the user's device for any user application.

DRINBUF Input Data Transfer

DRINBUF is an addressable 16-bit read-only register that receives data from the user's device for transmission to the LSI-11 bus. Data to be read is provided by the user's device on the IN0–15 H signal lines. Since the input buffer consists of gating logic rather than a flip-flop register, the user's device must hold the data on the lines until the data input transaction has been completed.

The input data is read during a DATI sequence while bus drivers are enabled by the SEL4IN L signal. The DATA TRANS pulse that is sent to the user's device by the function select logic informs the device of the transaction. Input data can be removed on the trailing edge of this pulse.

DROUTBUF Output Data Transfer

DROUTBUF comprises two 8-bit latches, enabling either 16-bit word or 8-bit byte output transfers. Two SEL2 signals function as clock signals for the latches. When in a DATO bus cycle, both signals clock data from the internal BRD0–15 H bus into the latches. However, when in a DATOB cycle, only one signal clocks data into an 8-bit latch, as determined by address bit 0 previously stored during the addressing portion of the bus cycle.

The NEW DATA RDY H pulse generated by the function select logic is sent to the user's device to inform the device of the data transaction. The data can be input to the device on the trailing edge of this pulse.

Interrupts

The DRV11 contains LSI-11 bus-compatible interrupt logic that allows the user's device to generate interrupt requests. Two independent interrupt request signals (REQ A H and REQ B H) are capable of requesting processor service via separate interrupt vectors. In addition, DRCSR contains two interrupt enable bits (INT EN A and INT EN B) (bits 6 and 5, respectively), which independently enable or disable interrupt requests. REQ A and REQ B status can be read by the processor in DRCSR bits 7 and 15, respectively. Since separate interrupt vectors are provided for each request, one of the requests could be used to imply that device data is ready for input and the remaining request could be used to imply that the device is ready to accept new data.

An interrupt sequence is generated when a DRCSR INT EN bit (A or B) is set and its respective REQ signal is asserted by the device. The processor responds (if its PS bit 7 is not set) by asserting BDIN L; this enables the device requesting the interrupt to place its vector on the BDAL bus when the interrupt request is acknowledged. The processor then asserts BIAKO L, acknowledging the interrupt request. The DRV11 receives BIAKI L and the interrupt logic generates VECTOR H, which gates the jumper-addressed vector information through the read data multiplexer and bus drivers and onto the LSI-11 bus. The processor then proceeds to service the interrupt request.

Maintenance Mode

The maintenance mode allows the user to check DRV11 operation by installing an optional BC08R cable between connectors J1 and J2. This maintenance cable allows the contents of the output buffer DROUTBUF to be read during a DRINBUF DATI bus cycle. In addition, interrupts can be simulated by using DRCSR bits CSR0 and CSR1. CSR1 is routed via the cable directly to the REQ B H input and CSR0 is routed to the REQ A H input. By setting or clearing INT EN A, INT EN B, and CSR0 and CSR1 bits in the DRCSR register, a maintenance program can test the interrupt facility.

Initialization

BINIT L is received by a bus driver, inverted, and distributed to DRV11 logic to initialize the device interface. The buffered initialize signal is available to the user's device via the AINIT H and BINIT H signal lines. DRV11 logic functions cleared by the BINIT signal include DROUTBUF, DRCSR (bits 0, 1, 5, and 6), and interrupt logic.

DRV11-B DMA INTERFACE

GENERAL

The DRV11-B is a general-purpose direct memory access (DMA) interface used to transfer data directly between the LSI-11 system memory and an I/O device. The interface is programmed by the processor to move variable length blocks of 8- or 16-bit data words to or from specified locations in memory by means of the LSI-11 bus. Once programmed, no processor intervention is required. The DRV11-B can transfer up to 250K 16-bit words per second in single cycle mode and up to 500K 16-bit words per second in burst mode. The control structure also allows read-modify-restore operations.

FEATURES

- Buffered input/output data
- Data transfer rate of up to 500K 16-bit words per second
- Transfer of up to 32K 16-bit words
- Compatible with LSI-11 bus
- 16-bit CSR available for control and status functions
- Two 40-pin I/O connectors mounted on module for interface with user's hardware
- Switch-selectable device address and interrupt vector

SPECIFICATIONS

Identification	M7950
Size	Quad
Power	+5 Vdc ± 5% at 1.9 A
Bus Loads	
AC	3.3
DC	1

CONFIGURATION

General

The interface consists of five registers (Table 1): word count register (WCR), bus address register (BAR), control/status register (CSR), input data buffer register (IDBR), and output data buffer register (ODBR). The module also includes bus transceivers and logic for interrupt requests, address control and protocol, and DMA requests.

Table 1 Standard Addresses

Description	Mnemonic	Read/ Write	Address
Register			
Word Count	WCR	R/W	172410
Bus Address	BAR	R/W	172412
Control/Status	CSR	R/W	172414
Input Data Buffer	IDBR	R	172416
Output Data Buffer	ODBR	W	172416
Interrupt			
Interrupt Vector	–	–	124

The DRV11-B contains one switch pack used to assign an appropriate device address to the DMA interface and one switch pack to select an interrupt vector.

The address of the DRV11-B interface and the interrupt vector selected by the position of the switches in switch pack S2 and S1, respectively. The location of the switches on the module is shown in Figure 1. The switches are set to the OFF position (open) to select a zero bit and the ON position (closed) to select a one.

Device Address Format

The DRV11-B decodes four addresses, one for each of the registers listed:

Register	Octal Address
WCR	1XXXX0
BAR	1XXXX2
CSR	1XXXX4
DBR	1XXXX6

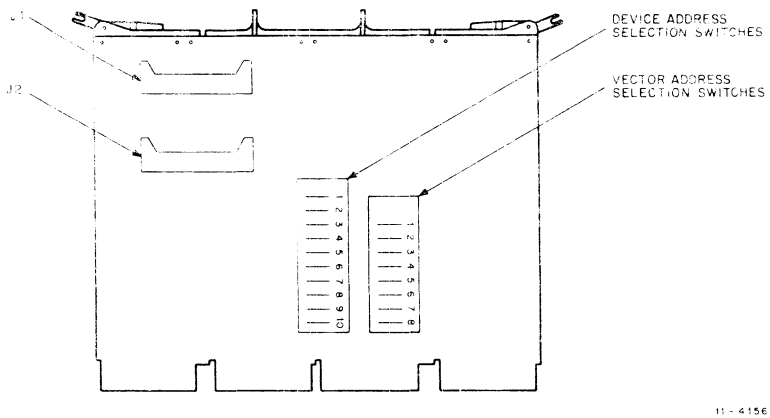


Figure 1 DRV11-B Connector and Switch Locations

Normally, the addresses assigned to the DMA start at 772410_8 and progress upward. Switches S2-1 through S2-10 select the base address as indicated by the X portion of the octal code and the individual registers are decoded by the DMA interface. The relationship between the address format and the switches is shown in Figure 2.

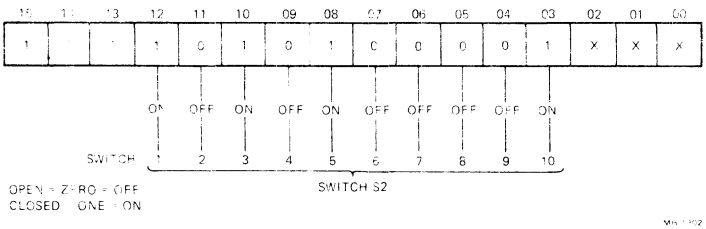


Figure 2 Device Address Switch S2 Selection

Interrupt Vector Selection

The interrupt vectors for the LSI-11 systems are allocated from $0-774_8$. The recommended vector assigned to the DRV11-B is 124_8. Switches S1-1 through S1-8 are used to select the vector. The relationship between the switches and vector format is shown in Figure 3.

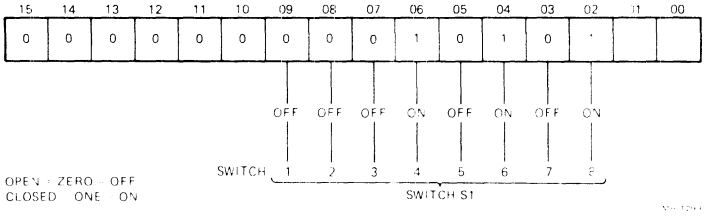


Figure 3 Interrupt Vector Switch S1 Selection

Registers
Each of the five registers can be addressed by the processor. The IDBR and ODBR are assigned the same address, and are read-only and write-only, respectively.

Word Count Register (WCR) – The WCR (Figure 4) is a 16-bit read/write counter which is loaded by the program with the 2's complement of the number of words or bytes to be transferred at one time between memory and the I/O device. At the end of each transfer, the WCR is incremented. When the count becomes zero (all 16 bits = 0), the DMA generates an interrupt request. The contents of the WCR can be monitored by the processor program.

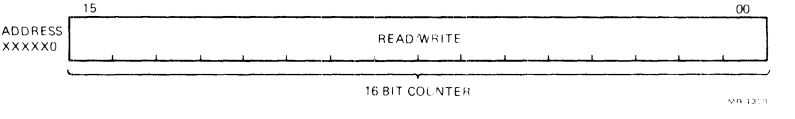


Figure 4 Word Count Register

Bus Address Register (BAR) – The BAR (Figure 5) is a 16-bit read/write register used to generate the bus address which specifies the location to or from which data is to be transferred. The register is incremented after each transfer. It will increment across 32K boundary lines via the extended address bits in the control/status register. Bus address bit 0 is driven by the user device.

Control and Status Register (CSR) – The CSR (Figure 6) contains 16 bits of information used to control the function and monitor the status of

the DMA transfers. The information in the CSR can be modified or read by the processor program in either 8-bit bytes or 16-bit words. Table 2 lists and defines each of the 16 bits.

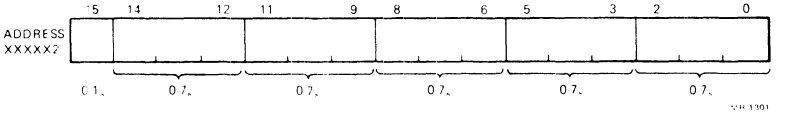


Figure 5 Bus Address Register

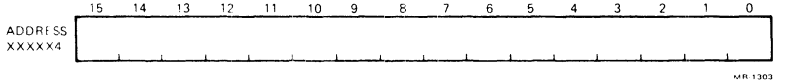


Figure 6 Control/Status Register

Table 2 DRV11-B Control/Status Register Bit Description

Bit	Name	Description
15	Error (Read-only)	1. Indicates a special condition. a. NEX (bit 14) b. ATTN (bit 13) 2. Sets READY (bit 7) and causes interrupt if IE (bit 6) is set. 3. Cleared by removing the special condition. a. NEX is cleared by writing to zero. b. ATTN is cleared by the user device.
14	NEX (Read/write zero)	1. Nonexistent memory indicates that as bus master, the DRV11-B did not receive BRPLY or that a DATIO cycle was not completed. 2. Sets error (bit 15). 3. Cleared by INIT or by writing to zero.

Table 2 DRV11-B Control Status Register Bit Description (Cont)

Bit	Name	Description
13	ATTN (Read-only)	1. Indicates the state of the ATTN user signal. 2. Sets error (bit 15).
12	MAINT (Read/write)	Maintenance bit used with diagnostic program.
11	STAT A (Read-only)	1. Device status bits that indicate the state of the DSTAT A, B, and C user signals. 2. Set and cleared by user control only.
10	STAT B (Read-only)	
9	STAT C (Read-only)	
8	CYCL (Read/write)	Cycle is used to prime a DMA bus cycle.
7	READY (Read-only)	1. Indicates that the DRV11-B is able to accept a new command. Requests an interrupt if IE (bit 6) is set. 2. Set by INIT.
6	IE (Read/write)	1. Enables interrupts to occur when READY (bit 7) is set. 2. Cleared by INIT.
5	XAD 17 (Read/write)	Extended address bit 17; cleared by INIT.
4	XAD 16 (Read/write)	Extended address bit 16; cleared by INIT.
3	FNCT 3 (Read/write)	1. Three bits made available to the user device. User-defined. 2. Cleared by INIT.
2	FNCT 2 (Read/write)	
1	FNCT 1 (Read/write)	

Table 2 DRV11-B Control Status Register Bit Description (Cont)

Bit	Name	Description
0	GO (Write-only)	Causes "NOT READY" to be sent to the user device indicating a command has been issued. Clears READY (bit 7). Enables DMA transfers.

Input Data Buffer Register (IDBR) – The IDBR (Figure 7) is used for read-only operations. Data is loaded into the register by the user's device. The data may be read from the IDBR as a 16-bit word, an 8-bit high byte, or an 8-bit low byte. Transfers are usually via DATO or DATOB DMA bus cycles. The register input connects to J2 mounted on the module.

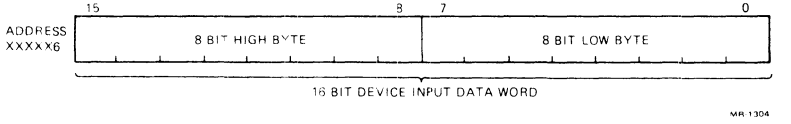


Figure 7 Input Data Buffer Register

Output Data Buffer Register (ODBR) – The ODBR (Figure 8) is used during write-only operations. Data from the LSI-11 bus is loaded into the register under program control and read from the register by the user's device. The register can be loaded with a 16-bit data word or with an 8-bit high byte, or as an 8-bit low byte. Transfers are usually via DATI or DATIO DMA bus cycles. The output of the register connects to J1 on the module.

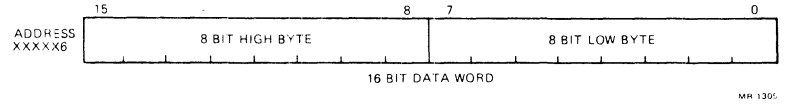


Figure 8 Output Data Buffer

PROGRAMMING

General

The DRV11-B interface operates as both a slave and master device. Prior to becoming bus master, all data transfers out (DATO) or data transfers in (DATI) are in respect to the processor. Once the DRV11-B is granted bus mastership by the processor, all data transfers are in respect to the DRV11-B.

DMA operation is initialized under program control by: loading the WCR with the 2's complement of the number of words to be transferred; loading the BAR with the first address to or from which data is to be transferred; or loading the CSR with the desired function bits. After the interface is initialized, data transfers are under control of the DMA logic.

Program Control Transfers

Data transfers may be performed under program control by addressing the IDBR or ODBR and reading or writing data.

DMA Control Transfers

DMA input (DATI) or output (DATO) data transfers occur when the processor clears READY. For a DATO cycle (DRV11-B to memory transfer), the user's I/O device presets the control bits [word count increment enable (WC INC ENB), bus address increment enable (BA INC ENB), C1, C0, A00, and ATTN], and asserts CYCLE REQUEST to gain use of the LSI-11 bus. When CYCLE REQUEST is asserted, input data is latched into the input DBR, the control bits are latched into the DRV11-B DMA control, and BUS goes low. A DATI cycle – memory to DRV11-B transfer – is handled in a similar manner, except that the output data is latched into the output DBR at the end of the bus cycle.

When the DRV11-B becomes bus master, a DATO or DATI cycle is performed directly to or from the memory location specified by the BAR. At the end of each cycle, the WCR and BAR are incremented and BUSY goes high while READY remains low. A second DATO or DATI cycle is performed when the user's I/O device again asserts CYCLE REQUEST. DMA transfers will continue until the WCR increments to zero, at which time READY goes high and the DRV11-B generates an interrupt (if interrupt enable is set) to the processor.

If burst mode is selected (SINGLE CYCLE low), only one CYCLE REQUEST is required for the complete transfer of the specified number of data words.

Device Cables and Signals

Data, status, and control signals are transferred between the user's I/O device and DMA by an input and an output cable assembly. The input cable attaches to connector J2 and the output cable attaches to connector J1. Tables 3 and 4 list the connector pin and designations for each signal. Table 5 lists several recommended cable assemblies that are available from DIGITAL in the lengths indicated. The H856 female connector mates with either J1 or J2 on the DRV11-B. To order cable assemblies in lengths not listed, contact a DIGITAL sales office. Cables up to 15.2 m (50 ft) maximum can be used.

Table 3 DRV11-B Input Connector Signals

J2* Connector Pin	Signal Name	Unit Loads
B	BUSY H	10 (drive)
D	ATTN H	1
F	A00 H	1
J	BA INC ENB H	1
K	FNCT 3 H	10 (drive)
L		
N	C0 H	1
R	FNCT 2 H	10 (drive)
T	C1 H	1
V	FNCT 1 H	10 (drive)
DD	08 IN H	
FF	09 IN H	1
JJ	10 IN H	
LL	11 IN H	
NN	12 IN H	
RR	13 IN H	
TT	14 IN H	
VV	15 IN H	
CC	07 IN H	
EE	06 IN H	
HH	05 IN H	
KK	04 IN H	
MM	03 IN H	
PP	02 IN H	
SS	01 IN H	
UU	00 IN H	

*All remaining pins connect in common to logic ground by board etch.

Table 4 DRV11-B Output Connector Signals

J1* Connector Pin	Signal Name	Unit Loads
B	CYCLE REQUEST H	1
D	INIT V2 H	10 (drive)
F	READY H	10 (drive)
J	WC INC ENB H	1
K	SINGLE CYCLE H	1
L	STATUS A	1
N	INIT H	10 (drive)
R	STATUS B	1
T, V	STATUS C	1
DD	08 OUT H	10 (drive)
FF	09 OUT H	
JJ	10 OUT H	
LL	11 OUT H	
NN	12 OUT H	
RR	13 OUT H	
TT	14 OUT H	
VV	15 OUT H	
CC	07 OUT H	
EE	06 OUT H	
HH	05 OUT H	
KK	04 OUT H	
MM	03 OUT H	
PP	02 OUT H	
SS	01 OUT H	
UU	00 OUT H	

*All remaining pins connect in common to logic ground by board etch.

Table 5 Recommended Cable Assemblies

Cable No.	Connectors	Type	Standard Lengths (ft.)
BC07D-XX	H856 to open end	2, 20 conductor ribbon	10, 15, 25
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25, 50
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25, 50

FUNCTIONAL DESCRIPTION

General

Basic functions comprising the DRV11-B are shown in Figure 9. The following paragraphs describe the DRV11-B registers, bus operations required for DMA transfers, and DMA transfer timing.

DRV11-B Registers

The DRV11-B contains five registers:

Word Count Register (WCR)
Bus Address Register (BAR)
Control/Status Register (CSR)
Output Data Buffer Register (ODBR)
Input Data Buffer Register (IDBR)

Word Count Register (WCR) – The WCR is a 16-bit read/write register that controls the number of transfers. This register is loaded (under program control) with the 2's complement of the number of words to be transferred. At the end of each transfer, the word count register is incremented. When the contents of the WCR are incremented to zero, transfers are terminated, READY is set, and, if enabled, an interrupt is requested. The WCR is word-addressable only.

Bus Address Register (BAR) – The BAR is a 15-bit read/write register. This register is loaded (under program control) with a bus address (not including address bit 0) which specifies the location to or from which data is to be transferred. The BAR is incremented after each transfer and can be incremented across 32K memory boundaries via the extended address feature of the DRV11-B. Systems with only 16 address bits will "wrap-around" to location zero when the extended address bits are incremented. The BAR is word-addressable only.

Control/Status Register (CSR) – The CSR is a 16-bit register used to control the functions and monitor the status of the interface. Bit 0 is a write-only bit and always reads as a zero. Bits 0–6 and bits 8 and 12 are read/write bits, while bits 7, 9–11, and 13–15 are read-only bits. Bit 14 can be written to a zero. Bits 4 and 5 are the extended addressing bits. The CSR is both byte- and word-addressable.

Input and Output Data Buffer Registers (DBRs) – The two DBRs are 16-bit registers. The input DBR is a read-only register; the output DBR is a write-only register. Data is loaded into the input DBR by the user's device and subsequently transferred to memory under DMA control by the DRV11-B, or under program control by the processor. Conversely, data is written into the output DBR from memory under DMA control by

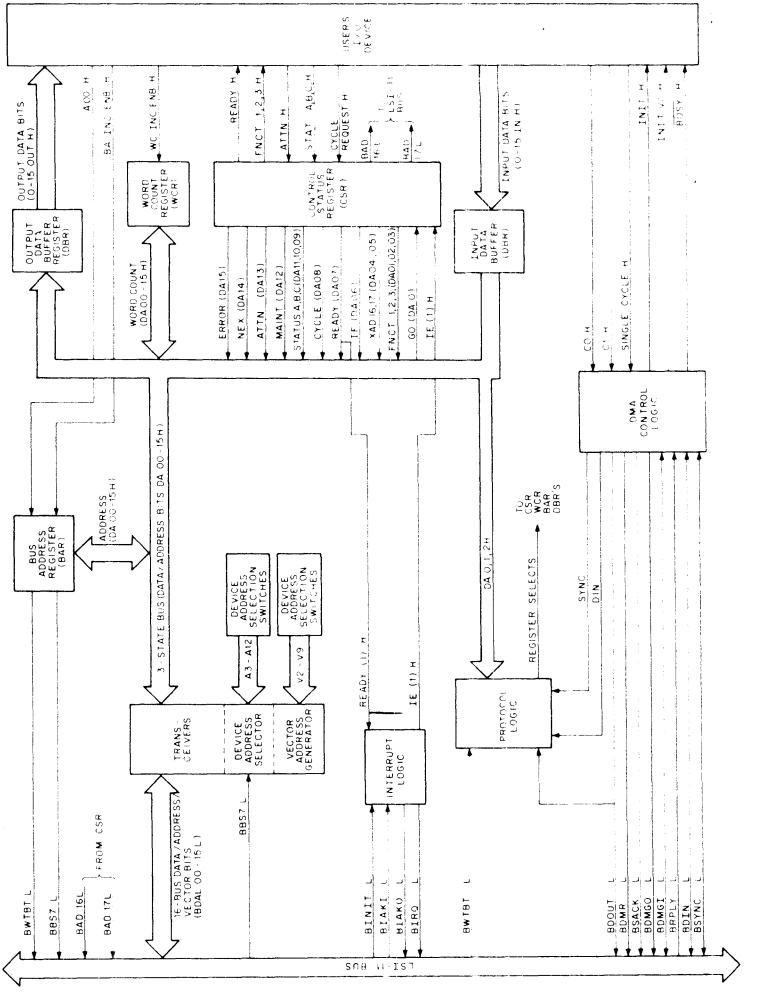


Figure 9 DRV11-B Logic Block Diagram

the DRV11-B, or under program control by the processor, and read by the user's device. The input and output DBRs interface to the user's device by means of two separate 40-pin I/O connectors. These connectors may be cabled together (for maintenance purposes) to function as a read/write register. The input and output DBRs share the same bus address and are byte- and word-addressable.

User's I/O Device to System Memory Transfer (DATO or DATOB)
Data transfers from the user's I/O device to the memory are DMA transfers. Figure 10 illustrates the data flow for a DMA DATO or DATOB cycle. Referring to Figure 9, DMA transfers are initialized under program control by loading the DRV11-B WCR (in 2's complement) with a count equal to the number of words to be transferred; loading the BAR with the starting memory address for word storage; and setting the CSR for transfers.

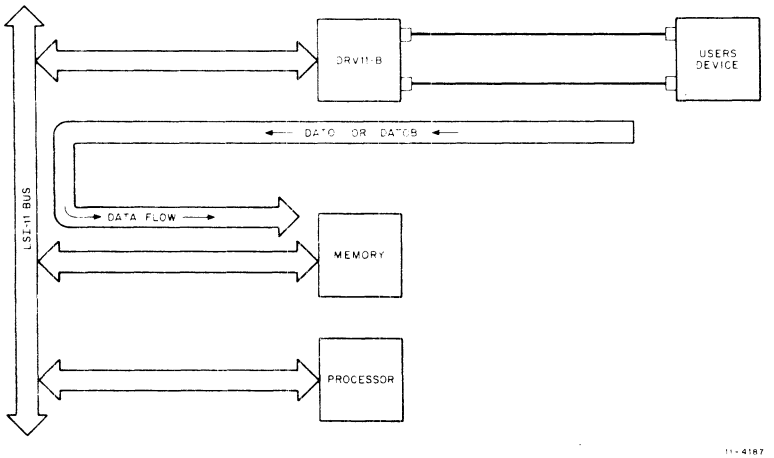


Figure 10 DMA DATO/DATOB Data Flow Diagram

When the GO bit of the CSR is written to a "one," READY goes low and the user's I/O device conditions the A00, BA INC ENB, WC INC ENB, ATTN, SINGLE CYCLE (high for normal DMA transfers), and the C0, C1 (Table 6) lines, and then asserts CYCLE REQUEST. The input data bits and control bits (C0, C1 and SINGLE CYCLE) are latched into the respective DRV11-B registers. CYCLE REQUEST sets CYCLE and causes the

Table 6 DRV11-B Interface Connector Signals

Mnemonic	Description
00 OUT – 15 OUT	16 TTL data output lines from the DRV11-B. One = high.
00 IN – 15 IN	16 TTL data input lines from the user's device. One = high.
STATUS A, B, C	Three TTL status input lines from the user's device. The function of these lines is defined by the user.
FUNCT 1, 2, 3	Three TTL output lines to the user's device. The function of these lines is defined by the user.
INIT	One TTL output line; used to initialize the user's device.
INIT V2	One TTL output line; present when INIT is asserted or when FUNCT 2 is written to a one. Used for interprocessor buffer applications.
A00	One TTL input line from the user's device. This line is normally high for word transfers. During byte transfers this line controls address bit 00.
BUSY	One TTL output line to the user's device. BUSY is low when the DRV11-B DMA control logic is requesting control of the LSI-11 bus or when a DMA cycle is in progress. A low-to-high transition indicates end of cycle.
READY	One TTL output line to the user's device. When the READY line goes low DMA transfers may be initiated by the user's device.
C0, C1	Two (2) TTL input lines from the user's device. These lines control the LSI-11 bus cycle for DMA transfers. C0, C1 codes for the four (4) possible bus cycles are listed below:

Bus Cycle	C0	C1
DATI	0	0
DATIO	1	0
DATO	0	1
DATOB	1	1

SINGLE CYCLE	One TTL input line from the user's device. This line is internally pulled high for normal DMA transfers. For burst mode operation SINGLE CYCLE is driven low by the user's device.

Table 6 DRV11-B Interface Connector Signals (Cont)

Mnemonic	Description
	CAUTION When SINGLE CYCLE is driven low, total system operation is affected because the LSI-11 bus becomes dedicated to the DMA device, and other devices cannot use the bus.
WC INC ENB	One TTL input line from the user's device. This line is normally high to enable incrementing the DRV11-B word counter. Low inhibits incrementing.
BA INC ENB	One TTL input line from the user's device. This line is normally high to enable incrementing the bus address counter. Low inhibits incrementing.
CYCLE REQUEST	One TTL input line from the user's device. A low-to-high transition of this line initiates a DMA request.
ATTN	One TTL input line from the user's device. This line is driven high to terminate DMA transfers, to set READY and request an interrupt if the interrupt enable bit is set.

DRV11-B to assert BDMR, which makes an LSI-11 bus request and causes BUSY to go low. In response to BDMR, the processor asserts BDMGO which is received as BDMGI. The DRV11-B becomes bus master and asserts BSACK and negates BDMR. The processor then terminates the bus grant sequence by negating BDMGO.

As bus master, the DRV11-B performs a DATO or DATOB bus cycle by placing the memory address on BDAL lines, asserting BWTBT, and then asserting BSYNC. The memory decodes the address; then the DRV11-B removes the address from the BDAL lines, negates BWTBT (BWTBT will remain active for a DATOB), places the user's input data on the BDAL lines, and asserts BDOUT. Memory receives the data and asserts BRPLY. In response to BRPLY, the DRV11-B negates BDOUT and then removes the user's input data from the BDAL lines. Memory now negates BRPLY, the bus cycle is terminated, and the bus is released when the DRV11-B negates BSACK and BSYNC.

At the end of the first transfer, the DRV11-B WCR and BAR are incremented, BUSY goes high, and READY remains low. With BUSY high and READY low, the user's I/O device can initiate another DATO or DATOB cycle by again asserting CYCLE REQUEST. DMA transfers can continue until the WCR increments to zero and generates an interrupt request, if the interrupt enable bit is set.

When the WCR increments to zero, READY goes high and the DRV11-B generates an interrupt request (if the interrupt circuits are enabled). The processor responds to the interrupt request (BIRQ) by asserting BDIN followed by BIAKI (interrupt acknowledge). BIAKI is received by the DRV11-B and in response places a vector address on the BDAL lines, asserts BRPLY, and negates BIRQ. The processor receives the vector address and negates BDIN and BIAKI. The DRV11-B now negates BRPLY, while the processor exits from the main program and enters a service program for the DRV11-B via the vector address.

Interrupt requests from the DRV11-B occur for the following conditions

1. When the WCR increments to zero – this is a normal interrupt at the end of a designated number of transfers.

2. When the user's I/O device asserts ATTN – this is a special condition interrupt which may be defined by the user to override the WCR

3. When a nonexistent memory location is addressed by the DRV11-B – this special condition interrupt is produced when no BRPLY is received from the memory.

System Memory to User's Device Transfers (DATIO or DATI)
DMA transfers from the memory to the user's I/O device occur in a manner similar to that described for user's I/O device to memory transfers. Figure 11 illustrates the data flow for a DMA DATIO or DATI cycle. Under program control, the DRV11-B WCR (Figure 9) is loaded with a count equal to the number of transfers, while the BAR is loaded with the starting address from which the first word will come; the CSR is set for transfers.

With the CSR set, READY goes low and the user's I/O device conditions the C0, C1 lines (Table 6) for a DATI or a DATIO and conditions the WC INC ENB, BA INC ENB, ATTN, SINGLE CYCLE (high for normal DMA transfers), signals, and asserts CYCLE REQUEST. BUSY from the DRV11-B goes low and the user's control bits are latched into the DRV11-B. The DRV11-B then asserts BDMR, which makes a bus request. When the request is arbitrated, the DRV11-B becomes bus master.

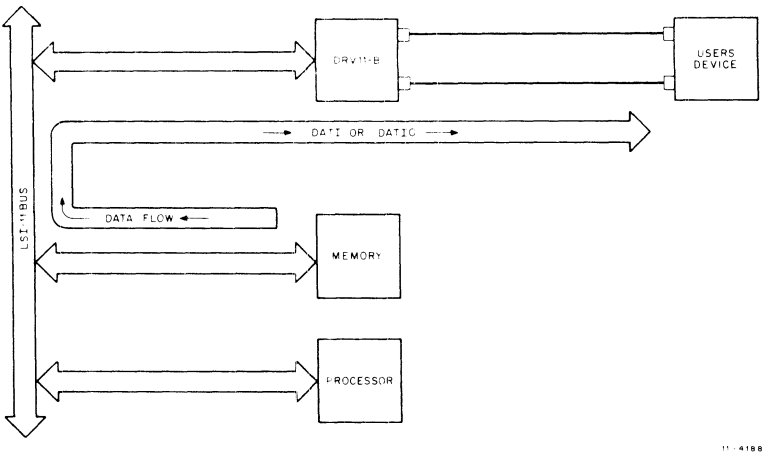


Figure 11 DMA DATIO/DATI Data Flow Diagram

When the DRV11-B becomes bus master, a DATI or DATIO bus cycle is performed (a DATI is described). The DRV11-B places the address of the memory location from which the first word is taken on the BDAL lines and asserts BSYNC. Memory decodes and latches the address. The DRV11-B then removes the address from the BDAL lines and asserts BDIN. Input data is now placed on the BDAL lines by the memory and the memory asserts BRPLY. The input data is accepted by the DRV11-B and BDIN is negated. Memory negates BRPLY and the DRV11-B negates BSACK and BSYNC to terminate the bus cycle and release the bus. The output data bits for the user's I/O device are stored in the DRV11-B output data buffer register. These bits can be read by the user's device at the low-to-high transition of BUSY.

At the end of the first transfer, the DRV11-B WCR and BAR are incremented, BUSY goes high, and READY remains low. The user's device can initiate another DATI or DATIO cycle by again setting CYCLE REQUEST. DMA transfers to the user's device can continue until the WCR increments to zero and causes an interrupt request to be generated.

DMA Transfers

The DRV11-B interface is designed for DMA transfers which the user can accomplish in several ways. DMA transfers are always set up by the processor when it loads the BAR and WCR and sets the READY bit. The

user then has the option of initiating transfers either by program control (setting the GO bit in the CSR) or by the user device asserting CYCLE REQUEST for 1 μs minimum.

Type of I/O to be Performed – The user has the option of selecting DATI, DATO, DATOB, or DATIO bus cycles by asserting C0 and C1 per Table 6. Note that if byte transfers are being performed, the byte address bit (A00) must be manipulated by the user. (Refer to section entitled "Word or Byte Transfers.")

Burst Mode vs Single Cycle DMA – Single cycle DMA allows the asynchronous transfer of data to or from the user's device. Each time the user's device is ready for a transfer, the user asserts CYCLE REQUEST for 1 μs. A DMA cycle is requested from the LSI-11 bus, and when the bus is granted to the DRV11-B, the BUSY line is asserted to inform the user that a data transfer is underway. The user must set up input data when CYCLE REQUEST is asserted, and hold it valid until the next assertion of CYCLE REQUEST. The user must strobe output data out of the DRV11-B on the rising edge of BUSY. The data will be valid 250 ns minimum before the rising edge of BUSY. (Figures 12 and 13 are detailed timing diagrams.)

Burst mode DMA allows synchronous transfer of data between a user's device and the DRV11-B. Once a DMA sequence is started (either by the user or by the processor), data will be transferred at a synchronous rate of 500K words per second. One data word will be transferred every 2 μs. The user must strobe data out of the DRV11-B into the user's device on the rising edge of BUSY. The data to be transferred to the DRV11-B must be set up when the READY line goes low (for the first data transfer) or on the rising edge of BUSY (for subsequent data transfers). (Figures 14 and 15 are detailed timing diagrams.)

Word or Byte Transfers – The DRV11-B can transfer words or bytes to memory. Transfers from memory are always on a word basis; if only one byte is required, the unused bytes are disregarded. To transfer data on a byte basis to memory, the following operations must be performed.

1. A00 must be manipulated by the user to address the proper byte in memory.

2. The byte to be transferred to memory must be input in its proper position in the input word, i.e., if A00 is 1, the byte to be input must be on input lines IN 8 H through IN 15 H (high byte being transferred).

3. WC INC EN H and BA INC EN H must be asserted during the write cycle of the fist byte of each word to inhibit the BAR and WCR from incrementing.

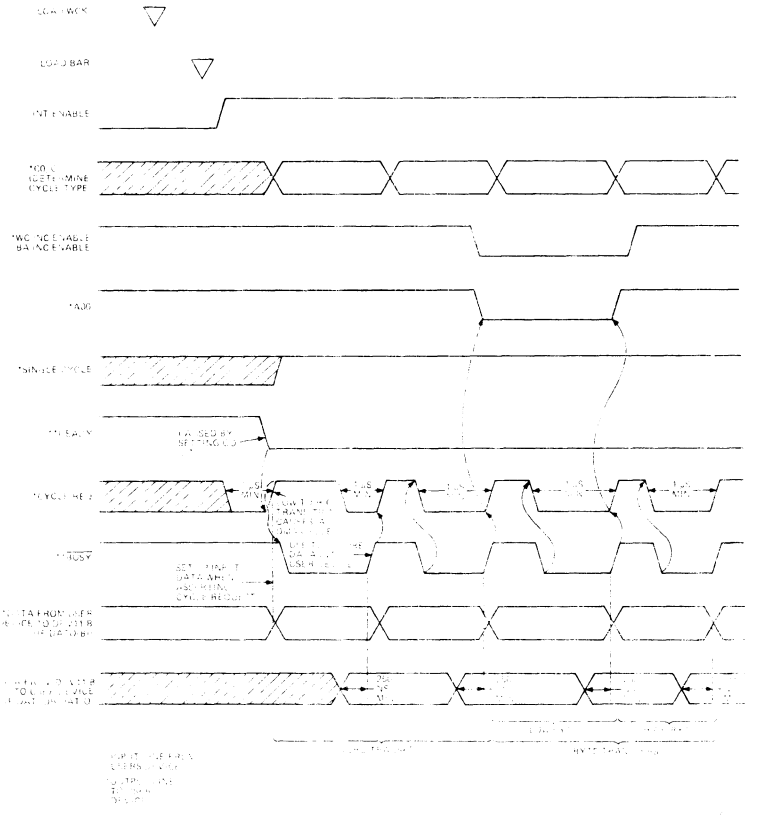


Figure 12 DRV11-B Timing: Single Cycle, Asynchronous, User-Initiated

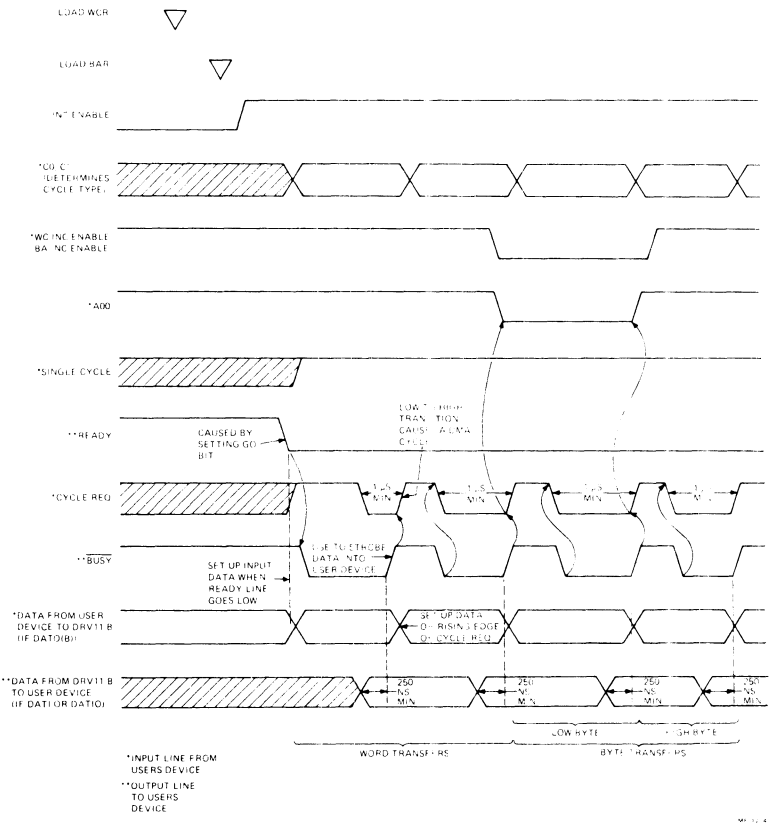


Figure 13 DRV11-B Timing: Single Cycle, Asynchronous, Program-Initiated

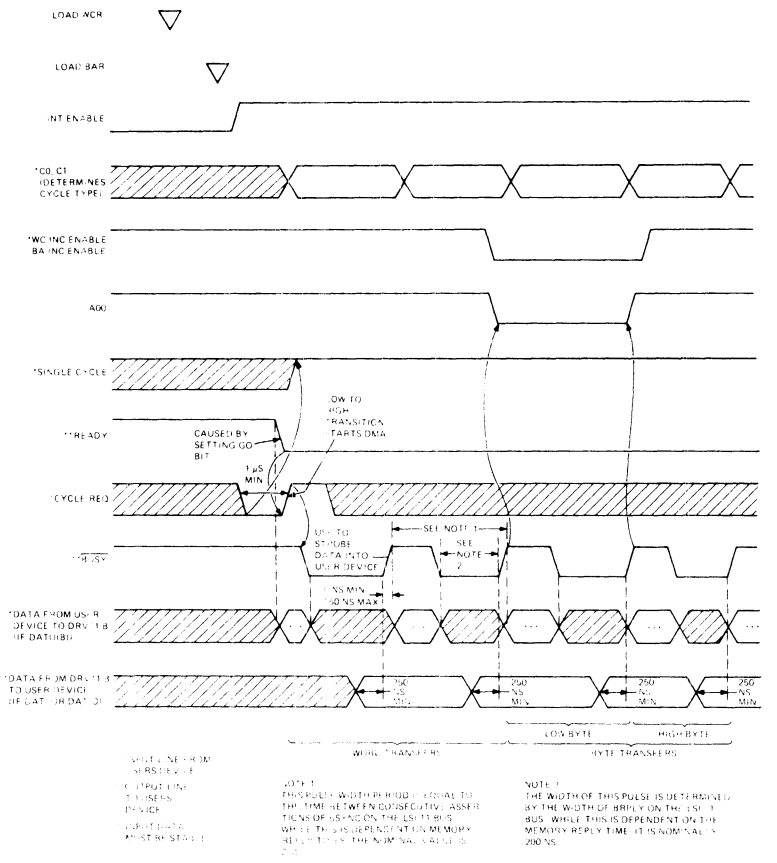


Figure 14 DRV11-B Timing: Burst Mode, User-Initiated

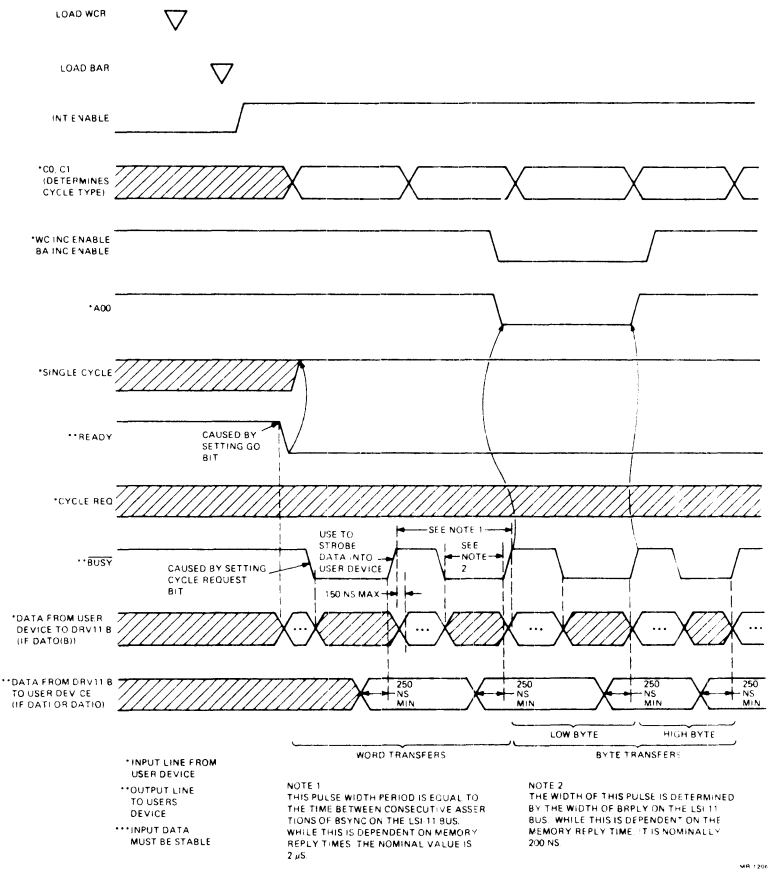


Figure 15 DRV11-B Timing: Burst Mode, Program-Initiated

Miscellaneous Signals – Four sets of signals exist to perform handshaking and status exchange between the processor and the user's device. They are:

STATUS A, B, C – These three TTL lines are used to input status to the DRV11-B from the user's device

FUNCT 1, 2, 3 – These three TTL lines are used to output status from the DRV11-B to the user's device

INIT, INIT V2 – INIT is asserted when the LSI-11 bus INIT signal is asserted. INIT V2 is asserted either when the LSI-11 bus INIT is asserted or when FUNCT 2 is a 1

ATTN – ATTN terminates a DMA transfer; this sets the READY bit and causes an interrupt (if the interrupt enable bit had been set).

DRV11-P LSI-11 BUS FOUNDATION MODULE

GENERAL

The DRV11-P is an LSI-11 bus-compatible foundation wire-wrap interface module. Approximately one-quarter of the module is occupied by bus transceivers, interrupt vector generator logic, device address comparator logic, protocol logic, and interrupt logic, as well as a 40-pin I/O connector. The remaining three-quarters of the module is for user application and has plated-through holes to accept ICs and wire-wrap pins (WP) for interconnecting the user's circuits. The plated-through holes can accept 6-, 8-, 14-, 16-, 18-, 20-, 22-, 24-, and 40-pin dual-in-line ICs or IC sockets in various mounting areas of the module, or discrete components can be inserted into the plated-through holes. The DRV11-P can be inserted into any one of the available interface option locations of any LSI-11 bus.

FEATURES

- An easy-to-use foundation module for custom interface applications.
- Factory-installed LSI-11 bus-compatible interface circuits.
- Device and interrupt vector that can be configured by the user.
- Compact - occupies only two device locations on the bus.
- Can accommodate up to 50 integrated circuits comprising the user's device logic.
- Wire-wrap pins are provided for all signals.
- All user control signal lines are TTL-compatible.

SPECIFICATIONS

Identification	M7948
Size	Quad
Power	5.0 Vdc ± 5% at 1.0 A
Bus Loads	
AC	2.1
DC	1 (plus user's logic)

DRV11-P

CONFIGURATION

General

The DRV11-P (Figure 1) is a versatile wire-wrap module that contains interface logic for operation with the LSI-11 bus and provides adequate board area for mounting and connecting integrated circuits (ICs) or discrete components. Because the bus interface logic is included the module can be efficiently configured by the user to satisfy a variety of device interface logic applications.

A 40-pin connector, conveniently mounted at the board edge, facilitates the connection to a device through several cable assembly types available from DIGITAL.

Except for the bus interface connections, all signals and voltages are terminated to wire-wrap pins for user connections. The bus control logic is provided with wire-wrap test points for monitoring the internal signals. The test points are spaced at 0.254 cm (0.1 in) between pins to allow a 40-pin connector to be inserted over the wire-wrap pins for automated test functions.

Approximately two-thirds of the surface area on the module consists of plated-through holes, each connected to a wire-wrap pin. The user can mount three different types of dual-in-line ICs or a variety of discrete components into the holes and connect the proper voltages and signals by wire-wrapping leads on the board.

Device Address Selection

The DRV11-P will respond to up to four consecutive addresses in the bank 7 area (addresses between 160000_8 and 177776_8). The register addresses are sequential by even numbers and are as follows.

Register	BBS7	Octal Address
1	1	16XXX0
2	1	16XXX2
3	1	16XXX4
4	1	16XXX6

The user selects a base address ending in zero for assignment to the first register by means of wire-wrap pins on the DRV11-P module. The module decodes this base address and the remaining register addresses are then properly decoded by the DRV11-P as they are received from the LSI-11 bus.

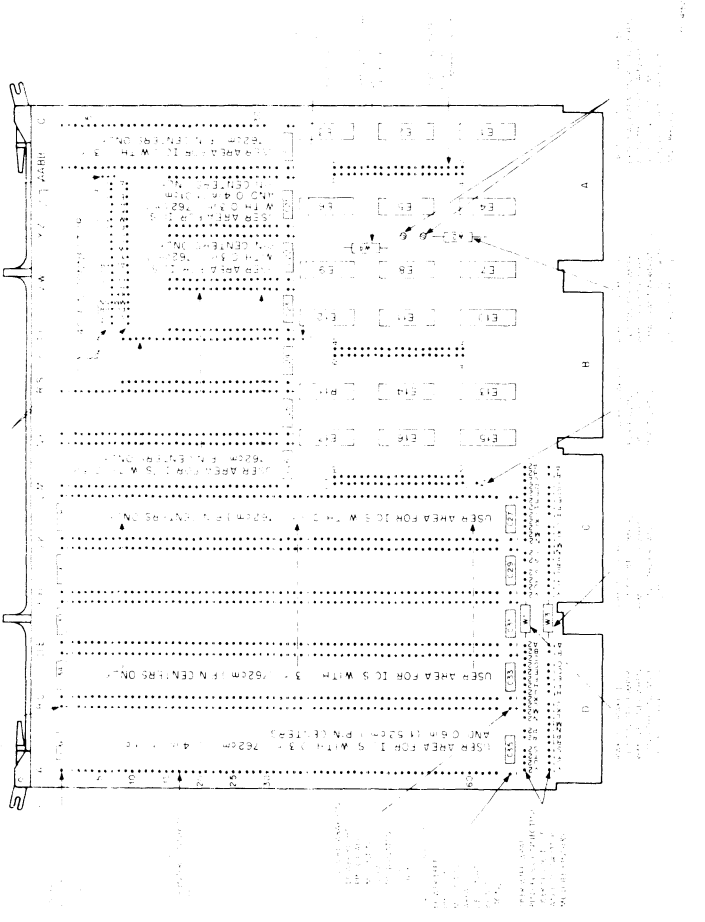


Figure 1 DRV11-P Component Mounting Locations

Figure 2 shows the address select format and presents the wire-wrap pin-to-bit relationship for device address selection. Bits to be decoded as "zero" bits in the base address are wire-wrapped to ground wire-wrap pins (WP). Bits to be decoded as "one" bits are left unwrapped as these bits are pulled up to the one state.

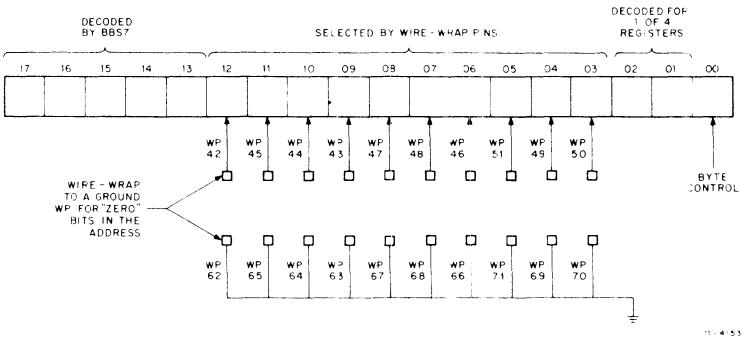


Figure 2 DRV11-P Device Address Select Format

Interrupt Vector Logic – The interrupt vector logic is used in conjunction with the interrupt control logic to generate a vector on bus lines BDAL 00 L–BDAL 07 L. The interrupt vector is specified by the user and selected by installing jumper leads between wire-wrap pins on the M7948 module. The vectors available are from 000_8 to 374_8. The vector range can be increased from 000_8 to 774_8 with additional logic and wiring.

When the VECTOR H signal is asserted as a result of a device interrupt request, the interrupt vector is placed on the bus lines.

Wire-wrap pins V3 through V7 are used to assign the vector bits. A jumper lead installed selects a logical 0 address bit for its associated line and no lead selects a logical 1 address bit according to the format in Figure 3.

Bit BDAL 02 L can be connected to the device interrupt request RQST A signal to specify a separate vector address for channel A and channel B.

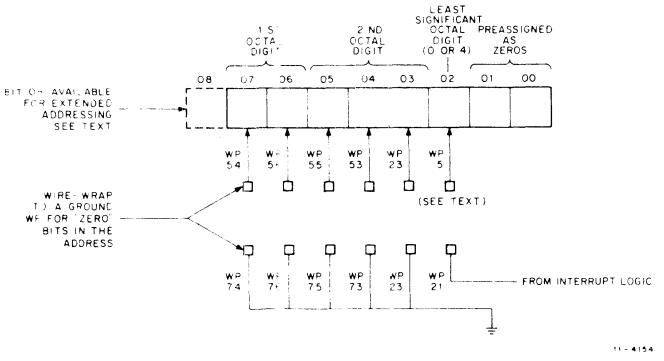


Figure 3 DRV11-P Vector Selection

Status and control information can be multiplexed through the same logic used to generate the vector address. Up to eight status and control bits can be assigned by the user and transferred to bus lines BDAL 00 L–BDAL 07 L. The information can be gated onto the bus lines using a select level generated by the address decoding logic.

Component Mounting Area

General – Twelve vertical areas (A–L) are available on the M7948 module for mounting integrated circuits or discrete components as shown on Figure 1. Each area has a double row of wire-wrap pins that connect to an associated plated-through hole located at 0.254 cm (0.1 in) vertical spacing. Area A is for multi-use and is capable of accepting ICs with pin centers at 0.762 cm (0.3 in), 1.01 cm (0.4 in), or 1.52 cm (0.6 in). Area K will also accept ICs with pin centers at 0.762 cm or 1.01 cm. All remaining areas will only accept ICs with pin centers at 0.762 cm.

Table 1 lists the total number of ICs with 0.762 cm spacing that can be mounted in the user areas of the module, A through L.

Table 1 DRV11-P IC Mounting Area

IC Type	Total Number
14-pin	60
16-pin	52
18-pin	44
20-pin	44

Connector Wire Wrap Pins – The 36 contact pins in rows C and D at the edge of the module connect to a double row of wire-wrap pins. These two rows are made available to the user for connecting signals and voltages from the backplane to the user-installed logic circuits. The following pins of rows C and D are normally dedicated to +5 V and GND.

The user can connect the power to the IC or components using the row C and row D wire-wrap pins.

+5 V	CA2, DA2
GND	CJ1, CM1, CT1 DJ1, DM1, DT1 CC2, DD2

Device Signals – Input and output data and status and control signals can be transferred between the device and the DRV11-P module using any one of several cable assemblies listed in Table 2 and available from DIGITAL. One end of each cable is terminated with a 40-pin female connector which mates with the 40-pin male connector J1 mounted on the M7948 module. The pins of J1 connect to the user-installed logic through a series of wire-wrap pins.

Table 2 Recommended Cable Assemblies

Cable No.	Connectors	Type	Length (XX)
BC07A-XX	H856 to open end	20-twisted pair	10, 15, 25
BC07D-XX	H856 to open end	2, 20-conductor ribbon	10, 15, 25
BC08R-XX	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 25, 50, 75, 100
BC04Z-XX	H856 to open end	Shielded flat	6, 10, 15, 25, 50

User Pin Selection

The DRV11-P provides many wire-wrap pins for the user to select that will assist him in determining his configuration. These pins and their functions are listed in Table 3.

Table 3 User Wire-Wrap Pins

Wire-Wrap Pin	Mnemonic	Function
WP1	SPARE 0	Spare input to the vector address multiplexer. This input can be used to read part of a control/status register.
WP2	SPARE 3	See WP1.
WP3		Ground for vector address bit V3. See WP23.
WP4	SPARE 1	See WP1.
WP5	V2	Vector address bit 2.
WP6	ENB CLK A H	ENB CLK A H is the clock input to the enable A flip-flop of the A interrupt logic. When ENB CLK A H goes high, ENB DATA A is clocked into the enable A flip-flop.
WP7	SPARE 2	See WP1.
WP8	ENB B ST H	ENB B ST H is the status output from the enable B flip-flop of the B interrupt logic. When ENB B ST H is high, the enable B flip-flop is set.
WP9	IAKI L	Test point for the BIAK I bus signal. BIAKI L is the processor's response to BIRQ L and is daisy-chained such that the first requesting device blocks the signal propagation. Non-requesting devices pass the signal on as BIAKO L. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP10	D01 L	Test point for data/address bit 1. Useful when testing the protocol logic. D01 is latched in the protocol logic at the asserted edge of BSYNC L. D01 and D02 are decoded to produce the SEL DEV outputs.
WP11	BWTBT L	Test point for the BWTBT bus signal; while BDOUT L is asserted, BWTBT L indicates a byte or word operation: BWTBT L asserted indicates byte operation; BWTBT L unasserted indicates word operation. BWTBT L decoded with BDOUT L and BDAL 0 L forms OUT LB L or OUT HB L.
WP12	R_XC_X	Test point for monitoring the delay of BRPLY.
WP13	BSYNC H	Test point for the BSYNC L bus signal. BSYNC L indicates that the address is valid. At the assertion of BSYNC L, address information is trapped in four latches. While unasserted, disables all outputs except the vector term of BRPLY L. BSYNC L is held throughout the entire bus cycle.
WP14	D00 H	One of 16 data or address lines from the transceivers for user applications. Address bit 0 is used for byte selection: 0 = low byte; 1 = high byte.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP15	BDOUT L	Test point for the BDOUT L bus signal. BDOUT is a strobe signal to effect a data output transaction. BDOUT L is decoded with BWTBT L and BDAL0 to form OUT LB L and OUT HB L. BDOUT L also causes BRPLY L to be issued through the delay circuit.
WP16	IN WD L	In word (IN WD) is used to gate input data from a selected register onto the LSI-11 bus. Enabled by BSYNC L and strobed by BDIN L.
WP17	D01 H	One of 16 data or address lines from the transceivers for user applications.
WP18	INIT 0 L	An initialize signal (asserted low) for user applications.
WP19	INIT 0 H	An initialize signal (asserted high) for user applications.
WP20	BRPLY L	Test point for the BRPLY L bus signal. BRPLY L is generated by VECTOR H (vector term), or by BSYNC and ENB in combination with either BDIN L or DBOUT L. Capacitor C37 can be added by the user to extend the delay.
WP21	VEC RQST B H	Used to distinguish whether device A or device B is making a request. VECT RQST B H is asserted for device B requests and unasserted for device A requests.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP22	RQST A H	When RQST A H is asserted, the bus request flip-flop is enabled, and BIRQ L becomes asserted if the interrupt enable flip-flop is set.
WP23	V3	Vector address bit 3. WP23 is used to select the state of vector address bit 3. When not wrapped to a ground pin, vector address bit 3 is a "one." When wrapped to WP3, vector address bit 3 is a "zero."
WP24	ENB DATA A H	Interrupt enable A data line. The level on this line, in conjunction with the ENB CLK A H (see WP6) line, determines the state of the A interrupt enable flip-flop within the interrupt logic.
WP25	BIAKO L	Test point for the BIAKO L bus signal. BIAKO L is the daisy-chained signal that is passed by all devices not requesting interrupt service (see WP9).
WP26	ENB CLK B H	ENB CLK B H is the clock input to the enable B flip-flop of the B interrupt logic. When ENB CLK B H goes high, ENB DATA B is clocked into the enable B flip-flop.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP27	ENB DATA B H	Interrupt enable B data line. The level on this line, in conjunction with the ENB CLK B H (see WP26) lines, determines the state of the B interrupt enable flip-flop within the interrupt logic.
WP28	RQST B H	When RQST B H is asserted, the bus request flip-flop for device B in the interrupt logic is enabled, and BIRQ L becomes asserted if the interrupt enable flip-flop is set.
WP29	VECTOR H	Test point for VECTOR H. This signal causes BRPLY L (vector term) to be generated through a delay independent of BSYNC L and ENB H. VECTOR H also gates the vector address onto the LSI-11 bus via the vector address generator.
WP30	D02 L	Test point for data/address bit 2. Useful when testing the protocol logic. D02 is latched at the asserted edge of BSYNC L. D02 and D01 are decoded to produce the SEL DEV outputs.
WP31	ENB H	Test point for ENB H. This signal is the result of a compare between the device address on the LSI-11 bus and the device address established by the user. When the addresses compare, ENB H is asserted and sent to the protocol logic.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP32	SEL DEV 6L	One of four select signals that is true as a function of BDAL1 L and BDAL2 L if ENB H (see WP31) is asserted at the asserted edge of BSYNC L. The four select signals indicate that a user's register has been selected for a data transaction. The select signals remain asserted until BSYNC L becomes unasserted.
WP33	SEL DEV 4L	See WP32.
WP34	SEL DEV 2L	See WP32.
WP35	SEL DEV 0L	See WP32.
WP36	OUT LB L	Out low byte is used to load (write) data into the low byte of a selected user register. See WP37.
WP37	OUT HB L	Out high byte is used to load (write) data into the high byte of a selected user register. If used with OUT LB L, the higher, lower, or both bytes can be written. OUT HB L is enabled by BSYNC L and the decode of BWTBT L and BDAL0 L, and strobed by BDOUT L.
WP38	BIRQ L	Test point for the BIRQ L bus signal This signal is asserted by a device needing interrupt service.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP39	BDMGO L	This signal is generated by DMA devices as a result of arbitrating the BDMGI L line. Jumper W2 must be removed if the DRV11-P is to be used for DMA service.
WP40	BDMGI H	Used as a source for the BDMGI signal to drive the user's DMA request arbitration logic. See WP39.
WP41	ENB A ST H	ENB A ST H is the status output from the enable A flip-flop of the A interrupt logic. When ENB A ST H is high, the enable A flip-flop is set.
WP42	A12	Used to select the user's device address along with WP45, 44, 43, 47, 48, 46, 51, 49, 50. When not wrapped to a ground pin, the particular device address bit will be a "one." When wrapped to a ground pin (WP62 for bit A12), the particular bit will be a "zero."
WP43	A09	User's device address bit 9. The associated ground pin is WP63. See WP42.
WP44	A10	User's device address bit 10. The associated ground pin is WP64. See WP42.
WP45	A11	User's device address bit 11. The associated ground pin is WP65. See WP42.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP46	A06	User's device address bit 6. The associated ground pin is WP66. See WP42.
WP47	A08	User's device address bit 8. The associated ground pin is WP67. See WP42.
WP48	A07	User's device address bit 7. The associated ground pin is WP68. See WP42.
WP49	A04	User's device address bit 4. The associated ground pin is WP69. See WP42.
WP50	A03	User's device address bit 3. The associated ground pin is WP70. See WP42.
WP51	A05	User's device address bit 5. The associated ground pin is WP71. See WP42.
W52	SPARE 4	See WP1.
WP53	V4	Vector address bit 3. The associated ground pin is WP73. See WP23.
WP54	V7	Vector address bit 7. The associated ground pin is WP74. See WP23.
WP55	V5	Vector address bit 5. The associated ground pin is WP75. See WP23.
WP56	V6	Vector address bit 6. The associated ground pin is WP76. See WP23.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP57	IN03 H	One of 16 data or address lines to the transceivers for user applications.
WP58	SPARE ENB 0	SPARE ENB 0 and SPARE ENB 1 (WP59) both must be driven low to write data from SPARE inputs 0 through 7 to the LSI-11 bus via the transceiver. For 8-bit input applications, SPARE ENB 0 could be driven by one of the SEL DEV lines, while SPARE ENB 1 could be driven by IN WD L.
WP59	SPARE ENB 1	See WP58.
WP60	IN00 H	See WP57.
WP61	D09 H	See WP17.
WP62		Ground for user's device address bit A12. See WP42.
WP63		Ground for user's device address bit A09. See WP42.
WP64		Ground for user's device address bit A10. See WP42.
WP65		Ground for user's device address bit A11. See WP42.
WP66		Ground for user's device address bit A06. See WP42.
WP67		Ground for user's device address bit A08. See WP42.
WP68		Ground for user's device address bit A07. See WP42.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP69		Ground for user's device address bit A04. See WP42.
WP70		Ground for user's device address bit A03. See WP42.
WP71		Ground for user's device address bit A05. See WP42.
WP72	D04 H	See WP17.
WP73		Ground for vector address bit V4. See WP23.
WP74		Ground for vector address bit V5. See WP23.
WP75		Ground for vector address bit V6. See WP23.
WP76		Ground for vector address bit V7. See WP23.
WP77	BBS7 H	Test point for the bank 7 select (BBS7) bus signal. This line is asserted by the bus master when an address in the upper bank is placed on the LSI-11 bus.
WP78	SPARE 6	See WP1.
WP79	D02 H	See WP17.
WP80	IN 02 H	See WP57.
WP81	D15 H	See WP17.
WP82	IN 13 H	See WP57.
WP83	D14 H	See WP17.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP84	D13 H	See WP17.
WP85	D12 H	See WP17.
WP86	IN 12 H	See WP57.
WP87	D03 H	See WP17.
WP88	D07 H	See WP17.
WP89	IN 10 H	See WP57.
WP90	SPARE 7	See WP1.
WP91	D10 H	See WP17.
WP92	IN 09 H	See WP57.
WP93		Not used.
WP94	TRANS ENB C L	Enables user's data to be placed onto the LSI-11 bus. Both TRANS ENB C and A (WP94 and WP120) and TRANS ENB D and B (WP95 and WP100) must be driven low prior to the processor's read data time.
WP95	TRANS ENB D L	See WP94.
WP96	IN 01 H	See WP57.
WP97	VEC ENB H	Test point for VEC ENB H. This signal gates the vector to the LSI-11 bus, provided that jumper W4 has not been removed. WP97 can be used as the source for VEC ENB H when adding an additional gate to the DRV11-P for vector expansion up to 774_8.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP98	IN 06 H	See WP57.
WP99	IN 04 H	See WP57.
WP100	TRANS ENB B L	See WP94.
WP101	IN 15 H	See WP57.
WP102	IN 14 H	See WP57.
WP103		Used to pull up the VEC ENB H line when jumper W4 is removed.
WP104		Not used.
WP105		Not used.
WP106	D08 H	See WP17.
WP107	D06 H	See WP17.
WP108	IN 11 H	See WP57.
WP109	D11 H	See WP17.
WP110		Not used.
WP111		Not used.
WP112	SPARE 5	See WPI.
WP113	IN 08 H	See WP57.
WP114		Not used.
WP115	BSYNC H	Test point for BSYNC H. At the asserted edge of this signal, address information is trapped in four latches. BSYNC H is the inversion of BSYNC L. See WP13.

Table 3 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP116		Not used.
WP117	D05 H	See WP17.
WP118	IN 07 H	See WP57.
WP119	IN 05 H	See WP57.
WP120	TRANS ENB A L	See WP94.
+3 V		There are two +3 V source wire-wrap pins on the DRV11-P. Each +3 V source can drive up to 13 TTL unit loads. These sources can be used for pulling up unused TTL inputs.

FUNCTIONAL DESCRIPTION

General

The DRV11-P contains 16 bus transceivers, device selection and interrupt vector generation logic, interrupt control, and control and status register functions. The device data inputs and outputs of the bus transceivers and the device control signals are made available to the user to complement control of up to four 16-bit registers.

Address Selection Logic

The address selection logic consists of a device address comparator and the protocol control logic. Up to four discrete addresses are made available with the existing logic on the DRV11-P and can be assigned to data registers, status and control registers, or word counters. By adding additional ICs, the user can increase the total number of addresses available. The main address of the DRV11-P is selected by monitoring the BBS7 bus line and decoding address information D03–D12 from the bus. The main device address is assigned by the configuration of jumper leads (A03–A08) attached to wire-wrap pins. When the selected and input bus addresses are the same, the device address comparator provides an ENB H level to the protocol control logic. The protocol control logic receives bus signals and address bits D01 and D02 to assert one of the four available output lines: SEL DEV 0L, SEL DEV 2L, SEL DEV 4L, and SEL DEV 6L. In addition, the protocol control logic provides output signals to specify word or byte transfers.

Table 4 lists and defines the function of the control signals required or available for the user logic.

Table 4 DRV11-P Protocol Control Logic Signals

Signal	Function
SEL DEV 0L SEL DEV 2L SEL DEV 4L SEL DEV 6L	Select device 0 through 4. One of four lines asserted by decoding the device address and available to select one of four user word registers.
OUT LB L OUT HB L	Out low byte, out high byte. Used to load (write) data into low byte (8 bits) or high byte (8 bits) or both bytes (16 bits) of the selected word register.
IN WD L	In word. Used to gate (read) data from the selected word register to the bus.

The format for the device address selection is shown in Figure 2. A logical 1 is specified when no jumper lead is installed between the appropriate wire-wrap pin from A3–A12. A logical 0 is specified when a jumper lead is installed.

Interrupt Control Logic

The interrupt control provides the circuits necessary to allow a program interrupt transaction between the bus and device. Two interrupt channels (A and B) are available to the user with channel A assigned to the highest priority. Table 5 lists and defines the user-available signals associated with the interrupt control logic.

Table 5 DRV11-P Interrupt Control Logic Signals

Signal	Function
RQST A H	Interrupt Request A. Asserted by device logic and sets the channel A interrupt request flip-flop when the channel A interrupt enable flip-flop is set.
ENB DATA A H	Interrupt Enable A Data. Asserted by device logic and sets the channel A interrupt enable flip-flop when the ENB CLK A signal is asserted.

Table 5 DRV11-P Interrupt Control Logic Signals (Cont)

Signal	Function
ENB CLK A	Interrupt Enable A Clock. Asserted by device logic to cause the channel A interrupt enable flip-flop to be set when ENB DATA A signal is asserted.
ENB A ST H	Interrupt Enable A Status. Indicates the status of the channel A interrupt enable flip-flop.
RQST B H	Interrupt Request B. Same as RQST A H signal except controls channel B interrupts.
ENB DATA B H	Interrupt Enable B Data. Same as ENB DATA A H signal except controls channel B interrupts.
ENB CLK B	Interrupt Enable B Clock. Same as ENB CLK A signal except controls channel B interrupts.
ENB B ST H	Interrupt Enable B Status. Same as ENB A ST H except controls channel B interrupts.
VECTOR H	Interrupt Vector Gate. Used by device logic to gate vector address onto the bus and to generate B RPLY signal.
VEC RQST H	Vector Request. Asserted by device logic to specify that channel A vector address is required; negated to specify channel B vector address is required.
INIT O L	Initialize Out. Buffered B INIT L signal from bus used for general initialization.

Device Address Comparator

The device address comparator (Figure 4, sheet 1) receives address bits D03 H–D12 H from the bus transceivers and compares these bits to the device address assignment bits (A03–A12) wired by the user on the DRV11-P module. If the two addresses compare, an ENB H signal is applied to the protocol logic. The device address comparator logic is designed around two type 8136 ICs. The user's device address is selected by means of wire-wrap pins. Wire-wrapping a device address pin to a ground pin makes that device address bit a "zero." Device address bits which are to be "ones" are left unwrapped. These bits will be pulled up to +5 V ("one" state) via resistors on the module.

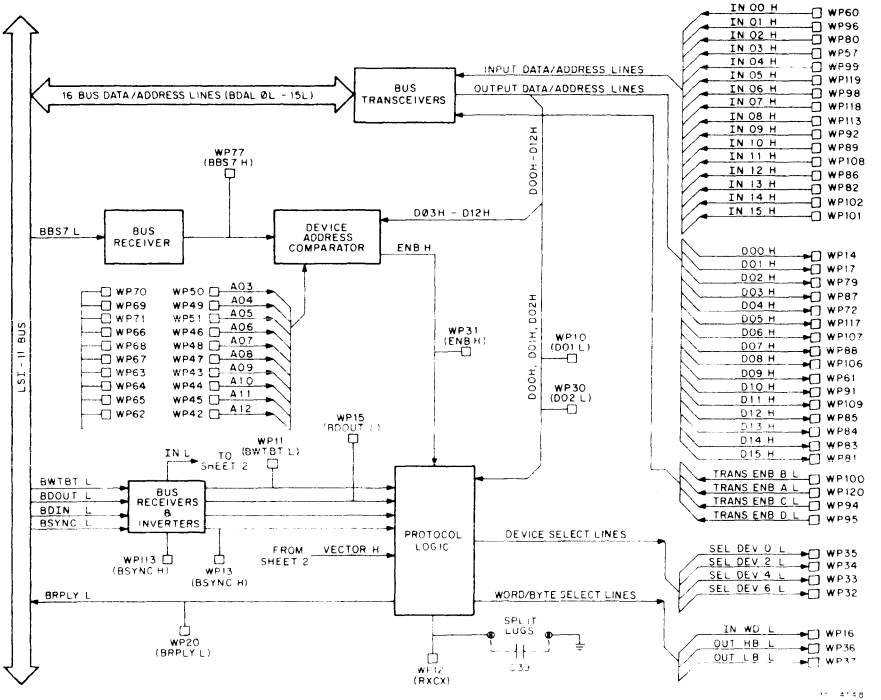


Figure 4 DRV11-P Block Diagram (Sheet 1 of 2)

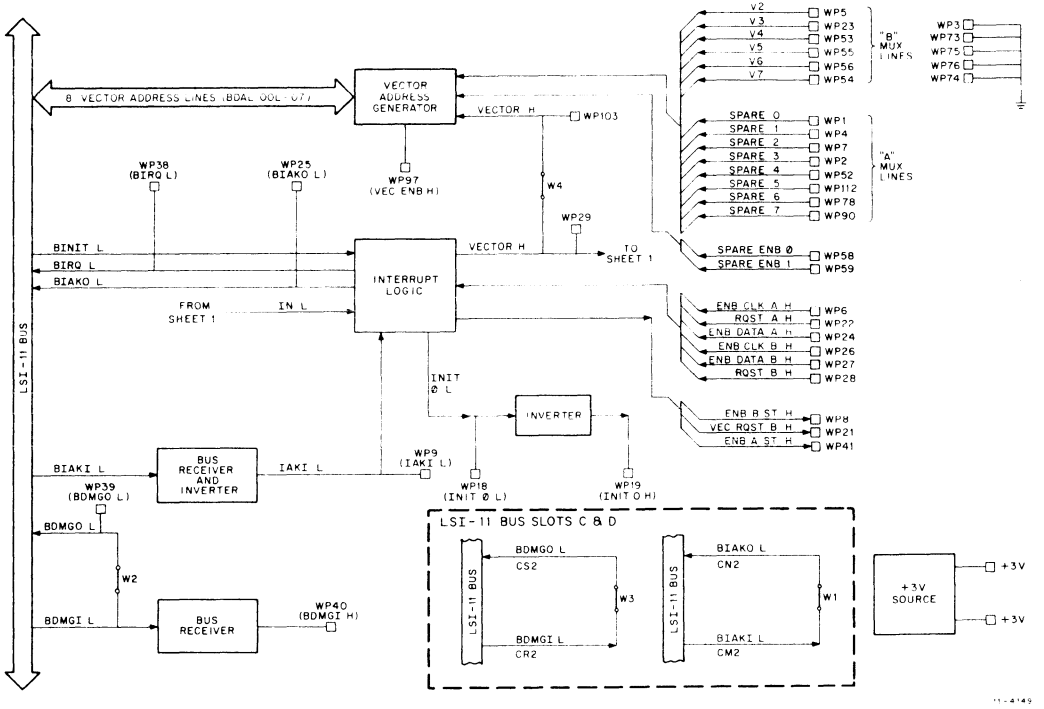


Figure 4 DRV11-P Block Diagram (Sheet 2 of 2)

Bus Transceivers

Referring to Figure 4, sheet 1, data output lines D00 through D15 reflect the state of the bus DBAL lines and will contain address and data information for any bus transfer, regardless of the device involved. Output data is usually clocked into a register for use by the interface or a peripheral since the length of time that the data is available on the bus during the bus cycle is very short. The device address comparator and the protocol logic determine if the data currently on the D00–D15 lines is intended for the DRV11-P.

Input data present at the IN00–IN15 lines will be applied to the bus when the TRANS ENB A, B, C, and D lines are asserted low. These lines are asserted by the protocol logic to gate data onto the bus at the proper time during a bus cycle when addressed by the processor. The SEL DEV and IN WD lines would be driven by the protocol logic to select a user's register. The bus transceivers consist of four type 8641 ICs.

Protocol Logic

The protocol logic (Figure 4, sheet 1) functions as a register selector, providing the signals necessary to control data flow into and out of up to four user registers (8 bytes). Designed around a special DIGITAL IC (DC004), the protocol logic operates as follows: when the proper device address has been decoded by the device address comparator, ENB H goes high, and is applied to a latch in the protocol logic. Address bits D01 H and D02 H are decoded by the protocol logic, producing one of the SEL DEV outputs, while bit D00 H and BWTBT are decoded for output word/byte selection (OUT HB L, OUT LB L). The device select lines (SEL DEV 0L, 2L, 4L, 6L) and word/byte select lines (IN WD L, OUT HB L, OUT LB L) are for user application and are available at wire-wrap pins (WP). Table 3 lists and defines the wire-wrap pins associated with the protocol logic. Generally, each DEV SEL output is used to select one of four user's registers, and the word/byte lines are used to determine the type of transfer (word or byte) to or from these registers. The active state of the user's lines from the protocol logic is a low assertion and the lines are TTL-compatible. The DEV SEL lines can sink up to 20 mA. Split lugs are provided on the DRV11-P to accommodate C37. This capacitor may be installed by the user to vary the delay between BDIN L, BDOUT L, and VECTOR H inputs and the BRPLY output.

The BRPLY L signal is normally issued within 85 ns (max.) of receiving either BDIN L or BDOUT L, depending on the bus cycle. If the user's interface requires more time before ending the bus cycle, the BRPLY L signal can be delayed up to a maximum of 10 μs by adding capacitor C37 across the split lugs in the BRPLY delay circuit.

The BRPLY L signal is also issued as the result of a signal on the VECTOR H input. This is used when transmitting the vector during an interrupt sequence.

Interrupt Logic

The interrupt logic (Figure 4, sheet 2) performs an interrupt transaction that uses the "pass-the-pulse" type arbitration scheme to assign priorities to peripheral devices. The DRV11-P interrupt logic has two channels (A and B) for generating two interrupt requests. Channel A has higher priority than channel B. If a user's device wants control of the LSI-11 bus, the interrupt enable flip-flop within the interrupt logic must first be set. This is accomplished by asserting (logical 1) the ENB DATA line and then clocking the enable flip-flop by asserting (positive transition) the ENB CLK line. With the interrupt enable flip-flop set, the user's device may then make a bus request by asserting (logical 1) RQST. When RQST is asserted, and if the interrupt enable flip-flop is set, the interrupt logic asserts (logical 0) BIRQ L, thus making a bus request. When the request is granted, the processor asserts (logical 0) BDIN L (Figure 4, sheet 1), which is applied to the interrupt logic as IN L (Figure 4, sheet 2). IN L causes the interrupt logic to assert (logical 1) VECTOR H, which is applied to the vector generator. A vector is thus placed on the LSI-11 bus to indicate the starting address of the service routine for the user's device which made the bus request.

As mentioned previously, two interrupt request channels (A and B) are contained within the interrupt logic. These channels can be used to service two user devices. However, because channel A has a higher priority than channel B, fast peripheral devices which cannot recover data if not serviced promptly should use channel A.

There are three status lines from the DRV11-P interrupt logic available to the user. These are: ENB B ST H, ENB A ST H, and VEC RQST B H. ENB B ST H and ENB A ST H indicate the status of the interrupt logic interrupt enable flip-flops. Each line is asserted (logical 1) when the appropriate enable flip-flop is set. The VEC RQST B line is asserted (logical 1) when the user's device connected to channel B has been granted use of the bus. When VEC RQST B is unasserted (logical 0), the user's device connected to channel A of the interrupt logic has been granted use of the bus. These status lines can function as part of the user's control and status register (CSR), which can be constructed on the DRV11-P module. Additionally, the INIT 0 and INIT 0 H outputs from the interrupt logic can be used to initialize the user's logic.

Interrupt Vector Generator

The interrupt vector generator (Figure 4 sheet 2) produces a vector which points to a location in memory containing the address where a service routine is stored for the user's device requesting interrupt service. The interrupt vector is selected by the user by means of wire-wrap pins (WP) on the DRV11-P. Vector bits V3 through V7 are hard-wired by the user for either logical 1s or 0s. Wire-wrapping an interrupt vector pin to a ground pin makes that vector bit a "zero." Vector bits which are to be "ones" are left unwrapped. These bits will be pulled up to +5 V ("one" state) via resistors on the DRV11-P. When VECTOR H from the interrupt logic goes high (logical 1), eight vector bits are gated onto the LSI-11 bus. It should be noted that the user can generally select the state of only six of the eight vector bits. The remaining bits, V00 and V01, are preset by the DRV11-P vector generator. With this arrangement, the user can select an interrupt vector in the normal user range of 000_8 to 374_8. However, by adding one gate to the interrupt vector generator encode logic, the user can accommodate nine bits in the vector and thus extend the interrupt to 774_8.

The interrupt vector generator is primarily designed around two type 74157 multiplexer ICs. Each 74157 has two separate 4-bit inputs which are multiplexed. Thus, both 74157s can accommodate two 8-bit bytes, one of which is used for vector generation. This leaves one spare 8-bit input for user application. The spare input can be used to gate onto the bus the lower byte of the user's CSR on the DRV11-P. The data on the spare input can be gated to the LSI-11 bus by driving both SPARE ENB 0 and SPARE ENB 1 inputs low (logical 0). This is best accomplished by using one of the SEL DEV lines from the protocol logic (Figure 4, sheet 1) along with the IN WD line. The actual use of the spare inputs is at the user's discretion, but SPARE ENB 0 and SPARE ENB 1 should not be permanently held low as this could affect interrupt vector. If not used, these inputs should be connected to the +3 V source.

Interrupt Vector Selection

As manufactured, the DRV11-P can generate vectors in the range from $0–374_8$. However, by adding one gate to the DRV11-P vector generation logic, the user can extend the vector to 774_8. The user selects the interrupt vector by means of wire-wrap pins (WP) on the DRV11-P module.

Figure 3 shows the vector select format and presents the wire-wrap pin-to-bit relationship for vector selection. Bits to be decoded as "zero" bits in the interrupt vector are wire-wrapped to ground wire-wrap pins (WP). Bits to be decoded as "one" bits are left unwrapped as these bits are pulled up to the one state.

It is recommended that WP5 (vector bit 2) be wrapped to WP21 (VEC RQST B H). This will automatically decode the least significant bit of the interrupt vector as a 0 or a 4. When the VECTOR H signal is issued as a result of the B half of the interrupt logic becoming bus master, the VEC RQST B H (WP5) signal is also issued, changing bit 2 of the interrupt vector, thus presenting a different vector for interrupt B.

The VEC RQST B H line can be thought of as a one bit code indicating which half of the interrupt logic is bus master. When bit 2 of the interrupt vector is a zero, the A half is bus master; a one indicates that the B half is master.

Bus Receivers
All LSI-11 bus data and control lines are fully buffered on the DRV11-P module. Buffering for the data and address lines (BDAL) is accomplished by the bus transceivers. Bus control lines (BWTBT, BDOUT, BDIN, BSYNC, BBSY, BIAKI, and BDMGI) are buffered on the DRV11-P with type 8640 bus receivers. These receivers are high-impedance receivers with the following input levels

High = 2.7 V min.
Low = 0.3 V max.

The receivers have standard TTL-compatible outputs which are made available (for most bus signals) to the user by means of wire-wrap pins (WP).

+3 V Source
There are two +3 V wire-wrap pins on the DRV11-P module. These pins provide a source of +3 V for pulling up unused TTL inputs. Each +3 V source is capable of driving up to 13 TTL unit loads. The +3 V sources are derived from resistor dividers placed across the +5 V logic source.

Wire-Wrap Pins
There are 112 user I/O lines and 122 wire-wrap pins (not counting the 40 pins for the I/O connector and the 70 pins for C and D module fingers) for user applications. The locations and functions of these pins are described in detail in Table 3.

DUV11 LINE INTERFACE

GENERAL

The DUV11 line interface is a buffered, program-controlled, single-line communications interface device which is used to establish a data communications line between any LSI-11 bus and a Bell 201 synchronous modem or equivalent. The module is fully programmable with respect to sync characters, character length (5 to 8 bits), and parity selection. The DUV11 provides serial-to-parallel and parallel-to-serial data communications, buffers TTL-to-EIA voltage levels and EIA-to-TTL voltage levels, and controls the modem for half- or full-duplex operation.

FEATURES

- Interfaces synchronous and isochronous communications data
- Interface signals meet EIA RS232C
- Operates in full-duplex or half-duplex modes
- Maximum baud rate is 19.2K baud
- Uses variable length characters (5, 6, 7, or 8 bits plus parity)
- Generates odd or even parity bits that are transmitted with the data character to the modem
- Verifies received character parity
- Inhibits transmitter output for maintenance purposes
- Provides control signals to the modem and monitors the modem status lines
- Establishes synchronization prior to receiving data
- Generates program interrupt requests

SPECIFICATIONS

Identification	M7951
Size	Quad
Power	+5 Vdc ± 5% at 0.86 A +12 Vdc ± 3% at 0.32 A
Bus Loads	
AC	1
DC	1

DUV11

CONFIGURATION

General

The following paragraphs describe how the user can configure the module so that it will function within his system. This module contains switches that are used to select the device address, vector interrupt, and the selection of special control functions. The descriptions of the registers and their standard factory addresses are listed in Table 1 and described below.

Table 1 DUV11 Factory Address Assignments

Register	Mnemonic	Read/ Write	DUV11 Address
Receiver Status	RXCSR	R/W	160010
Receiver Data Buffer*	RXDBUF	R	160012
Parameter Status*	PARCSR	W	160012
Transmitter Status	TXCSR	R/W	160014
Transmitter Data Buffer	TXDBUF	W	160016
Interrupt Vector	DONE	–	440

*Dual-purpose read or write register.

Device Address

The LSI-11 bus address and interrupt vector addresses must be determined prior to operating the DUV11. The bus address is selectable as are the interrupt vector. The bus address (also referred to as the device address) is controlled by switches contained in two switch banks (E38 and E39) (Figure 1), located in the address comparator logic. The position of these switches determines the required address state (1 or 0) of bus address bits 12–3. If a switch is set to ON, the switch contacts are closed and an address state of 1 is required on the related address bit to the address of the DUV11. Hence, electrically the DUV11 can have any device address within the range of 160000 to 177777. However, the Digital Equipment Corporation software requires that the device address fall within the floating address range of 160010 to 163776. The device address is set to 160010 at the factory to facilitate manufacturing testing. The switch positions for address selection are described in Table 1 and Figure 2.

NOTE

If a device address is selected which falls outside the floating address range, the software must be modified accordingly.

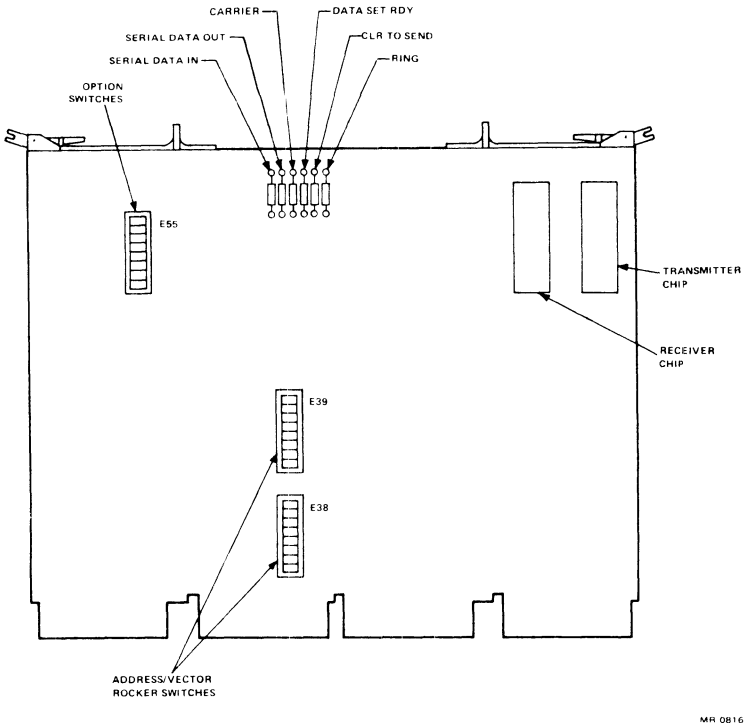


Figure 1 DUV11 (M7951) Major Components

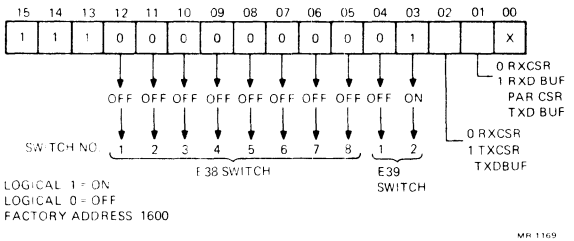


Figure 2 Device Address Selection

Interrupt Vector

The interrupt vector is also floating and is set to 440 at the factory to facilitate factory testing. If it is necessary to change the vector, simply change the six vector select switches contained in switch bank E39 (Figure 1) as required. These switches control vector bits 8–3; therefore, vectors can be generated in the range of 000 to 774. However, the software requires that the vector fall within the floating range of 300 to 777. The switch settings for vector selection are shown in Figure 3

NOTE

If a vector is selected which falls outside the floating address range, the software must be modified accordingly.

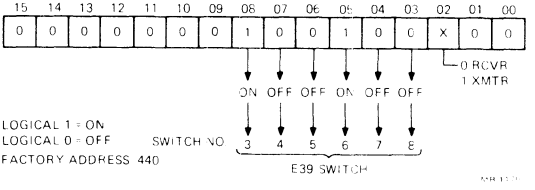


Figure 3 Interrupt Vector Selection

Option Switches

The DUV11 has the capability of selecting optional control functions that are used during operation. These control functions can be selected by using switches S1 through S8 of E55. The detailed operation of these switches is listed in Table 2.

Table 2 Switch Assignments

Switch No.*	Function
SW1	Optional Clear – Switch ON enables CLR OPT, which is used to clear RXCSR bits 3, 2, and 1.
SW2	Secondary Transmit – Switch ON enables secondary data channel between the modem and DUV11.

*All switches are located on component reference designation E55.

Table 2 Switch Assignments (Cont)

Switch No.*	Function
SW3	Secondary Receive – Switch ON enables secondary data channel between the modem and DUV11.
SW4	Sync Characters – Switch ON enables the receiver to synchronize internally upon receiving one sync character. The normal condition of receiving two sync characters exists when SW4 is off.
SW5	Special Feature – Switch ON allows external clock to be internaly generated; used when a modem is not being utilized.
SW6	Special Feature – Optional feature is switched ON for program control of data rate selection.
SW7	Maintenance Clock – Switch ON enables the clock that is used for maintenance purposes only.
SW8	Not used.

*All switches are located on component reference designation E55.

Optional Equipment

Mating Connector	H836
Cable	BC05C-XX

Registers

The RXCSR is a read/write register that controls the RCVR (receiver) portion of the interface; communicates interface status, requests, and supervisory data to the modem; and monitors status and supervisory data inputs from the modem.

The word format for the RXCSR is shown in Figure 4 and described in Table 3.

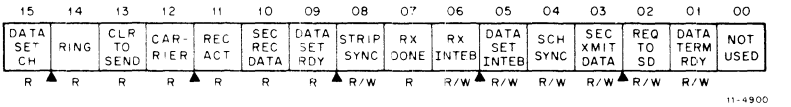


Figure 4 RXCSR Word Format

Table 3 RXCSR Word Format

Bit	Name	Description
15	DAT SET CH (Data Set Change)	When set, this bit indicates a modem status change. This bit is set by a transition of any of the following lines: • Ring • Clear to Send • Carrier • Secondary Received Data • Data Set Ready If bit 5 of this register is set, the setting of this bit will cause a RCVR interrupt. Read-only bit; cleared by INIT, master reset, and the DTI SEL 0 (RXCSR read strobe).
14	RING (Ring)	This bit reflects the state of the modem ring line. When set, this bit indicates that a ring signal is being received from the modem. Read-only bit.
13	CLR TO SD (Clear to Send)	This bit reflects the state of the clear to send line from the modem. When set, this bit indicates that the modem is ready to accept data from the interface for transmission. Read-only bit.
12	CARRIER (Carrier)	This bit reflects the state of the modem carrier. When set, this bit indicates the carrier is up. Read-only bit.

Table 3 RXCSR Word Format (Cont)

Bit	Name	Description
11	REC ACT (Receiver Active)	When the internal synchronous mode is selected, this bit is set when the proper number of contiguous sync characters (either 1 or 2, normally set for 2) have been received. If external synchronous or isochronous mode is selected, this bit follows the state of the search sync bit (bit 4 of this register). Read-only; cleared by INIT, master reset, and SCH SYNC (1) H (search sync) making 1 to 0 transition.
10	SEC RCV DAT (Secondary Receive Data)	This bit reflects the state of the secondary receive data line from the modem. This bit provides a receive channel for supervisory data from the modem to the processor. Read-only bit.
9	DAT SET RDY (Data Set Ready)	This bit reflects the state of the data set ready line from the modem. When set, this bit indicates that the modem is powered up and ready. Read-only bit.
8	STRIP SYNC (Strip Sync)	This bit determines whether sync characters received from the modem are to be presented to the program for reading. When this bit is set, receive characters that match the contents of the sync register do not cause a RCVR interrupt provided no errors are detected, i.e., bit 15 of the RXDBUF is clear. Read/write bit; cleared by INIT and master reset.

Table 3 RXCSR Word Format (Cont)

Bit	Name	Description
7	RX DONE (Receiver Done)	This bit is set when synchronization has been achieved and a character has been loaded into the RXDBUF, provided the STRIP SYNC bit is not set. If the STRIP SYNC bit is set and the received character is a sync character without errors, i.e., bit 15 of the RXDBUF is clear, this bit will not be set. When set, this bit will cause a RCVR interrupt request provided bit 6 of this register is set. Read-only bit; cleared by INIT, master reset, and the DTI SEL 2 (RXDBUF read strobe).
6	RX INTEB (Receiver Interrupt Enable)	When set, allows a RCVR interrupt request to be generated when the RX DONE bit is set. Read/write bit; cleared by INIT and master reset.
5	DAT SET INTEB (Data Set Interrupt Enable)	When set, allows a RCVR interrupt request to be generated when the DAT SET CH bit is set.
4	SCH SYNC (Search Sync)	When set in the internal synchronous mode, enables the RCVR synchronization logic and causes the RCVR to start comparing incoming data bits to the contents of the sync register in an attempt to recognize a sync character. When set in the isochronous mode, enables the RX DONE flag generation logic.

Table 3 RXCSR Word Format (Cont)

Bit	Name	Description
		When set in the external synchronous mode, enables the RX DONE flag generation logic and causes the RCVR to start framing incoming characters. Read/write bit; cleared by INIT and master reset.
3	SEC XMIT (Secondary Transmit Data)	This bit reflects the state of the secondary transmit data line to the modem. This bit provides a transmit channel for supervisory data from the processor to the modem. Read/write bit; cleared by INIT and master reset.
2	REQ TO SD (Request to Send)	When set, this bit causes the request to send line to the modem to be asserted. The request to send line is a control lead to the modem. This line must be asserted before the interface can transmit data to the modem. Read/write bit; optionally cleared by INIT and master reset.
1	DATA TERM RDY (Data Terminal Ready)	When set, this bit indicates the interface is powered up, programmed, and ready to receive data from the modem. Setting this bit causes the data terminal ready line to the modem to be asserted. The data terminal ready line is a control lead for the modem communication channel. When asserted, it permits the interface to be connected to the channel. Read/write bit; optionally cleared by INIT and master reset.

The receiver data buffer (RXDBUF) and the parameter status register (PARCSR) have the same address location, but RXDBUF is a read-only register and PARCSR is a write-only register. The RXDBUF register detects interface RCVR status flags and RCVR parallel data outputs. Its word format is shown in Figure 5 and described in Table 4. The PARCSR register establishes the overall operating parameters of the DUV11, i.e., the mode of operation (synchronous or isochronous), word length (5, 6, 7, or 8 bits plus parity), parity (enabled or disabled), parity sense (odd or even), and sync character configuration. Its word format is shown in Figure 6 and described in Table 5.

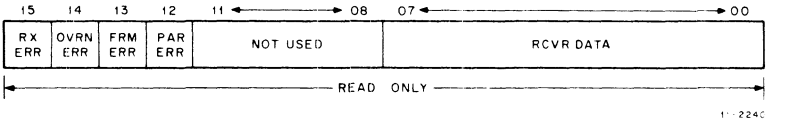


Figure 5 RXDBUF Word Format

Table 4 RXDBUF Word Format

Bit	Name	Description
15	RX ERR (Receiver Error)	This bit is set whenever one of the three receiver error bits is set (logical OR of bits 14, 13, and 12). Read-only bit; cleared only when bits 14, 13, and 12 are cleared.
14	OVRN ERR (Overrun Error)	When set, this bit indicates that the processor has failed to service the RX DONE flag within the time required to load another character into the RXDBUF, i.e., (1/baud rate) X (bits per character) seconds. Hence, the previous character was overwritten (lost). This condition indicates the loss of at least one character. Read-only bit; cleared by INIT, master reset, and DTI SEL 2 (RXDBUF read strobe).

Table 4 RXDBUF Word Format (Cont)

Bit	Name	Description
13	FRM ERR (Framing Error)	When set, indicates that character received was not followed by a valid stop bit. This error only occurs in the isochronous mode of operation. Read-only bit; cleared by INIT, master reset, and DTI SEL 2.
12	PAR ERR (Parity Error)	When set, indicates that the parity of the received character does not agree with the parity programmed (odd or even). If parity is not programmed, this bit is always cleared. Read-only bit; cleared by INIT, master reset, and DTI SEL 2.
7–0	RCVR DATA (Receiver Data)	This register holds the received character for transfer to the program. The buffer is right-justified for 5, 6, 7, or 8 bits. If parity is received it is also loaded into the buffer at the next vacant higher order bit position. Therefore, if a 5-bit character plus parity is framed by the RCVR, the parity bit would be loaded into bit position 5 in the RXDBUF and presented to the program for reading. If an 8-bit character plus parity is framed, the parity bit would not be presented to the program for reading. Read-only buffer; cannot be cleared; INIT or master reset set the buffer to all 1s. Reading the RDXBUF causes the RX DONE bit in the RXCSR to clear.

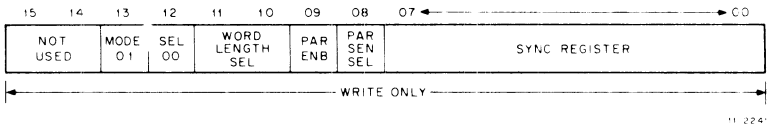


Figure 6 PARCSR Word Format

Table 5 PARCSR Word Format

Bit	Name	Description
13, 12	MODE SEL (Mode Select)	These bits control the mode of operation. Modes are selected as follows:

Mode	Bit 13	Bit 12
Internal Synchronous	1	1
External Synchronous	1	0
Isochronous	0	0
Illegal (not used)	0	1

Write-only bits.

Bit	Name	Description
11, 10	WORD LEN SEL (Word Length Select)	These bits control the length of characters received and transmitted by interface. Word length (not including parity) is selected as follows:

Bits/Char	Bit 11	Bit 10
5	0	0
6	0	1
7	1	0
8	1	1

Write-only bits.

Table 5 PARCSR Word Format (Cont)

Bit	Name	Description
9	PAR ENB	If this bit is set, parity for each character will be (parity enable) generated by the XMTR and checked by the RCVR. If character length is less than eight bits, the parity bit for received data is loaded into the RXDBUF for reading by the program. If bad parity is detected at the RCVR, the parity error flag is set (bit 12 of the RXDBUF). Write-only bit.
8	PAR SEN SEL (Parity Sense Select)	When the parity enable bit (bit 9 of this register) is set, the sense of the parity (odd or even) is controlled by this bit. When this bit is set, even parity is generated by the XMTR and checked for by the RCVR. (The program does not have to provide a parity bit to the XMTR.) When this bit is cleared, odd parity is generated and checked. Write-only bit.
7–0	Sync Register	This register contains the sync character. The sync character is used by the RCVR to detect received sync characters and thereby achieve synchronization. The sync character is used as a fill character by the XMTR when operating in the synchronous mode. Fill characters are operating in the synchronous mode. Fill characters are transmitted when the program fails to provide characters to the XMTR fast enough to maintain continuous transmission, i.e., (1/baud rate) X (bits per character) seconds – 1/2 (bit time).

DUV11

The transmitter status register (TXCSR) is a read/write register that controls the XMTR (transmitter) portion of the interface, controls the resetting and initialization of the interface, and controls and monitors the maintenance mode operation of the interface.

The TXCSR word format is shown in Figure 7 and described in Table 6.

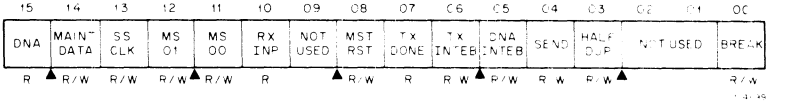


Figure 7 TXCSR Word Format

Table 6 TXCSR Word Format

Bit	Name	Description
15	DNA (Data Not Available)	This bit is set by the XMTR when a fill character is transmitted. This applies only to the synchronous mode of operation and is caused by late program response to a TX DONE interrupt request. The processor response to TX DONE must be within (1/baud rate) X (bits per character) seconds – 1/2 (bit time). If not, the fill character is transmitted. If bit 5 of this register is set, setting this bit causes an XMTR interrupt request. Read-only bit; cleared by INIT, master reset, and DTI SEL 4 (TXCSR read strobe).
14	MAINT DATA (Maintenance Data)	This bit is used in the internal loop and external loop maintenance modes by the diagnostic program to simulate serial input to the RCVR. Read/write bit; cleared by INIT or master reset.

Table 6 TXCSR Word Format (Cont)

Bit	Name	Description
13	SS CLK (Single Step Maintenance Clock)	This bit is used in the internal loop and external loop maintenance modes by the diagnostic program to simulate the XMTR and RCVR clocks. Read/write bit; cleared by INIT or master reset.
12, 11	MS01/MS00 (Maintenance Mode Select 01 & 00)	These bits are used to select the normal mode of operation or one of three maintenance modes. Modes are selected as follows: **Mode** — **Bit 12** — **Bit 11** Normal — 0 — 0 Internal Maintenance Loop — 0 — 1 External Maintenance Loop — 1 — 0 System Test — 1 — 1 Read/write bits; cleared by INIT and master reset.
10	RX INP (Receiver Input)	This bit monitors the RCVR input to the internal loop and external loop maintenance modes. Read-only bit.
8	MSTRST (Master Reset)	This bit is used to generate a CLR (clear) pulse, which initializes the registers and the XMTR and RCVR and inhibits the BRPLY L (bus reply) signal. This bit remains at a (1) for only 3 μs after being set. Read/write bit.

Table 6 TXCSR Word Format (Cont)

Bit	Name	Description
7	TX DONE (Transmitter Done)	This bit is set by INIT and master reset and when the first bit of the character contained in the XMTR register is placed on the XMTR output line. If bit 6 of this register is set when this bit is set, an XMTR interrupt request is generated. Read-only bit; cleared by LD TXDBUF (TXDBUF load strobe).
6	TX INTEB (Transmitter Interrupt Enable)	When set, this bit allows a XMTR interrupt request to be generated by the TX DONE bit. Read/write bit; cleared by INIT and master reset.
5	DNA INTEB (Data Not Available Interrupt Enable)	When set, this bit allows an XMTR interrupt request to be generated by the DNA bit. Read/write bit; cleared by INIT and master reset.
4	SEND (Send)	When set, this bit enables the XMTR and transmission will start when a character is loaded into the TXDBUF. This bit must remain set until the entire message is transmitted. If not, transmission of the character currently in the XMTR register is completed and the XMTR will enter the idle state. Read/write bit; cleared by INIT and master reset.
3	HALF DUP (Half Duplex)	When this bit is set, operation will be in the half-duplex mode. In this mode, the RCVR is disabled whenever bit 4 of this register is set.

Table 6 TXCSR Word Format (Cont)

Bit	Name	Description
		Read/write bit; cleared by INIT and master reset.
0	BREAK (Break)	When this bit is set, the serial XMTR output D5 SERIAL DATA OUT H is held in the space (constant low) condition; otherwise, operation is normal. This bit is used by the diagnostic program in the internal loop or external loop maintenance modes to inhibit the XMTR output while inputting data to the RCVR via bit 14 of this register. Read/write bit; cleared by INIT and master reset.

The transmitter data buffer (TXDBUF) is a write-only register that provides parallel data to the interface XMTR for serial transmission to the modem. The word format for the TXDBUF is shown in Figure 8 and described in Table 7.

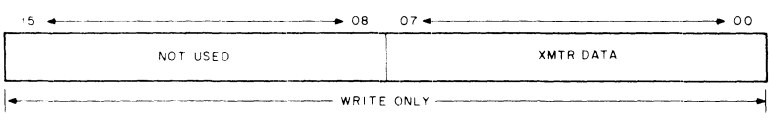


Figure 8 TXDBUF Word Format

Table 7 TXDBUF Word Format

Bit	Name	Description
7-0	XMTR DATA (Transmitter Data)	This register is loaded by the program with the character to be transmitted. Character length is from 5 to 8 bits. The character is right-justified. If a parity bit is enabled, it is generated by the interface. Write-only bits; an INIT or master reset places all 1s in this register.

FUNCTIONAL DESCRIPTION

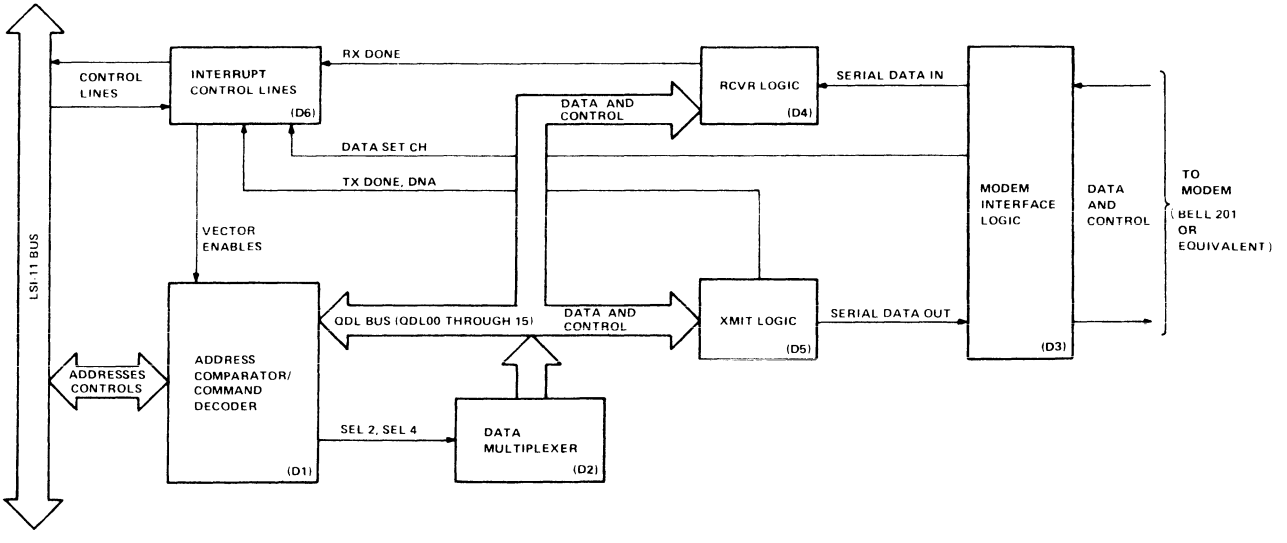
General

The DUV11 interface module can be divided into six functional blocks that will control the data flow between an LSI-11 bus and a Bell 201 modem or equivalent. The major functions, shown in Figure 9, are address comparator/command decoder, data multiplexer, modem interface logic, receiver logic, transmitter logic, and interrupt control logic. The address comparator provides addressable access to the LSI-11 bus and the command decoder receives its control from the LSI-11 bus via the address comparator and direct connections. The data multiplexer receives status data from the modem interface logic, the receiver logic, and the transmitter logic. It also controls the data and status information to the transceivers which is output to the LSI-11 bus. The modem interface logic converts the TTL logic levels to the EIA voltage levels required by the Bell 201 modem. It also contains the transmit data line to the modem and the serial data input line and has access to the modem control signals. The receiver logic accepts the EIA serial input and converts it into parallel data for the LSI-11 bus. The transmitter logic converts the parallel LSI-11 bus data into serial data for transmission over the communications lines. The interrupt control logic enables the DUV11 module to become bus master over the LSI-11 bus by generating a program interrupt to an interrupt address vector.

Address Comparator

The address comparator logic is made up of the bus transceivers and address/vector rocker switches. The rocker switches are set before operatinng the DUV11. When the processor addresses the DUV11, the bus transceivers compare the preset address with the address on the LSI-11 bus (BDAL 00 through 15). If they compare, the MATCH signal is asserted, which enables the command decoder (DC004 chip). Information then received at the transceivers is passed from the LSI-11 bus to the QDL BUS (QDL 00 through QDL 15) under control of the command decoder. Signal INWDB H enables the transceivers to receive data from the Q BUS and place that data onto the QDL BUS. This signal originates from the Q BUS as BDIN L, which is driven to become DIN L. DIN L is applied to the command decoder and is output as INWD L when MATCH is asserted by the address comparator. INWD L is then gated to become INWDB L. Similarly, the signals SEL 0 L, SEL 2 L, and SEL 4 L, which are functions of QDL 00, QDL 01, and QDL 02 when MATCH is asserted to the command decoder, are gated to become EN QDL TO BDAL. This signal enables data from the QDL BUS which is applied to the transceivers to pass on to the LSI-11 bus.

During an interrupt sequence, the address comparator circuitry provides passage of the preset interrupt vector address to the LSI-11 bus.



NOTE:
( ) indicates engineering drawing sheet of logical block.

11-5151

Figure 9 DUV11 Logic Block Diagram

Command Decoder (DC004)
The command decoder logic controls the flow of data into the status registers within the DUV11 and the passage of status information and data back out to the CPU.

The signals that enable the registers of the DUV11 such as LD PARCSR, LD TXDBUF, etc., are generated by gating the outputs of the command decoder. This logic receives bits 0 through 2 from the QDL BUS. When the address comparator outputs MATCH, these bus bits cause the command decoder logic to output the proper select signal. For example, if the control logic selector asserts SEL 6 L along with OUTLB L, the resultant gated output is LD TXDBUF (1) L, which causes the transmitter data buffer to load parallel data from the QDL BUS.

Data Multiplexer
The data multiplexer controls the passage of DUV11 status signals and data to the bus transceivers for output to the CPU. Two signals, SEL 2 L and SEL 4 L, enable the selection of status signals and data which will pass on to the QDL BUS.

Modem Interface Logic
The modem interface logic contains level converters to change the logic level signals to the operating voltage levels of the Bell 201 modem. All logic signals ranging from 2.4 to 3.5 V are converted to +6 V. All ground (0 V) logic signals are converted to −6 V.

Receiver Control Logic
The receiver circuitry contains the synchronous/asynchronous receiver chip (SAR) and its supportive logic. Within the SAR, serial data received from the modem is converted to parallel data for output onto the QDL BUS. Parameter data is supplied via the QDL BUS. PARCSR (1) L loads this data into SAR. Having stored these parameters, the receiver detects the serial received character, accomplishes synchronization, frames the received character, detects errors, raises the RX DONE flag, and holds the framed character (for program reading) until the next character is framed.

Once the RCVR logic is enabled, it operates as programmed. The SCH SYNC input enables the RVCR logic. The contents of the PARCSR determine:

1. Mode of operation (internal synchronous, external synchronous, or isochronous)

2. Length of character to be framed (5, 6, 7, or 8 bits plus parity)

3. Parity (enabled or disabled)

4. Parity sense (odd or even)

5. Sync character configuration.

The method of achieving synchronization is the principal difference between the modes of operation.

1. In the internal synchronous mode, two contiguous sync characters must be recognized by the RCVR logic to achieve synchronization. Once synchronization is achieved, the RCVR starts framing on the very next character bit. The received characters must arrive at the RCVR in a continuous serial bit stream or synchronization will be lost.

2. The external synchronous mode is designed for use with communication equipment which accomplishes synchronization external to the DUV11 interface. The external synchronization logic prohibits RCVR operation by inhibiting the assertion of SCH SYNC until synchronization with the XMTR has been achieved. When external synchronization is achieved, SCH SYNC asserts, forcing the CVR logic to the synchronized state. The RCVR then starts framing immediately, beginning with the very next character bit.

3. In the isochronous mode, each received character is preceded by a start bit and succeeded by a stop bit, which serves to synchronize the RCVR. In this mode, the receiver simply does not start framing until it recognizes a start bit. It then frames the character following the start bit and looks for a stop bit. If a stop bit is not detected, the character received is considered invalid, flagged as such, and held for reading by the program. Hence, in the isochronous mode, characters need not be preceded by sync characters and need not arrive contiguously at the RCVR.

The strip synchronization character (STRIP SYNC) input determines whether received sync characters are to be permitted to set the RX DONE flag. If STRIP SYNC is asserted, all sync characters are discarded provided no errors are detected.

Transmitter Control Logic

The transmitter circuitry contains the synchronous/asynchronous transmitter chip (SAT) and its supportive logic. The SAT accepts parallel characters from the program, raises the TX DONE flag to request the next character, and serially outputs the current character to the modem. Before transmitter operation can begin, the transmitter logic must be initialized and the PARCSR and TXCSR registers programmed.

The high-order bits from the QDL BUS are loaded into the XCSR when signal LD TXCSR HB H is asserted. The low-order bits are loaded into

the TXCSR when LD TXCSR LB H is asserted. The signal LD PARCSR (1) L asserted enables parameter data into the SAT.

The signal SEND (1) H enables the transmitter logic. Once the transmitter is enabled, it operates as programmed. The contents of the PARCSR determine:

1. Mode of operation (synchronous or isochronous)
2. Length of character to be transmitted (5, 6, 7, or 8 bits plus parity)
3. Parity (enabled or disabled)
4. Parity sense (odd or even)
5. Sync character configuration (used as fill character in synchronous mode).

There are distinct differences between the two modes of operation:

1. In the synchronous mode, the XMTR receives a parallel transmit character from the program, generates parity if programmed, serially outputs the character plus parity to the modem, and raises the TX DONE flag to request the next character. If the program fails to provide the next character before transmission of the current character is complete, the XMTR outputs fill characters to maintain continuous transmission until another data character is provided. Whenever a fill character is transmitted, the data not available (DNA) flag is raised to notify the program of fill character transmission.
2. In the isochronous mode, the XMTR receives a parallel transmit character from the program, generates parity if programmed, outputs a start bit, serially outputs the character plus parity, outputs a stop bit, and raises the TX DONE flag to request the next character. However, in the isochronous mode, if the program fails to provide the next character before transmission of the current character is complete, the XMTR simply pauses until the next character is provided. Hence, the DNA flag is never used in the isochronous mode.

The break input inhibits the XMTR output. Whenever the TXCSR break bit is set, the break input to the XMTR logic asserts and inhibits the XMTR output. This input enables the program to inhibit the XMTR output, while inputting data directly to the RCVR via the RCVR input select logic in the internal and external loop maintenance modes.

Interrupt Control Logic

The interrupt control logic consists of two DC003 chips and associated driving circuitry. When the interrupt control logic receives either RXDONE (1) H, TXDONE (1) H, DATA SET CH (1) H, or DNA H with their associated interrupt enable signal, it generates BIRQ L (interrupt request) to the processor. The processor responds with BIAKI L (interrupt acknowledge in), which searches the logic for the originator of the interrupt. If the interrupt was not originated at the DUV11, the signal BIAKO L (interrupt acknowledge out) is passed through with no action taken. If the DUV11 had originated the request, EN VEC to BUS H is asserted and, depending on the particular interrupt, EN UPPER VEC H may also be asserted. This signal asserted then causes the addressing logic to load, onto the LSI-11 bus, the contents of the preset vector address rocker switches. The processor will then perform the preprogrammed subroutine for that interrupt vector address.

Clear Logic

The clear logic generates clear (CLR) and optional clear (OPT CLR), which initialize all DUV11 logic. The INIT signal or MSTRST asserted will activate the clear signals. INIT is a function of BINIT, which is received by the interface whenever the computer activates the go function, the processor executes a reset instruction, or the power-fail sequence occurs. The clear logic outputs are asserted as long as the BINIT signal remains low. MSTRST is program-controlled and is generated by setting bit 8 of the TXCSR. When bit 8 of the TXCSR is set and LD TXCSR HB goes low, a 3 μs one-shot asserts MSTRST and the clear signals remain active for the duration of the one-shot.

The OPT CLR output resets RXCSR bits 1, 2, and 3 and thereby clears the control lines to the modem. By not selecting SW1 option switch, OPT CLR is disabled, allowing the DUV11 to be cleared without having to repeat the handshaking sequence. BRPLY is also inhibited as long as CLR is asserted.

Clock Control Logic

The clock control logic decodes the maintenance mode select bits and assigns the transmitter and receiver clocks. There are three possible clock sources: the modem, the programmable SS CLK (single step clock), and the system test clock. If the normal operating mode is decoded, the modem clocks are selected. MS00 (0) H is asserted, enabling the modem clock inputs (TRS CLK and REC CLK). If the internal loop or external loop maintenance mode is decoded, the SS CLK is selected. This program-controlled clock can be operated very slowly to facilitate troubleshooting. In the internal loop mode, MS00 (1) H is asserted, enabling the SS CLK (1) H. In the external loop mode, MS01 (1) H and MS00 (0) H are asserted, enabling SS CLK (0) H, TRS CLK, and

REC CLK. SS CLK (0) H drive CLK EXT, which is routed to the modem test connector, looped back and applied to the TRS CLK and REC CLK inputs. If the system test mode is decoded, the system test clock is selected. This output provides an asynchronous clocking source for the system test mode. MS01 (1) H and MS00 (0) H are asserted, enabling the internal system test clock to drive the transmitter and receiver. In this mode, the modem clock inputs (TRS CLK and REC CLK) are inhibited. When the DUV11 is transmitting in the half-duplex mode, REC CLK is inhibited. HALF DUP (0) L and SEND (0) L go high in this condition, inhibiting REC CLK from reaching the receiver.

+12 to -12 Power Converter

Circuitry is provided to produce -12 Vdc for use by the EIA drivers, the SAT, and the SAR chips. A 600 kHz clock is used to switch +12 V into a capacitor network to produce approximately -20 V unregulated. This unregulated voltage is then regulated to -12 V at the output of two twin zener diode networks. The zeners keep the -12 V to within ±5%.

Maintenance Indicators

Indicators in the form of light-emitting diodes are provided to display data lines and modem control states for maintenance purposes. Any of the following lines asserted will cause its respective LED to illuminate: RING H, CLR TO SEND H, DATA SET RDY H, CARRIER H, SERIAL DATA OUT H, and SERIAL DATA IN H.

DZV11 ASYNCHRONOUS MULTIPLEXER

GENERAL

The DZV11 is an asynchronous multiplexer interface module that interconnects the LSI-11 bus with up to four asynchronous serial data communications channels. The module provides EIA interface levels and enough data set control to permit dial-up (auto-answer) operation with modems using full-duplex operations such as Bell models 103, 113, 212, or equivalent. The DZV11 does not support half-duplex operations such as remote operation over private lines for full-duplex point-to-point or full-duplex multipoint as a control (master) station. The DZV11-B includes a BC11U cable assembly for interconnection to the communication devices.

The DZV11-B interface consists of the M7957 module, a BC11U-25 interface cable, and two accessory test connectors (H329 and H325). The H329 connector permits a staggered loopback. The H325 connector is used with the BC11U cable to provide a single-line loopback.

FEATURES

- Selectable baud rates of 50 to 9600
- Character length of 5-, 6-, 7-, or 8-level code
- Stop bits, 1 or 2, for 6-, 7-, and 8-level code
- Stop bits, 1 or 1.5, for 5-level code
- Parity generation and detection for odd, even, and no parity
- Transmitter and receiver interrupts
- Generates and detects break signals

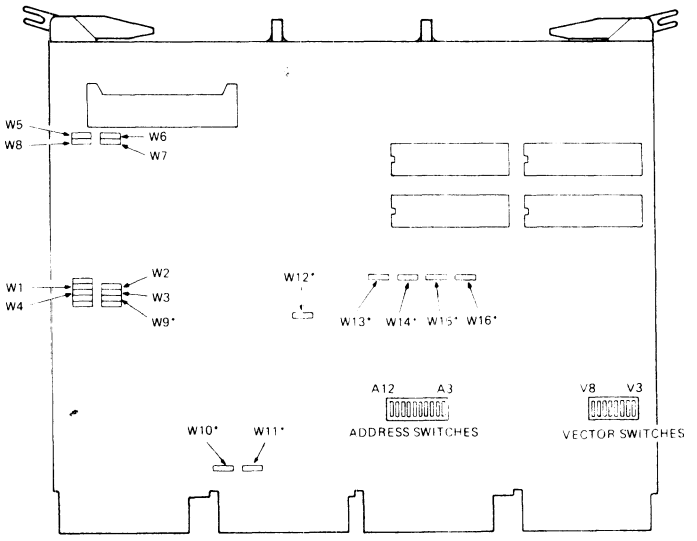
SPECIFICATIONS

Identification	M7957
Size	Quad
Power	+5 Vdc ± 5% at 1.15 A +12 Vdc ± 3% at 0.40 A
Bus Loads	
AC	4.1
DC	1
Performance	Interface signals meet EIA standard RS-232C

CONFIGURATION

General

The software control of the DZV11 is performed by six device registers. These registers are assigned addresses and can be read or loaded by the program. DIGITAL software requires that the device addresses be within the range of 160000 to 177777. The M7957 module utilizes the floating address space that starts at 160010 and extends to 164000. The control and status register (CSR) is assigned the basic address by setting the rocker switches of E30 on the module as shown in Figure 1. The correlation between the bit assignments and the switches are detailed in Figure 2. The remaining register addresses will sequentially follow the basic address as shown in Table 1. A basic address is preset at the factory; if the user requires a different address, the switches allow him to change the addresses to comply with his system. The interrupt vector is also programmable and can be used with DIGITAL software, provided that the address is within 300 to 777. The switches of E2 on the module (Figure 1) allow the user to select an interrupt vector to function within his system. The correlation between the bit assignments and the switches are detailed in Figure 3.



*NOTES

JUMPERS W9, W12, W13, W14, W15, AND W16 ARE REMOVED ONLY FOR MANUFACTURING TESTS. THEY SHOULD NOT BE REMOVED IN THE FIELD.

JUMPERS W10 AND W11 MUST REMAIN INSTALLED WHEN THE MODULE IS USED IN A BACKPLANE THAT SUPPLIES LSI-11 BUS SIGNALS TO THE C AND D CONNECTORS OF THE DZV11 (SUCH AS THE H9270). WHEN THE MODULE IS USED IN A BACKPLANE THAT INTERCONNECTS THE C AND D SECTIONS TO AN ADJACENT MODULE, JUMPERS W10 AND W11 MUST BE REMOVED.

Figure 1 M7957 Module

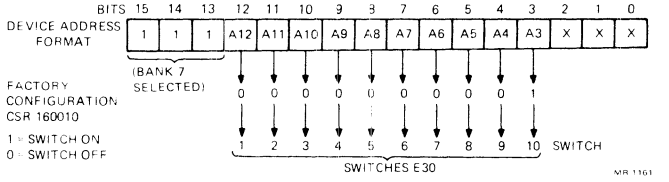


Figure 2 DZV11 CSR Address Bits

Table 1 DZV11 Register Address Assignments

Register	Mnemonic	Address*	Read/ Write
Control and Status	CSR	76XXX0	R/W
Receiver Buffer†	RBUF	76XXX2	R
Line Parameter †	LPR	76XXX2	W
Transmitter Control	TCR	76XXX4	R/W
Modem Status †	MSR	76XXX6	R
Transmit Data †	TDR	76XXX6	W

*XXX = Selected in accordance with floating device address scheme.
†Dual-purpose register.

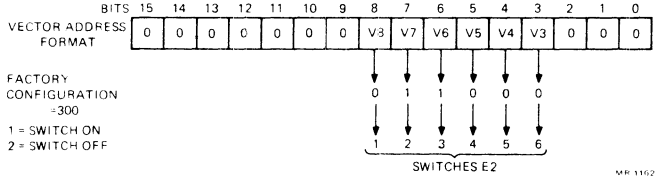


Figure 3 DZV11 Vector Bits

Jumpers

Modem Control – There are eight jumpers (W1–W8) used for modem control. Jumpers W1 through W4 connect data terminal ready (DTR) to request to send (RTS). This allows the DZV11 to assert both DTR and RTS when using a modem that requires the control of RTS. These jumpers must be installed to run the external cable and test diagnostic programs. Jumpers W5 through W8 connect the forced busy leads to the

request to send leads. When these jumpers are installed, the assertion of an RTS signal places an ON or busy signal on the corresponding forced busy lead. Forced busy jumpers W5–W8 are normally removed unless they are required for the modem. These modem control jumpers are listed in Table 2.

Table 2 MODEM Control Jumper Configuration

Jumper	Connection	Line
W1	DTR to RTS	03
W2	DTR to RTS	02
W3	DTR to RTS	01
W4	DTR to RTS	00
W5	RTS to FB	03
W6	RTS to FB	02
W7	RTS to FB	01
W8	RTS to FB	00

Bus Signals – Jumpers W10 and W11 must remain installed when the module is used in a backplane that supplies bus signals to C and D connectors such as the H9270. When the module is in a backplane that utilizes the C–D interconnect scheme (such as the H9273), then jumpers W10 and W11 must be removed.

Testing – Jumpers W9 and W12 through W16 are removed for manufacturing test purposes only. These jumpers should not be removed by the user.

Device Registers

All software control of the DZV11 is performed by six device registers. Each register is assigned a bus address that can be read or loaded. The following paragraphs define the bits within a register and their specific function to the operation of the DZV11. Bits that are designated as "not used" and "write only" are always read as zero and attempts to load these bits will have no effect on the operation.

Control and Status Register – The control and status register (CSR) is a byte and word addressable register. All bits in the CSR are cleared by an occurrence of BINIT or by setting device master clear (CSR 4). The format is shown in Figure 4 and the bit assignments are listed in Table 3.

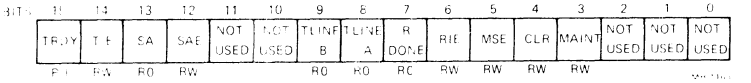


Figure 4 CSR Bit Assignments

Table 3 CSR Bit Assignments

Bit	Name	Description
0–2	Not used	
3	Maintenance	This bit, when set, loops all the transmitter's serial output leads to the corresponding receiver's serial input leads on a TTL basis. While operating in maintenance mode, the EIA received data leads are disabled. Normal operating mode is assumed when this bit is cleared. This bit is a read/write bit.
4	Master Clear	When written to a one, generates "initialize" within the DZV11. A readback of the CSR with this bit set indicates initialize in progress within the device. This bit is self-clearing. All registers, silos, and UART are cleared with the following exceptions: 1. Only bit 15 of the receiver buffer register (valid data) is cleared; the remaining bits 0 through 14 are not. 2. The high byte of the transmitter control register is not cleared by master clear. 3. The modem status register is not cleared by master clear.

Table 3 CSR Bit Assignments (Cont)

Bit	Name	Description
5.	Master Scan Enable	This read/write bit must be set to permit the receiver and transmitter control sections to begin scanning. When cleared, transmitter ready (CSR bit 15) will be inhibited from setting and the received character buffers (silos) will be cleared.
6	Receiver Interrupt Enable	This bit, when set, permits the setting of CSR bits 7 and 13 to generate a receiver interrupt request. This bit is a read/write bit.
7	Receiver Done	This is a read-only bit that will set when a character appears at the output of the FIFO buffer. To operate in interrupt per character mode, CSR bit 6 must be set and CSR bit 12 must be cleared. With CSR bits 6 and 12 cleared, character flag mode would be indicated. Receiver done will clear when the receiver buffer register (RBUF) is read or when master scan enable (CSR bit 5) is cleared. If the FIFO buffer contains an additional character, the receiver done flag will stay cleared a minimum of 1 μs before presenting that character.
8–9	Transmitter Line Number	These read-only bits indicate the line number whose transmit buffer requires servicing. These bits are valid only when transmitter ready (CSR bit 15) is set and will be cleared when master scan enable is cleared. Bit 8 is the least significant bit.
10–11	Not used	
12	Silo Alarm Enable	This is a read/write bit; when set, enables the silo alarm counter to keep count of the number of characters stored in the FIFO buffer. The counter will be cleared when the silo alarm enable bit is cleared. Conditioning of this bit must occur prior to any character reception.

Table 3 CSR Bit Assignments (Cont)

Bit	Name	Description
13	Silo Alarm	This is a read-only bit set by the hardware after 16 characters have been entered into the FIFO buffer. Silo alarm will be held cleared when silo alarm enable (CSR bit 12) is cleared. This bit will be reset by a read to the receiver buffer register and will not set until 16 additional characters are entered into the buffer. If receiver interrupt enable (CSR bit 6) is set, the occurrence of silo alarm will generate a receiver interrupt request. Reception with CSR bit 6 cleared permits flag mode operation of the silo alarm bit.
14	Transmitter Interrupt Enable	This bit must be set for transmitter ready to generate an interrupt. It is a read/write bit.
15	Transmitter Ready	This bit is read-only and is set by the hardware. This bit will set when the transmitter clock stops on a line whose transmit buffer may be loaded with another character and whose associated TCR bit is set. The transmitter line number, specified in CSR bits 8 and 9, is only valid when transmitter ready is set. Transmitter ready will be cleared by any of the following conditions: 1. Master scan enable cleared 2. When the associated TCR bit is cleared for the line number pointed to in CSR bits 8 and 9 3. At the conclusion of the load instruction of the transmit data register (low byte only). If additional transmit lines require service, transmitter ready will reappear within 1.4 μs from the completion of the transmit data register load instruction. The occurrence of transmitter ready with transmitter interrupt enable set will generate a transmitter interrupt request.

Receiver Buffer – The receiver buffer (RBUF) is a 16-bit read-only register which contains the received character at the output of the FIFO buffer. A read of the register causes the character entry to be extracted from the buffer and all other entries to bubble down to the lowest unoccupied location. Only the valid data bit (RBUF bit 15) is cleared by BINIT or by setting device master clear (CSR bit 4). Bits 0–14 are not affected. The bit assignments for the RBUF register are listed in Table 4 and the format is shown in Figure 5.

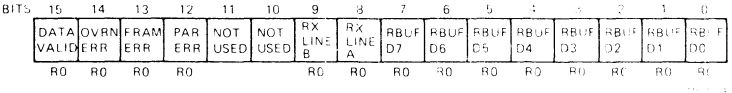


Figure 5 Receiver Buffer Bit Assignments

Table 4 RBUF Bit Assignments

Bit	Name	Description
0–7	Received Character	These bits contain the received character, right-justified. The least significant bit is bit 0. Unused bits are 0. The parity bit is not shown.
8–9	Received Character Line Number	These bits contain the line number upon which the aforementioned character was received. Bit 8 is the least significant bit.
10–11	Not used	
12	Parity Error	This bit is set if the sense of the parity of the received character does not agree with that designated for that line.
13	Framing Error	This bit is set if the received character did not have a stop bit present at the proper time. This bit is usually interpreted as indicating the reception of a break.
14	Overrun Error	This bit is set if the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer on that line.

Table 4 RBUF Bit Assignments (Cont)

Bit	Name	Description
15	Valid Data	This bit, when set, indicates that the data presented in bits 0–14 is valid. This bit permits the use of a character-handling program that takes characters from the FIFO buffer until there are no more available. This is done by reading this register and checking bit 15 until the program obtains a word for which bit 15 is zero.

Line Parameter Register – The line parameter register (LPR) controls the operating parameters associated with each line in the DZV11. The LPR is a word-addressable, write-only register. The line parameters for all lines must be reloaded following an occurrence of either BINIT or device master clear. Table 5 lists bit assignments and the format is shown in Figure 6.

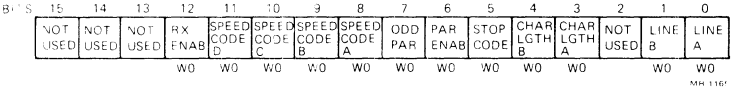


Figure 6 Line Parameter Register Bit Assignments

Table 5 LPR Bit Assignments

Bit	Name	Description
0–1	Parameter Line Number	These bits specify the line number for which the parameter information (bits 3 through 12) is to apply. Bit 0 is the least significant bit. This bit must always be written as a zero when specifying the parameter line number. Writing this bit as a one will extend the parameter line number field into nonexistent lines. Parameters for lines 0 through 3 will not be affected.
2	Not used	

Table 5 LPR Bit Assignments (Cont)

Bit	Name	Description
3–4	Character Length	These bits are set to receive and transmit characters of the length (excluding parity) shown below.

4	3	
0	0	5-bit
0	1	6-bit
1	0	7-bit
1	1	8-bit

5	Stop Code	This bit sets the stop code length (0 = 1-unit stop, 1 = 2-unit stop, or 1.5-unit stop if a 5-level code is employed).
6	Parity Enable	If this bit is set, characters transmitted on the line have an appropriate parity bit affixed; characters received on the line have their parity checked.
7	Odd Parity	If this bit and bit 6 are set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set but bit 6 is set, characters of even parity are generated on the line and incoming characters are expected to have even parity. If bit 6 is not set, the setting of this bit is immaterial.
8–11	Speed Code	The state of these bits determines the operating speed for the transmitter and receiver of the selected line.

11	10	9	8	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200

Table 5 LPR Bit Assignments (Cont)

Bit	Name	Description				
		11	**10**	**9**	**8**	**Baud Rate**
		1	0	0	0	1800
		1	0	0	1	2000
		1	0	1	0	2400
		1	0	1	1	3600
		1	1	0	0	4800
		1	1	0	1	7200
		1	1	1	0	9600
		1	1	1	1	Invalid
12	Receiver Enable	This bit must be set before the UART receiver logic can assemble characters from the serial input line. This bit will be cleared following a BINIT or device master clear.				
13-15	Not used					

Transmitter Control Register – The transmitter control register (TCR) is a byte- and word-addressable register. The low byte of the TCR contains the transmitter control bits which must be set to initiate transmission on a line. Each TCR bit position corresponds to a line number. For example, TCR bit 0 corresponds to line 0, bit 1 to line 1, etc. Setting of a TCR bit causes the transmitter scanner clock to stop if the UART for this line has a transmit buffer empty condition. An interrupt will then be generated if transmitter interrupt enable is set. The scanner clock will restart when either the transmit data register is loaded with a character or the TCR bit is cleared for the line on which the clock has stopped. TCR bits must only be cleared when the scanner is not running. The format is shown in Figure 7.

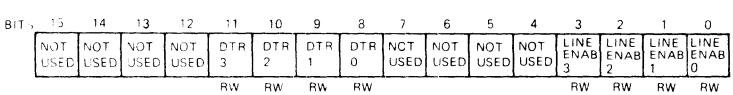


Figure 7 Transmitter Control Register Bit Assignments

The TCR bits are represented in bits 0 through 3. These bits are read/write and cleared by BINIT or device master clear. Bits 4 through 7 are unused and read as zero.

The high byte of the TCR contains the writable modem control lead, data terminal ready (DTR). Bit designations are as follows.

Bit	Name
8	DTR Line 0
9	DTR Line 1
10	DTR Line 2
11	DTR Line 3
12–15	Unused. Read as zero

Assertion of a data terminal ready bit puts an ON condition on the appropriate modem circuit for that line. Data terminal ready bits are read/write and cleared only by BINIT. Jumpers have been provided to allow the request to send circuits to be asserted with data terminal ready assertions.

Modem Status Register – The modem status register (MSR) is a 16-bit read-only register. A read to this register results in the status of the readable modem control leads, ring and carrier. The ON condition of a modem control lead is interpreted as a logical 1. Bits 4 through 7 and 12 through 15 are unused and read as a zero. Remaining bit designations are shown in Figure 8 and explained below.

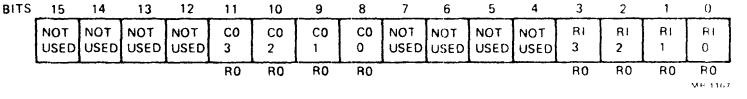


Figure 8 Modem Status Register Bit Assignments

Bit	Name
0	Ring Line 0
1	Ring Line 1
2	Ring Line 2
3	Ring Line 3
4–7	Unused. Read as zero.
8	Carrier Line 0
9	Carrier Line 1
10	Carrier Line 2
11	Carrier Line 3
12–15	Unused. Read as zero.

Transmit Data Register – The transmit data register (TDR) is a byte- and word-addressable, write-only register. Characters for transmission are loaded into the low byte. TDR bit 0 is the least significant bit. Loading of a character should occur only when transmitter ready (CSR bit 15) is set. The character that is loaded into this register is directed to the line defined in CSR bits 8 and 9. The high byte of the transmit data register is designated as the break control register. The bit designations are shown in Figure 9.

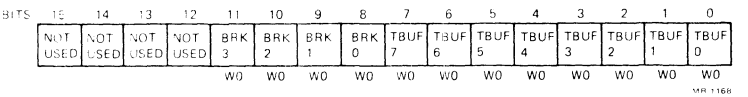


Figure 9 Transmit Data Register Bit Assignments

Each of the four multiplexer lines has a corresponding break bit for that line. TDR bit 8 represents the break bit for line 0, TDR bit 9 for line 1, etc. TDR bits 12 through 15 are unused. Setting a break bit will force that line's output to space. This condition will remain until cleared by the program. This register is cleared by BINIT or device master clear. The break control register can be utilized regardless of the state of the device maintenance bit (CSR bit 3).

FUNCTIONAL DESCRIPTION

General

The DZV11 module transmits communication data from the LSI-11 bus, through the interface, to the transmitter data register in the UARTs. There it is converted from parallel data to serial data and sent to the EIA transmitters. The transmitters convert the serial data from TTL levels to EIA levels and send it to the communication line. A functional diagram of the module is shown in Figure 10.

Data coming in from the communication lines is converted from EIA to TTL by the EIA receivers, then from serial to parallel by the UARTs. The parallel data leaves the UART receiver buffers and is stored in the silo buffer. From there it is transferred via multiplexers to the bus interface. The bus interface places the data on the LSI-11 bus.

The interrupt logic requests interrupt service when a transmitter is empty and when the silo buffer has either 1 or 16 characters of received data, as selected by the program.

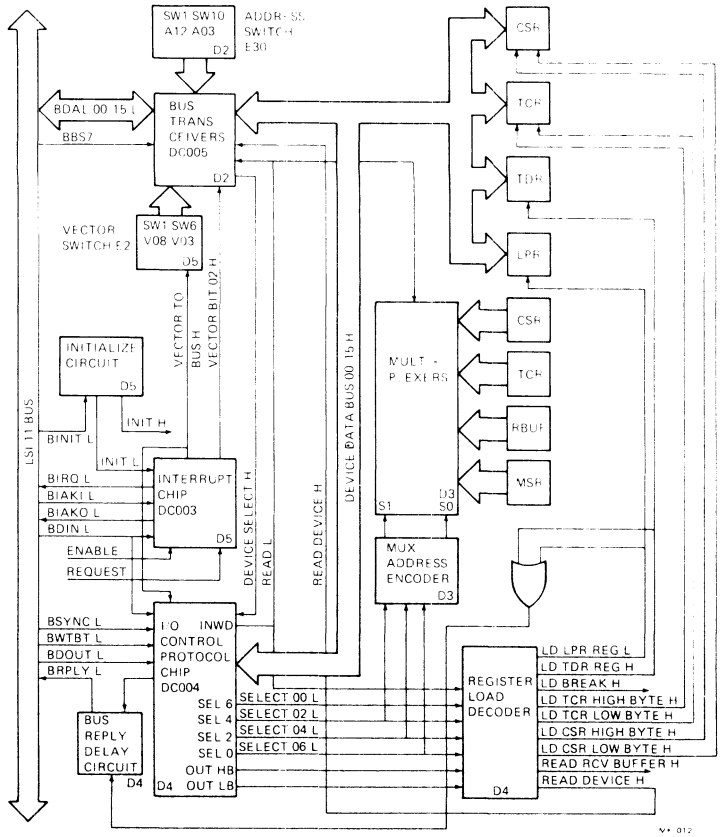


Figure 10 Bus Interface, I/O Control, and Interrupt Logic

The transmitter control determines which of the four possible lines is to be used, and controls the loading of the data.

The receiver control scans the receiver status and controls the loading and unloading of the silo.

The speed and format control generates clock signals for the UARTs. Under program control, it selects baud rate and stop bit, parity bit, and character length parameters.

The break logic inhibits output data to create a break signal. The four lines operate independently and under program control.

The maintenance mode data selector provides the capability of switching the data outputs and the data inputs. This is used to verify module operation.

The power supplies convert voltages available on the LSI-11 bus into other voltages also required by the module.

Bus Interface

Data and control signals move between the LSI-11 bus and the DZV11 transmit and receive circuitry by means of a group of bus transceivers, multiplexers, and latches. Figure 10 indicates the functional relationship of these circuits to the addressable device registers.

The bus transceivers are contained in four DC005 transceiver chips. These interface LSI-11 bus lines BDAL 00 through BDAL 15 to the module's internal device data bus lines 0 through 15. The device data bus lines have three logical conditions: TTL low, TTL high, and disabled. The disabled state has a very high impedance. This permits the internal bus lines to be used in both directions by high-speed, low-power devices.

The transceiver chips also perform the functions of address decoding and vector generation. Address decoding is accomplished by comparing the states of BDAL 03 through BDAL 12 with the states selected by address switches A03 through A12 (switches 10 through 1, respectively, on switch pack E30). When the LSI-11 addresses an I/O device, it asserts BBS7 L (bank select 7) during address time. This indicates that the address is in the 28–32K range of addressing space, and enables the DC005 transceivers to decode the address. If the address matches the switch selection, the circuit asserts DEVICE SELECT H to the I/O control logic.

During data time, the transceivers transfer data from the LSI-11 bus lines to the device data bus lines if the operation is an output data transfer. If the operation is a input data transfer, the I/O control logic asserts READ L and READ DEVICE H. This switches the transceivers to their opposite state, in which they transfer data from the device data bus to the LSI-11 bus.

The bus interface logic generates vector addresses under the control of the interrupt logic and vector address switches V03 through V08 (switches 6 through 1, respectively, on switch pack E2.) The vector switches set the states of vector bits 3 through 8 when the interrupt

logic enables vector generation. Bit 2 is controlled directly by the interrupt logic. It is set for a transmitter interrupt and cleared for a receiver interrupt.

When an interrupt occurs, the conditions selected by the vector switches are immediately placed on the LSI-11 bus lines. The transceivers do this without need of READ L or READ DEVICE H from the I/O control circuit.

I/O Control
The I/O control logic controls the flow of status bits and data bits between the LSI-11 and the device registers. It monitors the three least significant bits of the address word to determine which register is to be read or loaded, and which byte in the register is affected. It monitors BWTBT L (write byte) to determine if a byte is being loaded or a word is being loaded. (The LSI-11 can write bytes, but reads only words.) Control signals BDIN L and BDOUT L indicate whether data is to be moved into the computer or out of it.

The major element in the I/O control circuit is a DC004 protocol chip. The chip uses device data bus bits 1 and 2 to decode the device register address and then asserts one of four register select lines. It uses device data bus bit 0 and BWTBT L to select either OUT HB for a high byte or OUT LB for a low byte. If the operation is an output data transfer (indicated by BDOUT L), the register load decoder uses OUT LB or OUT HB (or both) and the register select signals to produce a load pulse. The load pulse enables the proper byte or bytes of the selected register to be loaded from the device data bus.

The register select lines are also used to control the address lines on a group of eight multiplexers. If the operation is an input data transfer (indicated by BDIN L), the I/O control switches the multiplexers to the selected register and asserts READ L and READ DEVICE H. READ L enables the multiplexers to place the data from the selected register onto the device data bus. READ L and READ DEVICE H together enable the bus transceivers to transfer the data from the device data bus to the LSI-11 bus.

Vector Operation – The I/O control has the additional function of asserting BRPLY L in response to VECTOR-TO-BUS H from the interrupt control circuit. This action is part of the interrupt sequence, and is independent of the BSYNC L and DEVICE SELECT H.

Initialize Circuit – This circuit produces two initialization signals (INITIALIZE H and INITIALIZE L) when it receives either BINIT L from the LSI-11 bus or the master clear bit from the CSR. In addition, both input signals generate other clear signals. The initialization and clear signals clear the registers and latches on the module to set initial conditions.

Interrupt Logic
Most of the logic for interrupts is contained in a single DC003 interrupt chip. The chip contains two interrupt channels: one for receiver interrupts and one for transmitter interrupts. The circuit generates a receiver interrupt either when the RBUF has one character ready for the computer (receiver done interrupt) or when the silo buffer has 16 characters ready (silo alarm interrupt.)

The receiver done interrupt is enabled by setting CSR bit 6. The silo alarm interrupt is enabled by setting bit 12. Setting bit 12, however, inhibits the receiver done signal from the RBUF. Therefore, receiver done interrupts do not occur when silo alarm interrupts are enabled.

The circuit generates a transmitter interrupt when the transmitter data register is empty and ready for another data output from the computer. The transmitter ready interrupt is enabled by setting CSR bit 14.

Both the transmitter and receiver interrupt enable bits are located physically in the DC003 interrupt chip although they are functionally part of the CSR.

The LSI-11 bus interrupt acknowledge signal (BIAKI L/BIAKO L) is daisy-chained through the devices on the LSI-11 bus. A device priority is established by its position in the interrupt acknowledge daisy-chain. In the DZV11 interrupt logic, the chain goes through both the receiver section and the transmitter section of the interrupt chip. It passes through the receiver section first, thereby giving receiver interrupts priority over transmitter interrupts.

Interrupt Transactions – When interrupts are enabled and a condition requiring service occurs, the interrupt sequence proceeds as follows:

1. The interrupt logic asserts BIRQ L, the interrupt request line.

2. The LSI-11 bus responds to BIRQ L by asserting BDIN L and then BIAKI L. BIAK is the bused interrupt acknowledge signal. It is passed down the priority chain until it reaches the section of the interrupt chip that initiated the request.

3. When the interrupt logic receives both BDIN L and BIAKI L, it asserts VECTOR-TO-BUS H to the vector selection switches. If the interrupt is a transmitter interrupt, the circuit also asserts VECTOR BIT 02 H. This signal adds four to the base (receiver interrupt) vector that is asserted by VECTOR-TO-BUS H. The circuit also negates BIRQ L.

4. VECTOR-TO-BUS H causes the I/O control logic to issue BRPLY L to the LSI-11. VECTOR-TO-BUS H and, if applicable, VECTOR BIT 02 H cause the bus transceivers to place the selected vector on the LSI-11 bus lines.

5. The computer reads in the interrupt vector and then, as a result of receiving BRPLY L, negates BDIN L. Shortly after this, it also negates BIAKI L.

6. The interrupt logic negates VECTOR-TO-BUS H and, if applicable, VECTOR BIT 02 H.

7. The negation of VECTOR-TO-BUS H causes the I/O control logic to negate BRPLY L and the bus transceivers to remove the vector from the LSI-11 bus lines.

An interrupt transaction does not require BBS7 L, DEVICE SELECT H, BSYNC L, or READ L. The interrupt logic overrides the normal I/O protocol.

A silo alarm interrupt can be distinguished from a receiver done interrupt by checking the corresponding bits in the CSR when entering a service routine.

EIA Receivers

The DZV11 receives three modem signals for each of the four communication lines it interfaces. Carrier detect, ring indicator, and received data are received and converted from EIA levels to TTL levels. The carrier and ring signals go to the modem status register. The received data signals go to the RBUF (in the UARTs).

EIA Transmitters

The DZV11 can control up to three modem control signals for each of the four communication lines it interfaces. Control bits from the transmitter control register are converted from TTL levels to EIA levels to drive modem control lines. For each line there is a single control bit that is always connected to data terminal ready. These signals may be jumpered to also control request to send. If this is done, they may then be further jumpered to control forced busy (for Bell model 013E and 113B modems with the forced busy option).

Data to be transmitted from the computer to the lines moves from the transmitter data buffer to the EIA transmitters, where it is converted from TTL levels to EIA levels and placed on the lines.

UARTs

The DZV11 uses four universal asynchronous receiver/transmitter (UART) chips, one for each of the four communication lines. Each UART performs part of the functions of the receiver buffer (RBUF), transmitter data register (TDR), and line parameter register (LPR) for the channel under its control. The RBUF takes serial data received by the EIA receivers, strips off the start, stop, and parity bits, converts it to parallel data, and places it on the device data bus. The TDR takes parallel data from the device data bus, appends start, stop, and parity bits, converts it to serial data, and sends it to the EIA transmitters. The LPR controls the speed, parity, and number of stop bits that the RBUF and TDR use.

Setting Line Parameters – The low byte of the LPR is contained inside the UARTs, and controls the data format. The high byte is contained in the baud rate generator circuits and controls the speed at which data is transmitted and received.

When the computer addresses the LPR, the I/O control logic generates a load pulse. The load pulse enables LPR bits 0 and 1 to strobe the selected UART and baud rate generator. Bits 3 through 7 are latched into the UART to select the data format. Bits 8 through 11 are latched into the baud rate generator to select the speed. Bit 12 enables the receiver clock signal to reach the UART.

UART Receiver Operation – Serial data coming in from the EIA receiver is applied to the receiver section of the selected UART. The UART samples the serial input at the receiver clock rate (16 times the data bit rate.) The line is in a continuous marking state when idle. When a start bit arrives, the UART detects the mark-to-space transition. It samples the line again at the time corresponding to the middle of the start bit. If the line is marking, the UART logic assumes that the first sample was noise, and resumes sampling. If it finds that the line is still spacing, however, the logic assumes it is receiving a start bit, and enters the data entry mode. In this mode the UART shifts the data serially into an internal register. If parity is enabled, the UART checks the total of the received data bits plus the parity bit. (It checks for an even total if even parity has been selected, and an odd total if odd parity has been selected.) A parity error causes the UART to set the parity error flag bit in the high byte of the RBUF word.

The UART checks the stop bit to see if it is marking. If the line is spacing instead, the UART sets the framing error flag bit. If the line is marking, the UART logic assumes there is a valid stop bit.

About half-way through the stop bit time, the UART transfers the received character data, the parity error bit, and the framing error bit from the serial shift register to the holding register. At this time it asserts the

data available signal to the receiver control logic. If the previous character has not yet been serviced by the receiver control logic, the UART sets the overrun error flag bit to indicate that the previous character was lost.

The receiver control loads the contents of the RBUF (data and status) into the silo buffer for subsequent transfer to the computer. The receiver control circuit determines when and what type of receiver interrupt to request.

UART Transmitter Operation – During idle time, the UART transmits a continuous marking signal and holds the transmitter ready signal (TBMT) asserted. The transmitter control circuitry uses this signal to determine when to initiate a transmitter interrupt request.

When the computer has data to transmit to a communication line, it uses a DATO or DATOB sequence to address the TDR and place the data on the bus lines. The low byte of the TDR word is loaded into a holding register in the UART. When the data enters the holding register, the UART negates TBMT. It then transfers the data in parallel from the holding register to a serial shift register and reasserts TBMT. In the serial shift register, the UART attaches start, stop, and parity bits, as set by the LPR. The assembled character is then shifted serially out to the EIA transmitter.

Because the transmitter, like the receiver, is double-buffered, it can be loading in a second character before the first one moves out.

Break Bits

The transmission and reception of break bits are closely related to the transmission and reception of data. A break signal is a continuous spacing condition on the serial data line. When a UART receives a break signal, it interprets the continuous space as a character that is missing a stop bit. Therefore, it sets the framing error flag. The program then determines how a framing error is handled.

A break signal may be transmitted by interrupting the flow of serial data leaving the UART. The high byte of the TDR may be thought of as a break register. It contains one break bit for each of the four communication channels. Setting one of these bits will inhibit the flow of data from the UART transmitter to the EIA transmitter, thereby causing a break to be transmitted on the communication line.

Speed and Format Control

The circuits controlling speed and format include the line parameter register, two dual baud rate generator chips, an oscillator, and two addressable latches.

When the LSI-11 bus writes a word out to the LPR, the following events occur.

1. During address time the bus interface and I/O control circuitry decode the address and produce a load pulse, LD LPR REGISTER L.

2. During data time, the load pulse enables two addressable latches to be addressed by bits 0 through 2. One latch routes the state of bit 12 to a gate that inhibits or enables the receiver clock to the selected UART. For a receive operation the clock is enabled; for a transmit operation it is inhibited.

   The other latch applies an enabling signal (CONTROL STROBE H) to both the UART and the baud rate generator chip section that control the communication line selected by bits 0 through 2.

3. Bits 3 through 7 are strobed into the selected UART to select the number of data bits, the number of stop bits, and odd, even, or no parity.

4. Bits 8 through 11 are strobed into the selected baud rate generator chip to control the amount by which the 5 MHz oscillator is divided to produce the UART clock signal.

Thus, the line parameter register is formed by the latches located in the UARTs, baud rate generators, and addressable latches.

Receiver Control

Receiver Scanner – The receiver scanner circuit samples the states of the data available signals from the UARTs. When it detects a true condition, it generates a load pulse to transfer the received data from the UART to the silo buffer. The sequence in which the receiver data available (DA) flags are scanned and the characters loaded into the silo buffer is controlled by a 4-phase timing sequencer and a group of multiplexers, demultiplexers, and counters.

The sequencer produces four timing signals. The signal times are designated Phase 1 through Phase 4.

During Phase 1, a signal toggles the address generator to increment by one count. The two least significant bits of the counter are used as a 2-bit address code, designated RCV SCAN LEAD A and RCV SCAN LEAD B. These two signals address a multiplexer. The multiplexer selects the data available line from the UART corresponding to the address code and applies it to a gate. The other input to the gate is a ready signal from the silo buffer. This signal is asserted when the silo is ready to load data.

If the data available signal is set and the silo buffer is ready, the gate asserts SILO LOAD REQUEST H. The load request is applied to the load silo flip-flop.

RCV SCAN LEAD A and RCV SCAN LEAD B also address a demultiplexer. The demultiplexer places an enabling signal (RCV DATA ENABLE) on the line to the UART addressed by the scan leads. This is the same UART that is having its DA line sampled. The RCV DATA ENABLE signal enables the UART to place the contents of its receiver holding register on the lines to the silo buffer (RD1 through RD8).

During Phase 2, the sequencer clocks the load silo flip-flop. If SILO LOAD REQUEST H is true, the flip-flop sets. When the flip-flop sets, one output goes to the silo buffer as LOAD SILO H and strobes received data from the UART into the silo buffer. At the same time the data enters, status information is also loaded into the silo. Framing error, overrun error, and parity error bits from the selected UART are routed via multiplexers into the silo. The states of RCV SCAN LEAD A and RCV SCAN LEAD B are loaded into the silo to indicate which communication line the received character came from.

LOAD SILO H also goes to a latch in the sequencer. From there it passes through a demultiplexer and asserts RESET DA to the selected UART. RESET DA clears the data available flag in the UART so that another character may be received.

At the beginning of Phase 4 time, the transition out of Phase 3 clocks the silo counter. The silo counter increments by one count to keep a tally of the number of times the silo buffer has been loaded.

Phase 4 reestablishes the initial conditions of the scanner circuit for the next scan cycle.

Silo Buffer – The silo buffer comprises four 4 × 64 bit 3341 serial memory chips. The chips are arranged as a 16-bit long, 64-word deep first in-first out memory. Data is entered in the "top" of the memory as described in the previous section. The in ready signal means there is a vacancy in the top word of the memory. Similarly, the out ready signal indicates there is a word in the "bottom" of the silo waiting to be shifted out.

The buffer stores full RBUF words. Received character data is stored in the low byte, and receiver status data in the high byte. The buffer shifts data in when it receives LOAD SILO H from the load silo flip-flop, and it shifts data out when it receives UNLOAD SILO H from the unload control.

Data is shifted out as a result of either a receiver done interrupt or a silo alarm interrupt. The presence of an output ready signal from each of the four chips asserts RECEIVER DONE H to the interrupt logic. If the receiver done interrupt enable bit is set, the interrupt logic will assert the interrupt request signal to the CPU.

If the silo alarm interrupt enable bit is set, RECEIVER DONE H is inhibited at the interrupt logic. In this case, a receiver interrupt is not requested until the silo buffer has 16 characters ready. Setting silo alarm enable allows the silo counter to increment each time the silo is loaded. On the 16th count, the silo counter overflows, and the carry out signal sets the silo alarm flip-flop. The flip-flop in turn asserts SILO ALARM H to the interrupt logic.

When the interrupt request is acknowledged, the silo is unloaded. The unloading sequence is the same for both types of receiver interrupts. It proceeds as follows.

1. When data reaches the bottom of the silo, the out ready signals are gated together to produce RECEIVER DONE H.

2. RECEIVER DONE H is applied to a latch. When a CPU input transaction (DATI) addresses the RBUF, READ RCV BUFFER H latches the state of RECEIVER DONE H.

3. The output of the latch is VALID DATA H. This signal conditions one input of a one-shot.

4. The trailing edge of READ RCV BUFFER H triggers the one-shot, which generates UNLOAD SILO H.

5. UNLOAD SILO H causes the silo buffer to shift out an RBUF word (character and status data). The word is transferred via a multiplexer to the device data bus. From there the bus transceivers place it on the LSI-11 bus. VALID DATA H is applied to the multiplexer along with the output of the silo buffer, where it becomes bit 15 of the RBUF word.

Transmitter Control

The transmitter control circuit checks the transmitter control register to determine which lines are enabled. It checks the UARTs to determine which are ready to transmit, and it enables the UART controlling the highest priority line to load data from the CPU.

The sequence begins with the master scan enable signal from the CSR. MASTER SCAN ENBL H triggers a 350 ns one-shot. The leading edge of the one-shot output clocks a 4-bit latch. A true bit in the latch indicates

that the corresponding line is enabled and that the transmitter buffer empty flag is set for the UART controlling that line. Outputs from the latch are applied to a priority encoder. The priority encoder generates a 2-bit code to represent the communication line number. When more than one channel is ready at the same time, the code always indicates the one having the highest priority. (Line 3 has the highest priority; line 0, the lowest.) This code addresses two multiplexers in the transmitter control circuit, and also goes to CSR bits 8 and 9. CSR bits TLINE A and TLINE B tell the program on which line the next character will be transmitted. The priority encoder also applies a ready signal to the transmitter ready flip-flop when any of the bits in the latch are true.

The trailing edge of the 350 ns one-shot output performs two functions:

1. The zero (false) output clocks the transmitter ready flip-flop. Assuming a line enable bit is set and a TBMT signal is true, the transmitter ready flip-flop asserts TRANSMITTER READY H to the interrupt logic and the CSR. If enabled, a transmitter interrupt request will be initiated.

   The transmitter ready flip-flop also disables the gate controlling the input to the 350 ns one-shot. This inhibits further clocking until the line can be serviced. At the same time, the signal enables the contents of the line enable latch to enter a multiplexer.

2. The second function of the trailing edge of the 350 ns one-shot is to trigger a 100 ns one-shot. The output of the 100 ns one-shot disables the input to the 350 ns one-shot. The 350 ns one-shot is inhibited to prevent loosing the latched-in line number.

The assertion of TRANSMITTER READY H ultimately results in the CPU performing a DATOB to load data into the TDR. During address time the I/O control asserts load pulse LD TDR REGISTER H. LOAD IN PROGRESS L from the I/O control strobes LD TDR REGISTER H into a demultiplexer. The demultiplexer output is a transmitter holding register load pulse (THRL). It is routed to the UART that controls the line addressed by the priority encoder. This enables the UART transmitter to load character data from the device data bus during data time.

When LD TDR REGISTER H returns to the negated state, the trailing edge triggers a 100 ns one-shot. The output of the one-shot clears the transmitter ready flip-flop. It also disables the gate controlling the input to the 350 ns one-shot. The 350 ns one-shot is inhibited in order to allow the UART sufficient time to drop its transmitter buffer empty flag before the circuit starts another scan cycle.

When the program is finished sending a message, it clears the line enable bit in the TCR. This occurs after enable bit and TMBT signals have already been latched in and TRANSMITTER READY H has not asserted. It is therefore necessary to prevent the scanner from locking up on a line for which there is no data. This is accomplished by clearing the transmitter ready flip-flop if it is set for a line which is no longer enabled. The states of the line enable bits from the TCR are applied to a multiplexer. The bit corresponding to the line addressed by the priority encoder is passed to a pulse forming circuit. If the bit is in the clear state, a 50 ns pulse is formed. This pulse clears the transmitter ready flip-flop, thereby negating TRANSMITTER READY H and allowing the 350 ns one-shot to fire for the next transmitter scan cycle.

Maintenance Mode

The DZV11 can be switched to receive the data that it is transmitting. The four serial data lines leaving the UARTs are applied to both a data selector and the EIA transmitters. The data selector controls the inputs to the UART receivers. During normal operation, data from the EIA receivers is routed through the data selector to the UART receivers. In the maintenance mode the data selector ignores the inputs from the EIA receivers. Instead, it routes the output data to the UART receivers. This internal "wrap-around" feature is enabled by setting the maintenance bit in the CSR. Setting CSR bit 3 asserts MAINTENANCE H, which switches the data selector.

Power Supplies

In addition to the +12 and +5 V available on the LSI-11 bus, the DZV11 also requires +3, −9, and −12 V. The +3 V source is a voltage divider. The negative voltages are produced by two capacitive charge pump circuits.

Each of the two charge pumps use the following scheme:

1. An oscillator running at approximately 500 kHz switches a pair of drivers on and off.

2. The outputs of the drives are capacitively coupled to a rectifier.

3. The negative-going output of the rectifier builds up a charge on a capacitor.

4. The charge is zener-regulated back to the required negative voltage.

IBV11-A INSTRUMENT BUS INTERFACE

GENERAL

The IBV11-A is an option that interfaces the LSI-11 bus with the instrument bus as described in IEEE Standard 488-1975, "Digital Interface for Programmable Instrumentation." An IBV11-A can be installed in any LSI-11 system. The IBV11-A consists of an M7954 interface module and a BN11-A cable for connecting the first instrument. Additional instruments may be connected using a BN01A cable.

The IBV11-A makes an LSI-11-based programmable instrument system possible

FEATURES

- PDP-11 software-compatible
- Board-mounted, user-configured switches allow easy device (register address) and interrupt vector address selection
- Software support available under FORTRAN IV
- System hardware-compatible with any LSI-11 component system
- Instrument bus compatible with the IEEE 488-1975 standard
- The module supports cable length up to 20 m (65.6 ft) total
- 15 devices (maximum) can connect to the bus

SPECIFICATIONS

Identification	M7954
Size	Double
Power	+5.0 Vdc ± 5% at 0.8 A
Bus Loads	
AC	1.8
DC	1

The IBV11-A, *when connected to the LSI-11,* will meet the following subsets of IEEE Standard 488-1975:

SH1	SR1	C1
AH1	RL1	C2
TS	PP2	C3
TE5	DC1	C4
LE3		

This module is designed to be the only controller on the IEEE bus. Therefore, it will not respond to another controller on the bus that issues either a parallel poll configure command or a parallel poll control signal.

CONFIGURATION

General

The IBV11-A option can be installed in any LSI-11 bus to interface various instruments via an "instrument bus." The instrument bus is defined in the IEEE Standard 488-1975, "Digital Interface for Programmable Instrumentation." Any instruments designed to interface with the bus defined in that standard can be interfaced to the LSI-11 system via the IBV11-A.

The following paragraphs contain only the basic information necessary for configuring device register addresses and vector interrupts, general installation and interface to the instrument bus, and basic programming (device register functions, etc.).

Device Address

Device address switches provide a convenient means for the user to configure the IBV11-A's register addresses. Only switches corresponding to BDAL lines (03:12) are provided. By PDP-11 convention, the upper 4K address space (bank 7) is normally reserved for peripheral devices, such as the IBV11-A. The processor module asserts BBS7 L whenever a bank 7 address [BDAL (13:15) L are asserted] is placed on the bus. Thus, BBS7 L must be asserted to enable an "address match" output from the address selection function. Any address ranging from 16000X to 17777X can be configured that does not conflict with other device addresses within the system; the X in the address represents register and byte selection within the module.

Each IBV11-A module is factory-configured for a standard device register address (160150) and interrupt vector (420). Switches S1 (interrupt vector) and S2 (device register address) configure the module. A summary of register addressing and interrupt vectors is provided in Figures 2 and 3. Observe that only the IBS register address is always the IBS address plus 2. Similarly, only the error interrupt vector is configured. The remaining three vectors are permanently assigned sequential addresses in address increments of four as shown in Table 1.

Table 1 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address
Registers			
Control/Status	IBS	R/W	160150
Data	IBD	R/W	160152
Vectors			
Error	ER2, ER1		420
Service	SRQ		424
Command and Talker	CMD, TKR		430
Listener	LNR		434

Switches S1 and S2 are located on the IBV11-A module as shown in Figure 1. S1 and S2 are switch assemblies, each containing several individual switches. The individual switches indicated in Figures 2 and 3 are clearly marked on the S1 and S2 assemblies. The ON and OFF positions are also clearly marked.

Interrupt Vectors

The IBV11-A is capable of generating four separate interrupt requests; each have separate interrupt vectors and normally would have separate service routines. Interrupts can be requested only when the IBS IE (interrupt enable) bit is set. Interrupt requests are priority structured in the IBV11-A. A summary of the four interrupt types is provided below.

Priority	Vector	Associated IBS Bit	Cause of Interrupt
Highest	000XNN00	ER2, ER1	Error condition.
Second highest	000XNN04	SRQ	A device connected to the instrument bus is requesting service.
Third highest	000XNN10	TKR, CMD	The IBV11-A is an active talker and it is ready for the processor to output a byte to the low byte of the IBD register. [The IBV11-A will normally then transmit the byte over the instrument bus to the active listener(s)].

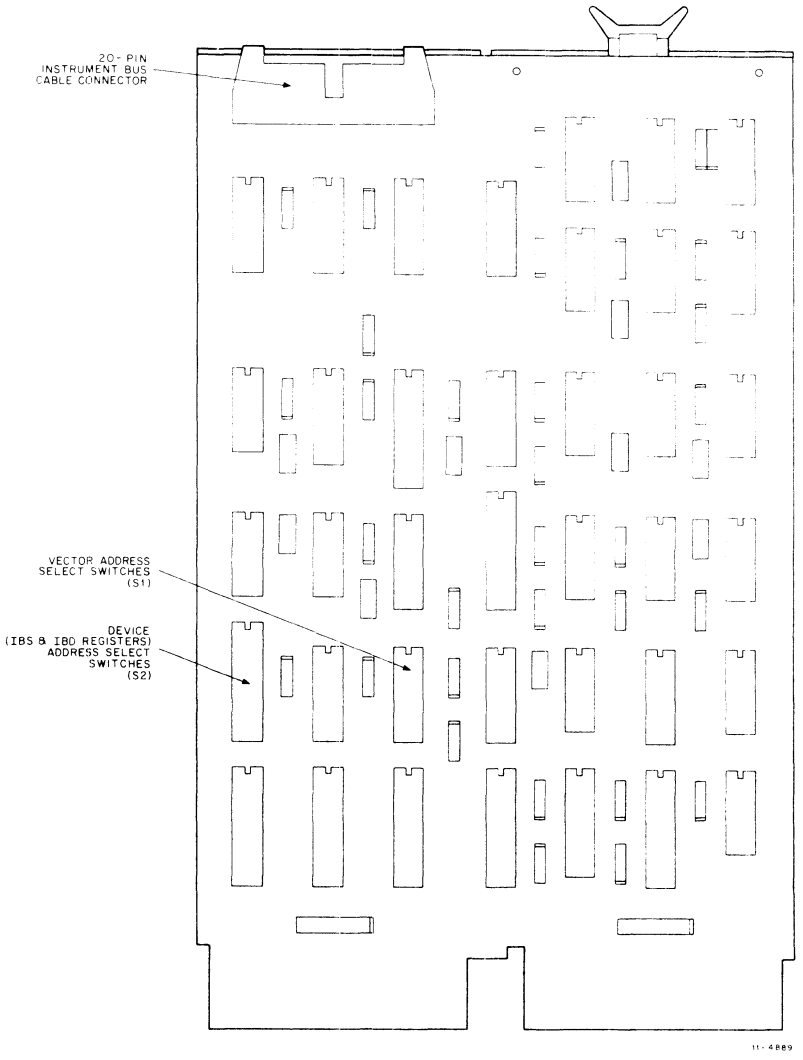


Figure 1 IBV11-A Module Switch Locations

Lowest	000XNN14	LNR	The IBV11-A is an active listener and has a data byte to be read by the processor.

NOTES

1 X = User-configured interrupt vector octal digit.

2 N = User-configured interrupt vector binary bits.

3 Associated IBS bits shown, when set, produce interrupt requests if the IE bit is set.

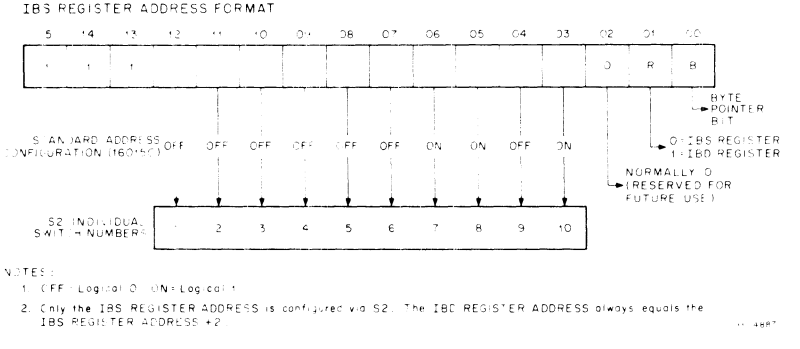


Figure 2 Register Addresses

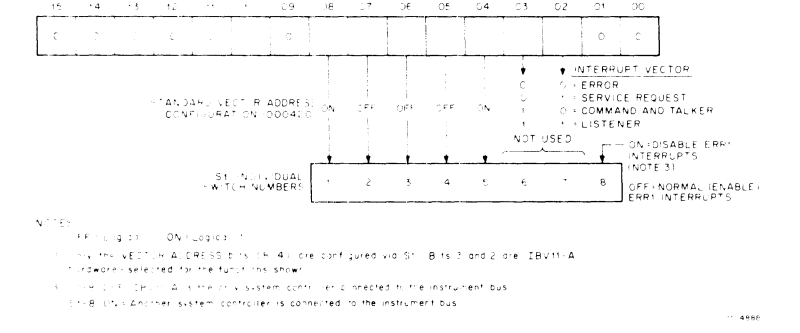


Figure 3 Interrupt Vector

Interrupt	Interrupt Vector
Error	"n" (configured vector)
Service	n + 4
Command and Talker	$n + 10_8$
Listener	$n + 14_8$

Preferred value range for "n" = $300 \leqslant n \leqslant 760$.

Registers

The IBV11-A communicates with devices connected to the instrument bus under the control of the program being executed. All communication between the processor and the IBV11-A is via the instrument bus status (IBS) and instrument bus data (IBD) registers. The programmer must be aware of the functional significance of each bit in both registers before any programs can be written that will control specific devices on the instrument bus. In addition, the programmer must establish instrument (device) addresses and conform to programming rules specified for each instrument connected to the instrument bus. See Figure 4 for a description of the IEEE bus.

The instrument bus status (IBS) register is similar in function to other device control/status registers (CSRs). The instrument bus data (IBD) register is a 16-bit register that contains 8 read/write data bits in the low byte and 8 read-only bits in the high byte. The eight read-only bits allow the program to read the logical state of the control and management signals of the instrument bus.

The IBS register provides the means for controlling the instrument bus signals control and management and IBV11-A functions relative to the LSI-11 bus. The low byte of the IBD register, on the other hand, is used for passing commands to devices connected to the bus and for transmitting and receiving data between the processor and talker and listener devices. In addition, the high byte of the IBD register allows for processor monitoring of all instrument bus signal (control) lines. IBS and IBD registers are shown in Figure 5 and described in Tables 2 and 3.

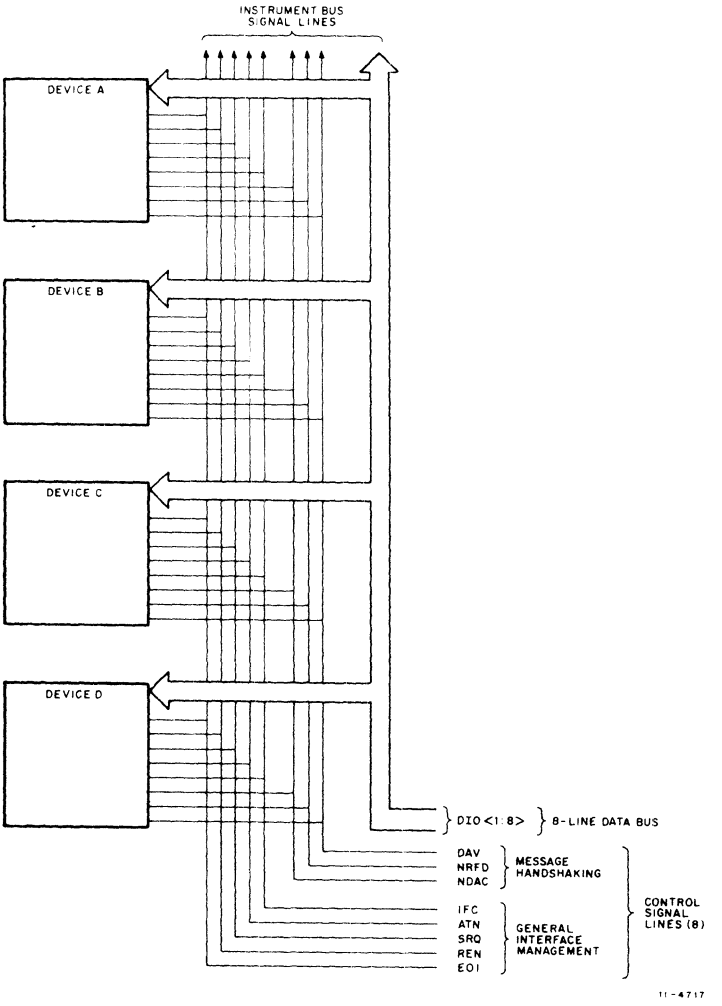


Figure 4 Instrument Bus Signal Lines

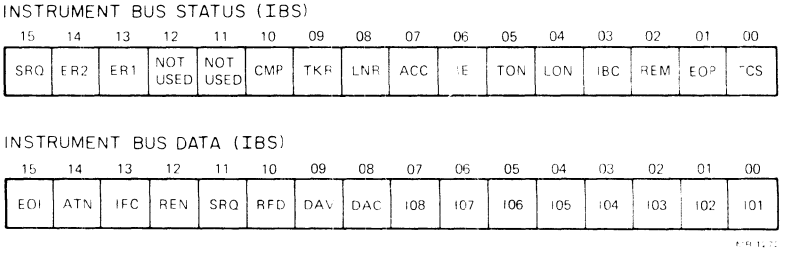


Figure 5 Register Word Format

Table 2 Instrument Bus Status Word Format

Bit	Name	Description
15	SRQ (Service Request)	Monitors the state of the instrument bus service request line at all times. Set when the IB SRQ line is low. Will cause an interrupt when both SRQ and the interrupt enable bits are set. When the ER1-inhibit switch is set, this bit will be written by any type of instruction that writes into the IBS. Read/write.
14	ER2 (Error 2)	Asserted if the IB reports that DAC is true when the IBV11-A tries to send a data or command byte. This condition will exist when there is no active listener or command acceptor on the IB. An ERR interrupt occurs when both the ER2 and the interrupt enable bits are set. Cleared by clearing both TON and TCS. Read-only.
13	ER1 (Error 1)	Unless inhibited by the ER1-inhibit switch, this bit is asserted whenever a conflict occurs between the IB ATN, IFC, or REN lines and their IBV11-A control hardware, i.e., if one or more of these control lines is

Table 2 Instrument Bus Status Word Format (Cont)

Bit	Name	Description
		asserted when it should not be asserted or not asserted when it should be asserted. When asserted, the IBV11-A will not assert the ATN line even though the TCS bit remains set. An ERR interrupt occurs when both the ER1 and the interrupt enable bits are set. This condition can only be cleared by clearing the cause. Read-only.
12	0	Always read as a zero. Read-only.
11	0	Always read as a zero. Read-only.
10	CMD (Command Done)	Set when the IBV11-A is ready to send a command byte. Set by a successful TCS to indicate that ATN was asserted and the first command byte may be issued. Also set by DAC when a command has been completely accepted. A CMD/TKR interrupt occurs when both the CMD and the interrupt enable bits are set. This bit is cleared by INIT, received IFC, writing a command into the IBD low byte, or by turning TCS off. Read-only.
9	TKR (Talker Ready)	Set when the IBV11-A is ready to send a data byte. Set when TON is on while TCS is turned off or by DAC when TON is on. A CMD/TKR interrupt occurs when both the TKR and the interrupt enable bits are set. Cleared by INIT, received IFC, writing a data byte into the IBD low byte, or by turning TON off or TCS on. Read-only.

Table 2 Instrument Bus Status Word Format (Cont)

Bit	Name	Description
8	LNR (Listener Ready)	Set when the IBV11-A has a data or command byte ready for reading from the IBD low byte. Set by DAV when LON is on. A LNR interrupt occurs when both the LNR and the interrupt enable bits are set. Cleared by reading the IBD low byte if ACC is off or by clearing the IBD low byte if ACC is on. Also cleared when LON is turned off and by INIT or received IFC. Read-only.
7	ACC (Accept Data)	Set and cleared under program control. When clear, reading the IBD will automatically clear the LNR and assert DAC. When set, the programmer must write zero to the IBD low byte in order to clear the LNR bit and assert DAC. When the TCS, LON, and TON bits are all off (clear), setting this bit will assert NRFD. Cleared by INIT or received IFC. Write-only.
6	IE (Interrupt Enable)	Set and cleared under program control to enable and disable all interrupts. Cleared by INIT. Write-only.
5	TON (Talker On)	Set and cleared under program control to enable and disable the talker function. Cleared by INIT or received IFC. Write-only.
4	LON (Listener On)	Set and cleared under program control to enable and disable the listener function. Cleared by INIT or received IFC. Write-only.
3	IBC (Interface Bus Clear)	Set under program control to cause the IFC line to be asserted for about 125 μs. TCS will automatically be asserted at the end of IBC (out-going IFC). Cleared by INIT.

Table 2 Instrument Bus Status Word Format (Cont)

Bit	Name	Description
2	REM (Remote On)	Set and cleared under program control to assert and unassert the REN line. Cleared by INIT or received IFC. Write-only.
1	EOP (End or Poll)	Set and cleared under program control to assert and unassert the E01 line. Cleared by INIT or received IFC. Write-only.
0	TCS (Take Control Synchronously)	Set and cleared under program control to take control synchronously or to unassert ATN. Setting TCS will cause NRFD to be asserted for at least 500 ns before DAV is checked. ATN is then asserted when DAV is unasserted. NRFD is unasserted and CMD is set no sooner than 500 ns after ATN is asserted. Cleared by INIT or received IFC. Write-only.

Table 3 Instrument Bus Data Word Format

Bit	Name	Function
15	EOI (End or Identify)	Monitors the IB EOI line at all times. Set when the IB EOI line is low. Read-only.
14	ATN (Attention)	Monitors the IB ATN line at all times. Set when the IB ATN line is low. Read-only.
13	IFC (Interface Clear)	Monitors the IB IFC line at all times. Set when the IB IFC line is low. Read-only.
12	REN (Remote Enable)	Monitors the IB REN line at all times. Set when the IB REN line is low. Read-only.

Table 3 Instrument Bus Data Word Format (Cont)

Bit	Name	Function
11	SRQ (Service Request)	Monitors the state of the instrument bus service request line at all times. Set when the IB SRQ line is low. Will cause an interrupt when both SRQ and the interrupt enable bits are set. Read-only.
10	RFD (Ready for Data)	Monitors the IB NRFD line at all times. Set when the IB NRFD line is high. Read-only.
9	DAV (Data Valid)	Monitors the IB DAV line at all times. Set when the IB DAV line is low. Read-only.
8	DAC (Data Accepted)	Monitors the IB NDAC line at all times. Set when the IB NDAC line is high. Read-only.
7–0	DIO8–DIO1 IB Data I/O Lines	Reading the IBD low byte picks up unlatched data directly from the IB DIO lines. Data on the IB DIO lines may change if the LNR bit is not set. Generally, the only reason to read the DIO lines when LNR is now set is when a parallel poll response is expected. Writing data to the IB DIO lines is permitted when TON is set and DAV is clear or when TCS and ATN are set and DAV is clear. Otherwise, writing into the IBD low byte will have no effect on the DIO lines but will set DAC if both ACC and LNR are set. Write-only. The data and command output buffer is cleared by INIT or received IFC.

Connecting to External Equipment

Connection from the IBV11-A to the first device on the instrument bus is via a type BN11A cable (supplied with the M7954 module) as shown in Figure 6. One end is terminated with a 20-pin connector that mates with the 20-pin connector on the IBV11-A module. The other end is terminated with a 24-pin "double-ended" connector that conforms with the IEEE 488-1975 standard; the cable can be connected to any device conforming to that standard. The double-ended connector contains a male 24-pin and a female 24-pin connector in the same connector housing. This allows for "linear" and "star" connections to instruments connected to the instrument bus, as shown in Figure 7. One BN11A is included in the IBV11-A option.

The linear arrangement shown in the figure includes five devices (or instruments), A through E. There is no particular significance to the sequence shown or electrical position along the instrument bus. Unlike the LSI-11 bus, position along the bus does not structure device priority in the system.

The star arrangement shown in the figure allows five devices to be connected by stacking instrument cable connectors on the BN11A's double-ended connector. Double-ended connectors on instrument bus cables will normally include captive locking screws on each connector assembly (two each), allowing stacked connectors to be secured together in a single assembly.

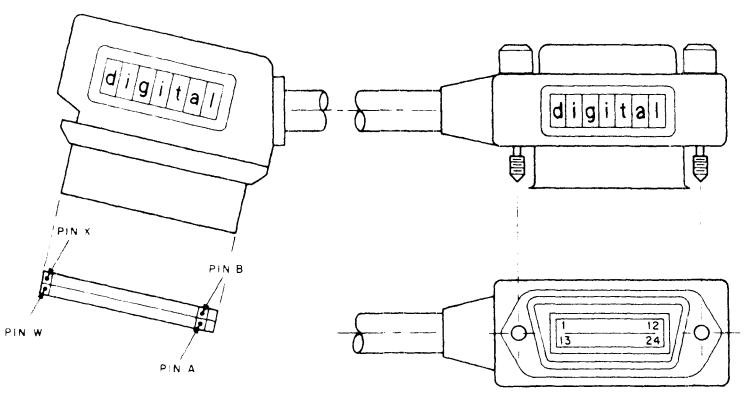


Figure 6 BN11A Instrument Bus Cable

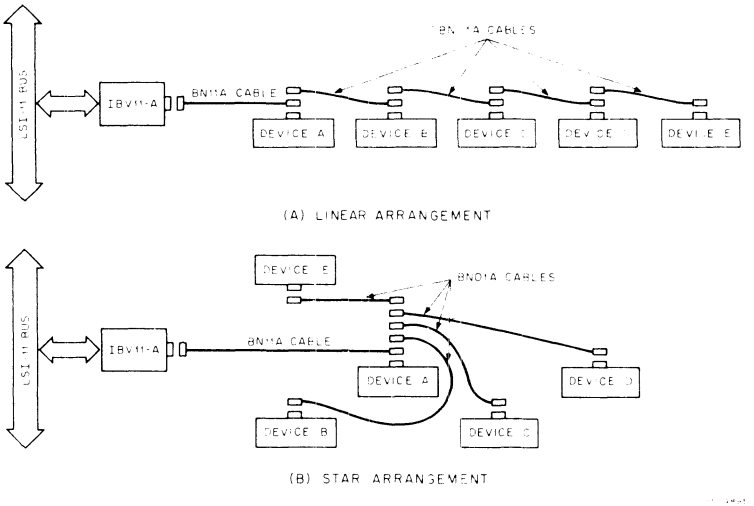


Figure 7 Linear and Star Configurations

The BN11A cable connector pin signal assignments are listed in Table 4 for each connector. One BN11A cable is required for each IBV11-A module in a system.

Optional Cables

1. Connect M7954 module to first instrument:

BN11A-02	2 m (78.7 in)
BN11A-04	4 m (157.5 in)

2. Connect instrument to instrument:

BN01A-01	1 m (39.4 in)
BN01A-02	2 m (78.7 in)
BN01A-04	4 m (157.5 in)

PROGRAMMING EXAMPLES

Example 1 – IBV11-A to Listener Device
This programming example illustrates how the IBV11-A communicates with a listener device. Standard device and vector addresses are used, as

Table 4 BN11A Connector Pin Assignments

IBV11-A Connector Pin	Signal Name	Instrument Bus Connector Pin
U	DIO1	1
S	DIO2	2
P	DIO3	3
M	DIO4	4
R	EOI	5
T	DAV	6
V	NRFD	7
X	NDAC	8
B	IFC	9
J	SRQ	10
F	ATN	11
W	(SHIELD)	12
K	DIO5	13
H	DIO6	14
E	DIO7	15
C	DIO8	16
D	REN	17
N	GND (DAV GND)	18
	GND (NRFD GND)	19
	GND (NDAC GND)	20
A	GND (IFC GND)	21
L	GND (SRQ GND)	22
	GND (ATN GND)	23
W	GND (LOGIC)	24

shown in Figures 2 and 3. Once the program is started, and after pointers have been initialized and the IBV11-A has taken control synchronously, the program communicates with the IBV11-A via an interrupt-driven service routine. No "background" program is used; the program simply "waits" until another interrupt occurs.

Communication with the listener device includes the transmission of 2 command bytes (read as words from a message buffer), followed by 24 message bytes that program device functions. After all message bytes have been transmitted, the program halts (displayed HALT PC address = 1066).

A program flowchart for this example is shown in Figure 8, and a symbolic listing is shown in Figure 9.

Example 2 – IBV11-A to Talker Device

This programming example illustrates how the IBV11-A communicates with a talker device. As in example 1, this programming example assumes standard IBV11-A device and interrupt vector addresses. Communication between the instrument and the LSI-11 system is via IBV11-A interrupt-driven service routines. No background program is used; the program simply "waits" until another interrupt occurs.

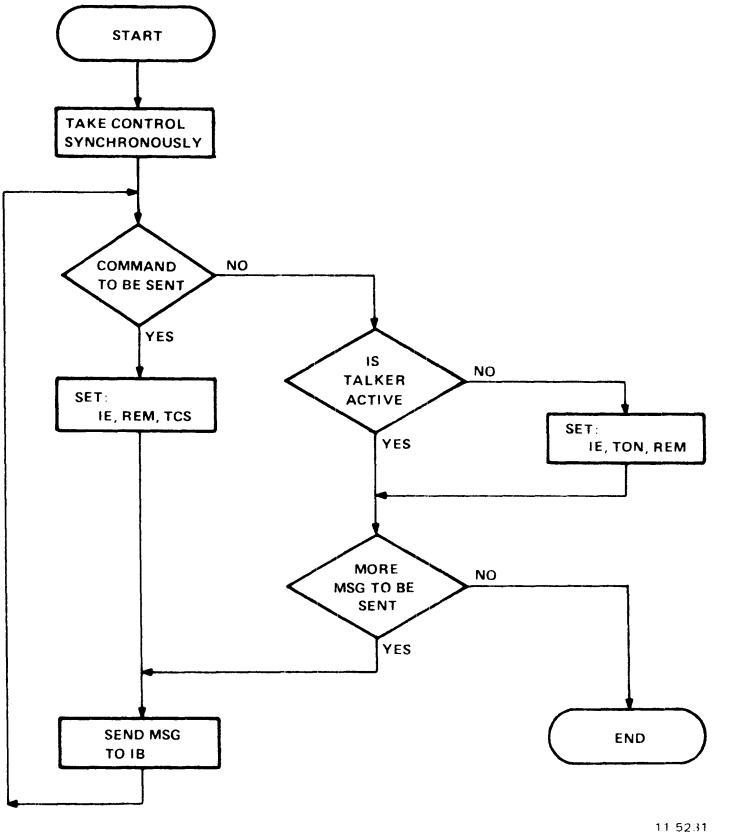


Figure 8 Communicating with a Listener Device (Program Flowchart)

ADDRESS	OCTAL CODE	ASSEMBLER SYNTAX	COMMENTS
	001000		; INIT RELOC ADDRESS
	000000		; PSW
001000	012706	START: MOV #500,R6	; SET UP STACK POINTER
001002	000500		
001004	012700	MOV #2000,R0	; R0 IS MSG BUFFER ADDRESS
001006	002000		
001010	012737	MOV #110,160150	; TAKE CONTROL
001012	000110		; SYNCHRONOUSLY TO BECOME
001014	160150		; CONTROLLER-IN-CHARGE
001016	000777	WAIT: BR .	; WAIT FOR INTERRUPT
001020	022700	CMP #2004,R0	; MORE COMMANDS TO BE SENT?
001022	002004		
001024	100006	BPL 20$	; IF NO,GO TO 20$
001026	012737	MOV #105,160150	; IF YES,SET IE,REM,AND
001030	000105		; ICS BITS OF IBS REG TO
001032	160150		; ACTIVATE CONTROLLER
001034	012037	SEND: MOV (R0)+,160152	; SEND MSG TO IB
001036	160152		
001040	000002	RTI	; RETURN TO WAIT--FOR
			; MSG TO BE ACCEPTED
001042	022700	20$: CMP #2004,R0	; IS TALKER ACTIVE?
001044	002004		
001046	003003	BGT 30$	; IF YES,GO TO 30$
001050	012737	MOV #144,160150	; OTHERWISE SET IE,TON
001052	000144		; AND REM BITS OF IBS REG
001054	160150		; TO ACTIVATE TALKER
001056	022700	30$: CMP #2062,R0	; HAD ALL MSG BEEN SENT?
001060	002062		
001062	100364	BMI SEND	; IF NO,GO SEND ANOTHER MSG
001064	000000	HALT	; OTHERWISE STOP

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Figure 9 Communicating with a Listener Device (Program Listing)

Communication with the instrument involves first transmitting the content of the command message buffer, in a manner similar to the program operation described for example 1, followed by accepting instrument output data and storing it in a received data buffer. The content of the command message buffer typically includes first activating the device via its listen address, followed by setting up range mode, etc., operating parameters for the instrument, an execute command, and finally, activating the device as an active talker via its talker address. Once the device has received the command message buffer data, it performs the programmed measurements (or the function, depending on the instrument) and returns data to the LSI-11 system via the IBV11-A; note that during this portion of program operation, the IBV11-A functions as an active listener on the instrument bus. Once all measurements have been stored by the program, the program halts with a displayed PC address = 1102.

A program flowchart for this example is shown in Figure 10 and a symbolic program listing is shown in Figure 11.

FUNCTIONAL DESCRIPTION

General

The functional logic blocks that comprise the IBV11-A are shown in Figure 12. LSI-11 software controls and communicates with the IBV11-A via programmed I/O transfers and interrupts. Programmed I/O transfers are made possible by assigning unique device addresses (also called "bus addresses") to the IBS and IBD registers.

LSI-11 Bus Interface

LSI-11 bus address selection, interrupt vector address generation, and bus data driver/receiver (transceiver) functions are provided by transceiver integrated circuits (DC005). Each integrated circuit provides the interface for four BDAL bus lines; thus, four transceivers comprise the 16-line BDAL (00:15) L LSI-11 bus interface.

Bit 1 of the least significant octal digit (BDAL 0) selects the IBS or IBD register. This is a byte pointer and it is significant for DATOB and DATIOB bus cycles only. Register address selection is actually performed in the LSI-11 bus protocol and register selection circuit (DC004); the transceiver integrated circuit (DC005) simply routes the received low-order three address bits [DA (2:0)] to that function.

All I/O transfers over the LSI-11 bus are done according to a strict protocol. One bus protocol integrated circuit (DC004) performs this function and the register address selection previously discussed. When an active ADDRESS MATCH signal is present and BSYNC L signal is asserted, the bus protocol integrated circuit is enabled to complete its register selection function. BWTBT L, BDOUT L, and BDIN L bus signals

are decoded in the integrated circuit, as appropriate, to produce the LOAD IBS LOW BYTE, SELECT IBS, LOAD IBD LOW BYTE, and RECEIVE internal control signals for the IBV11-A logic functions. The integrated circuit also asserts BRPLY L as required during the I/O sequence to complete the programmed transfer. Refer to Chapter 5 for a detailed description of the DC003, DC004, and DC005 integrated circuits.

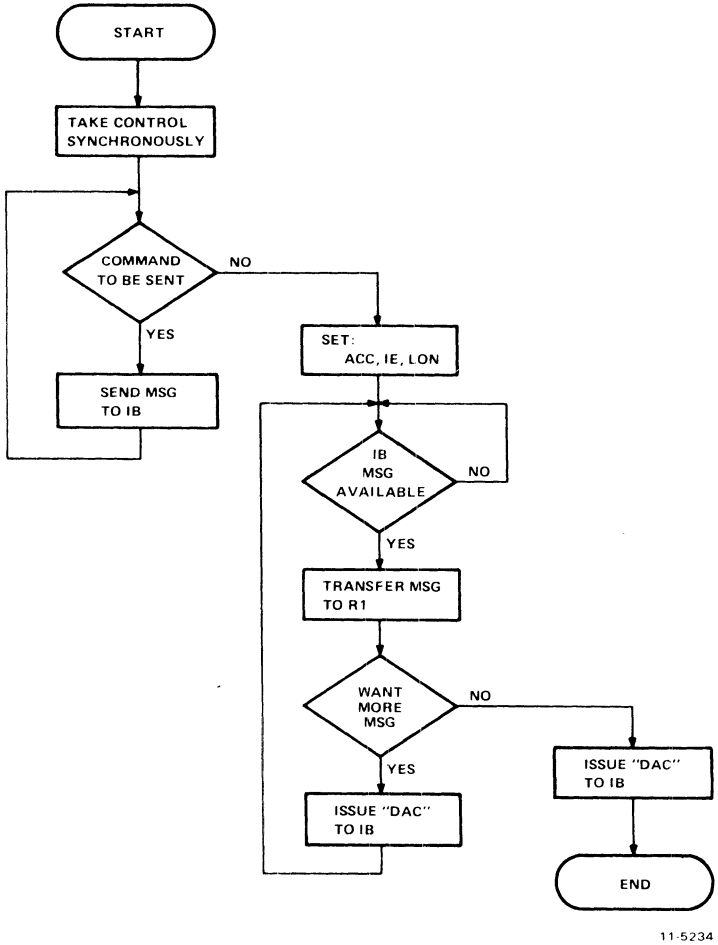


Figure 10 Communicating with a Talker Device (Program Flowchart)

```
ADDRESS  CODE      ASSEMBLER SYNTAX          COMMENTS

001000   001074                             ; COMMAND/TALKER INTR
                                            ; RETURN ADDRESS
001002   000700                             ; PSW
001004   001056                             ; LISTENER RETURN ADDRESS
001006   000700                             ; PSW

001010   012706  START:  MOV #500,SP         ; SET UP STACK
001014   000500
001016   012700          MOV #IBV11,R0      ; IBV11 A MSG BUFFER
001022   002000
001024   012701          MOV #BUF,R1        ; BUFF FOR RECEIVED MSG
001030   002000
001032   012737          MOV #1,@#160152     ; TAKE CONTROL SYNCHRONOUSLY
001036   000001                             ; TO BECOME CONTROLLER
001042   160152                             ; IN CASE WE'LL BE
001046   000777  WAIT:   BR .               ; WAIT FOR INTERRUPT
001050   012737          MOV #IBV11,@#160154 ; PREPARE TO SEND
001054   000000                             ; COMMAND MESSAGES
001056   160154
001062   027700          CMP #2024,R0       ; HAD ALL COMMANDS
001066   002024                             ; BEEN SENT?
001070   001404          BEQ 30$            ; IF YES,GO TO 30$
001072   012737          MOV (R0)+,@#160154 ; OTHERWISE SEND MSG
001076   160154
001102   000002          RTI                ; RETURN TO WAIT FOR
                                            ; MSG TO BE ACCEPTED
001104   012737  20$:    MOV #320,@#160150  ; IBV11-A SWITCHES FROM
001110   000320                             ; CONTROLLER TO LISTENER
001112   160150
001116   000002          RTI                ; RETURN TO WAIT---
                                            ; FOR DMM MSG
001120   013721          MOV @#160152,(R1)+ ; SAVE THE RECEIVED
001124   160152                             ; MSG IN R1
001130   022721          CMP #2540,(R1)     ; HAD 20 (OCTAL) MSG
001134   002540                             ; BEEN ACCEPTED?
001140   001403          BEQ 30$            ; IF YES,GO TO 30$
001142   005037          CLR @#160152       ; OTHERWISE ISSUE DAC
001146   160152
001152   000002          RTI                ; RETURN TO WAIT--FOR
                                            ; ANOTHER DMM MSG
001154   005037  30$:    CLR @#160152       ; ISSUE DAC TO IB
001160   000000          HALT               ; STOP-20 MSG RECEIVED
```

11-5235

Figure 11 Communicating with a Talker Device (Program Listing)

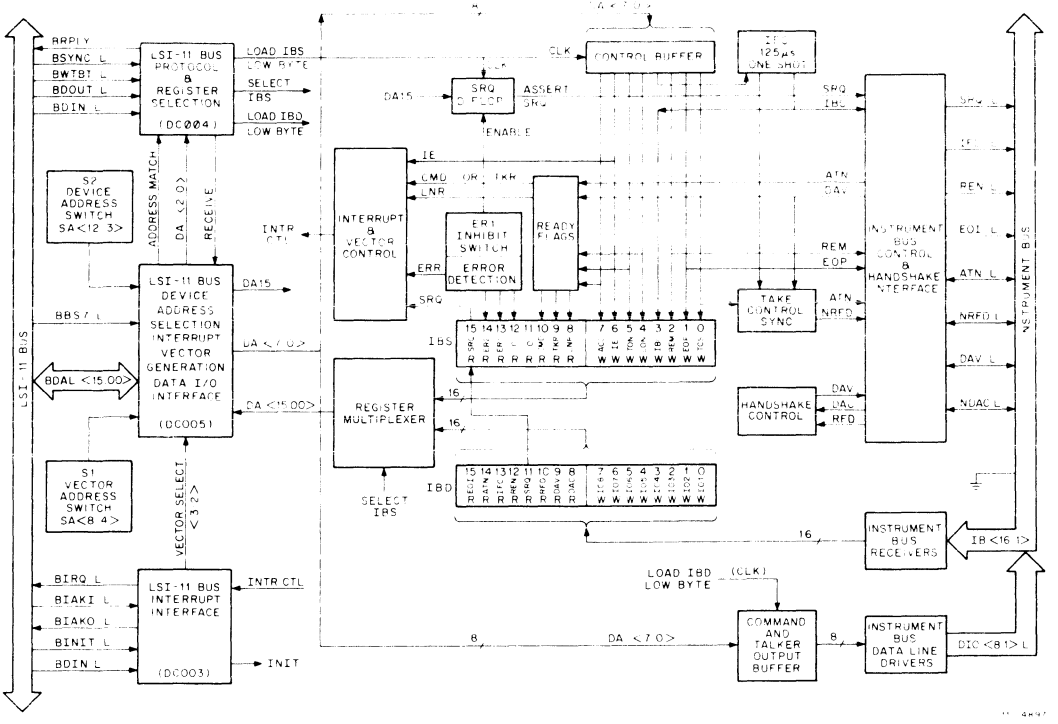


Figure 12 IBV11-A Functional Block Diagram

Interrupts are generated by one interrupt integrated circuit (DC003). Four interrupt vectors can be generated by this bus interrupt interface function. A 5-bit vector switch allows the user to select the interrupt vector for the IBV11-A module. The IBV11-A base interrupt vector is factory-configured for 420. The base interrupt vector can range from 300 to 760; however, vector interrupts must not conflict with other bus devices or with those interrupts reserved for system vectors.

Interrupt Vector	Interrupt Source
000420	Error
000424	Service request
000430	Command and talker
000434	Listener

These interrupt vectors allow the IBV11-A to generate interrupts that can most efficiently be serviced by four separate service routines.

Interrupt and vector control logic on the IBV11-A module generates the INTR CTL signals that initiate the interrupts. Inputs for this logic function include the interrupt enable (IE) bit (stored in the control buffer), command or talker (CMD or TKR) and listener (LNR) ready flags, error (ERR) status from the error detection logic, and the device service request (instrument bus control signal).

Instrument Bus Control

The control buffer is an 8-bit register that functions as the low byte of the IBS register. Bits stored in this register control generation of interrupts, instrument bus clear, and instrument bus control and status logic. Setting the IBC bit actually triggers a one-shot producing a 125 μs pulse that clears the instrument bus. Take control sync and handshake control logic function together with instrument bus control and handshake interface logic to communicate with instruments on the bus according to instrument bus protocol. Output transactions with the low byte of the IBD register result in data being stored in the 8-bit command and talker output buffer. Instrument bus line drivers gate this byte onto the instrument bus when the IBV11-A is an active talker or when it is an active controller.

Instrument Bus Interface

The IBV11-A interfaces with the instrument bus via four integrated circuits, type MC3441. These integrated circuits are bus transceivers, each containing four bus drivers, four bus receivers, and bus terminations that comply with instrument bus specifications.

KPV11-A,-B,-C POWER-FAIL/LINE-TIME CLOCK/TERMINATOR

GENERAL

The KPV11 is an LSI-11 power-fail/line-time clock (LTC) generator. Three versions of the KPV11 are available: KPV11-A, which has only power-fail and LTC functions; KPV11-B, which has 120 Ω bus terminations in addition to the power-fail and LTC; and KPV11-C, which is similar to the KPV11-B, but has 220 Ω bus terminations. The KPV11 is compatible with all LSI-11 component systems and LSI-11 backplane options. It is designed for installation into any LSI-11 bus-structured backplane or remote installation (not installed into a backplane) via an optional cable which connects the KPV11 to the LSI-11 backplane. In order to use the KPV11-B or KPV11-C as bus terminators, they must be installed in the LSI-11 backplane. An optional console panel and bezel are available for manual control of the LTC and the display of dc power on/off status and the processor run/halt state.

FEATURES

- Automatic generation of BPOK and BDCOK power-up/power-down signal sequence
- Automatic program restoration and starting when used with non-volatile memory and appropriate software routines
- Line-time clock time reference provided by a signal source (user-supplied) other than the power line
- KPV11-B and KPV11-C provide bus termination when plugged into an LSI-11 backplane
- Can be installed into the LSI-11 backplane or mounted remotely. An optional cable (DIGITAL part no. 70-12754) connects the KPV11 to the LSI-11 backplane.
- Expandable with the 54-11808 console panel option

SPECIFICATIONS

Identification	M8016 (KPV11-A) M8016-YB (KPV11-B) M8016-YC (KPV11-C)
Size	Double

Power	+5 Vdc ± 5% at 560 mA
System DC	
DC Sensing Inputs	+5 Vdc ± 5% at 0.11 mA +12 Vdc ± 3% at 0.82 mA
AC Line Monitor Input	24 Vac ± 10% at 200 mA with grounded center tap (Figure 4)
Bus Loads	
AC	1.6
DC	1.0
Options	
54-11808	Console Panel (PC assembly)
70-11656	Console Bezel
70-12754	Remote Signal Cable (for remote mounting of KPV11)
70-086120	Console Signal/Power Cable (for connecting optional console panel to the KPV11)

CONFIGURATION

General

The KPV11 can be installed into any LSI-11 system backplane or into a remote installation (not installed in a backplane). All KPV11 installations require a user-supplied, 24 Vac, center-tapped transformer capable of supplying at least 0.2 A. Remote KPV11 installations also require the optional remote signal cable (part no. 70-12754). Users requiring manual control of the LTC and desiring the display of dc power on/off status and processor run/halt status need the optional console panel, console bezel, and console signal/power cable. Mounting hardware for the console panel and remote installation must be provided by the user.

Configuring LTC Jumpers

LTC jumpers are located on the KPV11 module as shown in Figure 1 and are factory-configured for programmable operation with the LKS (line clock status) register at address (177546) as shown in Figure 2. Normally, it will not be necessary to reconfigure LTC jumpers; however it is possible to alter LTC operation as listed in Table 1 and the LKS device address as shown in Figure 2 and listed in Table 2.

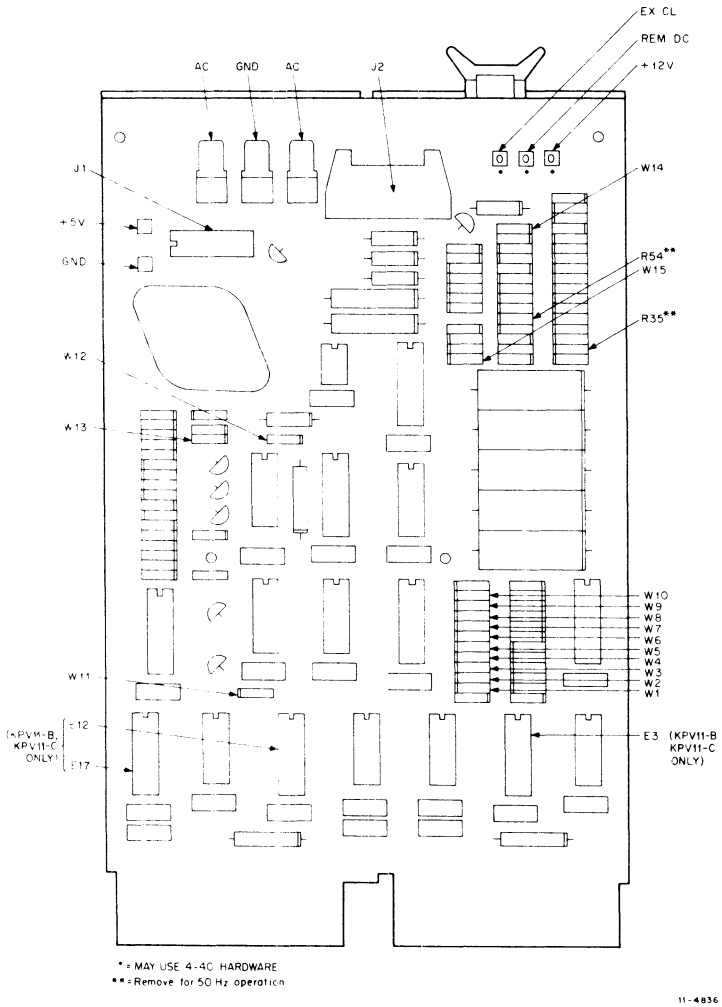


Figure 1 Jumper, Connector, Resistor, and Pad Locations

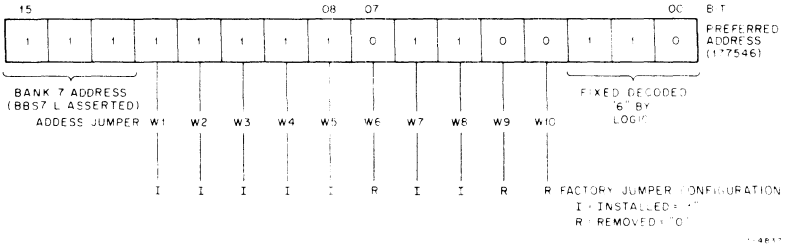


Figure 2 Device Address (LKS Register) Jumpers

Table 1 LTC Jumpers

Jumper	Installed	Removed
W12	Enable manual control or continuous LTC interrupt request operation. Do not install when W13 is installed.	*Disable continuous or manual operation.
W13	*LTC interrupt requests can be enabled and disabled by program. Do not install when W12 is installed.	LTC interrupt requests cannot be program controlled.
W14	*Console (optional) LTC ON/OFF switch enabled.	Console LTC ON/OFF switch disabled.
W15	*LTC signal occurs at the power line frequency.	LTC frequency is determined by an external source via EXT TIME REF etched pad on module.

* Factory-jumpered configuration

Table 2 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address
Register			
Line Clock Status	LKS	R/W	177546
Vector			
None			

Installation in the LSI-11 Backplane

The KPV11 module can be installed in any LSI-11 structured backplane. The KPV11 may be inserted into any option location when not used as a terminator. This option does not require the use of the daisy-chained grant signals (BIAK L and BDMG L) and is not priority dependent on device position in the backplane.

When used as a terminator (KPV11-B and KPV11-C), the module is inserted after the last module in the last backplane.

When the optional console panel is used with the terminator option and the RUN indicator is desired, the following must be performed.

- Insert the KPV11 module in the last option location in the backplane system.

- Connect a wire on the backplane from pin CH1 or AH1 on the KPV11 module to the SRUN L signal on the processor module. The wire must not exceed the length of the LSI-11 bus. This signal is located on pin AH1 of the processor.

Remote Installation

The KPV11 option can be mounted in a remote location (not installed in a backplane), as desired. Mounting holes are provided in the module for this purpose. Mounting details (mechanical) are shown in Figure 3.

NOTE

Program control of the LTC function and bus termination is not possible when remote installation is used. However, manual control of the LTC function is available via the optional console panel.

Electrical connection between the KPV11 option and the LSI-11 bus is made via a 10-pin connector (J1) on the KPV11 and a 10-pin connector on the backplane (H9270 or DDV11-B) in which the processor is installed. The optional signal cable (part no. 70-12754) provides the electrical connection between the two 10-pin connectors.

The +5 V and +12 Vdc voltage sense input must be provided by the user when the KPV11 option is not installed in an LSI-11 backplane. Etched pads are provided on the KPV11 module for this purpose and are located as shown in Figure 1. Connect the +5 V, +12 V, and GND pads to the respective LSI-11 backplane power terminals.

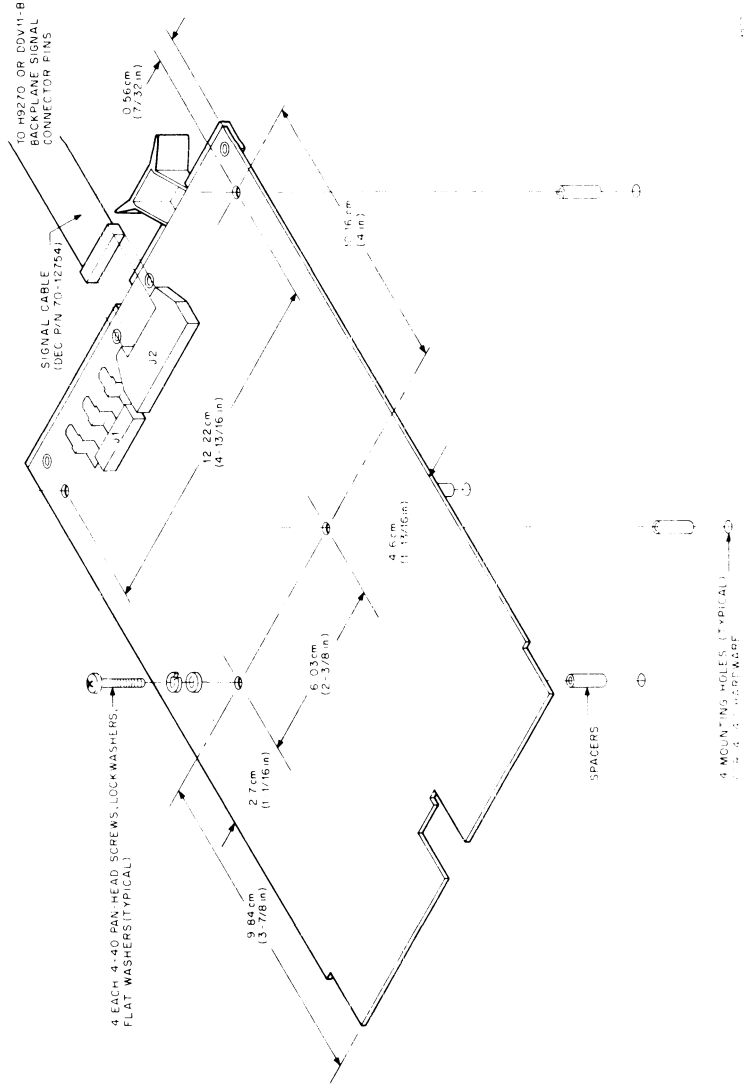


Figure 3 Remote Installation Details

If the optional console panel is to be used and the RUN indicator function is desired, a wire must be installed between the SRUN L pin (pin 3) on the 10-pin connector on the backplane and processor module pin AH1. A wire is normally factory-installed for this purpose on all backplanes except DDV11-B backplanes.

Power Sense Connections

Three tabs on the KPV11 are provided for connecting the option to a 24 Vac center-tapped transformer. This 50 or 60 Hz input voltage produces the required dc operating voltages for the option, provides the 50 or 60 Hz reference for the LTC function, and is the power-fail monitor signal for the power signal sequence circuit. This voltage must be supplied by the user. A transformer can be connected as shown in Figure 1 for this purpose. When the KPV11 is used with a 50 Hz input voltage, resistors R35 and R54 must be removed for proper power-fail time to compensate for the change in frequency. The location of these resistors is shown in Figure 4.

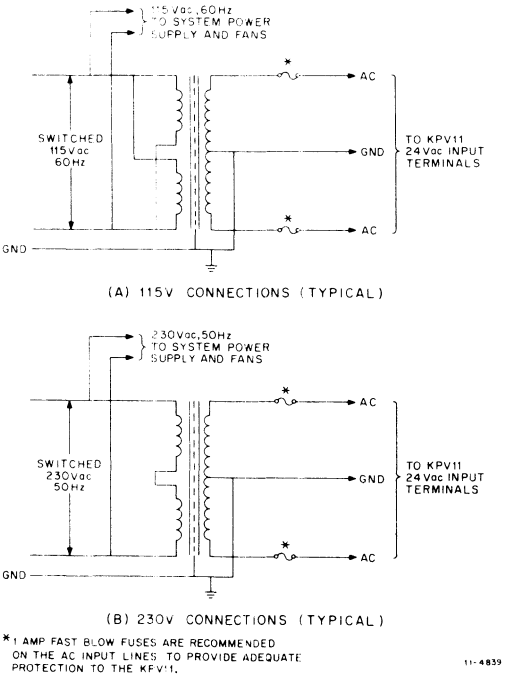


Figure 4 Power Line Monitor Transformer Installation

Installing Console Panel

The optional console panel can be mounted as shown in Figure 5. Electrical connections between the KPV11 and the console panel are made via 16-pin dual-in-line integrated circuit sockets located on each assembly. The electrical connection between the sockets is made using a signal/power cable (part no. 70-08612-OD).

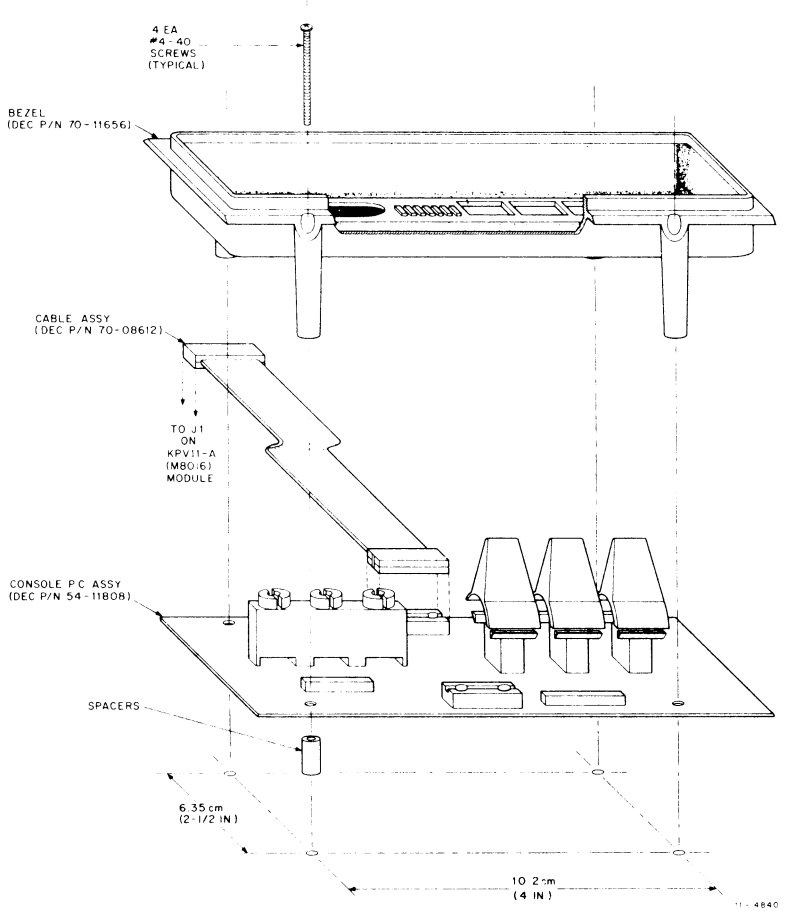


Figure 5 Console Panel Installation

In addition to the LTC ON/OFF and RUN/ENABLE switch functions, the console panel includes a DC ON/OFf switch. This switch, when in the OFF position, disables BDCOK H and BPOK H signal generation. If desired, this switch can also control the DC ON/OFF state of the user's power supply. This function is enabled by connecting the REMOTE DC ON/OFF and GND etched pads on the KPV11 module to an appropriate control circuit in the power supply. The signal thus produced is TTL-compatible and is capable of sinking 16 mA signal current in its logical low (DC ON) state. The logical high state is the DC OFF condition.

Using an External Time Reference

The KPV11 normally uses the 50 or 60 Hz input (via the three power tabs on the module) for LTC signal generation. However, an external frequency source may be used for producing LTC signals at frequencies other than the power line frequency. An etched pad is provided for this purpose on the KPV11 module. First, cut or remove jumper W15; this jumper and the external clock (EX CL) pad are located as shown in Figure 1. Then, connect the external frequency source to the EX CL and GND pads. The frequency source must be TTL logic-compatible; the KPV11 presents three TTL loads to the source.

Console Operation

The console panel option controls and indicators are shown in Figure 6 and described in Table 3.

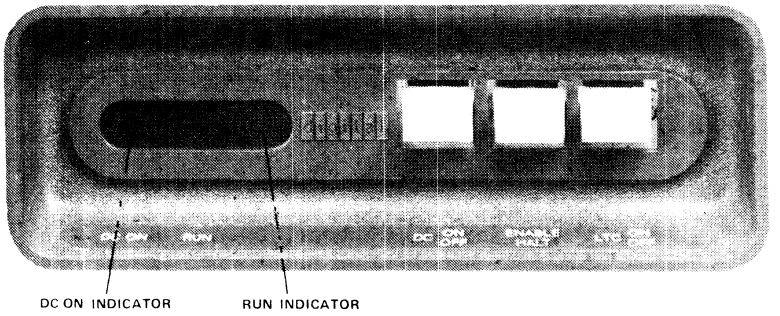


Figure 6 Console Panel Controls and Indicators
(P/N 54-11808 and 70-11656 shown)

Table 3 Console Panel Controls and Indicators

Control/ Indicator	Type	Function
DC ON	LED indicator	Illuminates when the DC ON/OFF toggle switch is set to ON and proper dc output voltages are being produced by the user's power supply and sensed by the KPV11 option. If either the +5 V or +12 V output from the power supply is faulty, the DC ON indicator will not illuminate.
RUN	LED indicator	Illuminates when the processor is in the run state (see ENABLE/HALT)
Spare	LED indicator	
DC ON/OFF	Two-position toggle switch	When set to ON, enables the dc outputs of the user's power supply (if connected for this function—see instructions for installing the console panel). The DC ON indicator will illuminate if the dc output voltages are of proper values. When set to OFF, the power supply dc outputs are disabled and the DC ON indicator is extinguished.
ENABLE/HALT	Two-position toggle switch	When set to ENABLE, the BHALT L line to the processor is not asserted and the processor is in the run-enable mode (RUN indicator is illuminated only when the processor is executing a program). When set to HALT, the BHALT L line is asserted. The processor halts program execution and executes console ODT microcode. The RUN indicator is extinguished.
LTC ON/OFF	Two-position toggle switch	When set to ON, enables KPV11 option generation of LTC interrupts. When set to OFF, disables LTC interrupts (W14 must be installed).

PROGRAMMING

Power-Down and Power-Up Routines – Power-down and power-up routine examples for systems using core memory are provided in Figures 7 and 8. The power-down routine shown provides an orderly power-down sequence of the system and saves the contents of the general-purpose registers along with the stack pointer and the processor status word. Other device registers which the user desires saved during power-down can be included through the use of the MOV @ NAME – (SP) instruction.

The power-down routine is entered via the routine's starting address ($PWRDN) in interrupt vector location 24; location 26 should contain 200_8 to disable device interrupts during the power down sequence. The first MOV instruction temporarily replaces the power-down vector address with the address of a HALT instruction ($HLT). This prevents an erroneous power-up attempt during the power-down routine execution. A sequence of MOV instructions then saves register contents on the stack. The second from the last MOV instruction, however, saves the SP in location $SAVR6, which is dedicated by the program for this purpose. It is the last register saved by the routine. The starting address ($PWRUP) for the power-up routine is then written into location 24, replacing the temporary $HLT address. Finally, the program halts and the power-down sequence is completed.

```
$PWRDN:  MOV     #$HLT,@#24        ;DISABLE FALSE
                                   ;RESTART SEQUENCE
         MOV     R0,—(SP)          ;PUSH R0 ON STACK
         MOV     R1,—(SP)          ;PUSH R1 ON STACK
         MOV     R2,—(SP)          ;PUSH R2 ON STACK
         MOV     R3,—(SP)          ;PUSH R3 ON STACK
         MOV     R4,—(SP)          ;PUSH R4 ON STACK
         MOV     R5,—(SP)          ;PUSH R5 ON STACK
         MOV     @NAME,—(SP)       ;SAVE ANY NECESSARY
                                   ;DEVICE REGISTERS
                 .
                 .
                 .
         MOV     SP,$SAVR6         ;SAVE SP
         MOV     #$PWRUP,@#24      ;SET POWER-UP VECTOR
$HLT:    HALT                      ;POWER-DOWN
                                   SEQUENCE
                                   ;DONE, READY FOR
                                   ;POWER-UP SEQUENCE.
$SAVR6:  .WORD 0                   ;SP SAVED HERE
```

Figure 7 Power-Down Routine Programming Example

```
$PWRUP: MOV     #$ILLUP,@#24    ;SET FOR FAST DOWN
        MOV     $SAVR6,SP       ;GET SP
        MOV     (SP)+,@NAME     ;RESTORE ANY DEVICE
                                ;REGISTERS SAVED
                .
                .
                .
        MOV     (SP)+,R5        ;POP STACK INTO R5
        MOV     (SP)+,R4        ;POP STACK INTO R4
        MOV     (SP)+,R3        ;POP STACK INTO R3
        MOV     (SP)+,R2        ;POP STACK INTO R2
        MOV     (SP)+,R1        ;POP STACK INTO R1
        MOV     (SP)+,R0        ;POP STACK INTO R0
        MOV     #$PWRDN,@#24    ;SET UP THE POWER-
                                DOWN VECTOR
        TYPE                    ;REPORT THE POWER
                                ;FAILURE
$PWRMG: .WORD   $POWER          ;POWER FAIL MESSAGE
        RTI                     ;POINTER
$ILLUP: HALT                    ;THE POWER-UP
                                ;SEQUENCE WAS
                                STARTED
        BR      .2              ;BEFORE THE POWER-
                                DOWN
                                ;WAS COMPLETE
$POWER: .ASCIZ  <15><12>"POWER"
```

Figure 8 Power-Up Routine Programming Example

When power is restored, the power-up routine is entered via the routine's starting address ($PWRUP) in interrupt vector location 24. The power-up routine shown in Figure 8 uses the $HLT and $SAVR6 locations shown in the power-down routine for disabling false power-down sequences and restoring the stack pointer, respectively. The first two MOV instructions reference those locations. A sequence of MOV instructions that follow restore device and processor registers, respectively. The last MOV instruction writes the starting address ($PWRDN) for the power-fail routine in location 24, replacing the temporary $HLT address. Finally, the RTI instruction pops the PC and PS of the program where the power-down sequence occurs from the stack and normal program execution is restored.

Programming the LTC – The LTC function normally divides time into 16-2/3 ms or 20 ms intervals determined by the line frequency source (60 Hz or 50 Hz, respectively). It is possible to disable the line frequency

source and use an external frequency source (user- supplied). The program communicates with the LTC function via the LKS register (Figure 9) contained in the KPV11 logic circuits. The LKS register's device address is normally configured to 177546 for system software compatibility.

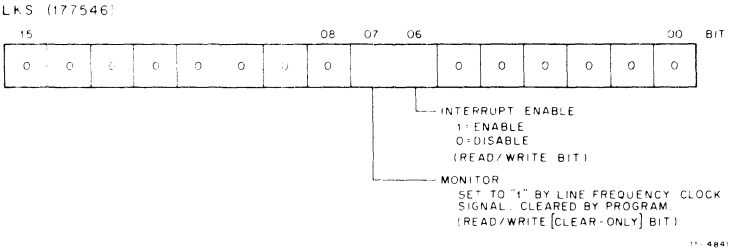


Figure 9 Line-Time Clock Status Register (LKS)

LTC interrupts, when enabled (LKS bit 6 = 1), occur as an interrupt request (bus low assertion) on the BEVNT L signal line. This causes the processor to execute a service routine via vector address 100. Memory location 100 must contain the PC (starting address) for the LTC service routine; similarly, memory location 102 must contain the PS (processor status word) for the service routine. As with all "external" interrupts, the processor will recognize the LTC interrupt request only when current PS bit 7 is cleared. When PS bit 7 = 1, external interrupts, including the LTC interrupt, are ignored. The LTC interrupt has highest priority of all external interrupts and does not require a vector address bus transfer. An interrupt request via the BEVNT L bus signal line, as previously stated, always results in access to the service routine via vector address 100.

The KPV11 is factory-configured for programmable operation as described above. If the user's hardware configuration also includes the optional console panel, the operator can disable or enable the LTC function by setting the LTC ON/OFF switch to the desired position. When set to the OFF position, the LTC switch overrides program control and LTC operation is disabled. W14 must be installed for this function.

FUNCTIONAL DESCRIPTION

General

The KPV11-A provides two main functions – power signal sequence circuits and programmable line-time clock circuits. The KPV11-B and KPV11-C have, in addition, bus termination circuits, 120 Ω for the

KPV11-B and 220 Ω for the KPV11-C. All KPV11 modules have an interface for the optional console panel. Figure 10 illustrates the basic KPV11 functions.

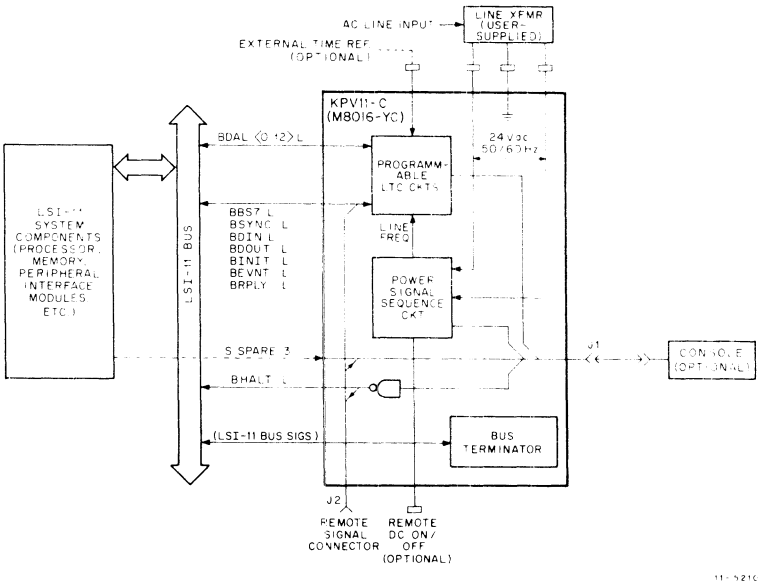


Figure 10 KPV11 Functional Block Diagram

Power Signal Sequence Circuits

The power signal sequence circuits generate the proper LSI-11 bus power sequencing signals (BPOK H and BDCOK H) for the processor power-up/power-down sequence and line-time clock interrupts at the power line frequency. Figure 11 illustrates the KPV11 power signal sequence timing.

Power signal sequence circuits are shown in Figure 12. Operating power for these circuits is obtained from the 24 Vac, 50 Hz or 60 Hz input at the two ac terminals and GND. Conventional full-wave rectifiers produce +17 V and −17 V operating voltages for the ac line monitor Schmitt trigger (Q1 and Q2) and a 5 V, 3-terminal regulator; the regulator +5 V is distributed throughout the power signal sequence circuit for operating power.

Power-Up – During the power-up sequence, ac voltage from the transformer secondary is applied to a Schmitt trigger circuit (Q1 and Q2). The Schmitt trigger squares the ac sine-wave and drives level converter Q3. Q3's output is a TTL-compatible signal. The square wave signal is applied to two 10 ms (nominal) one-shots (and the LTC circuits). One one-shot triggers on the positive-going transition of the square wave signal and the other triggers on the negative-going transition. The one-shot outputs are ORed, producing a high (normal) output at gate E6-13. Normally, one one-shot or the other will be in the set state. If a transition of the square wave signal is not followed by a transition of the opposite polarity within 20 ms, both one-shots will time out and the logic signal at E6-13 will go low; this is a power-fail condition.

During a power-up sequence voltage sense +5 V and +12 V (remote sense), or +5 V and +12 V (LSI-11 backplane voltages) inputs rise to voltage levels that cause voltage comparators A and B to produce high outputs. The comparator outputs are connected and applied to one input of gate A. The remaining input of gate A is enabled by the normally high gate E6-13 signal, which is applied (but not delayed) via the 3 ms delay circuit. Gate A's output goes high. This signal is then delayed 17 ms and inverted, producing a low signal which is applied to the non-inverting input of comparator C and gate C. Comparator C's output goes low, turning off Q4 and producing an active BDCOK H signal 17 ms (minimum) after ac power is applied.

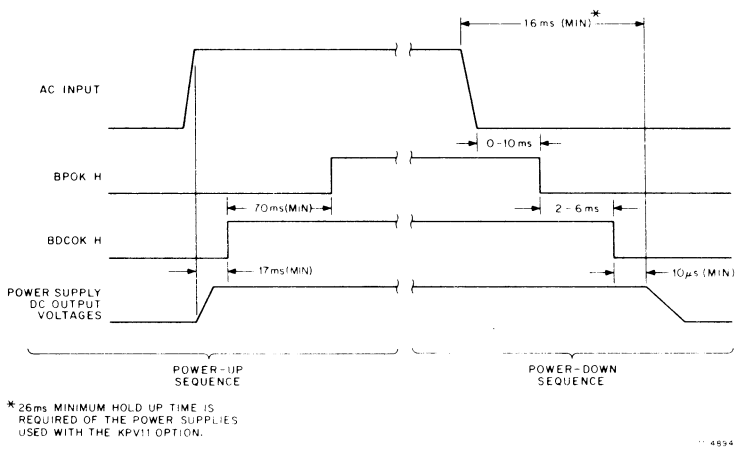


Figure 11 Power Signal Sequence Timing

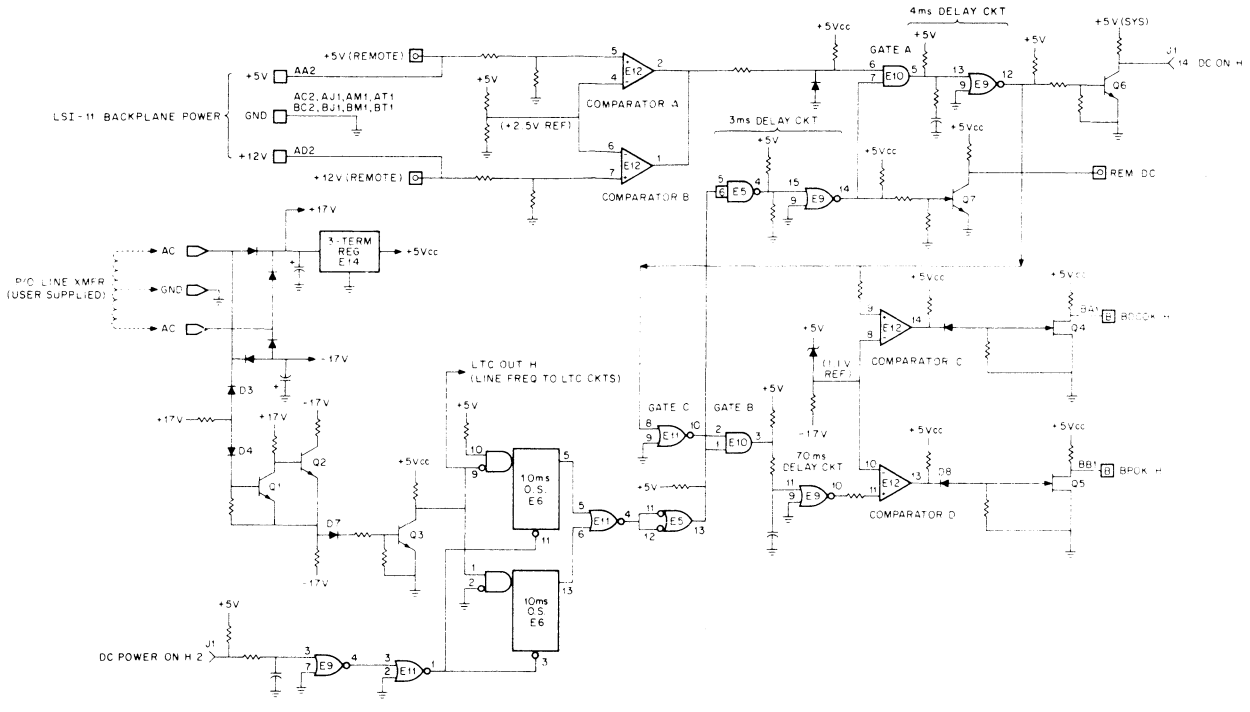


Figure 12 Power Signal Sequence Circuits

Gate C's output goes high, enabling gate B. The remaining gate B input is enabled by the high gate E6-13 output signal. Gate B's high output signal is delayed 70 ms and inverted, producing a low signal (E10-10) which is applied to the non-inverting input of comparator D. Comparator D's output signal goes low, turning off Q5, and producing the active BPOK H signal 70 ms after the active BDCOK H signal. With both signals in the active (high) state, normal system operation can proceed.

Power-Down – When an ac power failure occurs, the trigger pulses to the one-shots cease, and both one-shots time out. Gate E6-13 goes low, inhibiting gate B, and initiating the 3 ms delay. (E6-4 signal voltage starts to rise from the logical low state). Gate B's output goes low; this low signal is inverted, but not delayed, by the 70 ms delay circuit, and the resulting high signal is applied to the non-inverting input of comparator D. Comparator D's output goes high, turning on Q5, and negating BPOK H. Meanwhile, the 3 ms delay circuit, after the 3 ms delay, produces a low signal at E10-14. A low signal inhibits gate A, causing its output signal to go low. The low signal inhibits gate A, causing its output signal to go low. The low signal is inverted (but not delayed) by the 17 ms delay circuit, and applied to the non-inverting input of comparator C. Comparator C's output goes high, turning on Q4 and negating the BDCOK H signal 3 ms after BPOK H becomes negated. Q6 monitors the 17 ms delay circuit output and produces the DC ON H signal for the remote console panel display. When dc voltages are normal, E10-12 goes low; Q6 cuts off and DC ON H goes high. When dc voltages are not present, E10-12 goes high; Q6 turns on and negates DC ON H.

When the remote console panel is connected to the KPV11, the DC ON/OFF switch can simulate a power line failure and control the user's power supply. The simulated power line failure occurs when a low DC POWER ON H occurs (DC OFF switch position). This low signal produces a low signal that clears both one-shots, and the simulated power failure results.

Remote control of the user's power supply is made possible via the REMOTE DC ON/OFF etched pad. The signal present at this point is the 3 ms delay circuit signal (E10-14) inverted by Q7. Thus, when normal line voltage is sensed and the remote console panel DC ON/OFF switch is not in the OFF position, this signal goes low, activating a control circuit in the user's power supply that turns dc voltages on. When this signal is high – a result of power-fail or placing the remote console panel DC ON/OFF switch in the OFF position – the user's power supply dc output voltages should turn off.

Programmable Line-Time Clock (LTC) Circuits

Programmable line-time clock functions are shown in Figure 13. Jumpers allow selection of line frequency or external time base operation,

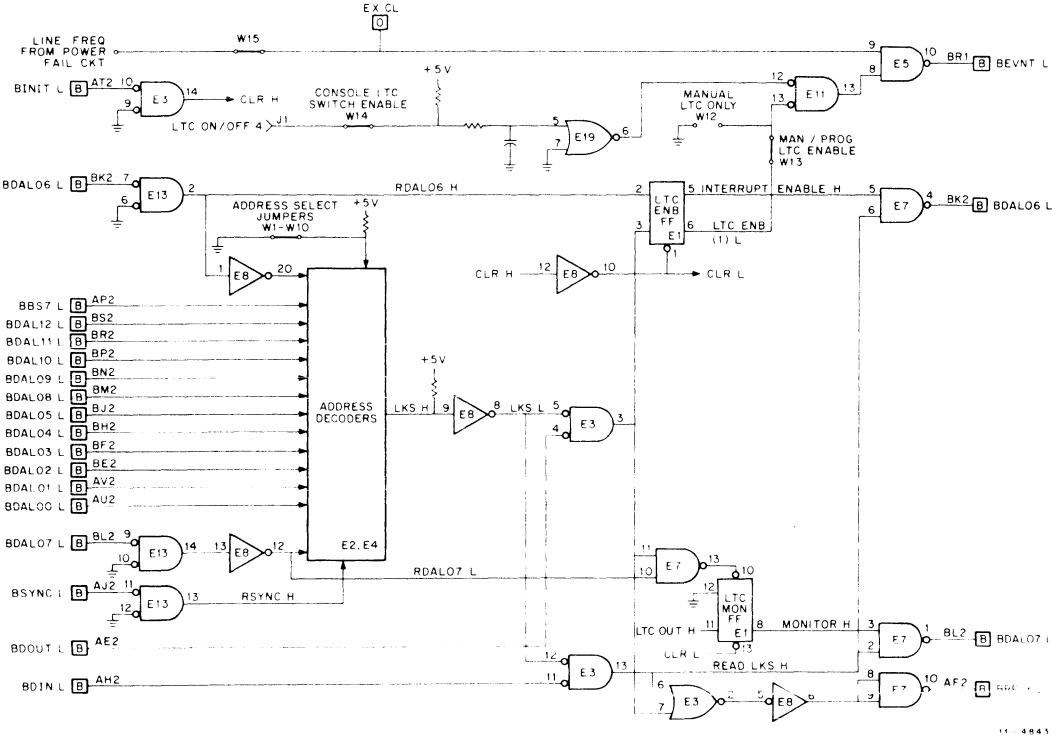


Figure 13 Programmable Line-Time Clock Circuits

console LTC ON/OFF switch enable/disable, and manual/programmable operation. Additional jumpers (W1–W10) select the device address for the LKS register. Jumpers are factory-configured as shown in Figure 2.

Program access to the LKS register is via the address configured by jumpers W1–W10. The processor first places the KPV11 LKS register address on BDAL (00:15) L and asserts BBS7 L. Note that BBS7 L is asserted only during an addressing operation when BDAL (13:15) L are asserted; hence, the address decoders receive only BDAL (00:12) L and BBS7 L. Device selection occurs on the leading edge of BSYNC L. If the address input matches the jumpered address, LKS H goes high (true), and remains true for the duration of the LSI-11 bus cycle.

Two flip-flops comprise the two significant bits of the LKS register. Bit 6 is produced by the LTC enable flip-flop. Similarly, bit 7 is produced by the LTC monitor flip-flop.

During a programmed write operation (DATO, DATOB, or the write portion of DATIO, or DATIOB bus cycle), LKS L (LKS H inverted) and BDOUT L are ANDed to produce an active (high) WRITE LKS H signal. The leading edge of LKS H clocks the logical state of RDAL06 H into the LTC ENB flip-flop, enabling or disabling LTC interrupts. The LTC MON flip-flop however, can only be preset during the write cycle. Note that the LTC MON flip-flop, when preset, is read as a logical 0 via the flip-flop's Q output; when the flip-flop is reset, it is read as a logical 1. RDAL07 L (0=high) is ANDed with WRITE LKS H, producing a low signal that presets the flip-flop; MONITOR H then goes low.

Normally, the LTC ON/OFF input to E10-5 is passive (high), producing a low at E10-6 that enables AND gate input E13-12. When interrupts are enabled, LTC ENB (1) L enables E13-11 and E13-13 goes high. This signal then enables one input of the BEVNT L bus driver. The remaining bus driver input is the LTC H signal. Thus, when LTC H goes high, BEVNT L goes low, and the LTC interrupt request is presented to the processor.

The leading edge of LTC H also clocks the LTC MON flip-flop to the reset state and MONITOR H goes true (high). MONITOR H conditions one input of the BDAL07 H bus driver. During a read cycle (DATI, or the read portion of the DATIO cycle), LKS L and BDIN L are gated to produce an active (high) READ LKS H signal. READ LKS H enables both BDAL07 L and BDAL06 L bus drivers, gating the monitor and interrupt enable status bits onto the LSI-11 bus.

During both programmed read and write bus cycles, the KPV11 must respond by asserting BRPLY L. READ LKS L and WRITE LKS L are ORed and applied to the BRPLY L to produce the appropriate device response according to LSI-11 bus protocol.

The optional console panel includes the LTC ON/OFF switch. When placed in the OFF position, J1-4 is low; E10-6 goes high, inhibiting E13-12 and LTC interrupt requests are disabled. This function can be disabled by removing W14.

When manual-only LTC operation is desired, W13 is removed and W12 is installed. E13-11 is continuously enabled and LTC interrupt requests can be disabled via the console panel LTC ON/OFF switch; W14 must be installed for this operation.

Bus Terminations

The KPV11-C provides 120 Ω bus termination, while the KPV11-B has 220 Ω bus terminations. Each bus signal line termination includes two resistors as shown in Figure 14. Termination resistors are contained in 16-pin dual-in-line packages that are physically identical to integrated circuit packages. Each package contains 14 terminations. Daisy-chained grant signals are jumpered but are not terminated. BIAKI L is jumpered to BIAKO L and BDBMGI L is jumpered to BDMGO L.

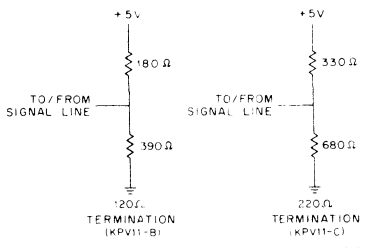


Figure 14 KPV11-B and KPV11-C Bus Terminations

Console Panel Interface

The option console panel interfaces with the system via the KPV11 module as shown in Figure 15. The DC ON indicator (D1) is directly driven by the DC ON H driver (Q6) in the power signal sequence circuit.

The RUN indicator is driven by the processor-generated SRUN L signal pulse. The 200 ms one-shot receives a continuous series of trigger pulses, when the processor is in the "run" (program execution) state, that keeps the one-shot in the retriggered state. When in this state, the one-shot produces a high signal that turns on the RUN indicator (D2) via the LED driver. When the processor is halted, the 200 ms one-shot times out, and the RUN indicator extinguishes.

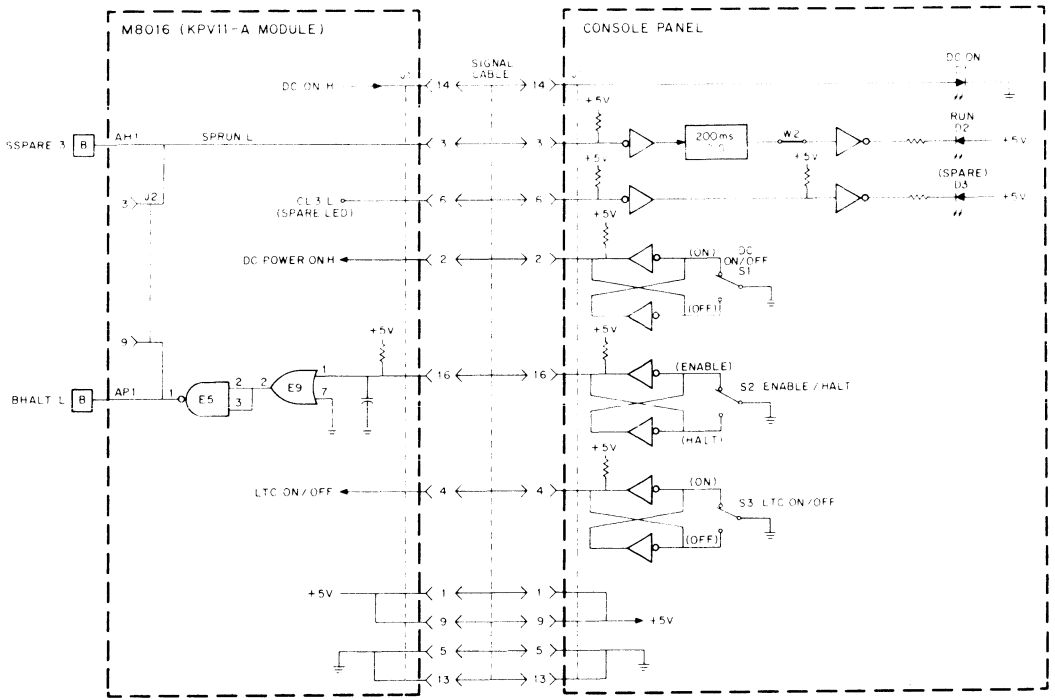


Figure 15 Console Panel Interface

The three console switches each include a "debounce" circuit composed of cross-coupled inverters. DC ON/OFF and LTC ON/OFF functions are used as previously described for power signal sequence and programmable line-time clock circuits, respectively.

The ENABLE/HALT switch enables the run mode (by not asserting BHALT L) or halts the processor; when halted, console ODT microcode operation is invoked. An R-C filter and BHALT L bus driver circuit on the KPV11 module interface this function to the LSI-11 bus.

KWV11-A PROGRAMMABLE REAL-TIME CLOCK

GENERAL

The KWV11-A is a programmable clock/counter that provides a variety of means for determining time intervals or counting events. It can be used to generate interrupts to the processor at predetermined intervals, to synchronize the processor to external events, or to measure time intervals or establish programmed ratios between input and output events. It can also be used to start the ADV11-A analog-to-digital converter either by clock counter overflow or by the firing of a Schmitt trigger.

The clock counter has a resolution of 16 bits and can be driven from any of five internal crystal-controlled frequencies (100 Hz to 1 MHz), from a line frequency input or from a Schmitt trigger fired by an external input. The KWV11-A can be operated in any of four programmable modes: single interval, repeated interval, external event timing, and external event timing from zero base.

The KWV11-A includes two Schmitt triggers, each with integral slope and level controls. The Schmitt triggers permit the user to start the clock, initiate A/D conversions, or generate program interrupts in response to external events.

FEATURES

- Resolution of 16 bits
- Can be driven by an external input or from any of five internal frequencies
- Four programmable modes
- Slope and reference signal level selection switches
- Can be used to start the ADV11-A analog-to-digital converter.

SPECIFICATIONS

Identification	M7952
Size	Quad
Power	+5 Vdc ± 5% at 1.75 A +12 Vdc ± 3% at 0.01 A
Bus Loads	
AC	3.4
DC	1

KWV11-A

Operational

Clock

Accuracy	0.01%
Range	Base frequency (10 MHz) divided into five selectable rates (1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz); line frequency, Schmitt trigger 1 input

Input Signals

1. ST1 IN (Schmitt Trigger 1 Input)

Input Range (maximum limits)	−30 V to +30 V
Assertion Level	Depends upon position of slope reference selector switch and level control; triggering range, −12 V to +12 V
Origin	User device
Response Time	Depends on input waveform and amplitude; typically 600 ns with TTL logic input
Hysteresis	Approximately 0.5 V, positive and negative
Characteristics	Single-ended input; 100 kΩ impedance to ground

2. ST2 IN (Schmitt Trigger 2 Input)

Same description as ST1 IN

Output Signals

1. CLK OV (Clock Overflow)

Asserted Level	Low
Destination	User device or ADV11-A
Duration	Approximately 500 ns

Characteristics

TTL open-collector driver with 470 Ω pull-up to +5 V

Maximum source current from output through load to ground when output is high (≥2.4 V): 5 mA

Maximum sink current from external source voltage through load to output when output is low (≤0.8 V): 8 mA

2. ST1 Out (Schmitt Trigger 1 Output)

   Same description as CLK OV

3. ST2 Out (Schmitt Trigger 2 Output)

   Same description as CLK OV

CONFIGURATION

The following paragraphs describe the procedure for device and interrupt vector address selection, slope and reference level selection, user connections, and programming. (Refer to the ADV11-A when using the KWV11-A with that module.)

Device Address Selection

The KWV11-A contains two device registers that can be addressed by the processor. These registers are the control/status register (CSR) and buffer/preset register (BPR). The BPR's address is always equal to the CSR address plus two. Thus only the CSR address is configured by the user as shown in Table 1.

Table 1 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address
Registers			
Control/Status	CSR	R/W	170420
Buffer/Preset	BPR	R/W	170422
Interrupts			
Clock Overflow	CLK OV	–	440
Schmitt Trigger 2	ST2	–	444

Slope selection is accomplished by separate switches for ST1 and ST2, respectively. When the related switch is on, the firing point effectively occurs on the positive slope of the input waveform. When the switch is off, the firing point occurs on the negative slope. R18 or R19 are used to set the level of the reference. Typical slope selection is shown in Figure 5.

NOTE

User should take care that both TTL and variable switches for either Schmitt trigger are not on simultaneously. This condition will do no damage to components, but produces unpredictable reference levels. Note also that if no signal is connected to a Schmitt trigger input, both threshold switches for that ST should be open for noise immunity. Alternatively, ST1 IN and ST2 IN can be grounded externally.

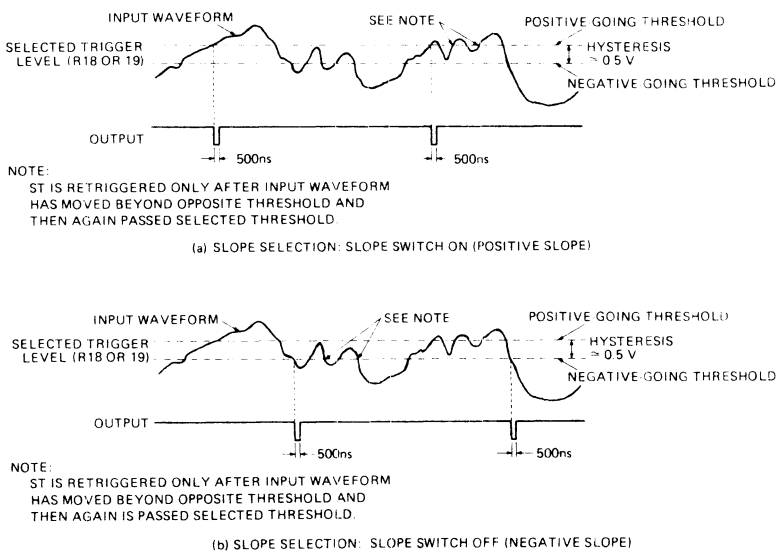


Figure 5 KWV11-A Slope Selection

Register Format

CSR Bit Assignments – CSR bit assignments are identified in Figure 6 and defined in Table 2.

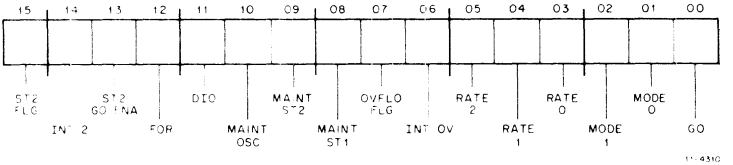


Figure 6 CSR Bit Assignments

Table 2 KWV11-A CSR Bit Definitions

Bit/CSR Name	Set By/Cleared By	Remarks
15/ST2 Flag Read/write to 0	Set by the firing of Schmitt trigger 2 or the setting of the MAINT ST2 bit in any mode while the GO bit or the ST2 Go Enable bit is set. Cleared under program control. Also cleared at the "1"-going transition of the GO bit unless the ST2 Go Enable bit has previously been set.	Must be cleared after servicing an ST2 interrupt to enable further interrupts. When cleared, any pending ST2 interrupt request will be cancelled. If enabled interrupts are requested at the same time by bits 7 and 15, bit 7 has the higher priority.
14/INT 2 (Interrupt on ST2) Read/write	Set and cleared under program control.	When set the assertion of ST2 Flag will cause an interrupt. If set while ST2 Flag is set, an interrupt is initiated. When cleared, any pending ST2 interrupt request will be cancelled.

Table 2 KWV11-A CSR Bit Definitions (Cont)

Bit/CSR Name	Set By/Cleared By	Remarks
13/ST2 Go Enable Read/write	Set and cleared under program control. Also cleared at the "1"-going transition of the GO bit.	When set, the assertion of ST2 flag will set the GO bit and clear the ST2 Go Enable bit.
12/FOR (Flag Overrun) Read/write	Set when an overflow occurs and the Overflow flag is still set from a previous occurrence, or when ST2 fires and the ST2 flag is already set. Cleared under program control and at the "1"-going transition of the GO bit.	This bit provides the programmer with an indication that the hardware is being asked to operate at a speed higher than is compatible with the software.
11/DIO (Disable Internal Oscillator) Read/write	Set and cleared under program control.	For maintenance purposes, this bit inhibits the internal crystal oscillator from incrementing the clock counter. Used in conjunction with bit 10.
10/MAINT OSC Write only	Set under program control. Clearing is not required. Always read as a "0."	For maintenance purposes, setting this bit high simulates one cycle of the internal 10 MHz crystal oscillator used to increment the clock counter.
9/MAINT ST2 Write only	Set under program control. Clearing is not required. Always read as a "0."	Setting this bit simulates the firing of Schmitt trigger 2. All functions initiated by ST2 can be exercised under program control by using this bit.

Table 2 KWV11-A CSR Bit Definitions (Cont)

Bit/CSR Name	Set By/Cleared By	Remarks
8/MAIN~ ST1 Write only	Set under program control. Clearing is not required. Always read as a "0."	Setting this bit simulates the firing of ST1. All functions initiated by ST1 can be exercised under program control by using this bit.
7/OVFLO FLAG Read/write to 0	Set each time the counter overflows. Cleared under program control and at the "1"-going transition of the GO bit.	If bit 6 is set, bit 7 will initiate an interrupt. Bit 7 must be cleared after the interrupt has been serviced to enable further overflow interrupts. If cleared while an overflow interrupt request to the processor is pending, the request is cancelled. If enabled interrupts are requested at the same time by bits 7 and 15, bit 7 has the higher priority.
6/INTOV (Interrupt on Overflow) Read/write	Set and cleared under program control.	When this bit is set, the assertion of OVFLO flag will generate an interrupt. Interrupt is also generated if bit 6 is set while OVFLO flag is set. If cleared while an overflow interrupt request to the processor is pending, the request is cancelled.

Table 2 KWV11-A CSR Bit Definitions (Cont)

Bit/CSR Name	Set By/Cleared By	Remarks
5-3/RATE Read/write	Set and cleared under program control.	These bits select clock counting rate or source. **5 4 3 Rate** 0 0 0 STOP 0 0 1 1 MHz 0 1 0 100 kHz 0 1 1 10 kHz 1 0 0 1 kHz 1 0 1 100 Hz 1 1 0 ST1 1 1 1 Line (50/60 Hz)
2-1/MODE Read/write	Set and cleared under program control.	**Function 2 1** Mode 0 0 0 Mode 1 0 1 Mode 2 1 0 Mode 3 1 1
0/GO Read/write	Set and cleared under program control. Also cleared when the counter overflows in mode 0.	Setting this bit initiates counter action as determined by the rate and mode bits. In modes 1, 2, and 3 it remains set until cleared. In mode 0 it clears itself when counter overflow occurs. Clearing bit 0 clears and inhibits the counter.

Buffer/Preset Register (BPR) – The BPR is a 16-bit, word-oriented, read/write register. Any attempt to write a byte into this register will result in a whole word being written. In modes 0 and 1, the program may load it with the 2's complement of the number of counts desired before overflow. In modes 2 and 3, it permits indirect reading of the clock counter.

Normal Control Sequences – Mode 0 (Single Interval)
Control code for operation in mode 0 must support the following sequence:

1. The control program writes the desired count (2's complement) into the BPR.

2. The program writes the control code into the control/status register as indicated in Table 3.

Table 3 CSR Bit Settings for Mode 0, Single Interval

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
15	ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of GO bit assertion except when ST2 GO ENA has previously been set.
14	INT 2	x	Set to 1 by program if interrupt on ST2 event is desired.
13	ST2 GO ENA	x	Set to 1 by program if GO is to be set by external signal to ST2. Cleared by leading edge of GO bit assertion.
12	FOR	(0)	
11	DIO	0	
10	MAINT OSC	0	
9	MAINT ST2	0	
8	MAINT ST1	0	
7	OVFLO FLG	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of GO bit assertion.
6	INT OV	x	Set to 1 by program for interrupt on counter overflow.
5	RATE 2	x	See Table 2.
4	RATE 1	x	
3	RATE 0	x	
2	MODE 1	0	Set by program to 0.
1	MODE 0	0	Set by program to 0.
0	GO	x	Set by program to 1 unless ST2 GO ENA is set; remains 1 until written to 0 by program. Cleared when counter overflows.

x = 0 or 1, depending on user requirements.
(0) = Automatically cleared by GO bit assertion.

3. If the GO bit is set high, KWV11-A responds by loading the 16-bit counter from the BPR and enabling the counter; if the GO bit is set low and the ST2 Go Enable bit is set high, KWV11-A waits for ST2 event, then sets the GO bit and loads and enables the counter.

4. The counter increments until overflow, then halts (GO bit is cleared).

5. KWV11-A raises the Overflow flag and issues an interrupt if the CSR INT OV bit is set; if the interrupt is not enabled, KWV11-A waits for program intervention.

6. The program responds to the interrupt or intervenes in consequence of other criteria (e.g., testing the Overflow flag or the A/D Done flag if overflow was used to start an A/D conversion). The program reads the CSR, clears the Overflow flag, and if no counting or mode changes are required, sets the GO bit or the ST2 GO ENABLE bit to reenter the sequence at step 3.

Mode 1 (Repeated Interval)
Control code for operation in mode 1 must support the following sequence:

1. The control program writes the desired count (2's complement) into the BPR.

2. The program writes the control code into the CSR as indicated in Table 4.

3. If the GO bit is set high, KWV11-A responds by loading the 16-bit counter from the BPR and enabling the counter; if the GO bit is set low and the ST2 GO ENABLE bit is set high, KWV11-A waits for ST2 event, then sets the GO bit and loads and enables the counter.

4. The counter increments until overflow.

5. KWV11-A reloads the counter from the BPR, reenables the counter, raises the Overflow flag in the CSR, and issues an interrupt to the processor if interrupt is enabled.

6. If a second overflow occurs before the first is serviced (i.e., if Overflow flag is still high when next overflow occurs), the KWV11-A Flag Overrun (FOR) bit in the CSR is set high to alert the program that data has been lost.

7. The program responds to the interrupt or intervenes in consequence of other criteria. The program reads the CSR, clears the Overflow flag, and if no counting or mode changes are required, sets the GO bit or the ST2 Go Enable bit to reenter the sequence at step 3.

Table 4 CSR Bit Settings for Mode 1, Repeated Interval

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
15	ST2 FLG	0	Will be set to 1 or ST2 event. Cleared by leading edge of GO bit assertion except when ST2 GO ENA has previously been set.
14	INT 2	x	Set to 1 by program if interrupt on ST2 event is desired.
13	ST2 GO ENA	x	Set to 1 by program if GO is to be set by external signal to ST2. Cleared by leading edge of GO bit assertion.
12	FOR	(0)	
11	DIO	0	
10	MAINT OSC	0	
9	MAINT ST2	0	
8	MAINT ST1	0	
7	OVFLO FLG	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of GO bit assertion.
6	INT OV	x	Set to 1 by program for interrupt on counter overflow.
5	RATE 2	x	See Table 2
4	RATE 1	x	
3	RATE 0	x	
2	MODE 1	0	Set by program to 1.
1	MODE 0	1	
0	GO	x	Same as for Mode 0, except that bit is not cleared when counter overflows.

x = 0 or 1, depending on user requirements.
(0) = Automatically cleared by GO bit assertion.

Mode 2 (External Event Timing)
Control code for operation in mode 2 must support the following sequence:

1. The program writes the control code into the CSR as indicated in Table 5.

Table 5 CSR Bit Settings for Mode 2, External Event Timing

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
15	ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of GO bit assertion except when ST2 GO ENA has previously been set.
14	INT 2	x	Set to 1 by program if interrupt on ST2 event is desired.
13	ST2 GO ENA	x	Set to 1 by program if GO is to be set by external signal to ST2. Cleared by leading edge of GO bit assertion.
12	FOR	(0)	
11	DIO	0	
10	MAINT OSC	0	
9	MAINT ST2	0	
8	MAINT ST1	0	
7	OVFLO FLG	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of GO bit assertion.
6	INT OV	x	Set to 1 by program for interrupt on counter overflow.
5	RATE 2	x	See Table 2
4	RATE 1	x	
3	RATE 0	x	
2	MODE 1	1	Set by program to 2.
1	MODE 0	0	
0	GO	x	Set by program to 1 unless ST2 GO ENA is set; remains 1 until written to 0 by program. Cleared when counter overflows.

x = 0 or 1, depending on user requirements.
(0) = Automatically cleared by GO bit assertion.

2. KWV11-A responds by incrementing the counter (cleared when the GO bit was cleared) at the selected rate until the GO bit is set to 0.

3. ST2 pulse loads the current counter contents into the BPR, sets the ST2 flag, and generates an interrupt if INT 2 is enabled.

4. Overflow sets OVFLO FLG high and, if INT OV bit is high, generates an interrupt.

5. The counter continues to increment until the processor sets the GO bit to 0.

Normally, the program enables the INT 2 and/or INT OV bits, permitting the processor to synchronize its operations with the external ST2 events and prevent loss of data by reinitializing the process after step 4.

Mode 3 (External Event Timing from Zero Base)
Operation is identical to that in mode 2 except that counter is cleared after the ST2 pulse. The counter continues to increment until the GO bit is set to 0.

Note that the interval between two ST2 events may be measured directly in mode 2 or 3 with processor assistance if the CSR ST2 Go Enable and interrupt 2 bits are set before the first event and the GO bit is left clear. Under these conditions, the first ST2 event will set the GO bit (and thus start the counting process) and simultaneously issue an interrupt. If the interrupt service routine now clears the ST2 flag bit, the next ST2 event will cause the BPR to be loaded from the counter in the normal mode 2 fashion. The choice of mode 2 or mode 3 for such measurements will depend on whether or not an on-going accumulation of time after the second event is required by the application. If such an accumulation is necessary, mode 2 is appropriate since the counter is not cleared after ST2 events.

Programming Example
Record the point in double-precision timeframe for each S12 event following GO. The program makes use of a 32-bit counter, the low-order bits of which are taken directly from the KWV11-A (KWBPR) and the high-order bits of which are taken from a software counter (HICNT) that is incremented with each KWBPR overflow.

```
MTPS    #0                  ;CLEAR PSW
MOV     #ST2SRV, @ST2VEC    ;LOAD ST2 VECTOR
                            ;ADDR
MOV     #200,@ST2PSW        ;SET UP PSW FOR ST2
                            ;INTERRUPT (DISABLE
                            ;ALL SUBSEQUENT
                            ;INTERRUPTS)
MOV     #OVSRV, @OVVEC      ;LOAD OV VECTOR
                            ;ADDR
MOV     #200,@OVPSW         ;SET UP PSW FOR OV
                            ;INTERRUPT (DISABLE
                            ;ALL SUBSEQUENT
                            ;INTERRUPTS)
```

```
                .
                .
                MOV     #BUFFER, R0             ;SET UP POINTER TO
                                                ;BEGINNING OF
                                                ;BUFFER AREA
CLKGO:          MOV     #40115,@#KWCSR          ;DEPOSIT 1MHZ, MODE 2,
                                                ;INT ON EF, INT ST2 EN,
                                                ;AND GO INTO KWCSR
COUNT:          WAIT                            ;FOR INTERRUPT
                                                ;BY OVFLO OR ST2
                BIT     #100000,@#KWCSR         ;IS EF BIT SET?
                BEQ     COUNT                   ;NO, CONTINUE
                JMP     FORSRV                  ;YES, SERVICE FLAG
                                                ;OVERFLOW CONDITION
OVSRV:          BIT     #100000,@#KWCSR         ;IS ST2 FLAG SET?
                BEQ     2$                      ;NO, CONTINUE
                TST     @#KWBFR                 ;DID ST2 OCCUR BEFORE OV?
                BPL     2$                      ;NO, BRANCH
                MOV     #1CNT,(R0)+             ;YES, SERVICE ST2 FIRST
                MOV     @#KWBFR,(R0)+
                BIC     #100000,@#KWCSR         ;ACKNOWLEDGE ST2
                                                ;OCCURRENCE
```

User Connections

A 40-pin type H854 connector (J1) is provided on the KWV11-A for user connections as shown in Figure 7. This connector will mate with an H856 connector. External user-supplied slope and level controls can be

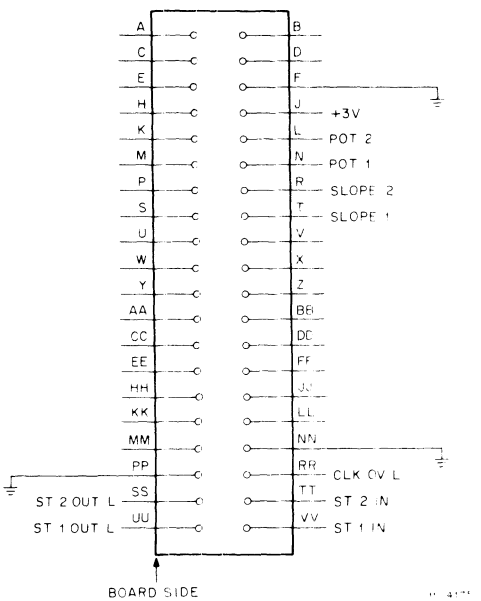


Figure 7 J1 40-Pin Connector Pin Assignments

interfaced via this connector as shown in Figure 8. J1 can be connected to the optional H322 distribution panel for convenient user access, via an optional BC08R cable.

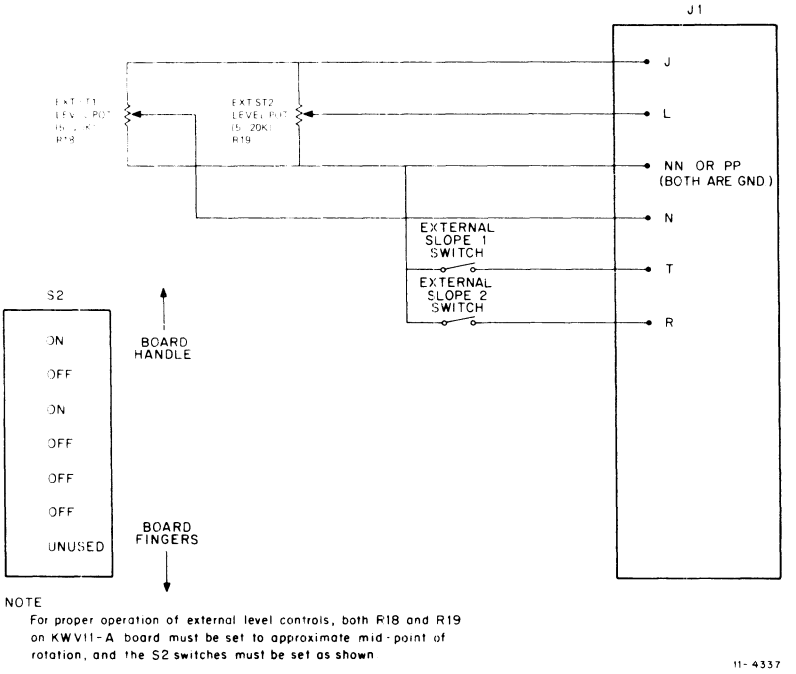


Figure 8 Connecting External User-Supplied Slope and Level Controls

In addition, two tabs (CLK and ST1) are located on the module as shown in Figure 1. These tabs are electrically connected to J1 pins RR (CLK OV L) and UU (ST1 OUT L); the tabs may be used to connect the KWV11-A functions to ADV11-A TAB S (external start) and TAB C (clock overflow), respectively, in an ADV11-A. Optional jumpers (DEC part no. 70-10771) are available for this purpose.

FUNCTIONAL DESCRIPTION

General

Functions comprising the KWV11-A are shown in Figure 9.

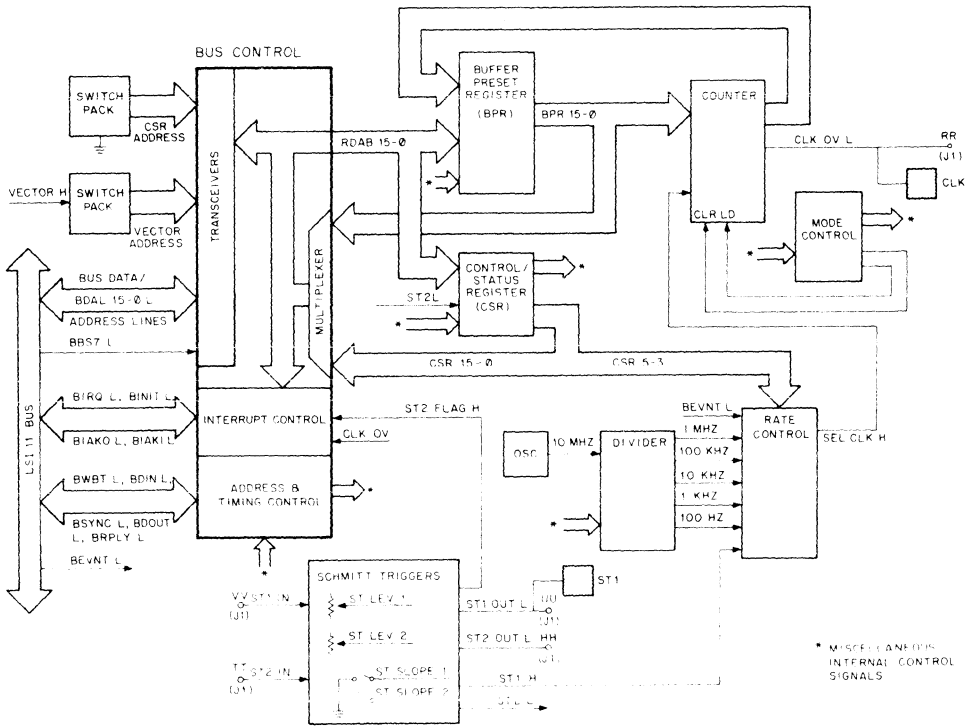


Figure 9 KWV11-A Real-Time Clock Block Diagram

The logic associated with the bus control block maintains proper communications protocol between the processor bus and the KWV11-A. This logic generates and monitors the bus signals involved during interrupts and data transfers between the processor and the KWV11-A. It permits the KWV11-A to recognize when it is being addressed by the processor (address defined by the address switch pack), to prescribe the location in memory pointing to the starting addresses of interrupt service routines (by means of the vector switch pack), to input control data from the processor, and to output data to the processor.

Interrupts can be enabled for both counter overflow and operation of ST2. Since each of these conditions raises a flag bit in the control/status register, and since separate interrupt vectors exist for each condition, the conditions may be distinguished either by vectors or by testing flag bits.

Control/Status Register
The control/status register (CSR) provides a means for the processor to control the operation of the KWV11-A and to derive information about its operating condition. Bits are provided for enabling interrupts, mode selection, maintenance operations, starting the counter, and overflow and Schmitt trigger event monitoring.

Mode Control
Logic circuitry associated with the mode control block permits KWV11-A operation in four different modes as specified by bits 2–1 of the CSR.

Mode 0 (Single Interval) – When the GO bit is set in this mode either by the processor or by a Schmitt trigger 2 event, the counter is loaded from the buffer/preset register (which has previously been loaded with the 2's complement of the number of counts desired before overflow). Once loaded, the counter will increment at the selected rate until it overflows. Overflow clears the GO bit, sets the Overflow flag, and interrupts the processor if that function has been enabled. If interrupt has not been enabled, the KWV11-A waits for processor intervention.

Mode 1 (Repeated Interval) – When the GO bit is set in this mode, the counter is loaded from the buffer/preset register (BPR) and is then incremented to overflow as for mode 0. In mode 1, however, overflow does not clear the GO bit; instead, it causes the counter to be reloaded from the BPR, raises the Overflow flag, initiates an interrupt sequence if the CSR Interrupt on Overflow bit is set, and causes the count to be continued with no loss of data.

Mode 2 (External Event Timing) – When the GO bit is set in this mode, the counter is set to 0 and then incremented at the selected rate as long as the GO bit remains set. An external signal to Schmitt trigger 2 (ST2) causes the current contents of the counter to be loaded into the BPR

while the counter continues to run. At the same time, the ST2 flag is set and, if Interrupt 2 is enabled, an interrupt is generated, thus permitting the program to read the value held in the BPR.

The counter continues to run after the ST2 event and also continues to run after overflow. Interrupt on Overflow may be enabled to alert the program to the overflow condition.

Mode 3 (External Event Timing from Zero Base) – Operation in mode 3 is identical to that in mode 2 except that the counter is zeroed each time an ST2 event loads its contents into the BPR.

Flag Overrun – In all modes, if a second overflow occurs before the Overflow flag is reset (i.e., before a prior event is serviced by the processor), or if ST2 fires when the ST2 flag is already set, the Flag Overrun bit is set.

Oscillator, Divider, Rate Control Chain
The circuitry associated with these blocks provides the time base that is fed to the counter. The KWV11-A permits eight clock conditions to be specified by bits 5–3 of the CSR: STOP, 1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz, an external time base applied to ST1, and line frequency (50 or 60 Hz) picked up from bus line BEVNT. External periodic or aperiodic pulses may be applied to ST1 and counted.

Buffer/Preset and Counter Registers
The buffer/preset register is a word-oriented, 16-bit read/write register that can be loaded either under program control or from the counter. In modes 2 and 3, the firing of ST2 causes the BPR to be loaded with the contents of the counter. The BPR cannot be loaded by the program in these modes as long as the GO bit is set.

The counter is a 16-bit internal register accessible only by way of the BPR; in modes 2 and 3 it can be read indirectly through the BPR.

Schmitt Triggers
Both Schmitt triggers are equipped with switches to permit selecting slope direction (+ or –) and threshold reference level (TTL or –12 V to +12 V continuously variable). Each Schmitt trigger is also equipped with a screwdriver-operated potentiometer to permit setting the variable threshold level. Switch pack and potentiometer terminals are all brought to multiple connector J1 to permit attachment of external user-provided slope and level controls.

The two Schmitt triggers are used in somewhat different ways.

ST1 – Performs as an external time base input or external input for aperiodic signals to be counted. Outputs both to ST1 Faston connector to provide external start signals to ADV11-A and, through rate control circuitry, to permit selection as input to the counter. Maximum frequency varies as a function of input waveform.

ST2 – When the ST2 Go Enable bit is set, firing ST2 in any mode sets the GO bit and initiates counter action, causes the ST2 flag to be asserted, and generates an interrupt if that function is enabled. When the GO bit is set in modes 2 and 3, firing ST2 causes the buffer/preset register to be loaded from the counter, the ST2 flag to be set, and an interrupt to be generated if enabled.

LAV11 PRINTER OPTION

GENERAL

The LAV11 is an option that enables a processor to interface with an LA180 DECprinter. The LAV11 option consists of an interface module, an LA180 DECprinter, and a BC11S-25 interface cable. The LAV11 is software-controlled by the processor and outputs ASCII characters to the printer. The LAV11 also monitors the various printer conditions that require operator control.

FEATURES

- Device addresses and interrupt vectors can be configured by user
- Completely compatible with LSI-11 bus protocol and LA180 protocol
- Software compatible with all DIGITAL operating systems

SPECIFICATIONS

Identification	M7949
Size	Double
Power	+5 V ± 5% at 0.8 A
Bus Loads	
AC	1.8
DC	1

CONFIGURATION

The LAV11 interface module is shipped from the factory with jumpers and switches configured for standard (Digital Equipment Corporation software-compatible) device and interrupt vector assignments. It is normally not necessary for the user to configure the address or vector switches, unless special device addresses and/or interrupt vectors are desired. The factory-installed jumpers and switches are shown in Figure 1. The jumpers can be removed by carefully cutting each end close to the printed circuit board. Table 1 lists the special jumpers and the associated function that they control when the jumper is installed on the interface.

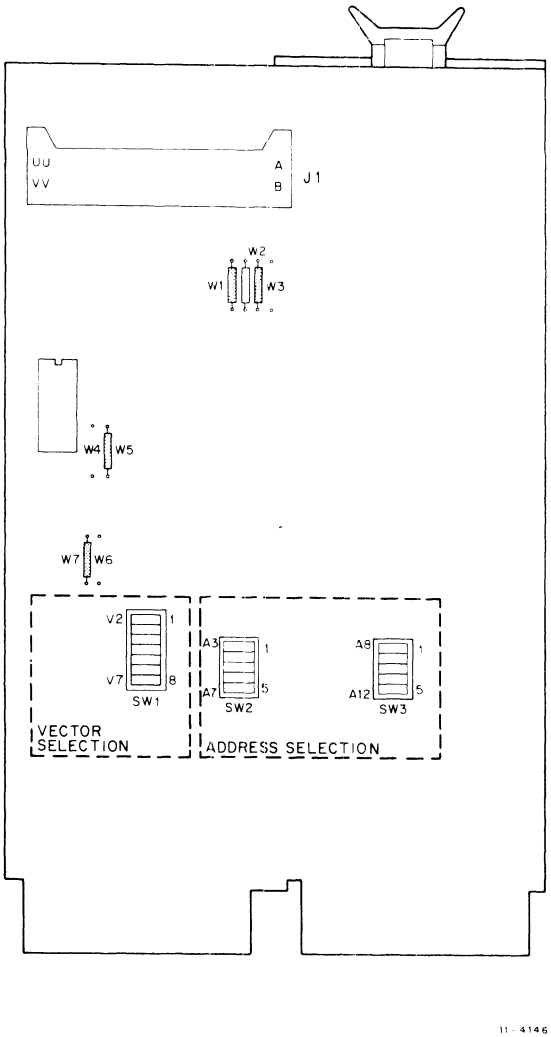


Figure 1 LAV11 Switch and Jumper Locations

Table 1 Special Jumpers

Jumper	Shipped Condition*	Function if Inserted
W1	I	Transmit parity on line
W2	I	+5 Vdc sense from LA180
W3	R	+5 Vdc sense from LAV11
W4	R	DEMAND is asserted low
W5	I	DEMAND is asserted high
W6	R	P STROBE is asserted low
W7	I	P STROBE is asserted high

*I = inserted R = removed

Device Address

The device address is selected by setting switches 1 to 5 in switch banks 2 and 3 to the standard address (Table 2). The LAV11 has a factory-set standard address of 177514 for the device control/status register. The data buffer register (DBR) is always set at the next address following the CSR address. The standard address for the DSR is 177516. If more than one LAV11 option is installed in the system, or if special device addresses are desired, set the switches (one for each CSR address bit) as directed in Figure 2.

Interrupt Vector

The interrupt vector is selected by setting switches 1 to 8 in the switch bank to the standard vector. The LAV11 module has a factory-set standard interrupt vector of 200_8. If more than one LAV11 option is installed in the system or if a special interrupt vector is desired, set the switches (one for each vector address bit) as directed in Figure 3.

Table 2 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Registers				
Control/Status	LPCSR	R/W	177514	(Use floating
Data Buffer	LPDSR	R/W	177516	address space)
Interrupt				
Done or Error	–	–	200	(Use floating vector space)

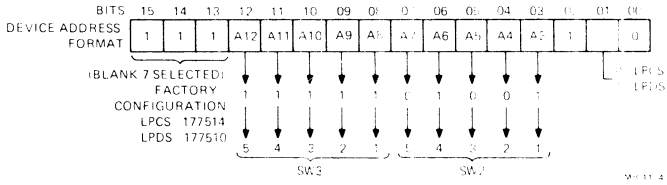


Figure 2 LAV11 Device Address Format

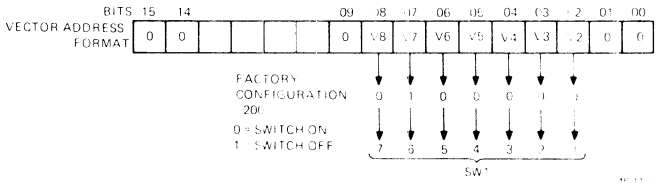


Figure 3 LAV11 Interrupt Vector Format

Parity (W1)
This jumper will allow a parity bit to be transmitted to the LA180 when inserted. Removing the jumper will disable the parity bit.

+5 Vdc Sense (W2, W3)
These jumpers allow the user to sense 5 Vdc from either the LA180 printer or the LAV11 interface. To sense the 5 Vdc from the LA180, leave W2 installed and remove W3. To sense 5 Vdc from the interface module, leave W3 installed and remove W2. Under no conditions should both jumpers be installed or removed.

Demand (W4, W5)
These jumpers allow the user to assert INTERNAL DEMAND from the LA180 on either a low level (zero) or a high level (one). For a low level, the user will leave W4 installed and remove W5. For a high level, the user will leave W5 installed and remove W4. Under no conditions should both jumpers be installed or removed.

P Strobe (W6, W7)
These jumpers allow the user to assert P STROBE on either a low level (zero) or a high level (one). For a low level, the user will leave W6

installed and remove W7. For a high level, the user will leave W7 installed and remove W6. Under no condition should both jumpers be installed or removed.

LA180 to LAV11 Interface Cable
The only acceptable cable for use between the LA180 and the LAV11 is the BC11S. The cable end labeled P2 must be attached to the LA180. The end labeled P1 must be attached to the LAV11.

LA180 Modifications
Jumper W6 must be inserted on the LA180 logic board (54-11023). This ensures +5 Vdc sense to the LAV11. Failure to insert this jumper will result in a continued error condition in the LAV11 LACS buffer.

Device Registers
All software control of the LAV11 is performed by means of two device registers. Each register has been assigned a bus address and can be read or loaded (with the exceptions noted) using any instruction that refers to those addresses.

The following discussion presents the bit assignments within the two device registers. Bits referenced as "unused" and "write-only" are always read as zeros. Loading "unused" and "read-only" bits has no effect on those bits.

Control and Status Register (CSR) – The address of the CSR is 177514 and the register data contains the control and status of the system. The data bit assignments of the register are shown in Figure 4, and the bit assignments are described in Table 3.

Data Buffer Register (DBR) – The address of the DBR is 177516 and the register data contains the data being processed by the system. The data bit assignments on the register are shown in Figure 5, and the bit assignments are described in Table 4.

Interrupt Servicing
Both the error and done bits are enabled by the same CSR bit (interrupt enable). When granted, the interrupt occurs using the vector block at location 200_8 (interrupt vector is limited to location 777_8). These bits do not occur in the set condition simultaneously. When servicing an interrupt, therefore, the routine must check the state of error and done in the CSR (bits 15 and 7) to determine which of the two flags caused the interrupt. Because the LAV11 is normally connected to the LSI-11 bus BIRQ L line, servicing the LAV11-originated interrupt request depends on its closeness to the processor via the priority daisy-chain network.

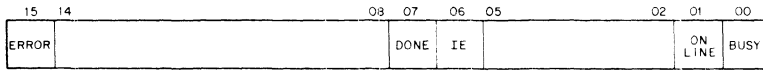


Figure 4 LAV11 CSR Bit Assignments

Table 3 LAV11 CSR Bit Definitions

Bit	Name	Description
15	Error	The error bit is asserted (1) when an error condition (i.e., torn or no paper) exists in the LA180. This is a read-only bit, which is reset only by manual correction of the error condition.
14–8	Unused	
7	Done	The done bit is asserted (1) when the printer is ready to accept another charac ter. This is a read-only bit set by INIT. The done bit is cleared by loading the LADB register. An interrupt sequence is started if IE (interrupt enable, bit 6) is also set.
6	Interrupt Enable	The interrupt enable bit is set or cleared (read or write bit) under program control. It is cleared by the INIT (initialize) signal on the LSI-11 bus. (INIT is caused by programmed reset instruction, console start function, or a power-up or power-down condition.) When IE is set, an interrupt sequence is started if either error or done is also set.
5–2	Unused	
1	On-Line	The on-line bit is asserted (1) when the LA180 printer (only) is on-line. It is a read-only bit.
0	Busy	The busy bit is asserted (1) when the LA180 printer (only) is performing a print or paper advance operation.

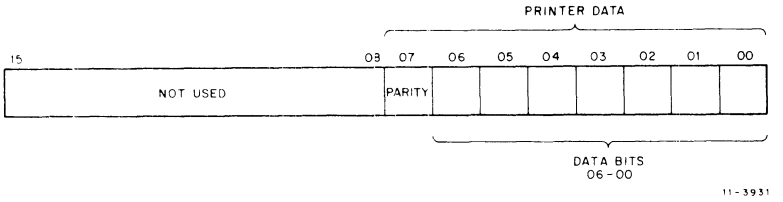


Figure 5 LAV11 DBR Bit Assignments

Table 4 LAV11 DBR Bit Definitions

Bit	Name	Description
15–8	Unused	
7	Parity	The parity bit is loaded with the data word if the parity jumper is installed. It is a write-only bit.
6–0	Data	The data character comprises seven bits, with bit 6 being the most significant. This buffered 7-bit character will be transferred to the LA180. These bits are all write-only bits.

FUNCTIONAL DESCRIPTION

General

The LAV11 controller handles data one character at a time by means of an interrupt service routine. Basically, the controller may be divided into three major functions: address selection logic, interrupt logic, and LA180 control logic. No data is stored in the controller; rather, the controller synchronizes the data flow between the processor and the LA180 DECprinter. A block diagram of the LAV11 is shown in Figure 6. The LA180 contains a 132-character buffer, which is loaded serially, character by character. Although characters are loaded serially into the buffer, each character is formed by loading seven bits (plus a parity bit) in parallel, resulting in an 8-bit character.

Adddress Selection Logic — Determines if LAV11/LA180 DECprinter has been selected for use and what type of operation (load data or read status) is to be performed.

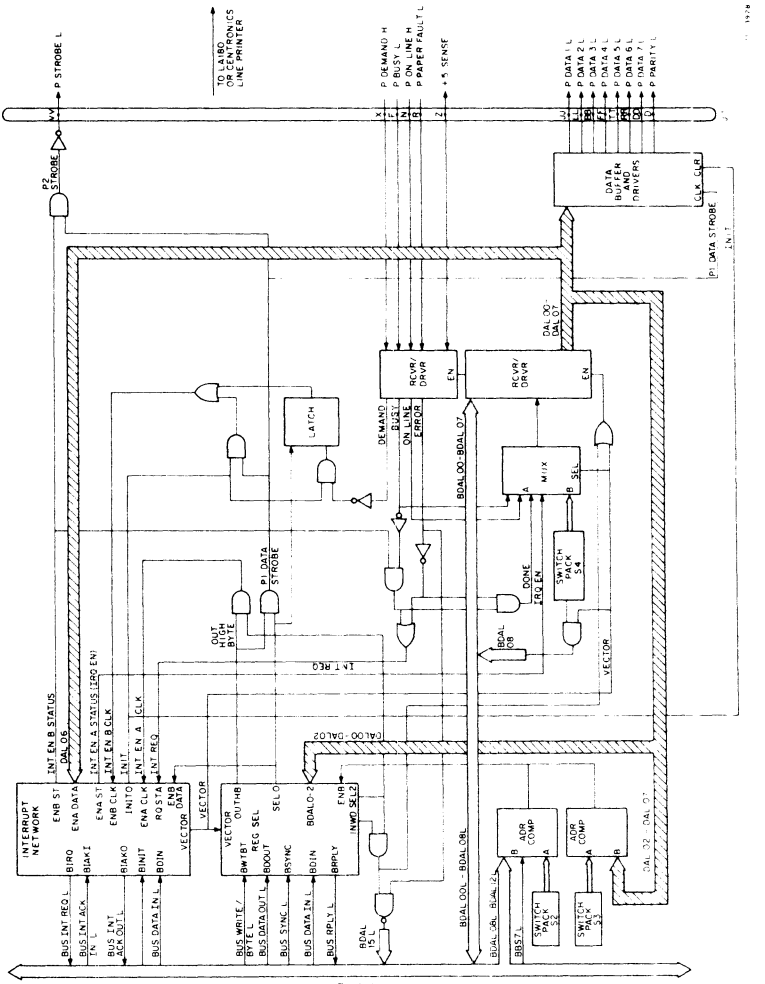


Figure 6 LAV11 Block Diagram

Interrupt Logic	Permits the LAV11 controller to interrupt the operation (background program) and cause execution of a device service routine before returning control to the background program.
LA180 Control Logic	Transfers data from the LAV11 to the LA180 and monitors the status register for conditions of interrupt enable, done, and error. It contains data receivers/drivers, status logic, interrupt network control, strobe circuitry, and all controlling logic.

All signals to and from the LA180 are true in the low (0.0 to +0.8 V) state, except P DEMAND and P ON LINE, which are true high (+2.0 to +5.0 V). These two signals determine the operational state of the LA180. The signals are applied from the LA180 to the LAV11. The P ON LINE H signal indicates that the LA180 primary ac power is on, all paper interlocks are closed, and the unit is on-line. The LA180 indicates that it is able to accept another printable character by causing P DEMAND H to go high

Nine output lines originate in the controller logic and terminate in the LA180. Seven of these are P DATA lines (P DATA 1 through P DATA 7), one is a parity bit (P PARITY) transferred with the character code, and the ninth is the P STROBE L line. When the P STROBE L signal asserts, information on the eight lines (7-bit character plus parity bit) is parallel transferred into the LA180, causing P DEMAND H to go low until the LA180 logic has shifted the printable character into its associated memory.

Address Selection

The address selection logic decodes the address information from the LSI-11 bus and provides four gating signals (only three are used) and four select line signals (only two are used) to control the LAV11 controller register selection. Switch packs are arranged so that the LAV11 responds to standard device register addresses 177514 and 177516. Actually, the device is capable of addressing from 16000x to 17777x (x = 0 or 2) with the use of these switch packs. Therefore, although these specific addresses have been selected by DIGITAL as the standard address assignments for the LAV11 controller, the user may change the switches to any address desired. However, any program that references the LAV11 controller standard address assignment must be modified if other than the standard address assignments are used.

The first five octal digits (17751x) indicate that the LAV11 has been selected as the device to be used. The final octal digit, compris ng DAL 00–02, determines which register has been selected (status/data buffer) by DAL 01–01 and if either a word or byte operation (DAL 00) s taking place. Two mode control lines (BDIN L and BDOUT L) determine whether the selected register is to perform an input or output function. Notice that signals BDIN L and BDOUT L are always used with respect to the LAV11 controller. Thus, an out-transfer (BDOUT L) is a transfer of data from the processor, through the LAV11 controller, to the LA180. Likewise, an in-transfer (BDIN L) is the operation of the controller furnishing information to the processor.

The address selection logic decodes the incoming address as described below:

1. Line DAL 00 is used for byte control.0

2. Lines DAL 01–02 are decoded to select one of the two registers.

3. Decoding of lines DAL 03–12 is determined by the switch packs. When a given line has its respective switch asserted, the address logic searches for a 0 on that line. If the switch is off (not asserted), the logic searches for a 1.

The address comparators compare the switch selected address with DAL 02–12 and BBS7 L. Signal BBS7 L is asserted by the LSI-11 when an address in its upper 4K bank is placed on the bus. The BSYNC L synchronize signal is then asserted by the LSI-11 to indicate that it has placed an address on the bus. The transfer is considered to be in progress until signal BSYNC L is negated. When the comparison is equal (DAL lines with the switches), a high output from the comparators asserts the ENB input on the register selection chip. This enable signal is latched internally with the assertion of BSYNC L and is used to enable the select outputs and the address term of signal BRPLY L. The bus then asserts either BDOUT L or BDIN L. Signal BDOUT L, when asserted, implies that valid data is available on the BDAL 00–15 lines, and that an output transfer (with respect to the LAV11) will take place. When asserted during BSYNC L time, signal BDIN L implies an input transfer will occur when the LAV11 is ready to accept information. (It should be noted here that when signal BDIN L is asserted without signal BSYNC L, an interrupt operation is occurring.)

Signal BRPLY is asserted in response to BDIN L or BDOUT L and during interrupt operations. The signal is generated by the LAV11 (to the LSI-11) to indicate that it has the expected address on the BDAL lines, or that it has accepted output data from the bus. Signal BDOUT L is deskewed with respect to data on the bus and the LAV11 must assert

BRPLY L to complete the transfer. Signal BDIN L also requires the BRPLY L response; the LAV11 must deskew input data from BRPLY L.

The VECTOR H (interrupt vector gating) signal from the interrupt network generates signal BRPLY L and gates the appropriate vector address onto the bus.

The address selection (register select) logic outputs permit selection of the two LAV11 device registers and provides three signals that are used for gating information into and out of the LAV11. Signals SEL 0 L and SEL 2 L (two additional lines are not used) are asserted by a function of DAL 01 or 02 if signal ENB H is asserted (at BSYNC L time). They indicate that a word register (status/data buffer) has been selected for a data transaction. Asserted with signal BSYNC L, they do not negate until BSYNC L negates.

The OUTHB H (out high byte) signal is a function of DAL 00, BWTBT L, and BSYNC L, and is used to load data into the higher byte of the selected register. While signal BDOUT L is asserted, signal BWTBT indicates either a byte or word operation (asserted = byte, not asserted = word). It is decoded with signals BDOUT L and latched BDAL 00 to form OUTLB L or OUTHB L (only OUTHB is used).

Interrupt Logic

The interrupt network logic allows the LAV11 controller to perform an interrupt operation. A switch pack offers the user a range of vector addresses from 000 to 777_8. The switches are arranged, however, so that the logic has a normal vector address of 200_8. Although this is the recommended vector address, the user may alter the switches to any desired address, but MAINDEC diagnostic programs and other software referencing the standard vector address assignment of 200_8 must be changed to reflect the new assignments.

An LAV11 interrupt is generated by a 1 being written into the interrupt enable (IE) bit (DAL 06) of the control/status register. When a 1 is written into bit 6 of the control/status register, it sets the ENA flip-flop to produce signal INT ENA STATUS H (IRQ EN), which determines the status of the internal interrupt enable "A" flip-flop. The data into the flip-flop is the 1 from DAL 06 and the clock input is the ENA CLK signal, INT ENA CLK (OUTHB and SEL 2 H).

When the LAV11 is not busy, signal -BUSY H is inverted and generates INT REQ H (RQSTA). If signal RQSTA is generated when the ENA ST flip-flop is asserted, the BIRQ L signal is developed by the interrupt network and placed on the LSI-11 bus. This tells the processor that an interrupt request is being made by the LAV11. The bus interrupt acknowledge in (BIAKI L) signal, preceded by BDIN L, is the processor's

response to BIRQ L being true. This signal is daisy-chained so that the first requesting device blocks the signal propagation while the non-requesting devices pass the signal on as BIAKO L to the next device in the chain. The leading edge of signal BIAKI L causes signal BIRQ L to be negated by the LAV11.

Once signal BIRQ L is acknowledged, signal BIAKI L is seen on the bus. This results in signal VECTOR H being generated, which gates the appropriate vector onto the bus. The signal also goes to the register selector logic to produce signal BRPLY, the reply to the bus starting the interrupt was generated.

Once the interrupt is generated, the interrupt vector is selected by the switch pack switches (V2–V8). The selectable 4-byte vector for the LAV11 is 200_8.

LA180 Control Logic

The LA180 control logic contains the data receivers/drivers and all the logic relative to the two device registers.

When the control/status register is to be read, signal DAL 02 L must be asserted with BDIN L asserted. Signal DAL 02 L enables the status register select line (SEL 2). Then signal BDIN L, the strobing signal from the processor, effects a data input transaction. This gates the control/status register (LACS) onto the bus.

The data buffer is a write-only register. Data is transmitted to the LA180 DECprinter by means of the output portion of a DATIO bus operation to the data buffer register (LADB). To place data on the P DATA 0–7 lines, both the DAL 02 and DAL 01 signals must be asserted low. This causes signal SEL 0 to be asserted low, placing a low on the ENB DATA input of the interrupt network.

Simultaneously with SEL 0 L, signal OUTHB L generates PI DATA STROBE H, which loads the byte to be written (sent to the printer) into the data buffer register. Signal SEL 0 also inputs to a latching network. When the P DEMAND H arrives from the printer, the latching network (enabled by INIT) outputs a pulse to the ENB CLK input of the interrupt network. This is the clock pulse for the ENB DATA line. The ENB STATUS output produced is delayed and inverted, and generates the P2 STROBE H signal. The strobe is deskewed by 75 ns to guarantee that P DATA has had time to settle at the line printer. Signal P2 STROBE H is inverted and becomes P STROBE L, which then sends P DATA 0–7 (and P PARITY) to the LA180 to be printed. When the printer receives P STROBE and samples the data lines, signal P DEMAND H goes false.

If the line printer is not operational, due either to a paper fault or a hardware error, an ERROR H signal is developed. This signal qualifies the same logic as described before to generate an INT REQ. Once the processor has received the interrupt request, it can read the status register bits to determine if the interrupt was caused by a data transfer being completed or because an error condition exists. The program can then take appropriate action.

An AND gate prior to DONE is qualified whenever the ERROR, BUSY, and ENB STATUS signals occur. This permits the LAV11 controller to recover and continue strobing without first issuing an INIT or delayed P2 STROBE. Once the error condition has been removed, the printer simply asserts P DEMAND H and operation begins.

Basic bus signal and printer control timing requirements are illustrated in Figure 7

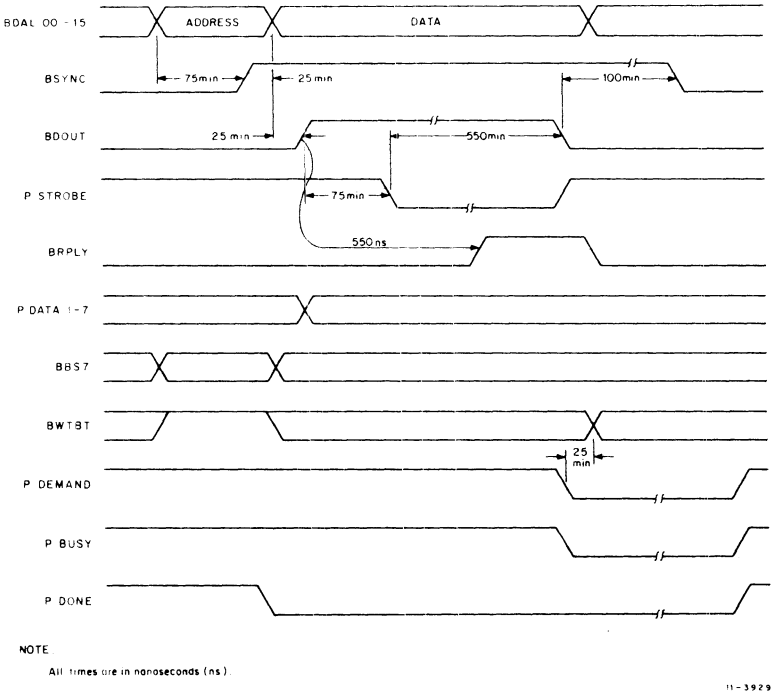


Figure 7 Bus Signal and LA180 Control Timing (Typical DOUT Bus Cycle)

LPV11 PRINTER OPTION

GENERAL

The LPV11 printer option is a high-speed line printer system for use with an LSI-11 system. The system consists of an LPV11 interface module, an interface cable, and a line printer (either an LP05 or LA180). The LPV11 interface module functions that are used with an LP05 or LA180 line printer are similar; however, the printer strobe signals required for each printer are different. The specific interface cable allows the interface module to detect which printer it is interfacing to, and automatically supplies the correct timing signals for the specific type of printer. The interface module is program-controlled to transfer data from an LSI-11 bus to the line printer. There are 12 option numbers that define the type of printer and four primary power (line) voltages. Printer types include the LA180 DECprinter and two LP05 line printer models (uppercase letters only, and both uppercase and lowercase letters). These models and their interface cables are defined in Table 1.

Table 1 LPV11 Option Model Numbers

Option No. (Model)	Interface Cable*	Primary Power	Model	Printer Description
LPV11-PA	BC11S-25	115 V, 60 Hz	LA180-PA	180 char/s
LPV11-PB	BC11S-25	230 V, 60 Hz	LA180-PB	printer, 132
LPV11-PC	BC11S-25	115 V, 50 Hz	LA180-PC	column, upper-and
LPV11-PD	BC11S-25	230 V, 50 Hz	LA180-PD	lowercase letters
LPV11-VA	70-11212-25	115 V, 60 Hz	LP05-VA	300 line/min
LPV11-VB	70-11212-25	230 V, 60 Hz	LP05-VB	printer, 132
LPV11-VC	70-11212-25	115 V, 50 Hz	LP05-VC	column, uppercase
LPV11-VD	70-11212-25	230 V, 50 Hz	LP05-VD	letters only
LPV11-WA	70-11212-25	115 V, 60 Hz	LP05-WA	240 line/min
LPV11-WB	70-11212-25	230 V, 60 Hz	LP05-WB	printer, 132 column
LPV11-WC	70-11212-25	115 V, 50 Hz	LP05-WC	upper- and lower-
LPV11-WD	70-11212-25	230 V, 50 Hz	LP05-WD	case letters

*7.62 m (25 ft) interface cable is supplied with each option.

FEATURES

- Models available for 115 or 230 Vac operation at either 50 or 60 Hz
- Line printers available with 132-column upper- and lowercase letters, or uppercase only

LPV11

- Line printers available with speeds of 180 characters per second (LA180), or 300 or 240 lines per minute (LP05)
- Interface module and interface cable supplied.

SPECIFICATIONS

Module	
Identification	M8027
Size	Double
Power	+5 V ± 5% at 0.8 A
Bus Loads	
AC	1.4
DC	1
Interface Cable	
Type	BC11S-25 or 70-11212-25, depending on LPV11 model (Table 1)
Length	7.62 m (25 ft) maximum
LP05 Line Printer	
Power	115 Vac ± 10%, 50/60 Hz ± 3 Hz or 230 Vac ± 10%, 50/60 Hz ± 3 Hz 700 W
Printable Characters	
64-Character Set	!"#$%&'( )*+,-./0123456789::<=>?@ ABCDEFGHIJKLMNOPQRSTUVWXYZ [\]^—
96-Character Set	All of the above plus a through z ~
Type	Open Gothic print
Size	Typically 0.024 cm (0.095 in) high; 0.065 cm (0.065 in) wide
Code Format	ASCII
Characters Per Line	132

Character Drum Speed	64-character drum: 1200 r/min 96-character drum: 800 r/min
Printer Characteristics	
Format	Top-of-form control; single line advance with automatic perforation step-over, and carriage return. Automatic vertical format control is optional.
Paper-Feed	One pair of pin-feed tractors for 1.27 cm (1/2 in) hole center, edge-punched paper.
Paper Slew Speed	50.8 cm (20 in) per second
Print Area	33.53 cm (13.2 in) wide, left justified
Character Spacing (horizontal)	0.254 ± 0.0127 cm (0.1 ± 0.005 in) between centers; maximum possible accumulative error for normal spacing is 0.0254 cm (0.01 in) per 80- or 132-character line.
Line Spacing	0.424 ± 0.025 cm (0.167 ± 0.01 in) at 6 lines per inch; 0.3175 cm (0.125 in) at 8 lines per inch. Each character within ± 0.254 cm (0.1 in) from mean line through character.
Line Advance Time	50 ms maximum
Character Synchronization	Variable reluctance pick-off senses drum position.
Physical Characteristics	
Height	1.14 m (45 in)
Width	0.81 m (32 in)
Depth	0.56 m (22 in)
Weight	150 kg (330 lb)
Ribbon Characteristics	
Type	Inked roll
Width	38.1 cm (15 in)
Length	18.288 m (20 yd)
Thickness	0.01 cm (0.004 in)

LPV11

Paper Characteristics	
Type	Standard fanfold, edge punched, 27.94 cm (11 in) between folds
Width	10.16 cm to 42.55 cm (4 in to 16-3/4 in) 15-lb bond minimum (single copy), 12-lb bond with single-sheet carbon for up to six parts (multiple copy)
Weight	15-lb bond minimum (single copy) 12-lb bond with single-sheet carbon for up to six parts (multiple copy)
Environmental	
Operating Temperature	10° to 32° C (50° to 90° F)
Humidity	30 to 90% (no condensation)
Print Rates	
LP05-VA, -VB, -VC, -VD (64-character drum)	300 lines/min
LP05-WA, -WB, -WC, -WD (96-character drum)	240 lines/min

LA180 DECprinter

Power	90–132 Vac or 180–264 Vac 50 or 60 Hz ± 1 Hz 400 W max (printing) 200 W max (idle)
Printable Characters	96 upper- and lowercase character set (7 X 7 dot matrix): +,-./0123456789:;<=>?@ ABCDEFGHIJKLMNOPQRSTUVWXYZ[\] ^_-abcdefghijklmnopqrstuvwxyz {|}~!"#$%&'()*
Code Format	ASCII
Non-Printable Characters	Six commands: BEL,BS,LF,FF,CR,DEL
Number of Characters Per Line	132 max
Type of Character Transfer	Parallel (7-bit plus parity)
Printer Characteristics	
Print Cycle Speed	Up to 180 characters per second

Line Printing Speeds	70 lines per minute on full line 300 lines per minute on short lines
Print Size	0.254 cm (10 characters per inch) horizontal 0.233 cm (6 lines per inch) vertical

CONFIGURATION

General

The M8027 interface module is shipped from the factory with jumpers configured for standard (DIGITAL software-compatible) device and interrupt vector assignments. It is normally not necessary for the user to configure the address or vector jumpers, unless special device addresses and/or interrupt vectors are desired. The factory-installed jumpers are shown in Figure 1. These jumpers can be removed by carefully cutting each end close to the printed circuit board. In addition to the factory jumpers, there is an alternate set of wire-wrap pins that allow the user to install additional or replacement jumpers by using the designated wire-wrap pins. In Figure 1, the dots represent wire-wrap pins and a line indicating a pair of pins shows the electrical connection that must be wire-wrapped to insert that jumper. Table 2 lists the factory jumpers installed and the additional jumpers that can be installed, as well as the associated functions. The factory-set addresses are listed in Table 3.

NOTE

Jumpers F+ (factory-installed W6) and F– do not have associated wire-wrap pins. These jumpers must be installed by soldering and removed by cutting or unsoldering.

Table 2 Jumper Designations

Jumper*	Function	Jumper*	Function
A3	Device Address	P	Parity
A4 (W2)	Device Address	T (W7)	Translate to Uppercase
A5 (W3)	Device Address	V2 (W9	Interrupt Vector
A6	Device Address	V3 (W10)	Interrupt Vector
A7 (W4)	Device Address	V4 (W11)	Interrupt Vector
A8	Device Address	V5 (W12)	Interrupt Vector
A9	Device Address	V6 (W13)	Interrupt Vector
A10	Device Address	V7	Interrupt Vector
A11	Device Address	V8 (W14)	Interrupt Vector
A12	Device Address	W1	Bus Reply Timing
F (W6)	Error Filter		

*Jumpers without W designation are not normally installed by factory.

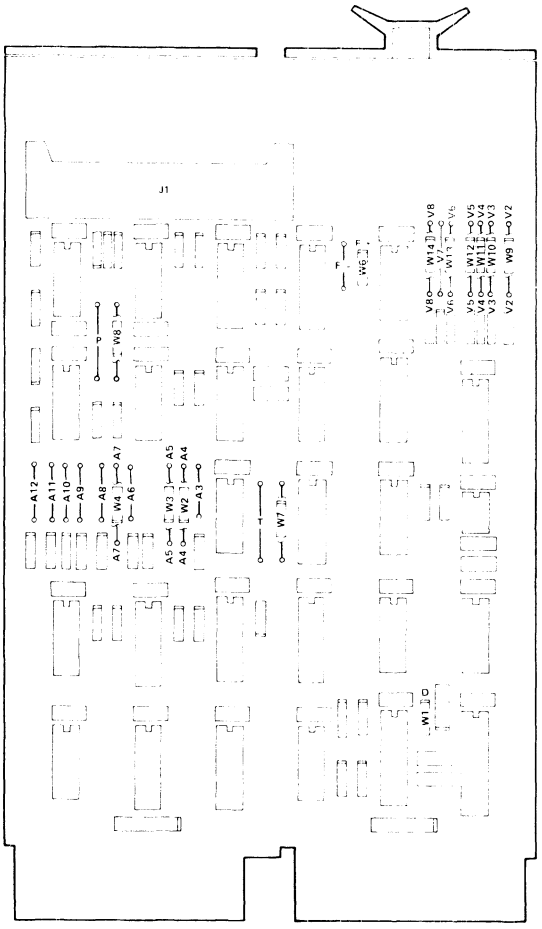


Figure 1 LPV11 Interface Module

Table 3 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Registers				
Control/Status	LPCS	R/W	177514	(Use floating
Data Buffer	LPDB	R/W	177516	address space)
Interrupts				
Done or Error		–	200	(Use floating vector space)

Device Address

The LPV11 is factory-configured for a device control/status register (CSR) address equal to 177514. The data buffer register (DBR) is always the configured CSR address +2; thus, the standard DBR address is 177516. If more than one LPV11 option is installed in the system, or if special device addresses are desired, remove and/or install jumpers (one for each CSR address bit) as directed in Figure 2.

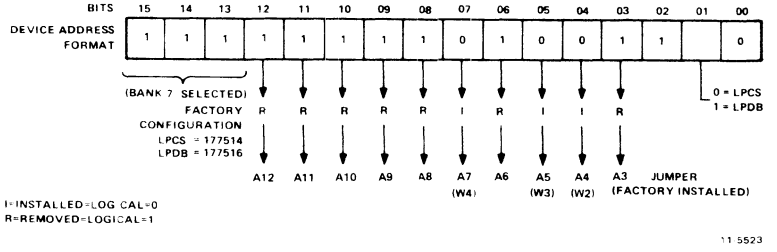


Figure 2 LPV11 Device Address Format and Jumpers

Interrupt Vector

The LPV11 is factory-configured for an interrupt vector equal to 200_8. If more than one LPV11 option is installed in the system, or if a special interrupt vector is desired, remove and/or install jumpers (one for each vector bit) as directed in Figure 3.

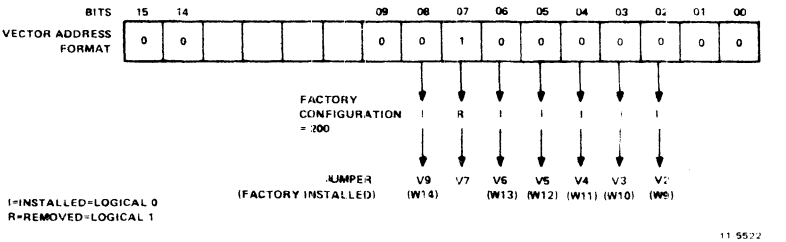


Figure 3 LPV11 Interrupt Vector Format and Jumpers

Bus Reply Timing
Jumper D (W1) is factory-installed to delay the BRPLY L bus signal timing for LPV11 use with LA180 printers. If desired, this jumper can be removed for use with future printers; however, the LP05 will function if it is left installed.

Uppercase Only
Jumper W7 is factory-installed and jumper T is not installed, enabling upper- and lowercase letters to be printed. If lowercase letters are not desired, remove W7 and install jumper T. This will cause the LPV11 interface to translate all lowercase letters to uppercase letters before transmission to the printer. This feature will allow printing files configured for 96-character printers on 64-character printers with minimum software overhead.

Do not configure the module with both jumpers W7 and T installed.

Parity
Jumpers W8 and P select the desired parity mode. The LPV11 is factory-configured with W8 installed and jumper P not installed, enabling parity bit 7 to be transmitted to the printer. Configure the parity option desired as follows.

Parity Option	Jumper W8	Jumper P
Normal parity bit	Installed	Removed
No parity, bit 7 low	Removed	Removed
No parity, bit 7 high	Removed	Installed

Do not configure the module with both jumpers W8 and P installed.

NOTE

If the LPV11 interface module is used with an LP05 printer equipped with the Direct Access Vertical Form Unit (DAVFU), it is recommended that the user remove jumper W8. The LPV11 interface module does not support the DAVFU function.

Error Filter

The LPV11 interface module contains an error filter (time delay) circuit that is automatically selected when the module is used with an LA180 DECprinter. Jumper F+ (W6) is factory-installed, selecting the error filter for use with LP05 printers; however, its use with the LP05 is optional. If desired, remove the error filter by removing jumper W6 and installing jumper F–. Do not configure the module with both F– and W6 installed.

LPV11 Device Registers

All programmed communication with the LPV11 option is via two device registers in the LPV11 interface module. These registers include the line printer control and status (LPCS) and line printer data buffer (LPDB). These registers are factory-configured with LSI-11 bus addresses 177514 and 177516, respectively, and are software-compatible with DIGITAL software. However, if additional LPV11 options are added to the system, or if the user requires addresses other than those factory-configured, it will be necessary to alter interface module jumpers and provide an LPV11 program using these special device addresses. Each register is described in Tables 4 and 5 and both are shown in Figure 4.

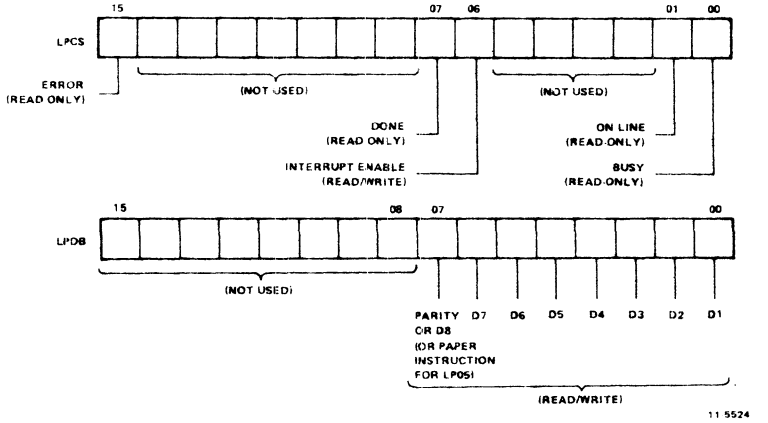


Figure 4 LPV11 Word Formats

Table 4 LPCS Register Bit Functions

Bit	Name	Description
15	Error	Asserted (1) whenever an error condition exists in the line printer. Error conditions include: LP05 Errors 1. Power off 2. No paper 3. Printer drum gate open 4. Over-temperature alarm 5. PRINT INHIBIT switch off 6. Printer off-line 7. Torn paper LA180 Errors 1. Fault (paper fault) 2. On-line switch (in OFF position) Reset by manual correction of error condition if LPCS bit 6 is not set. If bit 6 is set, bit 15 is reset by manual correction of the error and: (1) reading the interrupt vector if the interface is "ready," or (2) after reading the LPCS if the interface is "not ready." Read only.
14–8	Not used	Read as 0s.
7	Done	LP05 – Asserted (1) whenever printer is ready for next character to be loaded. Indicates that previous function is either complete or has been started and continued to a point where the printer can accept the next command. This bit is set by the processor asserting BINIT L; if bit 6 is also set, an interrupt sequence is initiated. Also set by the printer when on-line and ready to accept a character. Cleared by loading (writing into) the LPDB register. Inhibited when bit 15 is set. Read only.

Table 4 LPCS Register Bit Functions (Cont)

Bit	Name	Description
		LA180 – Asserted (1) when the printer is ready to accept another character. Done is set by the processor asserting BINIT L and is cleared by loading (output transfer to) the LPDB register. If the Interrupt Enable bit is set, setting Done will initiate an interrupt request.
6	Interrupt Enable	Set or cleared by the program. Also cleared by the processor asserting BINIT L. When set, an interrupt sequence is initiated if either the Error or Done bit is set.
5–2	Not used	Read as 0s.
1	On Line	Not supported and not required by DIGITAL software. The following information is provided for reference only. LA180 – Set when the LA180 is on-line. Read only. LP05 – Not used. Read as 0.
0	Busy	Not supported and not required by DIGITAL software. Information is provided below for reference only. LA180 – Set when the LA180 is printing a line or advancing paper. LP05 – Not used. Read as 0.

Table 5 LPDB Register Bit Functions

Bit	Name	Description
15–8	Not used	Read as 0s. Data written into these bits is lost.
7	Parity or D8	Optional use. Read as 0. LA180 – Optional parity bit LP05 – Optional paper instruction bit. Not supported by the LPV11. Read as 0.
6–0	Data	7-bit ASCII character register. Characters are sequentially output to the printer buffer via this register. Read as 0s.

Interrupts

Programs written for use with the LPV11 are generally composed of an interrupt-driven routine. When the LPCS register Interrupt Enable bit is set and either the Done or Error bit is set, an interrupt request is initiated. Entry to the LPV11 service routine is normally via the factory-configured vector addresses 200_8 (PC) and 202_8 (PS). When servicing an interrupt and a second interrupt occurs, the second (and subsequent) interrupt may not be recognized. This condition can be avoided by checking for both interrupt conditions (Done and Error) in the interrupt service routine.

FUNCTIONAL DESCRIPTION

General

The M8027 interface module can be divided into functional blocks as described in Figure 5. These functions control the flow of data between the LSI-11 bus and the line printer. The interface signals are different for the LP05 and the LA180 line printers, but the LPV11 detects a ground in the interface cable, and automatically configures itself for the proper printer. Each function of the interface is described in the following paragraph. The LA180 and LP05 strobe timing diagrams are shown in Figures 6 and 7.

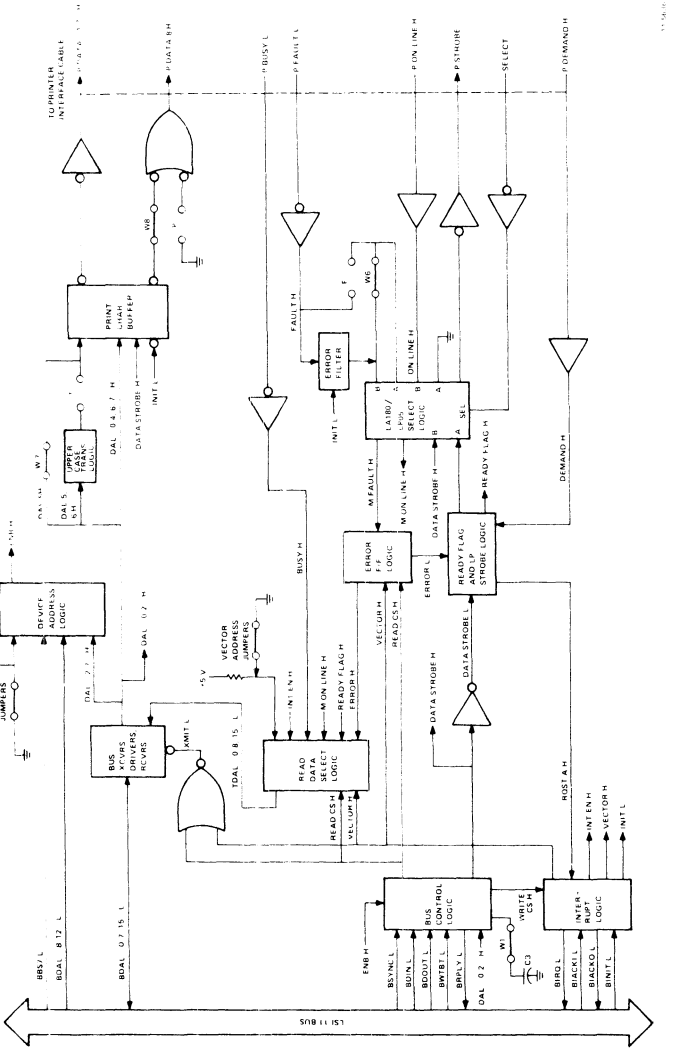
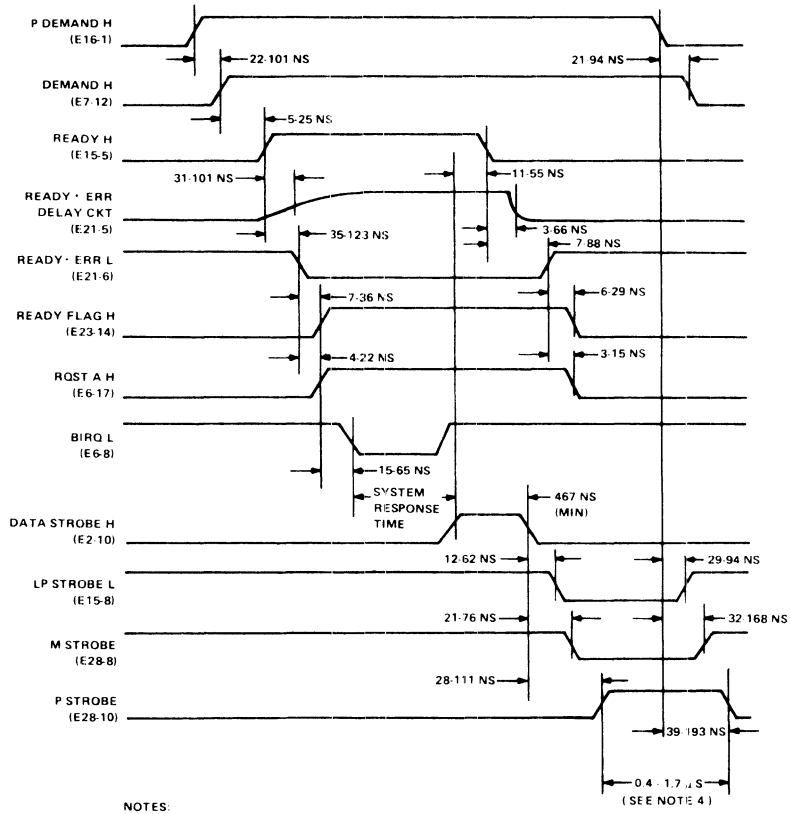


Figure 5 LPV11 Interface Logic Functions

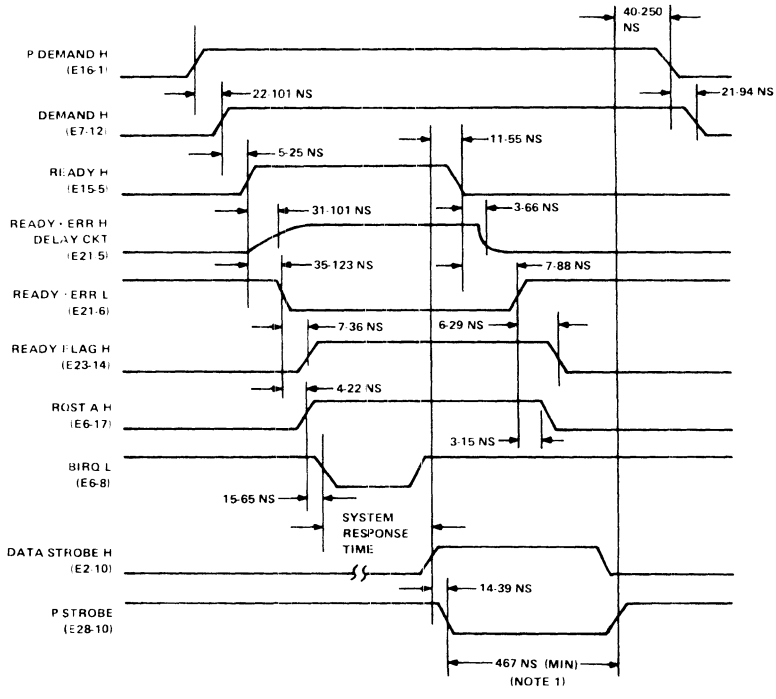


NOTES:

1. TIMING SHOWN IS TYPICAL, AND SHOWN FOR REFERENCE PURPOSES ONLY
2. TIMING SHOWN WITH JUMPER W1 INSTALLED
3. ( ) = INTEGRATED CIRCUIT PINS.
4. TIME IS DETERMINED BY LP05 PRINTER LOGIC.

11-5638

Figure 6 LP05 Internal Timing



NOTES
1. JUMPER W1 INSTALLED (REQUIRED) FOR TIMING SHOWN.
2. TIMING IS TYPICAL, AND SHOWN FOR REFERENCE PURPOSES ONLY.
3. ( ) = INTEGRATED CIRCUIT PINS.

11-5637

Figure 7 LA180 Internal Timing

Bus Transceivers and Drivers

Bus transceivers (DEC 8641) receive the LSI-11 bus BDAL (0:7) L signals and distribute the bits on DAL (0:7) H lines. In addition, they transmit LPCS bits or interrupt vector address bits during a DATI bus cycle or interrupt sequence. Bus drivers (DEC 8881) transmit LPCS bits 8 and 15 during a DATI bus cycle in which the LPCS is addressed.

Device Address Decoding
Device address decoding logic receives DAL (2:7) H, BDAL (8:12) L, and BBS7 signals and compares the address to the device address jumpers; when LSI-11 bus address bits 2 through 15 equal the jumper-configured address for the LPV11, ENB H goes active. Note that address bits 13, 14, and 15 are not decoded by the LPV11; the processor asserts BBS7 when these bits are all logical 1s, indicating an address is present in bank 7. In addition, address bits (0:2) are decoded for the device register (and byte) in the bus control logic. Bus control logic programmed transfer functions are enabled by the active ENB H signal.

Print Data Transmission
Print data is transmitted to the printer from the LSI-11 bus under program control. The print character buffer functions as the LPDB register. It is an 8-bit register, including the optional parity/D8 bit. The bus control logic produces WRITE DB H during a DATO or DATOB bus cycle in which the LPDB is addressed. Jumper W8 can be removed to disable program transfer of LPDB bit 7 to the printer. When W8 is removed, P DATA 8 is forced low; if desired, jumper P can be installed to force P DATA 8 high.

Uppercase translation logic gives the user the option to print upper/lowercase data files on an uppercase letters-only printer (LP05-VA, VB, VC, or VD). Software overhead is reduced by performing the lowercase to uppercase translation in hardware, rather than in software. Jumper W7 normally applies unmodified upper/lowercase ASCII characters to the print character buffer. When the lowercase to uppercase letters translation is desired, jumper W7 is removed and jumper T is installed. The result is that ASCII codes 140 through 177 are translated to 100 through 137 (bit 5 = 0), as shown in Table 6.

Read Data Select Logic
Read data select logic functions enable the processor to read the LPCS register under program control or the LPV11s interrupt vector during an interrupt transaction. Control signals READ CS H and VECTOR H select the bits. LPCS bits are produced by various LPV11 interface functions as shown in Figure 5.

Ready Flag and LP Strobe Logic
The ready flag (LPCS bit 7) and line printer (LP) strobe logic provide the proper control signal interface to the printer. The LP strobe function is used only for LP05 printers; the LA180 uses the DATA STROBE H signal generated by the bus control logic. Selection of the appropriate strobe source is automatically produced by the LA/LP select logic function. Connecting the proper interface cable for the LA180 grounds the SELECT line, causing the LA/LP select logic to select LA180 (data selector port B) functions. When the LP05 is used, the interface cable does

Table 6 Uppercase-Only Code Translation

ASCII Input		ASCII Output	
Code	**Character**	**Code**	**Character**
140	`	100	@
141	a	101	A
142	b	102	B
143	c	103	C
144	d	104	D
145	e	105	E
146	f	106	F
147	g	107	G
150	h	110	H
151	i	111	I
152	j	112	J
153	k	113	K
154	l	114	L
155	m	115	M
156	n	116	N
157	o	117	O
160	p	120	P
161	q	121	Q
162	r	122	R
163	s	123	S
164	t	124	T
165	u	125	U
166	v	126	V
167	w	127	W
170	x	130	X
171	y	131	Y
172	z	132	Z
173	{	133	[
174	¦	134	\
175	}	135	]
176	^	136	^
177	DEL	137	_

not ground the line and LP05 (data selector port A) functions are selected. The LA180 strobe is a negative-going pulse. The LP05 strobe is a positive-going pulse initiated by the leading edge of P DEMAND H and cleared by the trailing edge of P DEMAND H.

The ready flag is produced by the logic function when the printer is requesting a character (P DEMAND H goes active) and no error is present. In addition to setting the LPCS ready flag, the RQST A signal input to the interrupt logic goes active; if interrupts are enabled (LPCS bit 6 is set), an interrupt request is initiated (BIRQ L goes active). The ready flag is cleared by an active DATA STROBE L signal when writing a new character into the print character buffer.

When an error condition occurs in the printer, the printer asserts P FAULT L. The fault is applied to the error flip-flop logic (via the M FAULT H signal), producing an active ERROR L signal and an active ERROR H signal (LPCS bit 15). The ready flag logic function responds by not producing a ready flag, although P DEMAND H may be active, and by producing an active RQST A H signal. Thus, an error condition will initiate an interrupt request (if LPCS bit 6 is set) and set LPCS bit 15. The error flag is cleared by the processor reading the LPCS register if the ready flag is not set, or when the LPV11 interrupt vector is read.

Error Filter
The error filter is always used (automatically selected) with the LA180 printer and jumper-selected for optional use with the LP05 printer. This function is produced by a clock pulse generator/counter circuit that requires an active P FAULT L signal for 8 ms before the M FAULT H signal is produced. The minimum time requirement for the fault signal presence prevents false errors due to noise.

BRPLY Delay
Bus control logic generation of BRPLY L signals is delayed 400 ns (approximately) by factory-installed jumper W1. W1 connects C3 to the DC004 RxCx input pin, delaying the BRPLY L signal for proper operation with LA180 printers. When LP05 printers are used, the jumper may be either left installed or removed to reduce the BRPLY delay, as desired.

Initialization
The processor initializes devices on the LSI-11 bus by asserting BINIT L. BINIT L is received by the interrupt logic and distributed as the INIT L signal. INIT L clears the print character buffer, error flip-flop logic, and interrupt enable bit (LPCS bit 6), and sets the ready flag.

LP05 Line Printers
LP05 printers use a 132-column, 64- (LPV11-VA, -VB, -VC, -VD) or 96- (LPV11-WA, -WB, -WC, -WD) character rotating drum, and solenoid-driven hammers to print characters. Characters are transmitted to the LP05's print buffer under program control via the M8027 interface module. The LP05 print buffer stores up to a 132-character line. Each print cycle is initiated by a terminating character. Terminating characters include carriage return (CR), line feed (LF), and form feed (FF). Printing

requires two revolutions of the drum. Odd-numbered and even-numbered columns are printed during alternate revolutions of the drum. Cir cuits in the LP05 scan the print buffer characters stored for a line in synchronization with the rotating drum. Each character is printed, as appropriate, by driving the hammer for those odd- or even-numbered columns in which a particular character appears. An inked ribbon and paper pass between the drum and the hammers, and thus the characters are printed.

Note that LP05 printers are available with uppercase letters only (64-character set) or upper- and lowercase letters (96-character set), depending on model. All models are capable of printing numerals and punctuation marks.

LA180 DECprinter

The LA180 DECprinter included with LPV11-PA, -PB, -PC, and -PD models is a free-standing, pedestal-type impact printer that is capable of printing a maximum of 132 characters per line. To initiate a print cycle, a line terminator character (LF, FF, or CR) is required. The printer contains a 256 by 8 character buffer, which stores printable and non-printable characters. This buffer is loaded character-by-character via the LPV11 interface under program control. After each character is stored in the buffer, a read function is performed to determine if the character is a line terminator character. If it is, the characters stored in the buffer are printed; if it is not, the next characters are input until the complete line is stored, as indicated when the line terminator character is received and stored.

Each character is transferred to the printer as a parallel 7-bit ASCII plus optional parity code. The printer is a high-speed dot matrix printer that prints at speeds up to 180 characters per second. It produces a hard copy original plus up to five duplicate copies on tractor-driven continuous forms, varying in width from 10.2 cm (4 in) to 37.8 cm (14-7/8 in). The average printing speeds are 70 lines per minute on full lines, and 300 lines per minute on short lines. The printer responds only to codes representing the LA180 character set and six command characters. All other codes are ignored.

MMV11-A 4K BY 16-BIT CORE MEMORY

GENERAL

The MMV11-A 4K by 16-bit core memory option provides nonvolatile read/write storage of user programs and data. Memory 4K addressing is user-selected by switches contained on the option. The MMV11-A is LSI-11 bus-compatible but it is limited to backplanes that contain the LSI-11 bus in both A/B and C/D slots. The MMV11-A is capable of either programmed I/O data transfers with the processor or transfers with another LSI-11 DMA bus device.

FEATURES

- 4096 by 16-bit capacity
- Typical access time = 425 ns (475 ns maximum); full read/restore cycle time = 1.15 μs
- Nonvolatile read/write storage – stored data remains valid when power is removed
- User-selected bank address – three switches allow the user to select the bank address for the option
- +5 V and +12 V power – only the normal backplane power is required to power the option
- No adjustments, no periodic maintenance

SPECIFICATIONS

Identification	G653/H223
Size	Two quads
Power	
Standby	5.0 Vdc ± 5% at 3.0 A 12.0 Vdc ± 3% at 0.2 A
Operational	5.0 Vdc ± 5% at 7.0 A 12.0 Vdc ± 3% at 0.6
Bus Loads	
AC	1.9
DC	1.0

CONFIGURATION

General

The MMV11-A is contained on two modules which are mated to comprise a single assembly as shown in Figure 1. The modules include memory interface and timing board (module type G653) and core stack (module type H223). The G653 module includes handles and retractors on the top edge and fingers on the bottom edge which plug into the LSI-11 bus. Circuits contained on this module include interface, control and timing logic, bus receivers and drivers, the 16-bit data paths, sense amplifiers, and a +5 Vdc to −5 Vdc inverter. The H223 module is slightly smaller, includes no handles or bus fingers, and plugs onto the No. 2 (solder) side of the G653 module via special connector pins. Spacers are located between the modules to stiffen the assembly and to maintain the 2.3 cm (0.9 in) dimension. Circuits contained on the H223 module include the 4096 by 16 core stack, 12-bit address register, X and Y drives, stack charge, temperature compensation, and a series +11 V, V_{CC} switch which removes drive power when BDCOK H goes low (power fail) or BINIT L is asserted.

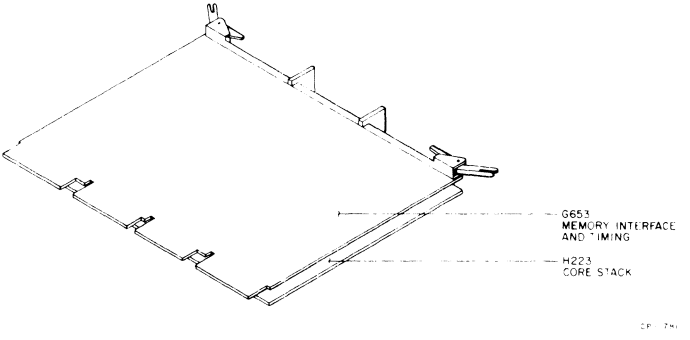


Figure 1 MMV11-A Core Memory Option

The MMV11-A core memory option comprises two modules (G653 and H223) that are mated by connector pins in a single assembly. It requires two device locations (electrical positions) on the backplane when installed in H9270 slots A4–D4; otherwise, because of its total thickness (2.3 cm, 0.9 in), the MMV11-A requires four physical device locations

when installed in any other backplane slot. Memory capacity is 4096 16-bit words. Switches select the 4K bank address to which the MMV11-A will respond.

NOTE

The MMV11-A can only be installed in backplanes that contain the LSI-11 bus in both A/B and C/D slots.

Switch-Selected Addressing

The only preparation required for the MMV11-A before it is installed in the backplane is to select its bank address. This is accomplished by opening or closing switches in appropriate address bit locations to produce the desired bank address decoding.

MMV11-A bank address switches are located on the G653 module (component side) as shown in Figure 2. Bank address switches are used as shown in Figure 3, which illustrates a 16-bit address and how switches are assigned to each address bit. Open or close switches to produce the desired bank address as shown in Figure 3.

Backplane Jumpers

The BDMGI L and BIAKI L bus lines must be jumpered to BDMGO L and BIAKO L lines, respectively, under the H223 module when installed between the processor and I/O device interface modules in order to maintain daisy-chain signal continuity.

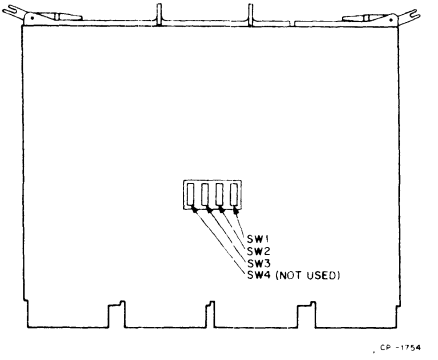
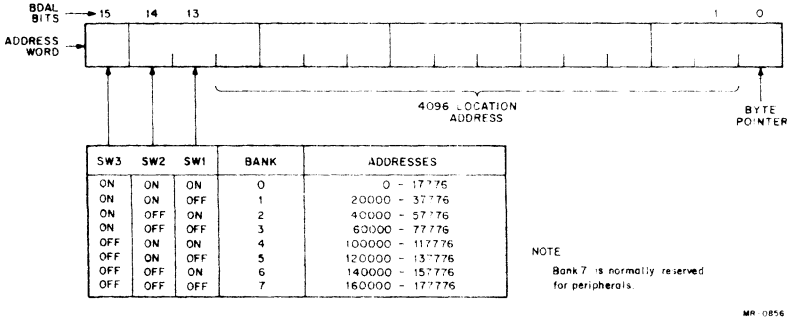


Figure 2 Bank Address Switch Locations



SW3	SW2	SW1	BANK	ADDRESSES
ON	ON	ON	0	0 - 17776
ON	ON	OFF	1	20000 - 37776
ON	OFF	ON	2	40000 - 57776
ON	OFF	OFF	3	60000 - 77776
OFF	ON	ON	4	100000 - 117776
OFF	ON	OFF	5	120000 - 137776
OFF	OFF	ON	6	140000 - 157776
OFF	OFF	OFF	7	160000 - 177776

Figure 3 MMV11-A Addressing

Pins which must be connected are:

From	To	Signal
C01N2	C04M2	BIAKI/OL
C01S2	C04R2	BDMGI/OL

PROGRAMMING

The program must terminate and issue a HALT instruction within 2 ms of the time that the BPOK signal indicates that a power failure trap occurred. Failure to do so could result in the loss of data in one or more memory locations.

FUNCTIONAL DESCRIPTION

General

The MMV11-A memory is a read/write, random access, coincident current magnetic core type with a cycle time of 1.15 μs and an access time of 425 ns. It is organized in a 3D, 3-wire planar configuration. Word length is 16 bits and the memory consists of 4096 (4K) words.

Major functions contained in the MMV11-A are shown in Figure 4. Memory data can be stored (written) or read by executing appropriate bus cycles: DATO (16-bit word) write; DATOB (8-bit byte) write; DATI (16-bit word) read; DATIO (16-bit word) read-modify-write; and DATIOB (16-bit word) read-modify-(8-bit byte) write.

Each of the functions shown in Figure 4 is briefly described below.

Bus Receivers and Drivers – These devices interface directly with the LSI-11 bus and the G653 logic circuits. BDAL bus drivers are gated on by DATA OUT L during a read operation [DATI or the input portion of a DATIOB(B) bus cycle].

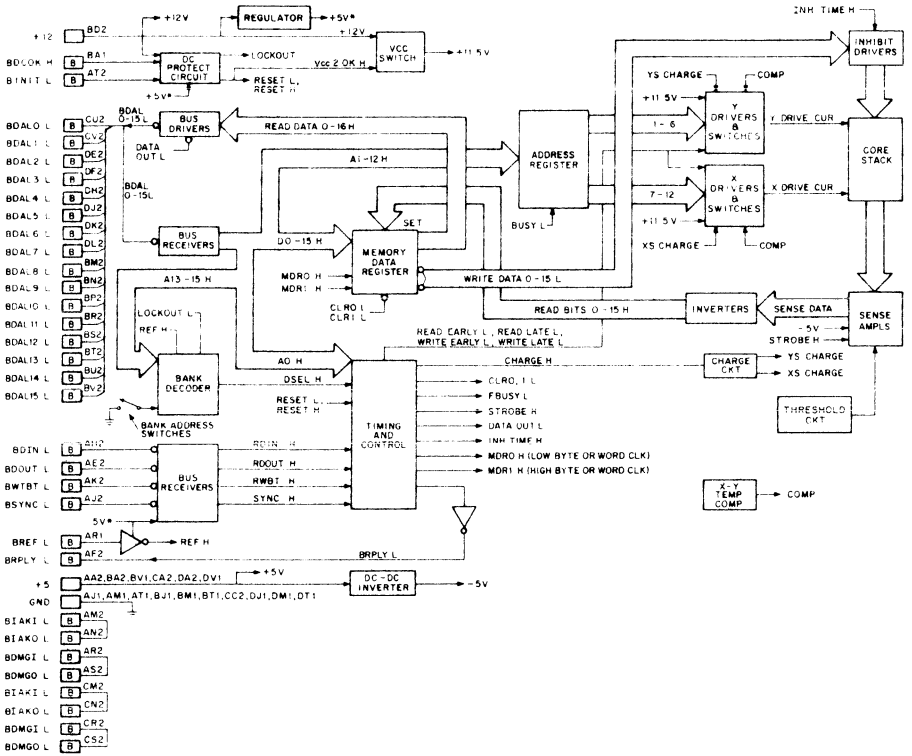


Figure 4 MMV11-A Logic Block Diagram

Bank Decoder – The bank decoder receives address bits A13–15 L and responds when the bank address is as user-selected on the three bank address switches on the G653 module. It responds by producing an acitve DSEL H signal which initiates memory cycle timing. This signal is enabled only when power is normal and bus initialize or referesh operations are not in progress.

Timing and Control – Timing and control circuits receive bus and internal control signals and generate appropriate read/write timing and control signals. It also generates the BRPLY L signal in response to BDIN L and BDOUT L.

Address Register – The address register stores the 12-bit word address within the 4K bank during the addressing portion of the bus cycle. Latched bits LA1–6H are applied to Y drive circuits and LA7–12H are applied to X drive circuits.

X and Y Drives – X and Y drive circuits control X and Y read/write currents through all core mats. Address decoding activates 1 out of 64 X wires and 1 out of 64 Y wires. Because the active X and Y wires each have one-half the current required for core saturation, only 1 core out of 4096 cores in each core mat is saturated. Direction of current is determined by a read or write operation.

Core Stack – The core stack comprises sixteen 4096-core mats. Each mat is associated with one memory bit position at all 4096 locations. Each core has three wires passing through it: one X, one Y, and one sense/inhibit wire. The sense/inhibit wire passes through all 4096 cores in one mat. Hence, the stack contains 16 sense/inhibit lines.

The sense/inhibit line ends terminate at sense amplifier inputs. During a write operation, an inhibit current, equal to saturation current, is applied to the center of the sense/inhibit line when a logical 0 is to be written in the addressed core. This current splits and one-half saturation current flows through all cores in the mat and into termination diodes at the sense amplifier inputs. The wire is threaded through the cores in a manner that causes the current to flow in a direction opposite to that of the Y write current; this prevents core saturation, which would write a logical 1 in the addressed core.

Sense Amplifiers – Sense amplifiers respond to induced voltage impulses during the read cycle. They are strobed during a critical time of the cycle, producing an active (high) output when a logical 1 is read, regardless of the induced polarity on the two ends of the sense/inhibit wires for each bit.

Inverters – The inverters receive sense amplifier outputs, invert them, and direct-set previously cleared memory data register bits when a logical 1 is sensed.

Memory Data Register – The 16-bit memory data register is cleared upon entry to a read cycle; sensed logical 1s set appropriate bits. During a restore cycle (DATI bus cycle) (no memory contents are to be modified), the same bits (low-active) are written into the same addressed location. During a write cycle [DATO, DATOB, or the write portion of a DATIO(B) bus cycle], bus data bits are clocked into the high and/or low byte(s), depending on the type of bus cycle (word or high byte or low byte).

Inhibit Drivers – Inhibit drivers, one for each bit position, produce an inhibit current during the write cycle at INH TIME H if a logical 0 is to be written. The current inhibits core saturation, which would produce a stored logical 1.

Charge Circuit – The charge circuit applies the correct operating voltage to X and Y drive circuits during the read and write memory cycles to prevent "sneak" currents through the unselected stack diodes.

X-Y Temperature Compensation – X-Y temperature compensation circuits alter drive currents over the required operating temperature range to provide reliable operation.

DC-DC Inverter – The dc-dc inverter circuit generates –5 V power for sense amplifiers from the +5 V power.

DC Protection – DC protection circuits respond to an active BINIT L or passive BDCOK H signal by producing active LOCKOUT L, RESET H, RESET L, and passive VCC2OK H signals. These signal conditions prevent memory circuit operation and the possible loss of stored data.

V_{CC} Switch – The V_{CC} switch applies +11.5 V to X and Y driver circuits when not in an initialize or power-fail condition.

Core Addressing

When a memory location is addressed, 1 core in each of the 16 mats is accessed for a read or write operation. Figure 5 illustrates a portion of the X-Y drive and associated circuits for one Y wire. Six address bits (A1–A6) select 1 of 64 Y wires. A similar circuit (not shown) involving the remaining six address bits (A7–A12) selects 1 of 64 X wires. Hence, by placing 64 cores (in each mat) on each Y wire and passing a different X wire through each core, 1 of 64 cores on the active Y wire will be selected. Since the remaining Y wires have a similar 64 cores each and

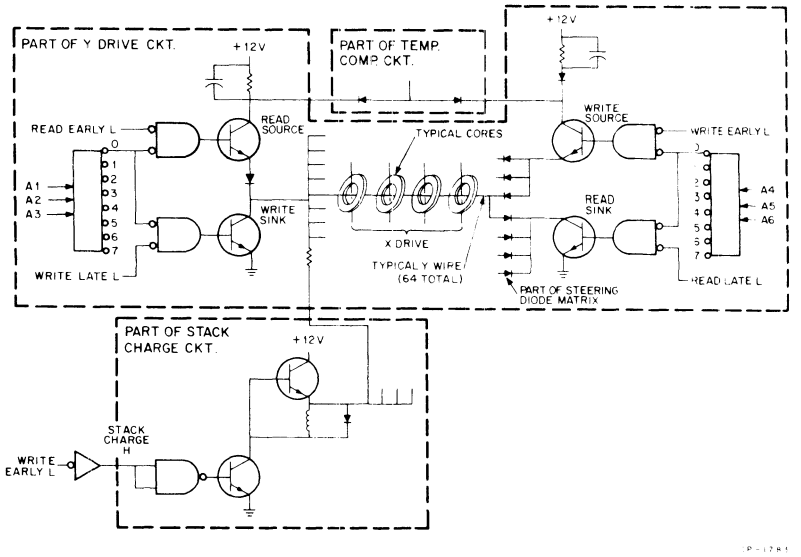


Figure 5 MMV11-A Core Addressing

receive the same X wires, 64 X 64, or 1 out of 4096 addressing is accomplished in each of the core mats. A single Y wire is driven as described below.

Two 1:8 (octal) decoders are used in Y wire selection, each receiving three address bits from the address register. Only one output from each decoder will be active during addressing. Assuming address XX00 (the zeros are the Y portion of the 12-bit address), the portion of the Y drive circuit shown will be enabled. During a read operation, READ EARLY L goes active and turns on one of the eight read current source transistors. A diode in its emitter circuit couples the drive to eight Y wires, each terminating at the diode steering matrix. The diodes provide a read current path to all eight read sink transistors. READ LATE L goes active 25 ns after the Y source is turned on, and turns on one of the eight read sink transistors, completing a read current path to ground. Hence, 1 of 64 Y wires is selected, producing a read half-current through 64 cores in all memory mats. Similar X drive circuits will produce an X read half-current in 64 cores in each mat in exactly the same manner. Only one core in each mat will receive an X and a Y read half-current, causing the core to saturate in the 0 state. If the core was previously in the 1 state, a voltage pulse will be induced in the sense/inhibit wire as it switches to the 0 state.

A write cycle is always preceded by a read cycle. The write operation is similar to the read operation, except write current flows through the addressed wire in a direction opposite to the read current direction. The core in each mat receiving X and Y write half-currents will respond by saturating in the 1 state. However, since a 0 may be desired, a third wire (sense/inhibit) will conduct a half-current which opposes the magnetizing effect of the Y write currents. Thus, core saturation is not attained and the cores where 0s are written remain saturated in the 0 state from the previous read cycle.

Temperature compensation is applied to driver circuits via a source current, which is inversely proportional to temperature; an increase in temperature decreases available drive current.

The stack charge circuit applies a +11 V (approximately) signal to the sink ends of all X (not shown) and Y wires during the write cycle. The level is applied during WRITE EARLY time. Since WRITE LATE L occurs 25 ns after WRITE EARLY L, the write sink transistor is cut off, and the full 11 V signal charges the stray capacitance of the X-Y lines, reducing the capacitive delay effect as the X and Y write source transistors turn on; the 11 V signal also reverse biases diodes not selected by addressing circuits, preventing sneak current. The addressed sink transistor, turned on by the active WRITE LATE L signal, provides the return path for the selected X and Y wires; only those two wires will go to approximately 0 V, causing one X and one Y diode to become forward biased, enabling the write half-currents to flow. Resistors coupling the charge voltage to write sink transistors limit the charge current through the addressed write sink transistors during the remainder of the write cycle. The circuit performs the same function for read cycles by grounding the buses and preventing sneak currents through unselected stack diodes.

Read/Write Data Path

The basic read/write data path is shown in Figure 6. Upon entering a read cycle, the memory data register is cleared by CLR0 and CLR1 L. X and Y read currents produce active sense amplifier outputs for those cores containing stored logical 1s as they are switched to the 0 states. These signals are inverted and applied to the direct-set inputs of the flip-flops comprising the memory data registers, setting the appropriate bits. During a write cycle, CLR0 L (DATOB low byte address), CLR1 L (DATOB high byte address), or both CLR0 and CLR1 L (DATO word address) clear the previously read data. The bus data is then received and clocked into the register flip-flops by CLK MDR0 H and/or CLK MDR1 H, as appropriate. Write data bits are then routed to inhibit drivers which inhibit writing 1s when write bits are 0s (high). Inhibit half-current through addressed cores prevents X-Y write half-currents from switching cores to the 1 state.

The sense/inhibit wire passes through all cores in a core mat, as shown in Figure 6. The circuit shown in the figure is repeated for each of the 16 core mats. During the read portion of a memory cycle, a logical 1 stored in the addressed core will cause an induced voltage to appear on the sense/inhibit wire as the core switches from the 1 saturation state to the 0 saturation state. If a 0 was previously written, no appreciable voltage

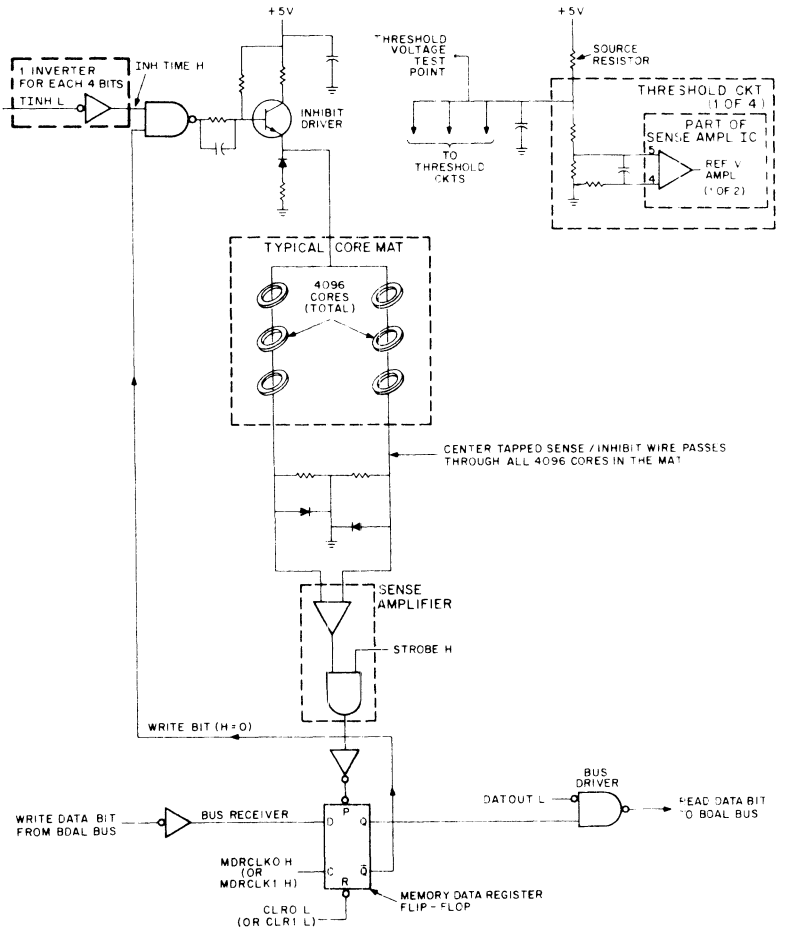


Figure 6 MMV11-A Read/Write Bit Data Path

is produced since the core is already saturated in the 0 state. During the read operation, the sense/inhibit wire functions as a loop whose ends terminate at the sense amplifier inputs. Any difference in potential (either polarity) will enable a sense amplifier output. STROBE H occurs during X and Y drive read currents at a critical time (the time of peak core switching output when 1s are read). Thus, only the correct voltage pulse produced when a core goes from the 1 state to the 0 state is gated into the memory data register flip-flop.

The threshold circuit establishes the signal voltage level at which a logical 1 is read during strobe time. A signal voltage magnitude greater than approximately 17 mV during strobe time results in a valid 1 level.

Signal levels less than the 17 mV threshold value are considered invalid and result in 0 levels being read. Four threshold circuits share a common source resistor. Each threshold circuit provides a reference amplifier input voltage to two sense amplifier ICs, each containing two sense amplifiers; hence, one threshold circuit provides a threshold voltage for four data bits.

When in the write portion of the memory cycle, the inhibit driver remains off if a 1 write data bit is stored in the memory data register flip-flop. However, if a 0 is to be written, the write bit is high, enabling a gate input for the inhibit driver. At INH TIME H during the write cycle, the inhibit driver produces an inhibit current equal to core saturation in a direction that would produce a logical 0. However, note that the inhibit current is applied to the center of the sense/inhibit wire. Thus, half-currents flow into each half of the sense/inhibit wire, preventing the addressed core from saturating in the 1 state. Diodes at the sense amplifier ends of the wire provide a ground return for the two inhibit half-currents. The two resistors terminate the ends of the wires. The inhibit driver transistor collector is clamped to ground through a diode and resistor to prevent breakdown during turnoff. The emitter resistor limits peak current.

Timing and Control

All memory bus cycles comprise a read and a write operation. During a DATI bus transaction, a memory read-restore cycle is executed. The data is first read and placed on the I/O bus. The same data is then written in the same addressed location. During a DATO bus transaction, a memory read-modify-write cycle is executed. After reading the contents of the addressed location, bus data is clocked into the memory data register. Previously read data is lost. The modified word is then written into the addressed location during the remainder of the cycle. If a DATOB bus transaction is being executed, only an 8-bit portion of the memory data register is modified, and one byte of the previously read word is retained

for the write operation. A DATIO bus transaction actually initiates two separate memory cycles. The first cycle (read-restore) is initiated by the master device by placing the memory address on BDAL0–15 L and asserting BSYNC L. After receiving and modifying the memory read data, the master device outputs the new data to the memory and asserts BDOUT L, which initiates the next memory cycle (read-modify-write). Timing and control logic functions generate all of the timing and control signals for the memory cycles described above. Logic operation for each type of bus transaction is described in detail in the following paragraphs.

A memory cycle is initiated when the correct bank address asserted by the bus master device is decoded on the leading edge of BSYNC L. DSEL H is the decoded bank address signal; note that it is inhibited during refresh bus cycles (when BREF L is asserted), or when an initialize or power-fail condition exists. The logical state of DSEL H is clocked into the busy flip-flop on the leading edge of SYNC H (Figure 7). When DSEL H is active (high), the busy flip-flop sets and FBUSY H and FBUSY L go to their true states. FBUSY L enables one input of the read initiate gate. The remaining gate input is enabled by the negative-going pulse produced by the RC circuit connected to FBUSY L. Thus, on the leading edge of FBUS L, the state of FBUSY H is clocked into the read flip-flop, causing it to go to the set state. This sequence is shown in Figures 8 and 9.

The read-restore (DN) cycle continues as shown in Figure 8. FREAD H activates the read time generator, producing time signals prefixed with "RT." Each signal is a 225 positive-going pulse whose leading edge is delayed with respect to FREAD H. Hence, the leading edge of RT225-H, shown in Figure 7, occurs 225 ns after the leading edge of FREAD H, and approximately 275 ns after BSYNC L is asserted. Note that RT225 H is inverted and applied to the clear input of the read flip-flop, establishing the 225 ns pulse width for RT pulses. RT225 H goes low 225 ns later. This time occurs 400 ns (total) after BSYNC L is asserted and it is referenced on Figure 7 as (T500L).

The pulse produced by the RC network on the leading edge of FBUSY L is inverted to produce the CLR0 L and CLR1 L signals, which clear the memory data register for the new read data. READ EARLY occurs on the leading edge of FREAD H and remains active for the duration of RT50 H, producing a 300 ns pulse. RT25 H goes high 25 ns later, producing the READ LATE L signal; this signal remains true for the duration of RT100, resulting in a 325 ns pulse. Read data is valid at the sense amplifier inputs from 200 to 275 ns after READ EARLY L goes active. RT175 H is gated with RT50 H to produce the sense amplifier strobes STROBE 0 and 1 H. The trailing edge of RT50 H occurs 100 ns after the leading edge of RT175 H, negating the strobes. During strobe time, the sense amplifier data bits set the appropriate flip-flops that comprise the memory data register, and store the memory read data.

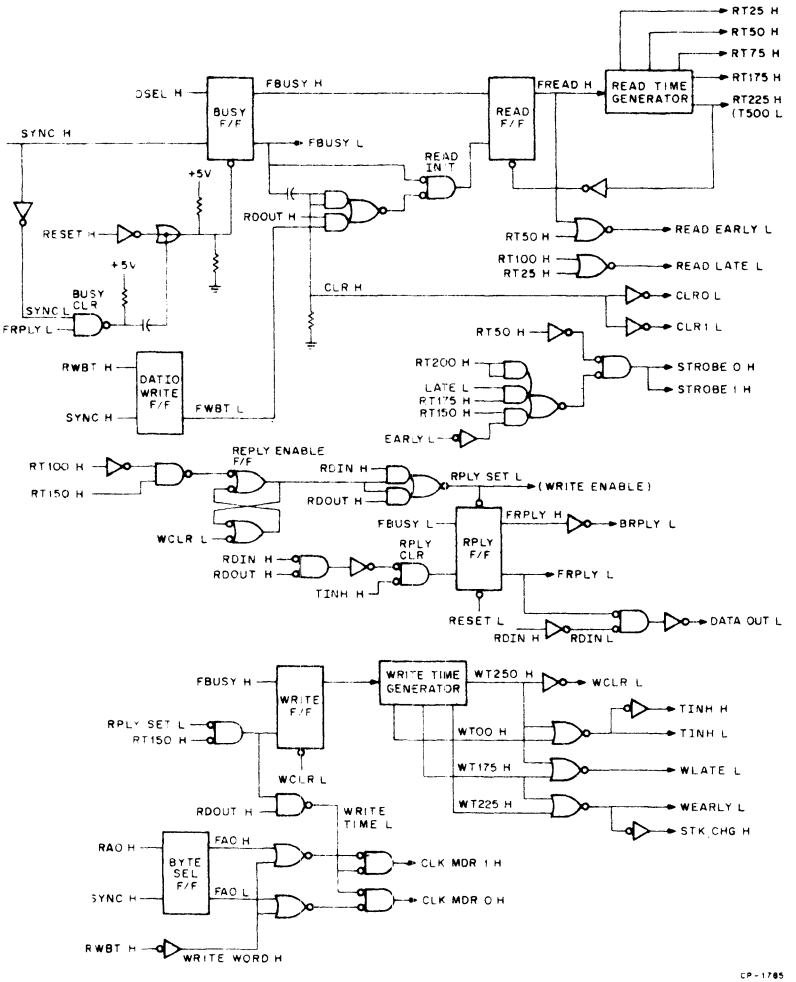


Figure 7 MMV11-A Timing and Control Circuits

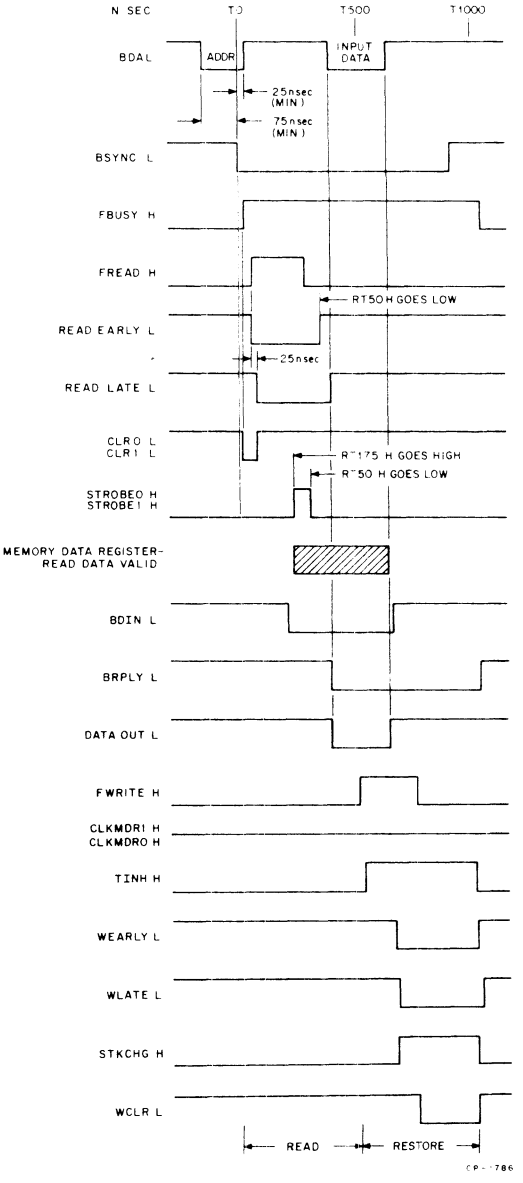


Figure 8 Read-Restore Memory Cycle Timing

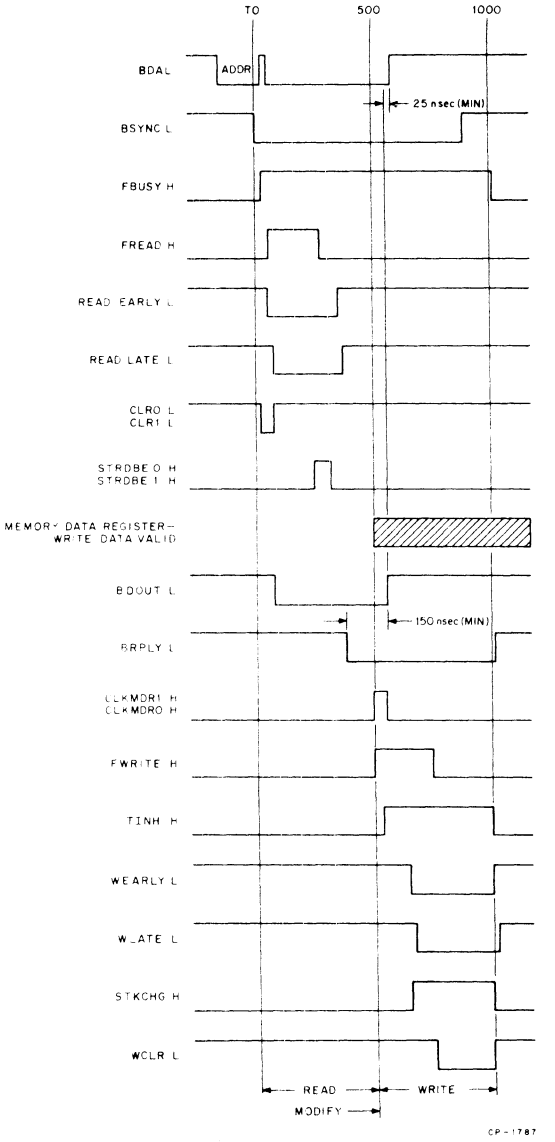


Figure 9 Read-Modify-Write Memory Cycle Timing

The bus master device initiates the data transfer portion of the DATI transaction by asserting BDIN L. The reply enable flip-flop is set on the trailing edge of RT100 H 375 ns after BSYNC L. If RDIN H (BDIN L inverted) is received earlier than 375 ns after BSYNC L, the reply flip-flop input gates wait 375 ns to produce an active RPLY SET L signal (Figure 8), which direct-sets the reply flip-flop and produces the active FRPLY H and BRPLY L signals. FRPLY L is gated with RDIN L and inverted, producing the DATA OUT L signal which gates memory data register bits onto the BDAL bus. If RDIN H is received later than 375 ns after BSYNC L, the reply flip-flop sets on the leading edge of RDIN H. The trailing edge of RT150 H (T425 L) is gated with RPLY SET L, producing a write initiate pulse which clocks the high FBUSY H signal into the write flip-flop, initiating the restore portion of the memory cycle.

Restore timing is produced by the write time generator in a manner similar to that described for read time generation. At W700 H time, TINH H and TINH L (475 ns pulses) are produced for the inhibit drivers. TINH H also inhibits the reply clear gate, and the reply flip-flop remains set for the remainder of the memory cycle. WEARLY L and STK CHG H go active on the leading edge of WT175 H and remain active for 350 ns. Similarly, WLATE L goes active on the leading edge of WT175 H and remains active for 325 ns. At WT250 H time, WCLR L is produced, clearing the reply enable and erite flip-flops; thus, write time generator outputs are 250 ns pulses. Memory data is restored (written) during the time that TINH H, WEARLY L, and WLATE L are active. The memory cycle terminates when both SYNC L and FRPLY L go to their passive states. The busy clear gate detects this condition, producing a low pulse which clears the busy flip-flop, and the memory cycle ends.

The DATO cycle is similar to the DATI cycle except that during the addressing portion of the bus cycle, the bus master device asserts BWTBT L. RWBT H goes high, and the leading edge of SYNC H clocks the byte flip-flop to the set state. The active FWBT L signal is only used when in the write portion of the DATIO cycle, as described later. However, during a DATO bus transaction, RDIN H is not received; instead, RDOUT H is received, enabling the REPLY SET L gates, as shown in Figure 9. RDOUT enables one input to the WRITE TIME L gate. At the same time that the write flip-flop clocks to the set state, WRITE TIME L goes low, enabling CLK MDR0 and 1 H gates. Since a DATO bus cycle is in progress, BWTBT L remains passive during the data transfer portion of the bus cycle. Hence, RWBT H is low, WRITE WORD H is high, and the two byte select OR gates apply low signals to the remaining CLK MDR gates. CLK MDR 0 and 1 H then clock the BDAL bus data into the memory data register; the previously read data is lost. The write portion of the cycle continues as described for the restore portion of the DATI operation.

When executing a DATOB bus transaction, BWTBT L and RWBT H remain active for the duration of the bus cycle. Hence, the WRITE WORD H signal remains passive. The byte select flip-flop that stores byte addressing bit RA0 H during addressing time enables generation of only one CLK MDR H signal. When RA0 H is low, FA0 L goes high and CLK MDR 0 H clocks low byte data bits from only BDAL0–7 L into the memory data register. Register bits 8–15 remain unchanged. Similarly, when RA0 H is high, FA0 H goes high and CLK MDR 1 H clocks high byte data bits from only BDAL8–15 L into the memory data register. Register data bits 0–7 remain unchanged. The write portion of the memory cycle then continues as previously described.

When executing a DATIO bus cycle, two complete memory cycles are executed. They include a DATI and a DATO or DATOB cycle as previously described. However, when executing a DATIO bus transaction, BSYNC L remains active for the duration of the transaction. Hence, SYNC H, which generates FBUSY L during the read-restore portion of the cycle, cannot initiate the second read-modify-write memory cycle. Instead, FWBT L, stored during the addressing portion of the cycle, enables a read initiate pulse on the leading edge of RDOUT H. The read flip-flop goes to the set state and operation continues as described for DATO or DATOB bus transactions.

DC Protection and V_{CC} Switch

DC protection and V_{CC} switch circuits are shown in Figure 10. The dc protection circuit is activated during power-fail or bus initialize conditions. BDCOK H and BINIT L are inverted and ORed to produce LOCKOUT L. Normally, this signal is passive (high), enabling bank addressing and resulting in an active DSEL H signal when the memory is addressed. However, if BDCOK H goes low (power-fail) or BINIT L is asserted low, LOCKOUT L immediately inhibits the bank addressing function.

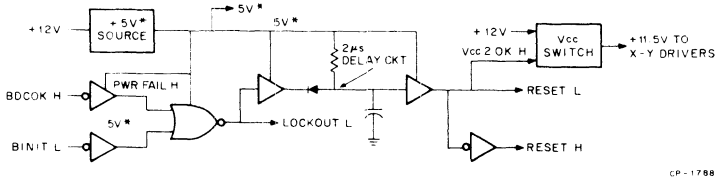


Figure 10 DC Protection and V_{CC} Switch Circuits

WARNING

The program must terminate and issue a HALT instruction within 2 ms of the time that the BPOK signal indicates that a power failure has occurred. Failure to do so could result in the loss of data in one or more memory locations.

The reset signals are also generated by this circuit. RESET L goes active (low) whenever LOCKOUT L is active. A 2 μs delay circuit enables the memory to complete its present cycle before RESET. RESET L is also inverted to produce RESET H; both signals are used to clear (initialize) memory timing control circuits.

To produce a 5 V* source for reset circuits and bus receivers BSYNC L, BDIN L, BDOUT L, BWTBT L, and BREF L, +12 V power is required. Thus, if +12 V is removed, all MMV11 memory operations are disabled. However, if +5 V is removed and the +12 V remains, the 5 V* allows memory protect logic to remain functional.

RESET L is also applied to the VCC20K H input to the V_{CC} switch circuit. This signal is high only when both +5 V and +12 V power sources are normal. The V_{CC} switch comprises a transistor (V_{CC} switch), which is turned on when power is normal to produce +11.5 V power for X-Y driver circuits.

DC-DC Inverter

The dc-dc inverter circuit is shown in Figure 11. It is comprised of an inverter oscillator using a saturable transformer, a negative rectifier, and a filter. A 3-terminal regulator chip produces the regulated -5 V for sense amplifier operation.

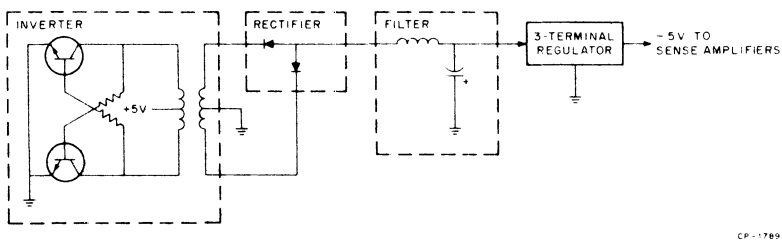


Figure 11 DC-DC Inverter Circuit

MRV11-AA 4K BY 16-BIT READ-ONLY MEMORY

GENERAL

The MRV11-AA is a basic read-only memory module on which the user can install programmable read-only memory (PROM) or masked read-only memory (ROM) chips.

FEATURES

- 4096 by 16-bit capacity using 512 by 4-bit chips, or 2048 by 16-bit capacity using 256 by 4-bit chips
- Compatibility with chips available from multiple sources
- Jumpers that allow the user to select the 4K memory address space to which the MRV11-AA will respond, chip type, and upper or lower 2K segment (when 256 by 4-bit chips are used)

SPECIFICATIONS

Identification	M7942
Size	Double
Power	
4K × 16 ROM less PROM integrated circuits	+5 V ± 5% at 0.4 A
Thirty-two 512 × 4 PROM integrated circuits	+5 V ± 5% at 2.8 A
Bus Loads	
AC	1.8
DC	1.0

CONFIGURATION

General

Depending on PROM type, the module's capacity is either 4096 16-bit words or 2048 16-bit words, using 512 by 4-bit or 256 by 4-bit PROMs, respectively. Full address decoding is provided on the module. The user can select the 4K address bank in which the module resides by installing (or removing) jumpers on the module. Similarly, when using 256 by 4-bit PROMs, the user can jumper-select the upper or lower 2K segment within the selected 4K address bank. Note that 512 by 4-bit and 256 by 4-bit PROMs cannot be mixed on a MRV11-AA module; the user configures jumpers on the module for the PROM type being used.

A partial listing of manufacturer's PROMs that will operate in the MRV11-AA is given in Table 1.

Table 1 MRV11-AA PROM Types

Manufacturer or Source	512 by 4-Bit PROMs	256 by 4-Bit PROMs
Digital Equipment Corp	MRV11-AC	–
Intersil	IM5624	IM5623
Signetics	82S131	82S129
MMI	6306	6301

PROMs used must be tri-state output devices that conform to the device pinning, data, and addressing described herein.

The user can install PROMs in increments of four each. When using 512 by 4-bit PROMs, memory expansion is in 512-word increments. When using 256 by 4-bit PROMs, memory expansion is in 256-word increments. Jumpers on the MRV11-AA can be cut by the user to prevent an incorrect BRPLY L signal from being generated when unpopulated locations are addressed on the module.

The following information will enable the user to prepare the MRV11-AA for use (jumper-selected addressing and PROM type selection) and includes information required for correct PROM and ROM programming.

PROM Type Jumpers

The module is supplied with jumpers W8, W9, and W10 installed for use with 512 by 4-bit PROMs. When using 256 by 4-bit PROMs, W8, W9, and W10 must be cut or removed and jumpers W11 and W12 installed; in addition, either W13 (lower 2K) or W14 (upper 2K) must be installed to properly address the lower 2K or upper 2K address segment within the 4K memory bank. Jumpers are located as shown in Figure 1.

Address and Reply Jumpers

The user must consider both 4-bank address selection and BRPLY L signal generation when configuring a module for use. PROMs are arranged in eight physical rows (CE0–CE7) of four each. Entire rows can be unpopulated, allowing those addressed locations to be used by read/write memory contained on another module. When this is done, the BRPLY L jumpers (W0–W7) associated with the unused rows should be cut or removed to prevent the MRV11-AA from returning a BRPLY L signal when those rows are addressed. A listing of octal addresses (within a 4K bank), physical rows, and BRPLY L jumpers is provided in Table 2; use data listed for the PROM type being used.

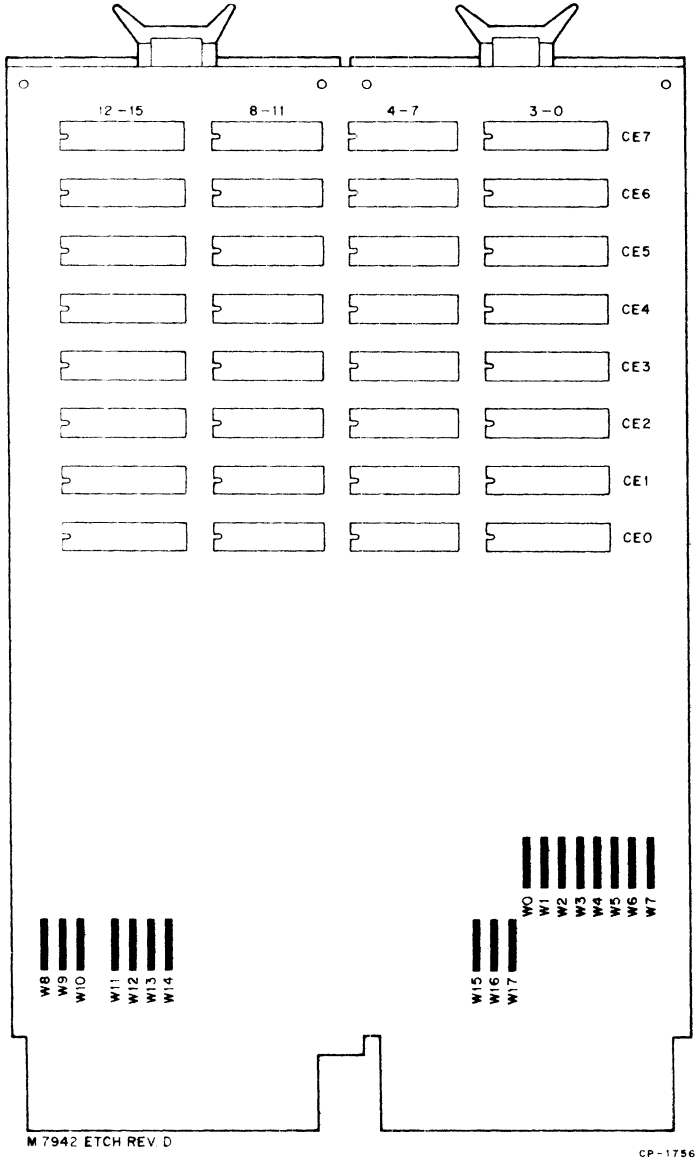


Figure 1 MRV11-AA Jumper Locations

Table 2 PROM/ROM Addressing Data

4K Bank Selection				
W15*	W16*	W17*	Bank	Word/Byte Address Range
I	I	I	0	0–17777
I	I	R	1	20000–37777
I	R	I	2	40000–57777
I	R	R	3	60000–77777
R	I	I	4	100000–117777
R	I	R	5	120000–137777
R	R	I	6	140000–157777
R	R	R	7	160000–177777

*R = jumper removed, I = jumper installed

512 by 4-Bit PROM Addressing Within a Bank

NOTE

Jumpers W8, W9, W10 are installed; W11, W12, W13, W14 are removed.

Reply Jumper*	Physical Row	Prom Octal Address Range
W0	CE0	0–1777
W1	CE1	2000–3777
W2	CE2	4000–5777
W3	CE3	6000–7777
W4	CE4	10000–11777
W5	CE5	12000–13777
W6	CE6	14000–15777
W7	CE7	16000–17777

*Jumper installed = BRPLY L enabled; jumper removed = BRPLY L not enabled.

Table 2 PROM/ROM Addressing Data (Cont)

256 by 4-Bit PROM Addressing Within Lower 2K Portion of Bank

NOTE

Jumpers W11, W12, W13 are installed; W8, W9, W10, W14 are removed.

Reply Jumper	Physical Row	PROM Octal Address Range
W0	CE0	0–777
W4	CE4	1000–1777
W1	CE1	2000–2777
W5	CE5	3000–3777
W2	CE2	4000–4777
W6	CE6	5000–5777
W3	CE3	6000–6777
W7	CE7	7000–7777

256 by 4-Bit PROM Addressing Within Upper 2K Portion of Bank

NOTE

Jumpers W11, W12, W14 are installed; W8, W9, W10, W13 are removed.

Reply Jumper	Physical Row	PROM Octal Address Range
W0	CE0	10000–10777
W4	CE4	11000–11777
W1	CE1	12000–12777
W5	CE5	13000–13777
W2	CE2	14000–14777
W6	CE6	15000–15777
W3	CE3	16000–16777
W7	CE7	17000–17777

The 4K bank in which the MRV11-AA resides is programmed by connecting bank address jumpers W15–W17, as appropriate. The module is supplied with all bank address jumpers installed (bank 0). Jumpers installed represent logical 0s; jumpers not installed represent logical 1s. Figure 2 illustrates addressing words used with the MRV11-AA. Refer to the addressing format for the type of PROMs or ROMs being used.

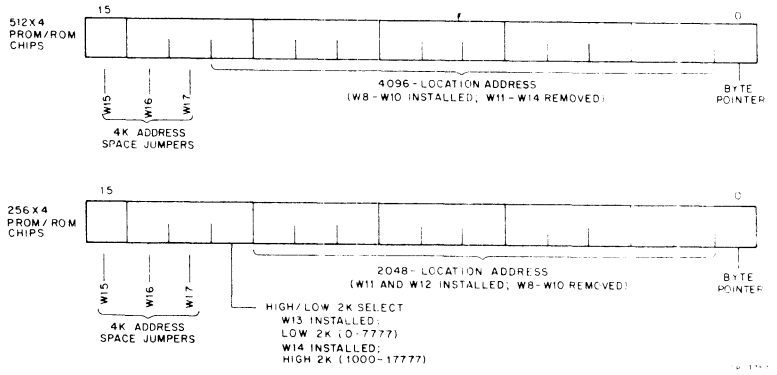


Figure 2 MRV11-AA Address Word Formats

PROM Integrated Circuits

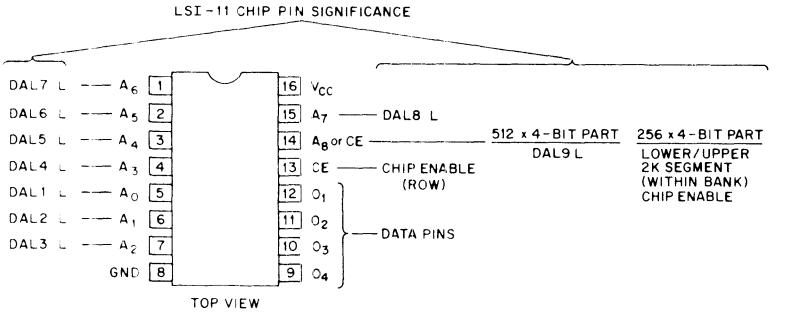
The actual procedure for loading data into PROMs (or writing specifications for masked ROMs) will vary, depending on the manufacturer. Those procedures are beyond the scope of this document. (See PROM/ROM manufacturer's data sheets.) However, the user must be aware of the PROM pins versus LSI-11 data bit relationship, and the pins versus memory address bits. Address and data pins are described below.

As previously discussed, PROMs are arranged in rows of four each. Each PROM contains locations of four bits. Hence, four PROMs are used to provide the 16-bit data word formats for each row. Rows are designated by their respective chip enable (CE0–CE7) signals. Depending on the PROM type used, a row of four PROMs contains 512 or 256 16-bit read-only memory locations. The actual PROM within a row is designated by one additional digit (0, 1, 2, or 3). Hence, the data pins are assigned to LSI-11 bus bits as listed in Table 3.

Table 3 Data Pin Assignments

PROM Pin	PROM 0	PROM 1	PROM 2	PROM 3
9	BDAL3	BDAL7	BDAL11	BDAL15
10	BDAL2	BDAL6	BDAL10	BDAL14
11	BDAL1	BDAL5	BDAL9	BDAL13
12	BDAL0	BDAL4	BDAL8	BDAL12

Addressing of PROMs is shown in Figure 3. All PROMs used on the MRV11-AA must conform to this information. Observe that the only difference between 512 by 4-bit and 256 by 4-bit PROM pins is pin 14. The 512 by 4-bit part uses this pin for address bit DAL9; the 256 by 4-bit part uses this pin for a chip enable when both bank address and 2K segment address are true. Also note that bus address bits do not follow in sequence with PROM manufacturer's address designations. The pinning arrangement shown allows for the use of commonly available PROMs and ROMs and optimum (compact) MRV11-AA module layout.



NOTE:
Designations immediately adjacent to pins are typical designations used by chip manufacturers — not LSI-11 designations. LSI-11 designations for correct addressing are located away from the chip. Observe that these signals are low — active, they are double-inverted bus signals (low = logical "1")

IC-0169

Figure 3 PROM/ROM Pin Addressing

Programming PROMs

Complete information for programming PROMs is contained in Chapter 3. Do not attempt to program PROMs until you are thoroughly familiar with the information contained in that chapter.

FUNCTIONAL DESCRIPTION

General

Major functions contained on the MRV11-AA module are shown in Figure 4. ROM data stored on the module can be addressed and read by the processor or other DMA devices by executing a DATI bus cycle. Data/address lines BDAL0–15 L and three bus interface control signals (BSYNC L, BDIN L, and BRPLY L) comprise all interface signals required for accessing the read-only memory. BREF L inhibits BRPLY L and BDAL bus drivers during memory refresh operations.

Addressing

A master device can address any 16-bit word in the 4K module by placing appropriate address bits on BDAL1–15 L during the addressing portion of the DATI cycle. BDAL0 is not used on the MRV11-AA since this address bit functions only as a byte pointer during DATOB and the write portion of DATIOB bus cycles. Bus receivers route DAL13–15 H to the bank select decoder and DAL1–12 H to the address storage latch. Bank selection occurs when the 4K address encoded on DAL13–15 H is equal to the user-configured value selected by jumpers W17–W15. The resulting bank select (BS H) and address bits DAL13–15 H are then stored in the address storage latch on the leading edge of BSYNC L. Stored address bits SA1–8 H are buffered to produce BA1–9 L, which are applied to all ROM/PROM chips on the module.

When 512 by 4-bit chips are used, SA9 H is routed via jumper W10 to a buffer, producing the inverted BA9 L address bit for all chips (pin 14). However, when 256 by 4-bit chips are used, W10 is removed and W12 is connected, forcing a low (chip enable) signal to be applied to all chips (pin 14); note that 256 by 4-bit chips do not receive address bit 9.

Memory chip sockets are arranged in eight physical rows of four sockets each. The memory is expanded by installing all four chips in each desired row. Four chips provide the full 16-bit word storage for LSI-11 instructions and data. Only one row is enabled by a chip enable (CE) signal, produced by chip row select logic and chip type jumpers.

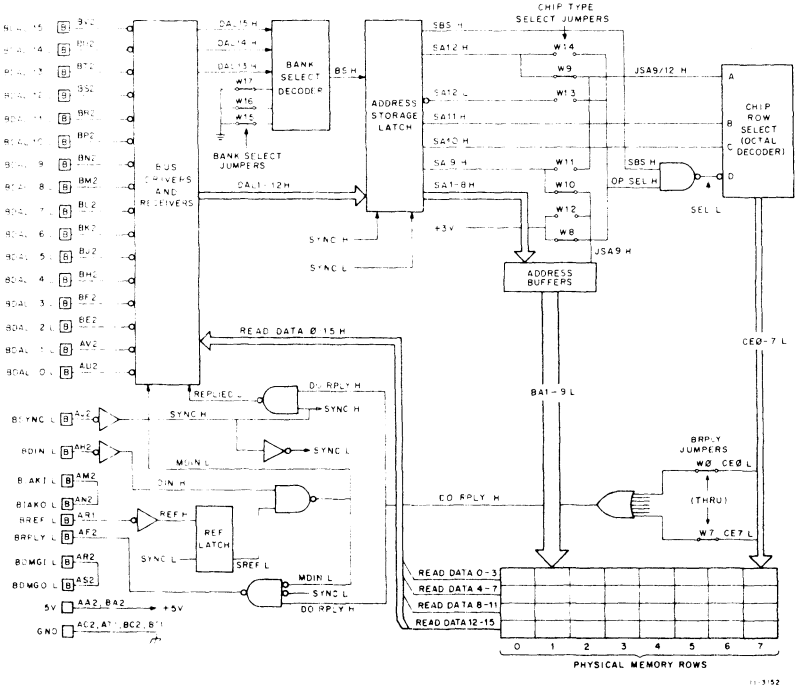


Figure 4 MRV11-AA Logic Block Diagram

When 512 by 4-bit chips are used, jumpers W8, W9, and W10 are installed. The chip row select octal decoder receives stored address bits SA10, SA11, and SA12 on its A, B, and C inputs, respectively, as shown in Figure 5. Bank select stored (SBS H) is gated to produce a low SEL L enable signal, which is applied to the D input of the decoder. (The decoder is actually a decimal decoder; whenever a high signal is applied to its D input, outputs 0–7 are inhibited.) One decoder output goes low, enabling the appropriate physical row addressed by bits SA10–12 L.

When 256 by 4-bit chips are used, jumpers W8, W9, and W10 are removed and jumpers W11, W12, and either W13 or W14 are installed, as shown in Figure 6. SA10 and SA11 are applied to octal decoder A and B inputs, respectively. Bit SA9, which is not used to directly address the 256 by 4-bit chips, is then applied to input C of the octal decoder.

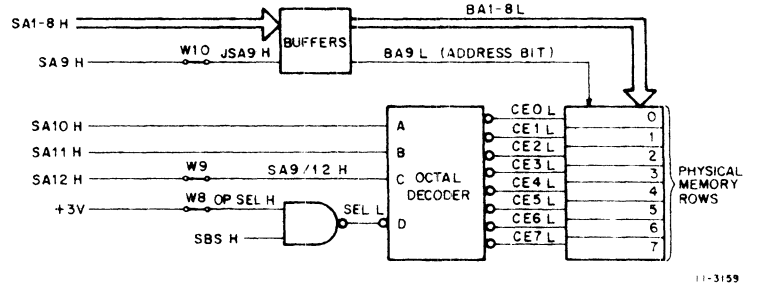


Figure 5 512 by 4-Bit Chip-Jumper Configuration

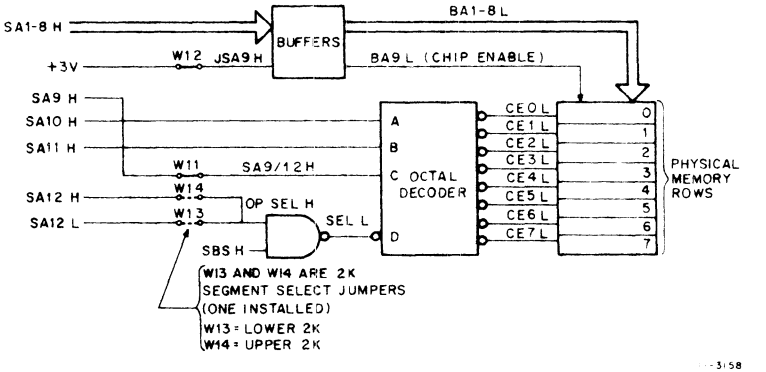


Figure 6 256 by 4-Bit Chip-Jumper Configuration

SA12 H and SA12 L are available for jumper selection of the desired 2K segment within the 4K bank. W13, when installed, selects the lower 2K; W14 selects the upper 2K. When the selected segment is addressed, OP SEL goes high. This signal is gated with SBS H to produce the low (active) octal decoder enable signal.

Caution must be used when assigning memory to bank 7 to avoid conflicts with preassigned device addresses. This 28–32K address space is normally used for peripheral device addresses. Certain DIGITAL-supplied

system programs and operating systems determine the presence or absence of some of these devices by accessing the assigned locations; if a response is obtained (i.e., no bus time-out occurs), the program assumes that the device is present. Thus, having a memory respond to any of these preassigned locations will give the erroneous indication that the corresponding device is installed in the system.

Data Read Operation

Once the ROM/PROM chip sockets are addressed, the data can be read by the bus master device. Data is available within 120 ns after BSYNC L is received. One active CE0–7 L signal produces the active DO RPLY H signal, which enables reply and DBAL bus driver gating. Active DO RPLY H and SYNC H signals are gated, producing the REPLIED L signal, which enables one of the two bus driver enable inputs. The remaining enable input is MDIN L. The bus master device asserts BDIN L to request the data. DIN H is ANDed with the passive (high) SREF L signal, producing MDIN L, and read data is enabled onto BDAL0–15 L. Active MDIN L, SYNC L, and DO RPLY H signals also enable the BRPLY L bus driver, producing the required response to BDIN L.

When the system is in a memory refresh operation, the MRV11-A must not respond to the BSYNC/BDIN refresh bus transactions. BREF L is asserted during the addressing portion of the bus cycle and the refresh latch stores REF H on the leading edge of SYNC L. SREF L goes low and inhibits the MDIN L signal. Hence, BDAL and BRPLY L bus drivers are not enabled.

I/O Timing and Bus Restrictions

Addressed memory read data is available within 120 ns after the BSYNC L signal is received by the MRV11-AA. Logic on the module responds to DATI bus cycles only. DATO or DATOB bus cycles will result in a bus time-out error. Logic functions on the module are not affected by the bus initialize (BINIT L) signal.

MRV11-BA LSI-11 UV PROM/RAM

GENERAL

The MRV11-BA is a memory option that contains eight sockets in which MRV11-BC ultraviolet (UV), erasable, programmable read-only memory (PROM) integrated circuits can be installed.

The MRV11-BA also contains 256 by 16-bit static random access memory (RAM) that can be used as a "scratchpad" and "stack" by system software. The RAM contents are volatile; that is, when operating power is removed, memory data is lost. PROM contents are not volatile; programs and data stored in PROMs are available when operating power is restored.

Each MRV11-BC PROM option includes one 1024 (1K) by 8-bit unprogrammed UV PROM integrated circuit (Intel 2708 PROM). UV PROMs can be erased by exposure to high-intensity ultraviolet light and then reprogrammed with new programs and data. A clear quartz window over the PROM chip allows the ultraviolet light to be directed onto the chip. Optional QJV11 ROM/PROM formatter software is available for conversion of absolute loader format programs into listings and paper tapes in PROM content format.

FEATURES

- On-board 256-word static RAM
- Sockets provided for installation of up to 4K words (8K bytes) of PROM in 1K increments
- PROM and RAM address space can be independently customer configured via jumpers.
- No special power is required. Only the normal +5 and +12 Vdc operating voltages present on the LSI-11 bus are required. An on-board "charge pump" circuit provides the necessary –5 V operating voltage to the PROM array.
- Completely compatible with LSI-11 bus protocol

MRV11-BA

SPECIFICATIONS

Identification	M8021
Size	Double
Power	
LSI-11 UV PROM less	+5 V ± 5% at 0.58 A
PROM integrated circuits	+12 V ± 3% at 0.34 A
With eight 1K × 8	+5 V ± 5% at 0.62 A
PROM integrated circuits	+12 V ± 3% at 0.5 A
Bus Loads	
AC	2.8
DC	1.0

CONFIGURATION

General

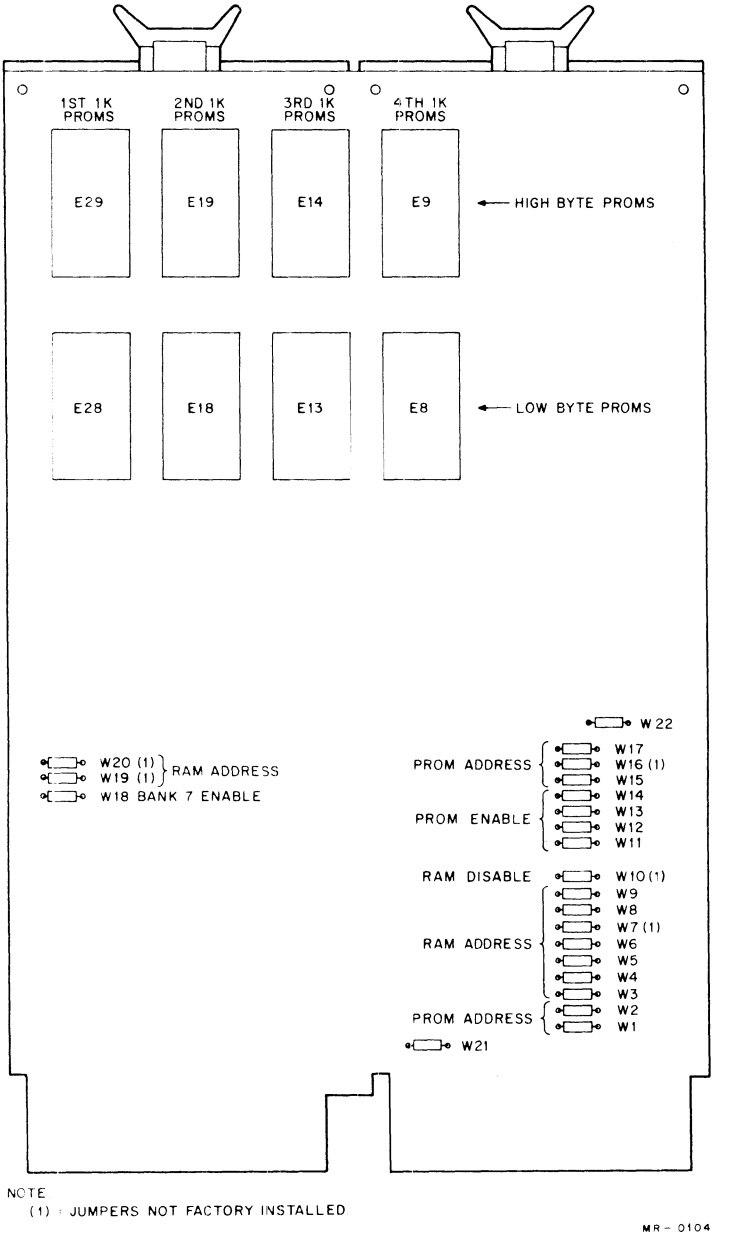
Jumper locations are included on the MRV11-BA module as shown in Figure 1. Jumpers allow independent selection of system memory starting addresses for the RAM and PROM memory functions. In addition, four special jumper locations (W10, W18, W21, and W22) are provided.

W10, when installed, disables the 256 RAM portion of the MRV11-BA when the RAM function is not desired. W18, when installed, enables PROM and/or RAM operation in bank 7 (the 4K memory addresses ranging from 160000 through 177777). Bank 7, by PDP-11 convention, is normally reserved for peripheral devices, and system memory would normally be configured for addresses ranging from 0 through 157777. The MRV11-BA is factory configured with W10 removed and W18 installed.

W21 and W22 control the MRV11-BA response to attempts to "write" in PROM locations. The module is factory-configured with W21 installed and W22 removed. When configured in this manner, any attempt to write in the PROM will result in a bus time-out error.

W21 can be removed and W22 can be installed to enable "pseudo-write" operations in PROM locations. Note that this jumper configuration only prevents bus time-out errors; it is not possible to actually write into (output data to) PROM locations. This jumper configuration is required to support the following instructions.

Mnemonic	Octal Code	Instruction
MTPS	1064SS	Move byte to PS
MUL	070RSS	Multiply
DIV	071RSS	Divide
ASH	072RSS	Shift arithmetically
ASHC	073RSS	Arithmetic shift combined



NOTE
(1) = JUMPERS NOT FACTORY INSTALLED

MR-0104

Figure 1 MRV11-BA Jumper and Socket Locations

All of the instructions listed require DATIO (read-modify-write) bus cycles. If the source operand (SS) refers to a PROM location, the MRV11-BA must be configured with W21 removed and W22 installed in order to avoid bus time-out errors. See Chapter 3 for additional details.

Address selection jumpers allow PROM and RAM addressing through a 128K address range. Bank 7 is the highest 4K portion of the address range. RAM addresses can reside within a populated PROM bank address. When this is done, RAM data will be properly accessed and PROM contents are not enabled. Detailed instructions for configuring address jumpers are provided below.

NOTE

System memory must include memory location 000004. This location may be either read-only or read-write memory. The processor executes a dummy read bus cycle during the power-up sequence using this address and requires a reply to complete the bus cycle. The actual memory contents read from the location are not used and can be any value.

RAM Address Jumpers

RAM addresses can be located in any 256-word portion of system memory, starting at 256-word-segment boundaries. The relationship between bus address bits and jumpers 19, 20, and 3 through 9 is shown in Figure 2. Configure the RAM starting address by removing and/or installing the appropriate jumpers.

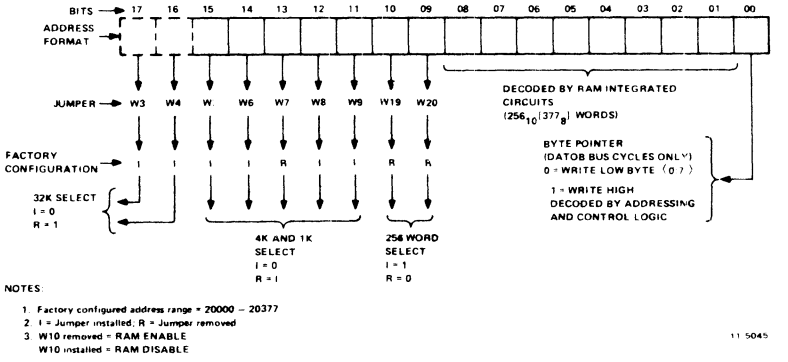
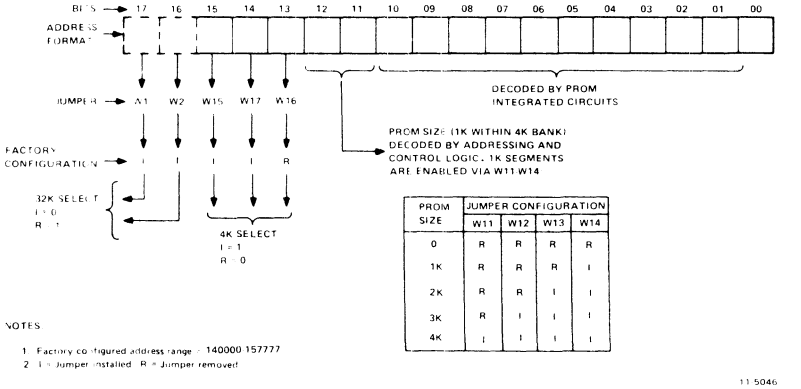


Figure 2 MRV11-BA RAM Addressing

PROM Address Jumpers

PROM addresses can be located in any 4K bank of system memory. The relationship between bus address bits, PROM size, and jumpers is shown in Figure 3. Configure the PROM starting address by removing and/or installing the appropriate jumpers. Remove or install PROM size jumpers W11 through W14 as shown in the figure; these jumpers must be removed to conform to PROM size (in increments of 1K) to prevent erroneous addressing of unpopulated sockets. The MRV11-BA is factory-configured with W11 through W14 installed.



PROM SIZE	JUMPER CONFIGURATION			
	W11	W12	W13	W14
0	R	R	R	R
1K	R	R	R	I
2K	R	R	I	I
3K	R	I	I	I
4K	I	I	I	I

Figure 3 MRV11-BA PROM Addressing

MRV11-BC Handling Precautions

MRV11-BC integrated circuit PROMs are metal oxide semiconductor (MOS) devices that can be damaged through improper handling. MOS devices can be easily damaged by static discharges due to their high input/output impedance. Safe installation requires that the conductive foam in which the chip is shipped be brought into physical and electrical contact with the MRV11-BA module or PROM programming equipment prior to removing the PROM from the foam. Unnecessary handling of PROMs should be avoided once removed from the foam. When programmed and installed in MRV11-BA sockets, there is no danger of static discharge damaging the PROMs.

Each MRV11-BC PROM is implemented in a 24-pin integrated circuit package. Mechanical damage to the PROMs can occur if they are carelessly handled. When installing PROMs, ensure that all pins are properly started into the socket before pressing the PROM pins all the way into the socket.

An instruction sheet illustrating proper handling procedures is included with each purchase of MRV11-BC PROMs. Refer to that sheet for PROM installation and removal instructions.

Installing the MRV11-BA Module

The MRV11-BA module can be installed in any LSI-11 bus. It only requires one option location and is not dependent on position (device priority) along the bus. Hence, the module can be installed in any option location in single and multiple backplane systems. The module requires no special power; all operating power (+5 V and +12 V) is supplied by the normal power present on the backplane. The MRV11-BA normally should not be configured for "pseudo-write" operation if it is being used in a DIGITAL operating system. The software may attempt to write in PROM locations resulting in bus time-out errors.

FUNCTIONAL DESCRIPTION

General

Four major functions comprise the MRV11-BA option: addressing and control logic, 4K × 16 PROM array, 256 × 16 RAM array, and charge pump circuit. These functions are shown in Figure 4. The PROM and RAM arrays comprise the actual memory portion of the module. The MRV11-BA option contains factory-installed RAM integrated circuits; PROM integrated circuits (MRV11-BC) are optional, and must be programmed prior to installation on the module. The charge pump circuit is a dc-dc voltage converter that produces −5 V operating power for the PROM array. Each function is described in the following paragraphs.

PROM Array

Optional PROMs comprise the PROM array shown in Figure 5. Each MRV11-BC PROM includes one 1K × 8 PROM integrated circuit. When two options are installed, they comprise a 1K × 16 read-only memory. The MRV11-BA option is expanded to 4K PROM by installing eight MRV11-BC options.

Four chip enable signals [CE (0:3) L] select the addressed pair of 1024-location by 8-bit (1K × 8) PROMs. Only one chip enable signal will go active when the PROM array is addressed, selecting a 1K portion of the 4K array. Addressing within the selected 1K portion is controlled by buffered address signals BA (1:10) H. Addressing and control logic functions control the chip enable and buffered address signals, and place the PROM output data DAL (0:15) on the LSI-11 bus where it can be read by the bus master. When not addressed by a chip enable signal, the PROM chip outputs go to a high-impedance state, effectively disconnecting the PROM array from the DAL signal lines.

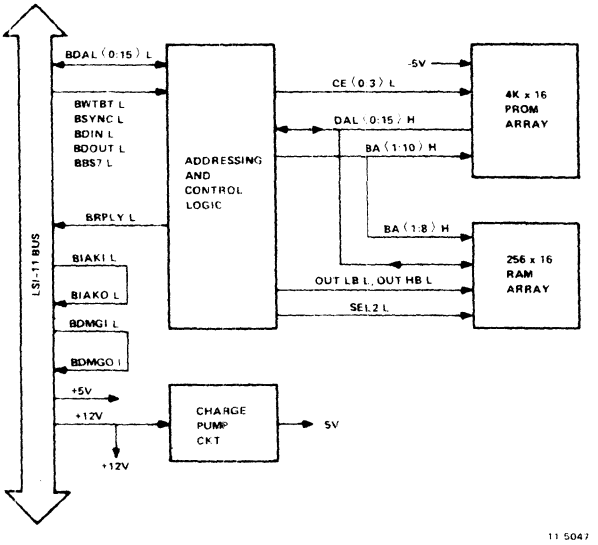


Figure 4 MRV11-BA Block Diagram

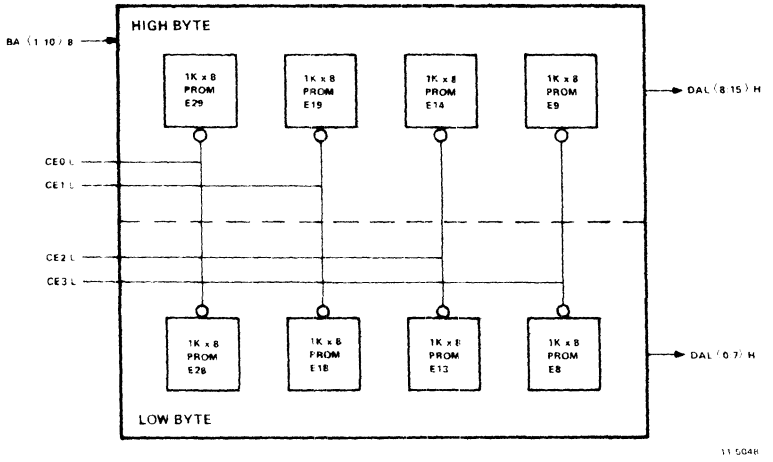


Figure 5 PROM Array

RAM Array

Four factory-installed 256-location by 4-bit (256 X 4) RAM integrated circuits comprise the RAM array, as shown in Figure 6. SEL2 L is asserted low by the addressing and control logic whenever the RAM array is addressed. When the RAM array is not addressed, SEL2 L goes high and the RAM input/output data pins [DAL (0:15) H] go to a high-impedance state, effectively disconnecting the array from the DAL lines.

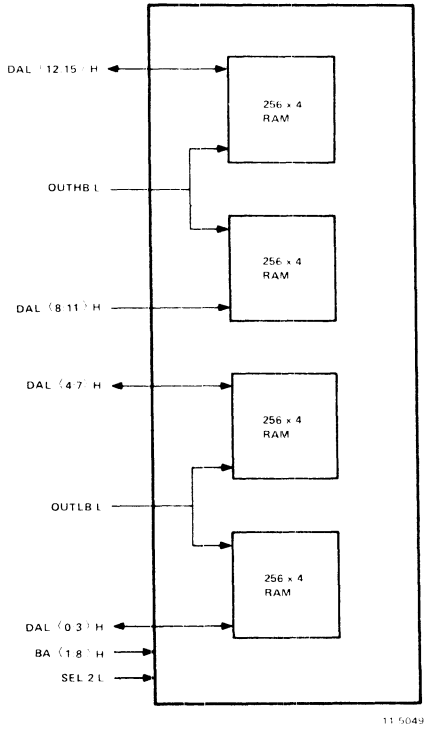


Figure 6 RAM Array

When addressed, OUT HB L and OUT LB L select a read or write operation. When a read operation (DATI) is in progress, both OUT signals are high (write inhibit). During a 16-bit (word) write (DATO) operation, both signals are low. During an 8-bit (byte) write (DATOB) operation, only one OUT signal will go low, selecting the addressed byte.

Addressing and Control Logic

Addressing and control logic functions are shown in Figure 7. Separate address decoding logic is included for PROM and RAM arrays. A common PROM/RAM address latch stores buffered address bits BA (1:12) H for both memory functions. Protocol logic contained in one integrated circuit (type DC004) controls the MRV11-BA interface according to a strict LSI-11 bus protocol.

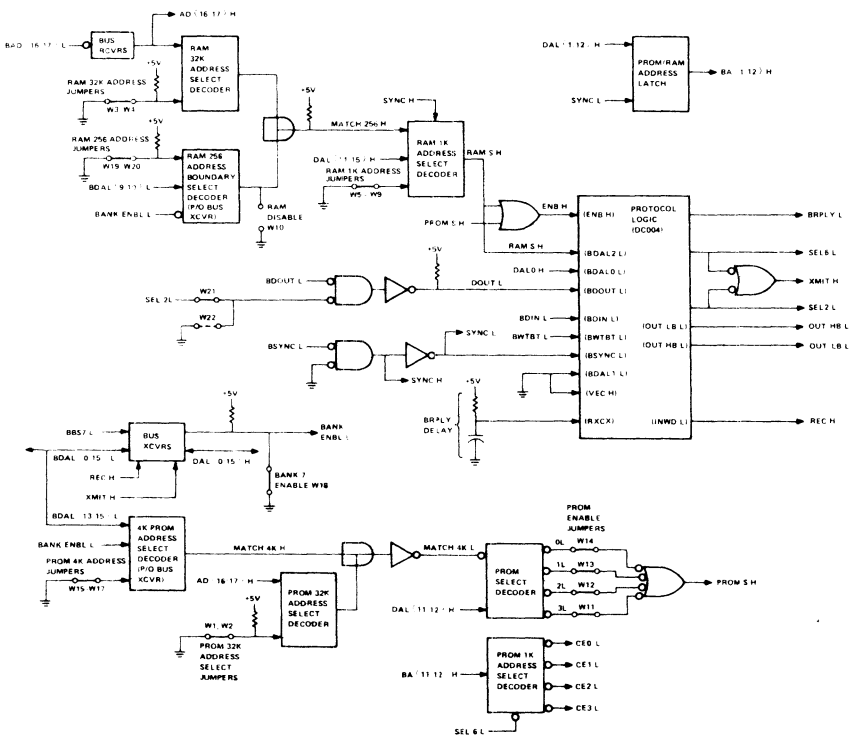


Figure 7 MRV11-BA Addressing and Control Logic

The addressing and control logic also includes bus transceivers that receive and transmit address and data bits to and from the LSI-11 bus.

REC H, when high, inverts and gates BDAL (0:15) L bits onto the DAL (0:15) H lines. These lines comprise an internal 16-bit bidirectional data/address bus for the MRV11-BA module. When XMIT H is high and REC H is low, inverted DA (0:15) H bits are placed on BDAL (0:15) L.

The PROM address can be configured via jumpers W15–W17 to reside in any 4K bank of system memory. PROM 32K address select decoder and jumpers W1 and W2 permit addressing in 128K memory systems (presently not implemented in LSI-11 systems).

When a bus master device places a PROM address on the LSI-11 bus, MATCH 4K H goes high; this signal is inverted and applied to the PROM select decoder, enabling further address selection. The state of DAL (11:12) H determine which PROM select decoder output will go active (low). Jumpers W11 through 14 apply the active signal to the PROM S H OR gate. Only one signal will go active during a PROM read sequence, indicating the addressed 1K segment within the 4K bank. The jumpers can be removed to disable PROM S H when PROM sockets do not contain PROMs. PROM S H is ORed with RAM S H, producing ENB H. When active, ENB H indicates a valid address is present, enabling protocol logic operation. During the addressing portion of the bus cycle, BSYNC L goes active, latching the buffered address bits BA (1:12) H. BA (11:12) H are applied to the PROM 1K address select decoder, producing one active chip enable signal (CE0 L through CE3 L) that enables the appropriate pair of 1K × 8 PROM integrated circuits for the duration of the PROM read sequence. BA (1:10) H select the addressed location within the selected pair of 1K PROMs.

RAM addressing is accomplished by first decoding the active 32K portion of memory configured via W3 and W4, and the 256-word portion within a 1K segment configured via W19 and W20. When a bus master places an address on the bus that is within the configured 32K and 256-word address space, MATCH 256 H goes active (high), enabling the RAM 1K address select decoder. On the leading edge of SYNC H, the RAM 1K address select decoder latches the "match" states of MATCH 256 H, the address space configured via jumpers W5–W9, and 1K address bits on DAL (11:15) H. If the address is within the configured range, RAM S H goes active (high), producing active ENB H and RAM S H (BDAL 2 L) input signals for protocol logic operations. Word addressing within the 256-word address space is controlled by buffered address bits BA (1:8) H. In addition, during a write byte operation (DATOB), the protocol logic produces one active (low) OUT HB L or OUT LB L signal that selects the appropriate RAM integrated circuit to write (store) data; during a word write operation (DATO), both signals go active, enabling both RAM integrated circuits to write data. If RAM operation is not desired, RAM disable jumper W10 can be installed. When installed, W10 prevents MATCH 256 H from going active and RAM addressing cannot occur.

Bank 7 addressing is normally reserved for devices other than system memory. By PDP-11 convention, the upper 4K address space contains peripheral device addresses that are compatible with system hardware and software options. W18 is factory-installed and BANK ENBL L remains active, enabling all bank addresses, including bank 7. With bank 7 enable jumper W18 removed, an active BBS7 L (bank 7) bus signal causes BANK ENBL L to go high; at all other times (bank addresses other than bank 7), this signal remains low, enabling RAM and PROM address decoders.

PROM Read Sequence – The PROM read sequence is initiated when the LSI-11 bus master device places a valid address on the BDAL (0:15) H lines (Figure 8). A bank address falling within the user-configured 4K address space enables an active (high) MATCH 4K H signal. Similarly, the PROM 32K address select decoder enables MATCH 4K H when the LSI-11 bus address is within the configured 32K space. When both conditions are true, MATCH 4K H goes high. This signal is inverted, producing MATCH 4K L, enabling the PROM select decoder. The decoder decodes DAL (11:12) H address bits and produces one active (low) output that represents a 1K segment of the addressed 4K bank. The active signal is routed via an appropriate jumper (W11 through W14) to the PROM S H OR gate. Thus, the resulting active PROM S H signal signifies that a populated portion of PROM is being addressed.

The active PROM S H is ORed with the passive RAM S H signal, producing an active ENB H signal input to the protocol logic. The leading edge of BSYNC L then stores buffered address bits BA (1:12) H and causes protocol logic generation of an active (low) SEL6 L signal. SEL6 L produces an active XMIT H signal that enables the bus drivers in the bus transceivers; however, data is not actually placed on the bus until REC H goes low. SEL6 L also enables the PROM 1K address select decoder. Only one decoder chip enable output (CE0 through CE3) goes low, enabling the addressed pair of 1K by 8 PROMs to place read data on DAL (0:15) H lines. The active chip enable signal and buffered address bits BA (1:10) H thus complete the addressing portion of the PROM read sequence.

The bus master then asserts BDIN L to initiate the data portion of the sequence. The protocol logic responds by negating REC H and PROM data is placed on BDAL (0:15) L where it can be read by the bus master device. After a 600 ns delay from the leading edge of BDIN L, the protocol logic produces an active BRPLY L signal, indicating that the MRV11-BA has placed valid data on the bus. The bus master then reads the data and negates BDIN L. The protocol logic responds by terminating BRPLY L. Finally, the bus master terminates the bus cycle by negating BSYNC L. The protocol logic responds by producing an active (high) REC H signal, inhibiting bus transmitter portions and enabling bus

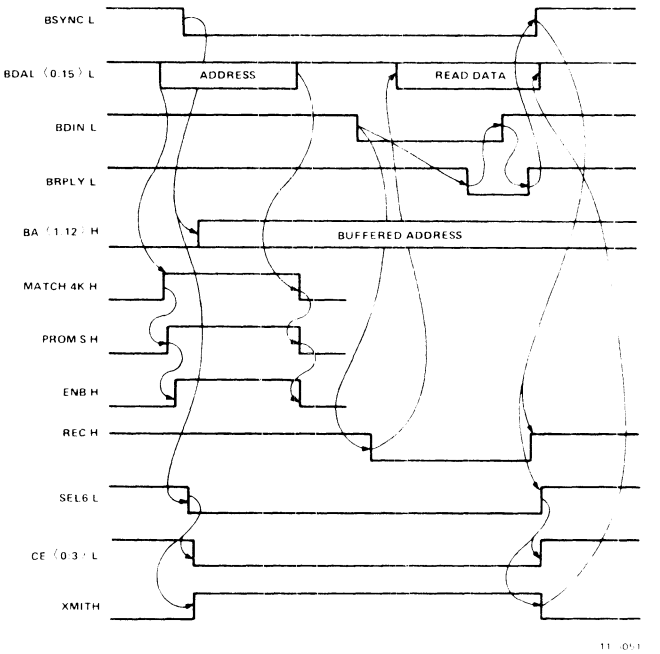


Figure 8 PROM Read Sequence (DATI)

receiver portions of the bus transceivers, and negating SEL6 L. The passive SEL6 L signal inhibits PROM chip enable signal decoding and produces a passive XMIT H signal, and the PROM read sequence is completed.

PROM Reply to DATIO(B) Bus Cycles – The MRV11-BA module is factory-configured to reply only to DATI (read) cycles when PROM is addressed. However, in certain applications the reply to the PROM pseudo-write sequence may be required to prevent bus time-out errors. The module is factory-configured with W21 installed and W22 removed. This enables the DOUT L signal input to the protocol logic (Figure 8) only when the 256 RAM is addressed (SEL2 L is asserted low). When PROM is addressed, SEL2 L goes high and inhibits DOUT. Thus, attempting to write in PROM will result in bus time-out since DOUT is not received by the protocol logic.

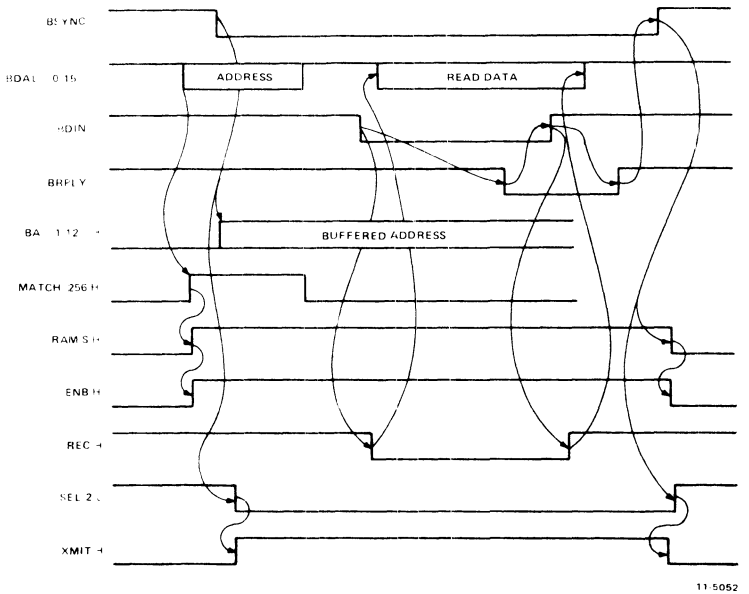


Figure 9 RAM Read Sequence (DATI)

When reply to DOUT is required, W21 is removed and W22 is installed. Thus, the protocol logic receives DOUT during PROM pseudo-write sequences. Note that no useful function is performed by the protocol logic other than asserting BRPLY L to complete the bus cycle; thus, bus time-out errors are prevented.

RAM Read Sequence – A RAM read sequence is initiated when a bus master device places an address on the LSI-11 bus (Figure 9). The RAM 32K and 256 (word) address select decoders produce a high (active) MATCH 256 H signal if the address is within the user-configured 32K and 256 address space. MATCH 256 H enables the RAM 1K address select decoder. If the bus address bits [BDAL (11:15) L] are equal to the user-configured 1K address segment, RAM S H goes high (active), producing an active ENB H signal that enables protocol logic operation. The bus master then asserts BSYNC L, latching the state of RAM S H and buffered address bits BA (1:12) H; the protocol logic responds to BSYNC L by producing an active SEL2 L signal, and the addressing portion of the sequence is completed.

The active SEL2 L signal is applied to RAM integrated circuit chip enable inputs, enabling data to be read. Buffered address bits BA (1:8) H select the addressed word within the 256-word memory array. SEL2 L also produces an active XMIT H signal, enabling the transmit function in the bus transceivers; however, data is not placed on the BDAL (0:15) L bus until REC H goes low.

The bus master enters the data portion of the bus cycle by asserting BDIN L. MRV11-BA protocol logic responds to BDIN L by negating REC H and asserting BRPLY L 600 ns after the leading edge of BDIN L, indicating the presence of valid RAM data. The bus master then reads the RAM data and negates BDIN L. MRV11-BA protocol logic then responds by producing an active REC H signal, removing data from the bus, and negating BRPLY L. The bus master then responds to the passive BRPLY L signal by negating BSYNC L, terminating the bus cycle. The MRV11-BA then responds to the passive BSYNC L signal by negating RAM S H and SEL2 L signals. The passive RAM S H signal inhibits ENB H. SEL2 L (high) produces a passive (low) XMIT H signal and the RAM read sequence is completed.

RAM Write Sequence – A RAM write sequence is initiated by the addressing portion of the bus cycle as described for the RAM read sequence. However, REC H remains high for the duration of the sequence (Figure 10), enabling the receiver portions of the bus transceivers. The data portion of the sequence is initiated when the bus master device places the write data word on BDAL (0:15) L for a DATO operation, or a data byte on BDAL (0:7) L (low byte) or BDAL (8:15) L (high byte). The bus master then asserts BDOUT L, indicating that valid write data is on the bus. The MRV11-BA protocol logic responds to BDOUT L by asserting both OUT HB L and OUT LB L if BWTBT L is presently not asserted (high) by the bus master (DATO bus cycle), or only one OUT HB/LB L signal if BWTBT L is asserted (low). The logical state of BDAL0 during the addressing portion of the sequence determines which OUT signal becomes active. In this manner, BDAL0 L serves as a byte pointer. If it was not asserted (high) during the addressing portion of the sequence, OUT LB L goes active (low), enabling writing into the low byte only of the addressed RAM location; similarly, if BDAL0 L was asserted (low), OUT HB L goes low, enabling writing into the high byte only of the addressed RAM location.

The protocol logic also responds to BDOUT L by asserting BRPLY L 600 ns after receiving BDOUT L, indicating that the write operation has been completed. The bus master responds to BRPLY L by negating BDOUT L. The protocol logic then responds to the high BDOUT L signal by negating the OUT HB L and/or OUT LB L signal(s) and terminating BRPLY L.

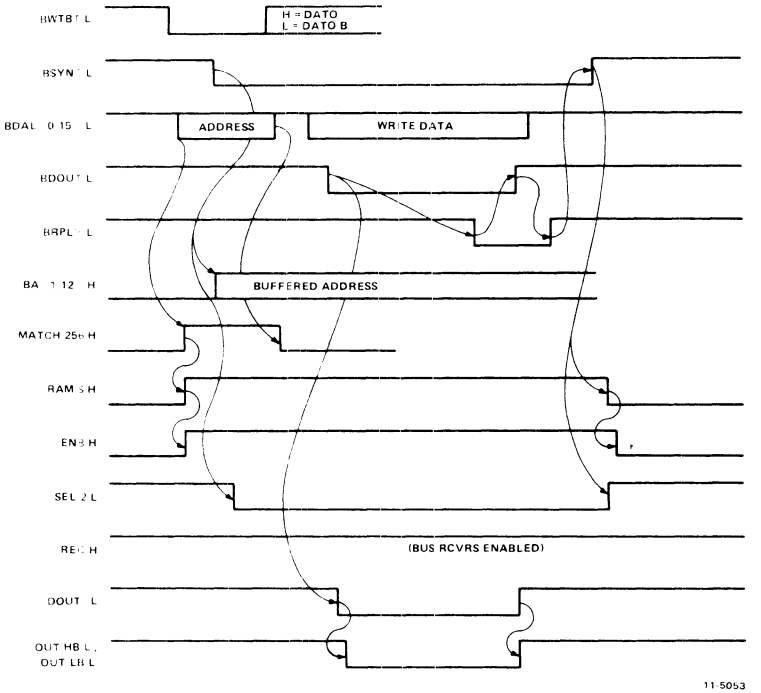


Figure 10 RAM Write Sequence (DATO or DATOB)

Finally, the bus master responds to the passive (high) BRPLY L signal by negating BSYNC L and terminating the bus cycle. The MRV11-BA then responds to the passive BSYNC L signal by terminating the RAM S H, ENB H, and SEL2 L signals and the RAM write sequence is completed.

Charge Pump Circuit

The charge pump circuit produces the −5 V operating power for the PROM array integrated circuits. The basic components comprising the charge pump circuit are shown in Figure 11. Input power is obtained from the +12 V present on the LSI-11 bus. Hence, the MRV11-BA module does not require external power other than the usual +5 V and +12 V present on the backplane.

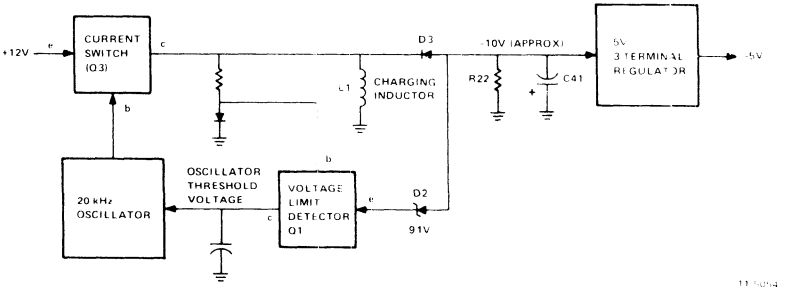


Figure 11 –5 V Charge Pump Circuit (Simplified)

The oscillator provides the basic rectangular pulse that drives current switch Q3. When the oscillator turns Q3 on, +12 V is applied to L1 for approximately 25 ms and an increasing current is produced. When the oscillator turns off, the energy stored in L1 produces a negative voltage (at the top of L1 as shown in the figure), charging C41 via diode D3. Thus, stored energy in L1 is transferred to C41 as a negative voltage. Successive oscillator pulses cause C41's voltage to build up to approximately 10 V. At this point, the zener voltage of D2 is exceeded and Q1 conducts. Q1 then produces a threshold control voltage that reduces the duty cycle of the oscillator drive voltage applied to Q3 ("on" time is decreased and "off" time is increased). The feedback circuit thus produced automatically adjusts the duty cycle of the 20 kHz oscillator to control the energy stored in L1 and maintain C41's voltage at –10 V under any normal load conditions.

The actual regulated –5 V output is produced by a 3-terminal, –5 V regulator. The regulator also contains overcurrent and thermal overload protection circuits.

MSV11-B 4K BY 16-BIT MOS READ/WRITE MEMORY

GENERAL

The MSV11-B is a 4K by 16-bit dynamic MOS read/write memory module which can be used for storage of user programs and data. The storage capacity is 4096 16-bit words. Memory address selection is user-configured by installing or removing jumpers contained on the module.

Memory refresh is directly controlled externally by LSI-11 bus signals. The MSV11-B is LSI-11 bus-compatible and capable of either programmed I/O data transfers with the processor or DMA transfers with other LSI-11 bus modules.

FEATURES

- 4096 by 16-bit word
- Fast access time – 550 ns maximum
- Lower power – 12.7 W for the module, maximum
- Dynamic MOS memory chips – Refresh is externally controlled
- User-configured 4K addresses – Three jumpers allow user address configuration.

SPECIFICATIONS

Identification	M7944
Size	Double
Power	+5 V ± 5% at 0.6 A +12 V ± 3% at 0.54 A
Bus Loads	
AC	1.9
DC	1.0

CONFIGURATION

General

The user can select the 4K address space (bank) in which the module is addressed by installing or removing jumpers. The MSV11-B module is factory-configured to respond to addresses in bank 0 (addresses 0–17776) and not reply to refresh.

Address Jumpers

MSV11-B address jumpers are located as shown in Figure 1. The module is supplied with all address jumpers installed. Figure 2 illustrates a 16-bit address and how jumpers are assigned for the MSV11-B module.

MSV11-B

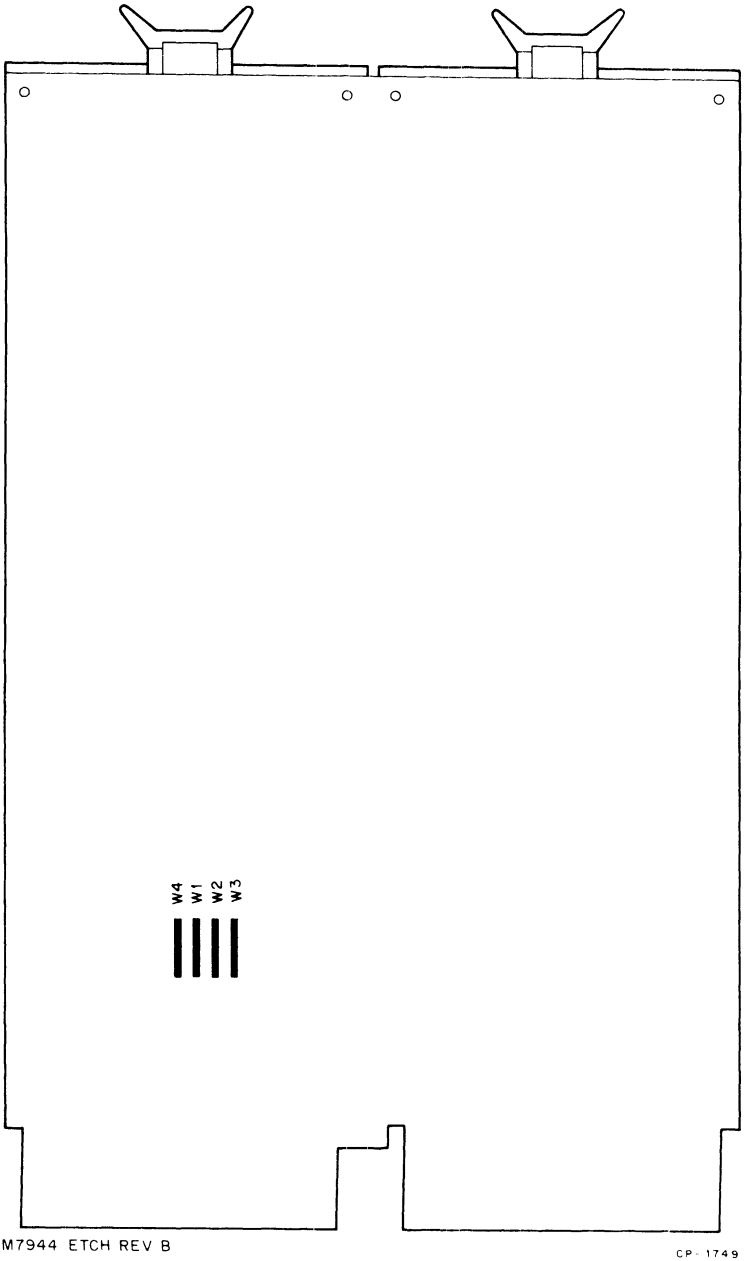
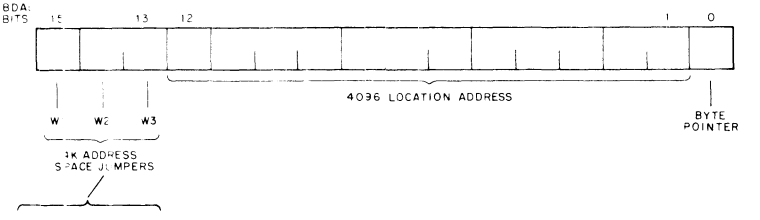


Figure 1 MSV11-B Jumper Locations



W1	W2	W3	Bank No.	Address Range	Octal Address Range
I	I	I	0	0-4K	000000-017776
I	I	R	1	4-8K	020000-037776
I	R	I	2	8-12K	040000-057776
I	R	R	3	12-16K	060000-077776
R	I	I	4	16-20K	100000-117776
R	I	R	5	20-24K	120000-137776
R	R	I	6	24-28K	140000-157776
R	R	R	7	28-32K	160000-177776

NOTE: I = Installed, R = Removed

CP-1883

Figure 2 MSV11-B Address Format/Jumpers

Reply to Refresh Jumpers

Only one dynamic memory module in a system is required to reply to the refresh bus transactions initiated by the refreshing device. The module selected to reply should be the module with the slowest access time or physically the farthest from the refreshing device. Jumper W4 enables or inhibits the MSV11-B reply as follows.

W4 installed: MSV11-B will not assert BRPLY in response to refresh bus signals.

W4 removed: MSV11-B will reply to refresh bus BSYNC/BDIN transactions by asserting BRPLY L.

Refresh Requirements

The MSV11-B module contains dynamic MOS integrated memory circuits which must be completely refreshed once every 2 ms or less. The refresh operation can be performed by the processor, by the REV11 series refresh/bootstrap module, or by special DMA logic provided by the user.

FUNCTIONAL DESCRIPTION

General

Major functions contained on the MSV11-B module are shown in Figure 3. Memory data can be stored (written) or read by the processor or other bus master devices operating in the DMA mode, with appropriate bus cycles: DATO (16-word write operation); DATOB (8-bit byte write operation); DATI (16-bit read operation); or DATIOB [16-bit read-modify-write (8- or 16-bit) operation].

Addressing is initiated by a master device (either the processor or a DMA device) by placing the 16-bit address on BDAL0–15 L and asserting BSYNC L, latching the address (and bank select information) in the address register. Address bits are routed from the BDAL bus receivers onto the module's DAL0–15 H bus to the 13-bit address and bank select register input. Address bits BDAL13–15 L are decoded by the bank address decoder. Decoded output signal BS H will go active (high) only when the jumper-selected bank address is decoded. The active BS H signal is stored along with the 13-bit memory address for the duration of the operation.

The memory array comprises sixteen 16-pin 4K by 1-bit memory chips which require the address multiplexer to address the array with two 16-bit bytes. Address multiplexer control logic responds to the active SYNC H and stored active bank select (LBS L) signal by immediately generating an active row address strobe (RAS). This signal remains active for the duration of the active SYNC H signal. Address multiplex control AMX L is initially passive (high), multiplexing the stored row address bits (LDAL7–12 H) through the 12:6-bit address multiplexer and into all memory chips. After approximately 150 ns, address multiplex control logic generates an active column address strobe (CAS) and an active AMX L signal. Multiplexer column address bits (LDAL1–6 H) are then strobed into all memory chips. This completes the chip addressing portion of the memory operation.

When in a memory read operation, the bus master device asserts BDIN L. The data from the accessed memory location is present on the D0–15 H bus and at bus driver inputs. Reply logic responds to BDIN L by generating an active DRIVE L signal which gates the memory read data onto BDAL0–15 L for input to the requesting device; reply logic also asserts BRPLY L to complete the data transfer portion of the cycle.

When in a memory write operation (or the write portion of a DATIOB cycle), the addressing portion of the operation is similar to the read cycle addressing. After the addressing portion of the cycle has been completed, the master device asserts BDOUT L, and BWTBT L either goes passive (high) if a DATO (word) write cycle is to be performed, or remains asserted if a DATOB (byte) write cycle is to be performed.

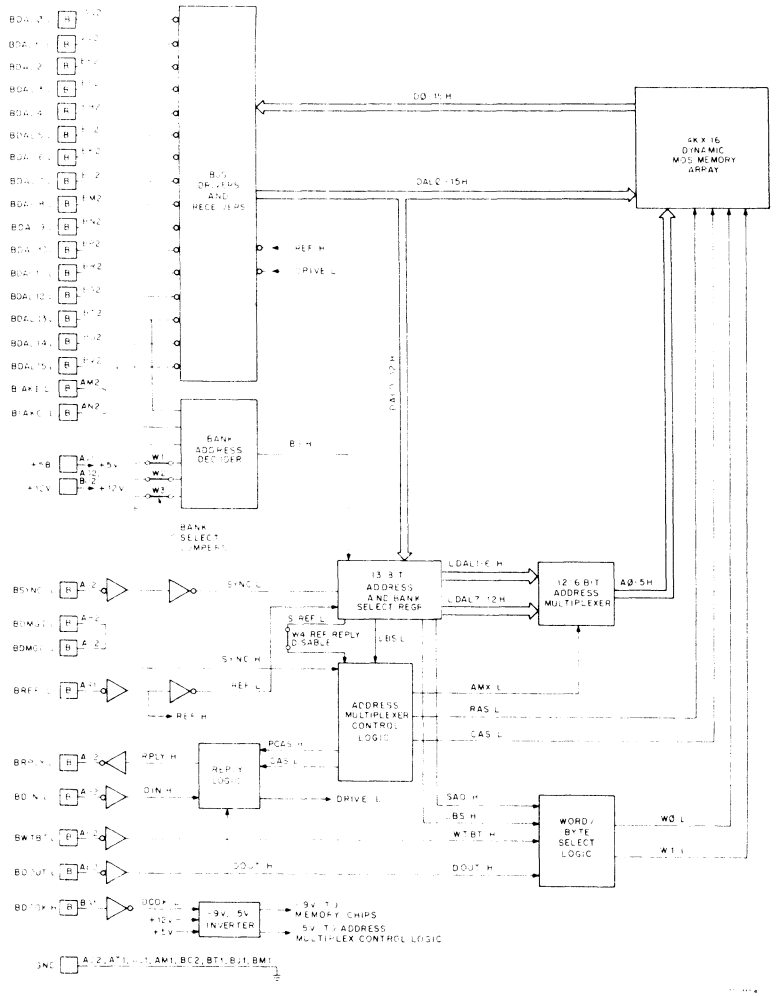


Figure 3 MSV11-B Logic Block Diagram

Word/byte select logic responds to the DATO cycle by asserting both WO L and W1 L for the duration of the cycle, enabling DALO–15 H bits to be written into the address location in all memory chips. However, in a DATOB cycle with AO H low (even byte), only WO L goes active, enabling the writing of DALO–7 H into the addressed location in the appropriate eight memory chips. Similarly, if AO H is high (odd byte), only W1 L goes active, enabling only DAL8–15 H bits to be written into the addressed location in the appropriate eight memory chips. The reply logic also responds to the active BDOUT L signal by asserting BRPLY L, indicating that the data has been written, completing the data transfer.

The memory chips in the MSV11-B require a refresh operation once every 1.6 ms. This operation is entirely under the control of either processor microcode or a DMA device, as selected by the user. The address multiplex control logic responds to BREF L, generated by the refresh-controlling device, by simulating a "bank selected" operation. (All system memory banks are simultaneously selected during refresh.) Refresh is then accomplished by a device by executing 64 successive BSYNC L/BDIN L operations while incrementing BDAL1–6 by one on each bus transaction. Refresh is simply a series of forced memory read operations where only the row addresses are significant. Each of the 64 rows in all dynamic MOS memory chips in an LSI-11 system are simultaneously refreshed in this manner. The REF H signal inhibits all BDAL bus drivers for the duration of the refresh operation.

A dc-to-dc inverter circuit is included on the module for negative voltage generation. Output voltages include –9 V for the MOS memory chips and –5 V for linear devices in the address multiplex control logic. Hence, only +12 V and +5 V power inputs are required for module operation. The BDCOK H signal starts dc-to-dc inverter oscillation when bus power is applied.

MSV11-CD 16K BY 16-BIT MOS READ-WRITE MEMORY

GENERAL

The MSV11-CD is a 16K dynamic MOS read/write memory option that can be installed in any LSI-11 bus. Memory contents are volatile; that is, when operating power is removed, memory data is lost.

FEATURES

- On-board refresh circuit that eliminates need for refresh signals on the LSI-11 bus.
- The system memory address space to which the option will respond is user-configured via switches contained on the module. An address can start at any 4K bank boundary.
- It will perform DATI, DATO, DATOB, DATIO, and DATIOB bus cycles according to LSI-11 bus protocol.
- Jumpers allow the module to be configured for using external bus refresh signals and disabling the internal refresh function.
- No special power is required. Only the normal +5 and +12 Vdc voltages are necessary. An on-board charge pump circuit provides the necessary −5 V operating voltage to the memory circuits.
- Jumpers allow the user to implement battery backup power.

SPECIFICATIONS

Identification	M7955-YD
Size	Quad

Power

System Power	**Operating**	**Standby**
+5 V ± 5%	1.1 A	1.1 A
+12 V ± 3%	0.54 A	0.16 A
Power	12 W	7.7 W

Battery Backup Power

+5 V ± 5%	0.8 A
+12 V ± 3%	0.16 A

Bus Loads

AC	2.3
DC	1

Operational
Operating Speed – The operating speeds stated below are based on the bus not attempting a memory cycle during a refresh operation and that an arbitration was not necessary.

Access Time

Bus Cycle Type	Access Time
DATI, DATIO	300 ns typ. (350 ns max. from RSYNC H)
DATO(B)	300 ns typ. (350 ns max. from RDOUT H).

Cycle Time

Bus Cycle Type	Cycle Time
DATI	650 ns typ. (750 ns max. from RSYNC H)
DATO(B)	650 ns typ. (750 ns max. from RDOUT H)

NOTE
If a bus cycle is being done as a result of winning the synchronization arbitration, the bus cycle will be delayed or increased from 0 to 80 ns. If a refresh operation is in progress when a cycle is requested, a delay from 0 to 750 ns will occur before the bus cycle starts.

CONFIGURATION

General
Configuring the MSV11-CD will alter its operation for a specific system application. The following items can be configured:

1. Select the starting address for the contiguous memory contained on the module
2. Select the number of banks required on the memory
3. Refresh mode: on-board or external refresh, and reply to external refresh signals
4. Battery backup power
5. Bus grant (BIAK L and BDMG L) signals.

In most applications, the user will simply configure the starting address and install the module. Refer to the following paragraphs for procedures for configuring each item.

Address Selection

The MSV11-CD address can start at any 4K bank boundary. The address configured is the starting address for the contiguous 16K portion of memory contained on the module. Set the switches, located as shown on Figure 1, to the desired starting address as listed in Table 1. The upper 4K address space is normally reserved for peripheral device and register addresses. Thus, bank 7 (addresses 160000–177777) normally should not be used for system memory in a 32K addressable system.

Number of Banks Selection

It may be necessary in some systems to use less than the 16K of memory that is available on the MSV11-CD. The 4K banks of memory can only be disabled consecutively from the top bank down. Table 2 identifies the proper configuration of the jumpers.

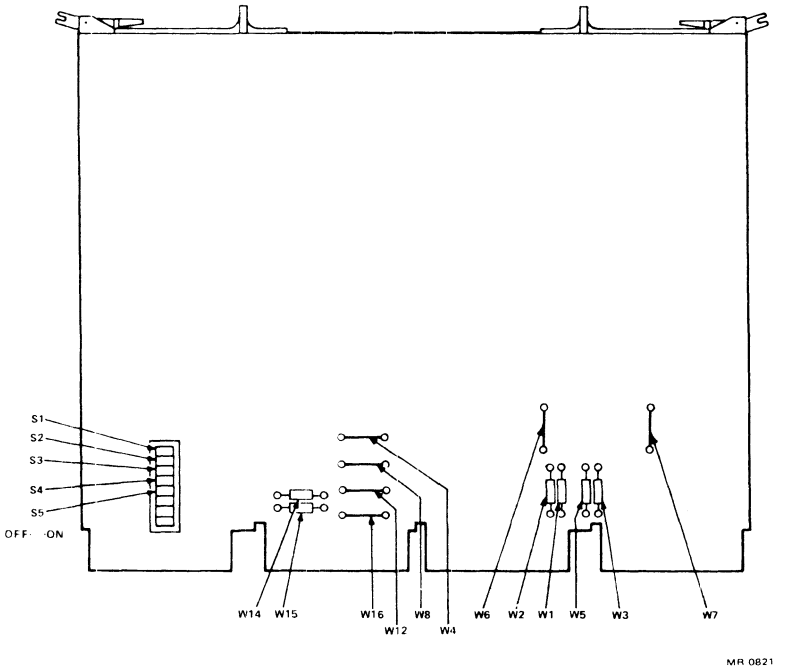


Figure 1 MSV11-CD Switch and Jumper Locations

Table 1 MSV11-CD Addressing Summary

Starting Address	Banks	Address Range	Switch Settings S1	S2	S3	S4	S5
0	0-3	0-77777	1	1	1	1	1
20000	1-4	20000-117777	0	1	1	1	1
40000	2-5	40000-137777	1	0	1	1	1
60000	3-6	60000-157777	0	0	1	1	1
100000	4-7	100000-177777	1	1	0	1	1
120000	5-10	120000-217777	0	1	0	1	1
140000	6-11	140000-237777	1	0	0	1	1
160000	7-12	160000-257777	0	0	0	1	1
200000	10-13	200000-277777	1	1	1	0	1
220000	11-14	220000-317777	0	1	1	0	1
240000	12-15	240000-337777	1	0	1	0	1
260000	13-16	260000-357777	0	0	1	0	1
300000	14-17	300000-377777	1	1	0	0	1
320000	15-20	320000-417777	0	1	0	0	1
340000	16-21	340000-437777	1	0	0	0	1
360000	17-22	360000-457777	0	0	0	0	1
400000	20-23	400000-477777	1	1	1	1	0
420000	21-24	420000-517777	0	1	1	1	0
440000	22-25	440000-537777	1	0	1	1	0
460000	23-26	460000-557777	0	0	1	1	0
500000	24-27	500000-577777	1	1	0	1	0
520000	25-30	520000-617777	0	1	0	1	0
540000	26-31	540000-637777	1	0	0	1	0
560000	27-32	560000-657777	0	0	0	1	0
600000	30-33	600000-677777	1	1	1	0	0
620000	31-34	620000-717777	0	1	1	0	0
640000	32-35	640000-737777	1	0	1	0	0
660000	33-36	660000-757777	0	0	1	0	0
700000	34-37	700000-777777	1	1	0	0	0
720000	x	x-x	0	1	0	0	0
740000	x	x-x	1	0	0	0	0
760000	x	x-x	0	0	0	0	0

NOTES

1. Switch settings:
   1 = ON
   0 = OFF
2. Each memory bank = one 4K address space.

Table 2 Bank Selection

Banks Disabled	W4	W8	W12	W16
None	I	I	I	I
3	I	I	I	R
2, 3	I	I	R	R
1, 2, 3	I	R	R	R

Refresh Mode Selection

The MSV11-CD module is factory-configured for internal (on-board) memory refresh and no reply (assertion of BRPLY L) in response to refresh cycles on the LSI-11 bus. Factory-installed wire-wrap jumpers W6 and W7, located as shown in Figure 1, provide these functions. W7, when installed, enables internal refresh. W6, when removed, enables the MSV11-CD to reply to external (LSI-11 bus) refresh cycles. W6 must be installed if W7 is installed to prevent erroneous assertion of the BRPLY L signal. A summary of refresh mode jumpers is provided in Table 3.

The reply to external refresh cycles is normally enabled when the module is deemed the slowest dynamic MOS memory device in the system. The slowest device (in this application) is generally the device located the greatest electrical distance from the device generating the refresh bus cycles. Only one device should be permitted to reply to refresh bus signals.

Table 3 Refresh Mode Selection

Jumper		
W6	W7	Refresh Mode Function
In	In	Factory configuration. Internal refresh; no reply.
Out	In	Illegal – do not use.
In	Out	External refresh; no reply.
Out	Out	External refresh; reply enabled.

Battery Backup

The MSV11-CD module is designed so that the dc power required to support it during a backup period is minimized. Jumper wires are provided on this module to allow the user to disconnect the memory and refresh logic from the normal bus power and connect it to a separate battery backup system. When supplied by DIGITAL, these jumpers allow the memory and refresh logic to be powered off the normal bus backplane power by having all power jumpers (W1, W2, W3, and W5) installed. The jumpers connect normal system power to battery backup

power pins. If battery backup is to be used with the MSV11-CD, cut or remove jumpers W1 and W5 as described below. The module will then receive dc operating voltages (+5 V and +12 V) from the battery backup source.

To support battery backup, the user-configurable jumpers shown in Figure 1 should be configured as follows.

W1, W5	Remove to separate the battery power from the bused system power.
W2, W3	Insert to connect the battery power to the refresh logic.
W6, W7	Insert to enable internal refresh and to prevent the module from asserting BRPLY during refresh.

If battery backup power is available but not desired for a particular MSV11-CD module, cut or remove jumpers W2 and W3; jumpers W1 and W5 must remain installed.

To use the MSV11-CD in a battery backup system, the battery system must be capable of supplying the following power.

	1 Module	**2 Modules**
+5 Vdc ± 5%	0.8 A	1.6 A
+12 Vdc ± 3%	0.18 A	0.32 A

These voltages must remain within ±3 percent of the voltages for the LSI-11 bus at all times and must not change by more than ±3 percent during the transition to or from the battery. One MSV11-CD module draws approximately 7.5 W of power while in the backup mode. This means that for a typical backup system that is 30 percent efficient, a 2.5 A-hr battery will support one module for approximately 1 5 hours.

When used in a PDP-11V03 system or equivalent, no additional cooling of this module is required during the backup period if the room temperature is maintained at less than 36° C (97° F) for one module and at less than 28° C (82° F) for two modules.

Bus Grant Continuity

Bus grant continuity jumpers W14 and W15 are factory-installed and normally should not be removed.

FUNCTIONAL DESCRIPTION

General

The basic functions that comprise the MSV11-CD are shown in Figure 2. All signals interface with the LSI-11 bus via bus receivers, bus drivers, and bus transceivers, which contain both receiver and driver functions. The receiver function of the bus transceivers shown in the figure distributes the 16 input data/address lines (D100–15 H) to the memory array and to addressing logic.

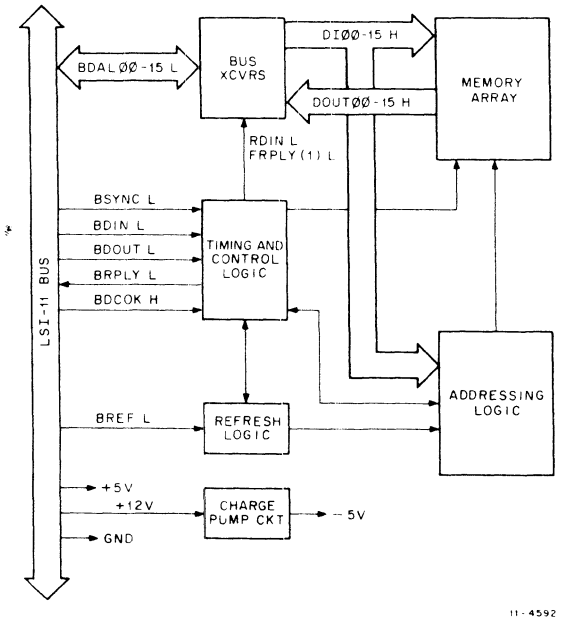


Figure 2 MSV11-CD Block Diagram

Timing and control logic receives BSEL H from the addressing logic whenever the bus address received is within the range configured by the operator. This is the signal that allows the timing and control logic to communicate with the bus and generate appropriate timing and control signals from the option.

The memory responds to address and control signals by storing (writing) an 8-bit byte or 16-bit word, or by outputting 16-bit (word) read data to the LSI-11 bus.

Additional functions include refresh logic and a charge pump circuit. The refresh logic is capable of responding to LSI-11 bus ("external") refresh signals, or it can produce refresh signals (including row address) independent of the LSI-11 bus ("internal refresh"). Memory chips are refreshed by forcing a read cycle at all 64 row addresses once every 2 ms, maximum. The MSV11-CD refresh logic refreshes one row address every 25 μs.

The charge pump circuit eliminates the need for backplane power other than the standard +5 V and +12 V. It contains an inverter circuit that receives +12 V input power and produces a negative voltage output. A zener-diode regulator produces –5 V for the memory integrated circuits.

Memory Array

The memory array (Figure 3) consists of sixteen 4K by 1-bit integrated circuits per memory bank; four memory banks are included in the option. Hence, 64 integrated circuits comprise the array. Each integrated circuit provides 1-bit by 4096-location storage.

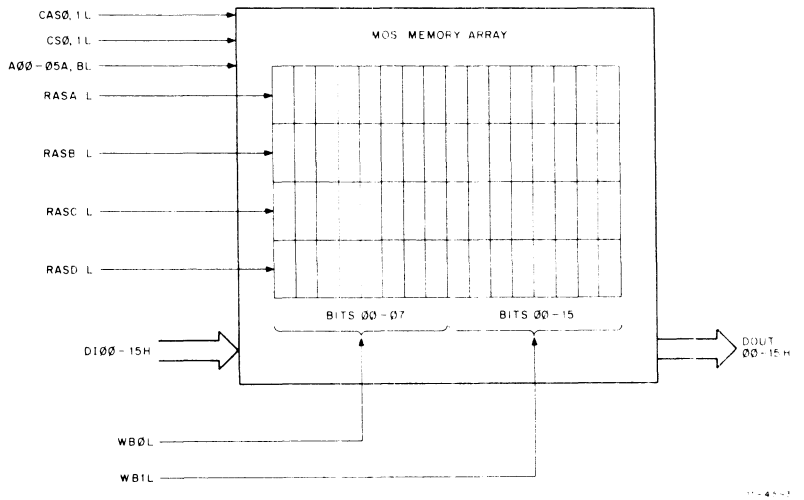


Figure 3 Memory Array

The memory array is arranged so that one bank out of four can be accessed at a time. The row address strobe (RASAL, RASBL, RASCL, and RASDL) signals select the desired bank. During a write operation, control signals WB0 L and WB1 L enable writing in the "low" byte (data bits 00–07) or "high" byte (data bits 08–15), or full word (both bytes accessed simultaneously).

Duplicate drivers are used for certain signals. These signals include column address strobe (CAS), chip select (CS), and address lines 00–05.

The duplicate driver output signals include:

Drivers	Output Signals
CAS	CAS0 L and CAS1 L
CS	CS0 L and CS1 L
Address	A00–05A L and A00–05B L

Each memory integrated circuit has six address input pins and contains a 12-bit address latch. Addressing the 4096 locations is accomplished by multiplexing the 12-bit address in two 6-bit segments. The low-order six bits (bus address bits 01–06) are first multiplexed onto A00–05A L/A00–05B L signal lines and latched in the addressed 16 integrated circuits by the active row address strobe signal. This is followed by multiplexing the high-order six bus address bits 07–12 onto the same six address lines; the column address strobe signals latch the address bits in the memory integrated circuits. The memory array is ready for the read or write operation once the addressing sequence has been completed. A detailed description of the complete addressing and read or write sequence is included in the following paragraphs.

Addressing Logic

The addressing logic (Figure 4) decodes a memory bank within the user-defined address space, latches the word or byte address within the selected bank, and routes time-multiplexed 6-bit address segments to the memory array for 1 of 4096 word addresses within the bank. In addition, it routes the refresh address to the memory bank during a refresh cycle. The following paragraphs describe addressing logic functions in detail. Generation of the control signals and how they relate to a complete memory read or write operation are described in the paragraph entitled "Timing and Control Logic."

A memory read or write cycle is initiated by the addressing portion of the LSI-11 bus cycle. The "bus master" first places the address on BDAL00–15 L and BAD16 and 17 L. (BAD16 and 17 L are presently not used by LSI-11 system hardware, but are available for future system configurations.) The bus master then asserts BSYNC L, indicating that a valid address is on the bus. LATCH L occurs on the leading edge of

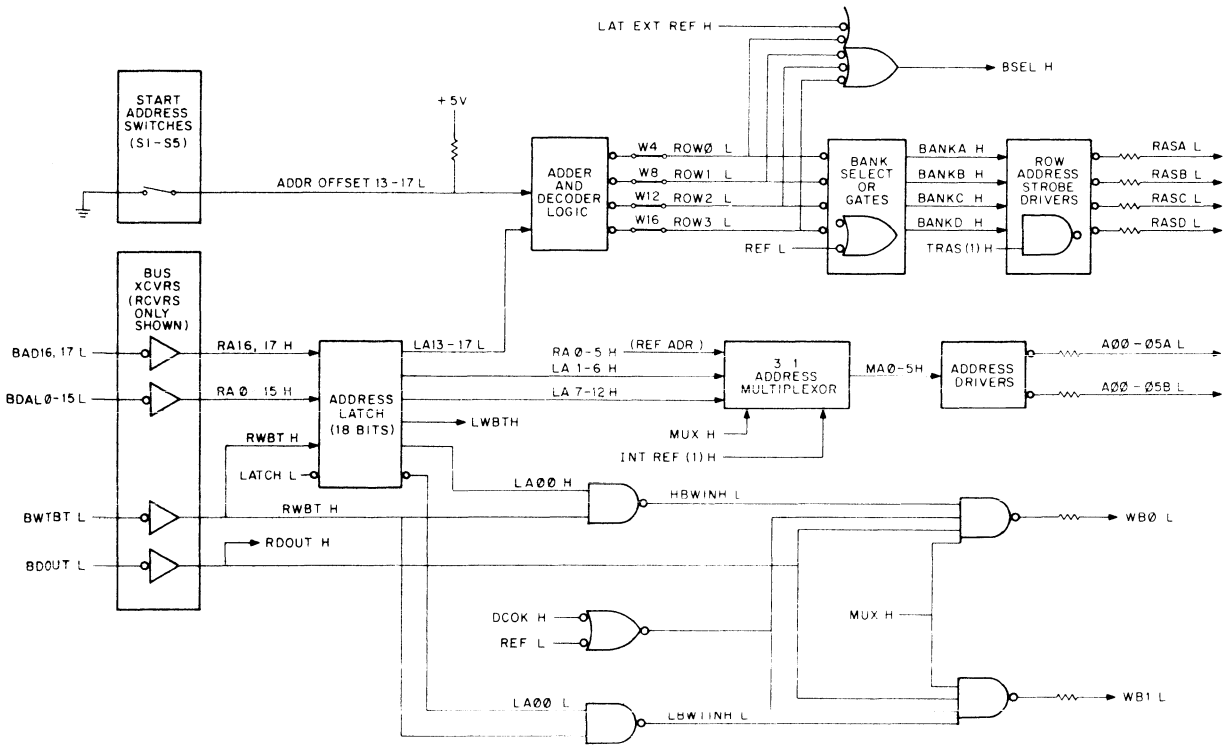


Figure 4 MSV11-CD Addressing Logic

BSYNC L, latching the received address bits RA0–17 H and the received bus write/byte control signal, RWBT H, for the duration of the bus cycle. Note that RWBT H is active during the addressing portion of DATO or DATOB bus cycles, indicating that a memory write operation will follow.

Start address switches S1–S5 are configured by the user to select the address space that the 16K memory will occupy. ADDR OFFSET 13–17 L signals are the encoded starting address switch bits. The bits are applied to the adder and decoder logic, where they are added to latched address bits LA13–17 L. One decoded output (ROW0–3 L) goes active (low) only when the latched address is within the 16K address space selected by the user. When the latched address is not within the assigned address space, the decoder outputs remain passive (high). These signals are applied to the BSEL H and bank select OR gates. Any active output (or an active LAT EXT REF L signal) produces an active (high) BSEL H signal; BSEL H enables the timing and control logic to start a memory cycle.

Bank select OR gates receive one active ROW signal via jumper W4, W8, W12, or W16 or an active REF L signal and produce one active BANK A-D H for normal memory cycles, or all active BANK A-D H signals during a memory refresh operation. The active BANK A-D H signal is ANDed with TRAS (1) H for proper timing during the memory cycle. The appropriate row address driver then produces one active RAS A-D L signal that enables one memory bank; all four signals go to the active state during a refresh operation to allow all memory banks to be refreshed simultaneously.

The 3:1 address multiplexer and address drivers select and apply the 6-bit address to the memory array. During a normal (non-refresh) memory cycle, MUX H and INT REF (1) H are passive (low), and the low-order six address bits are applied to the memory array and latched in each memory integrated circuit. MUX H then goes high, selecting the high-order six bits, which are then latched in the memory integrated circuits to comprise the 12-bit address. During an internal memory refresh operation, INT REF (1) H goes active, selecting the refresh address bits (RA0–5 H), which are applied to the memory array. If the external memory refresh mode of operation is configured by the user, the low-order address bits (LA1–6 H) are used for the refresh address.

During a write operation, the bus I/O sequence can be a DATO (word) or DATOB (byte) cycle. Bus signal BWTBT L goes passive during the data portion of a DATO cycle, enabling writing in all 16 bits of the addressed word. RWBT H goes low, inhibiting the byte inhibit gates, and HBWINH L and LBWINH L go passive (high), enabling WB0 L and WB1 L memory array drivers. The drivers are enabled only during an output data transfer (BDOUT L is active) and a non-refresh operation. The active MUX H

signal gates the drivers on at the proper time during the bus cycle. During a DATOB bus cycle, RWBT H goes active, enabling the byte inhibit gates. Latched address bit 0 (signals LA00 H and LA00 L) inhibits the WB0 L or WB1 L signals, as appropriate, to enable writing in only the addressed 8-bit byte within the addressed 16-bit location.

When backplane power is abnormal, DCOK H goes low. This signal inhibits WB0 L and WB1 L, preventing erroneous write operations.

Timing and Control Logic

Timing and control logic (Figure 5) interfaces the MSV11-CD to the LSI-11 bus and produces the internal control signals required for memory operation. This function produces timing and control signals for three types of memory cycles: read (DATI), write (DATO or DATOB), and refresh. In addition, read-modify-write cycles (DATIO or DATIOB) can be executed according to LSI-11 bus protocol. The MSV11-CD will also respond to externally generated refresh cycles if that refresh mode is configured by the user.

The control signal sequence for a memory read operation is shown in Figure 6. All bus transactions involving the MSV11-CD are initiated by the addressing portion of the bus cycle. The bus master first places an address on the BDAL00–15 L (and optional BAD16, 17 L) lines and asserts BSYNC L. BSYNC L is received and distributed as RSYNC H and LATCH L. The leading edge of LATCH L latches the address in the addressing logic and the address will remain valid for the duration of the bus transaction (during the active state of BSYNC L).

Initially, NO DIN L and LOCKOUT L are passive (high), enabling two inputs of the read cycle initiate gate. RSYNC H enables a third input to the gate. When the latched address is within the MSV11-CD's address space configured by the user, BSEL H goes high, producing a low (active) read cycle initiate gate output. The low signal is ORed, producing an active GOTIM H signal. This is the signal that starts the memory cycle.

GOTIM H is then applied to the 80-ns delay circuit. The delay circuit inserts an 80-ns delay only during internal refresh operation. The delay circuit is shown in Figure 7.

If an internal refresh cycle is in progress when BSYNC L is asserted, the memory read or write cycle cannot be executed until the refresh cycle has been completed. However, if an internal refresh cycle is requested after GOTIM H is generated for a read or write cycle, the read or write cycle is first executed.

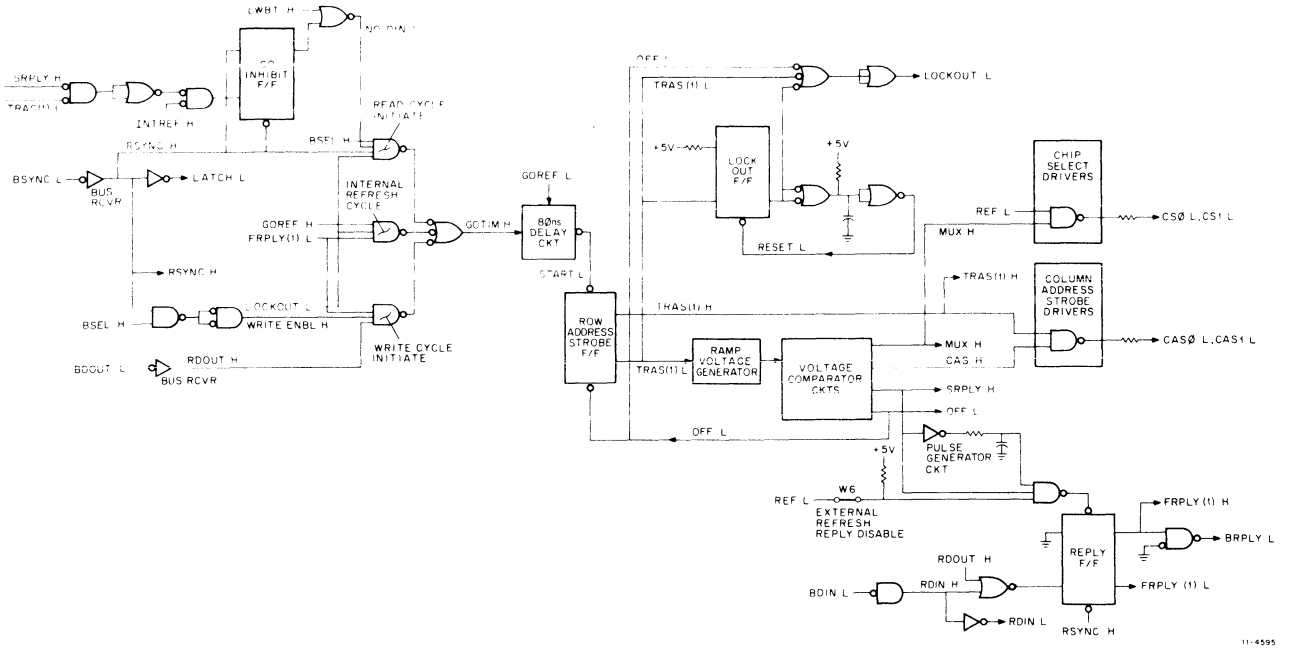


Figure 5 MSV11-CD Timing and Control Logic

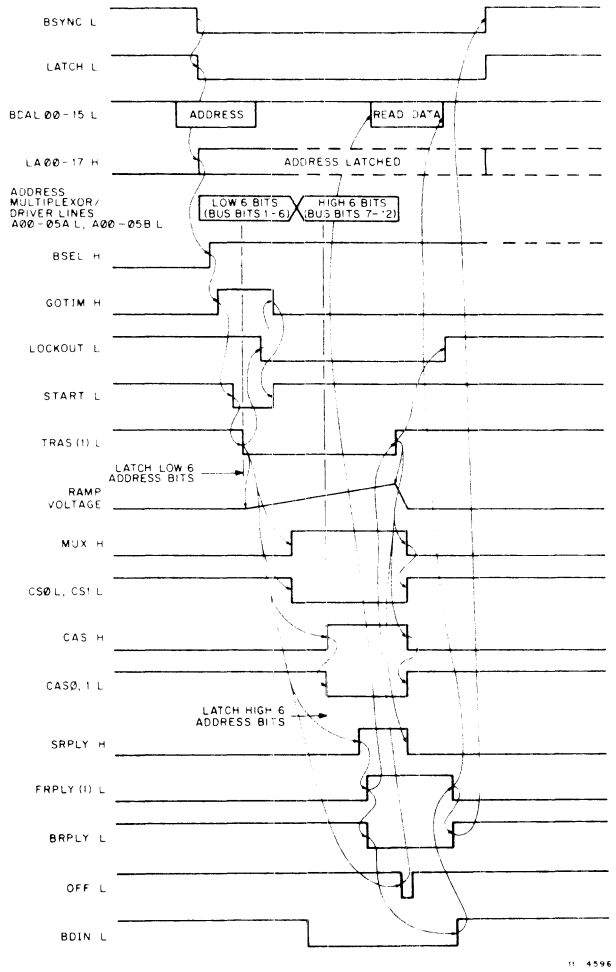


Figure 6 MSV11-CD Read (DATI) Sequence

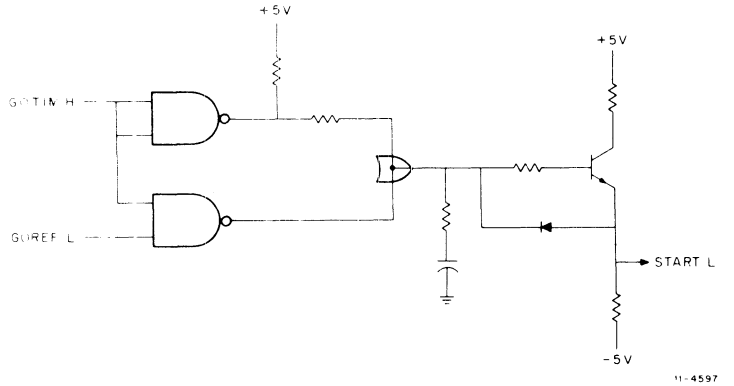


Figure 7 80 ns Delay Circuit

START L is the active (low) delay circuit output and it sets the row address strobe flip-flop. Active TRAS (1) H and TRAS (1) L signals are produced. Active TRAS (1) L is ORed with OFF L and the lockout flip-flop to generate LOCKOUT L. LOCKOUT L is ANDed in the read cycle initiate gate, the write cycle initiate gate, and the internal refresh gate to inhibit the GOTIM H signal from occurring until the present cycle is complete. The lockout flip-flop is used to generate a delay from the reset of TRAS (1) L to ensure proper memory timing. TRAS (1) L is gated with passive (low) SRPLY H and INTREF H signals, producing a high signal that clocks the Go Inhibit flip-flop to the set state; note that the high (active) RSYNC H signal applied to the data input of the flip-flop when clocked by the leading edge of TRAS (1) L enables the set state on the positive-going leading edge of the clock input to the flip-flop. The resulting high flip-flop output signal is ORed to produce an active (low) NO DIN L signal that inhibits the read cycle initiate gate to prevent multiple DATI cycles from occurring without RSYNC H being reset.

TRAS (1) H enables column address strobe drivers that latch the high-order 6-bit address in the memory array later in the read cycle.

TRAS (1) L activates an R-C ramp voltage generator that applies a rising voltage (Figure 6) to the voltage comparator circuits. Four voltage comparators, each having different reference voltage inputs, produce the four control signals: MUX H, CAS H, SRPLY H, and OFF L. The reference voltage applied to a comparator determines the point along the ramp voltage at which the comparator's output will change logical state.

Hence, the reference voltage, relative to the ramp voltage, determines the time delay produced by each comparator circuit.

The first active signal produced by the comparator circuit is MUX H. MUX H selects the high-order six address bits that are applied to the memory array. MUX H is ANDed with the passive REF L signal, producing the active chip select (CS0 L and CS1 L) signals.

The next voltage comparator output signal that goes active is CAS H. CAS H is ANDed with the active TRAS (1) H signal, producing the active column address strobe (CAS0 L and CAS1 L) signals. These signals latch the high-order six address bits in the memory array integrated circuits, completing the 12-bit address within the accessed 4K bank. Read data is then available on DOUT00–15 H.

The next voltage comparator output signal that goes active is SRPLY H. SRPLY H is applied to a pulse generator circuit whose 30 ns output pulse is ANDed with the passive REF L signal; the resulting low pulse sets the reply flip-flop, and FRPLY (1) H and FRPLY (1) L signals go to their active states. The BRPLY L bus driver asserts the BRPLY L signal and driver portions of the bus transceivers, enabled by RDIN L (received BDIN L) and FRPLY (1) L, place the memory read data on BDAL00–15 L.

The last voltage comparator signal produced is OFF L. OFF L clears the row address strobe flip-flop and TRAS (1) H and TRAS (1) L go to their passive states. The passive (low) TRAS (1) H signal inhibits the column address strobe drivers and CAS0 L and CAS1 L go to their passive states. The passive (high) TRAS (1) L signal resets the ramp voltage and MUX H, CS0 L, CS1 L, CAS H, SRPLY H, and OFF L go to their passive states.

The bus master responds to the active BRPLY L signal by reading the data from the bus and terminating the BDIN L signal. BDIN L (passive) is received and inverted, producing a negative-going trailing edge on BDIN H. BDIN H is ORed with RDOUT H, producing a positive-going transition at the clock input of the reply flip-flop. This transition clocks the flip-flop to the reset state. FRPLY (1) H goes low, inhibiting the BRPLY L bus driver and FRPLY (1) L goes high, inhibiting the BDAL00–15 L read data bus drivers. The bus master responds by terminating BSYNC L, and the memory read cycle is completed.

A memory write (DATO or DATOB) cycle is somewhat similar to the memory read cycle. However, during the addressing portion of the cycle, the bus master asserts BWTBT L, indicating an output (write) operation is to follow. The signal sequence for the timing and control logic write operation is shown in Figure 8. BWTBT is received (RWBT H) and

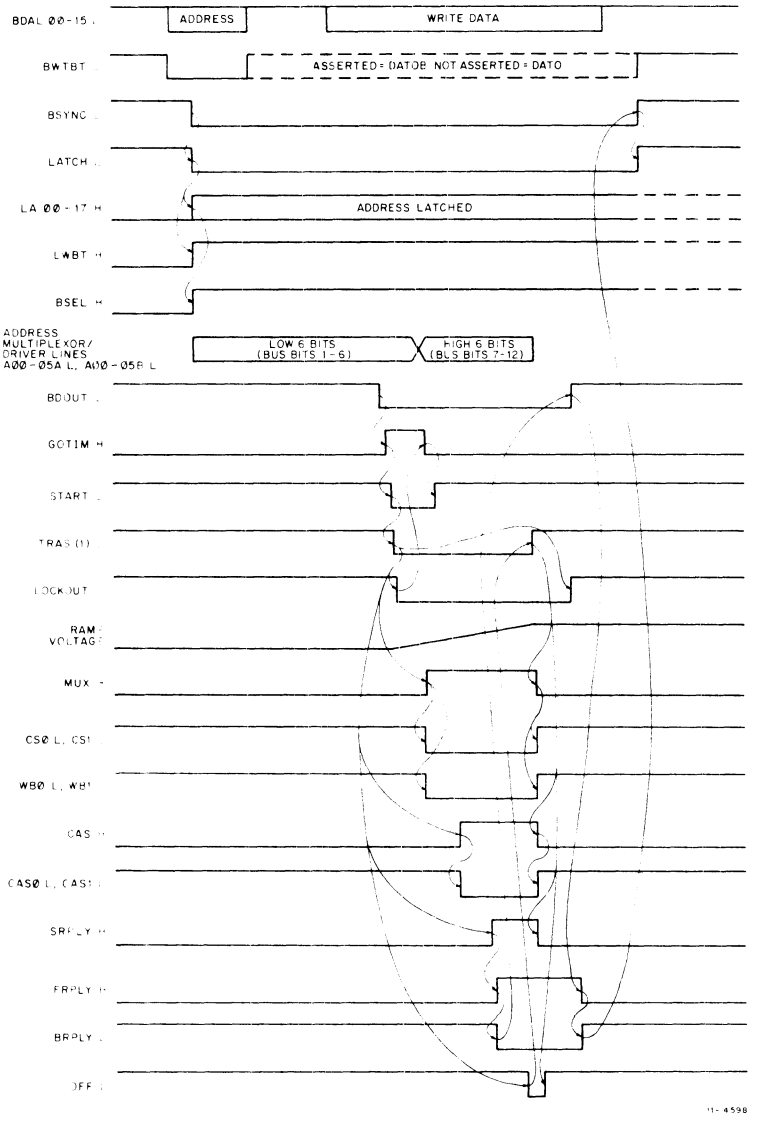


Figure 8 MSV11-CD Write (DATO or DATOB) Sequence

latched by the active LATCH L signal; the address bits are latched in the same manner as previously described. The latched signal (LWBT H) inhibits the read cycle initiate gate and prevents immediate generation of the GOTIM H signal. However, the latched row address bits LA1-6 H are routed via the 3:1 address multiplexer to the memory array.

The bus master then places the write data on the BDAL bus and asserts BDOUT L. BDOUT L is received, producing RDOUT H. RDOUT H is gated with passive (high) LOCKOUT L, FRPLY (1) L, and active WRITE ENBL H signals to produce the active GOTIM H signal.

Operation of the timing and control logic continues as described for read operation generation of the MUX H, CAS H, SRPLY H, and OFF L signals. However, the RDOUT signal enables WB0 L and/or WB1 L signal generation in the addressing logic, and the received data is written in the addressed location.

The bus master responds to the BRPLY L signal by terminating BDOUT L and removing the write data from the BDAL bus lines. RDOUT H, which is ORed with the passive RDIN H signal, goes low, and the low to high transition resets the reply flip-flop. BRPLY L then goes passive (high). The bus master responds by terminating BSYNC L and the write operation is completed.

The memory read-modify-write operation is produced by the DATIO (or DATIOB) bus cycle. The bus master first initiates a "memory read" operation at the addressed location. However, instead of terminating BSYNC L after the read portion of the cycle has been completed, BSYNC L remains asserted; the bus master places the write (modified) data on the bus and asserts BDOUT L. The MSV11-CD responds by writing the data in the addressed word or byte location. The BWTBT L signal is asserted with the write data to indicate a DATIO bus cycle is in progress, when appropriate. Except for the addressing portion being omitted for the write portion of the DATIO (or DATIOB) bus cycle, operation of the MSV11-CD is as previously described for memory read and memory write operations.

Memory Refresh Operation

Dynamic MOS memory integrated circuits comprising the memory array require periodic refreshing in order to retain stored data. This is accomplished by forcing a memory read operation on each of the 64 row addresses; one read operation is required for each row address. Each row address must be refreshed in this manner once every 2 ms (maximum).

MSV11-CD memory refresh can be accomplished by using the on-board (internal) refresh logic signals, or by using refresh signals present on the

LSI-11 bus (external refresh). The internal refresh circuit is most transparent to the LSI-11 system since it automatically refreshes one row address every 25 μs; bus-generated refresh cycles are not required when the internal refresh mode is selected. When other memory system components in the system require LSI-11 bus memory refresh signals, the MSV11-CD internal refresh mode can be disabled and the refresh operation can be controlled externally by LSI-11 bus signals. Note thatwhen the external refresh mode is selected, all system memory components are refreshed simultaneously.

The MSV11-CD refresh logic circuit is shown in Figure 9. The sequence of internal refresh operation is shown in Figure 10. When the internal refresh mode is selected, jumper W7 is installed, producing the active (high) CLK EN H signal. This signal activates the 25 μs clock and places a high level at the internal refresh cycle flip-flop's data input. The positive-going transition of the 25 μs clock clocks the flip-flop to the set state, causing GO REF L and GO REF H to go to their active states (low and high, respectively). GO REF H conditions the data input of the internal refresh flip-flop.

When the MSV11-CD is not involved in a read or write operation, FRPLY (1) L and LOCKOUT L are passive (Figure 5). These passive signals are gated with the active GO REF H signal, producing an active GOTIM H signal. The leading edge of GOTIM H clocks the internal refresh flip-flop to the set state and INTREF (1) H goes high. INTREF (1) H is ORed with the passive LAT EXT REF H signal to produce an active (low) REF L signal.

GO REF L is applied to the 80 ns delay circuit (Figure 7), forcing the 80 ns delay to occur. The delay provides settling time for the internal refresh flip-flop. After the 80 ns delay has completed, START L goes active, setting the row address strobe flip-flop, and TRAS (1) L and TRAS (1) H go to their active states. TRAS (1) L provides an active LOCKOUT L signal, inhibiting the GOTIM H signal. Operation then continues as in the memory read cycle, except the active INTREF (1) H signal selects RA00–05 H refresh address (row) bits, which are routed through the address multiplexer and applied to the memory array; passive (low) column address bits are applied to the memory array during the active state of MUX H, but are not significant during the refresh operation. The active REF L signal, applied to the reply circuit via jumper W6, also inhibits SRPLY H from setting the reply flip-flop and generating an erroneous BRPLY L signal.

SRPLY H is gated with INTREF (1) H, producing a low clear signal for the internal refresh cycle flip-flop, and GO REF L and GO REF H go passive. GOTIM H goes passive and the 80 ns delay circuit START L signal goes passive. OFF L then goes active (low), clearing the internal

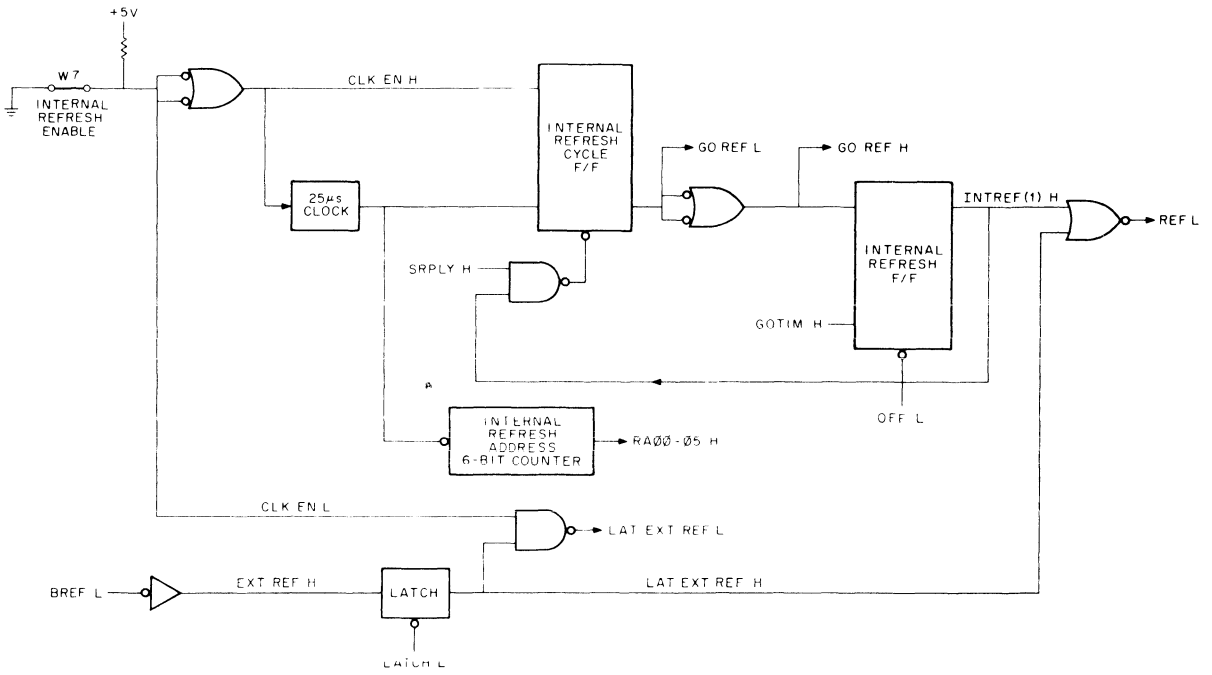


Figure 9 MSV11-CD Refresh Logic

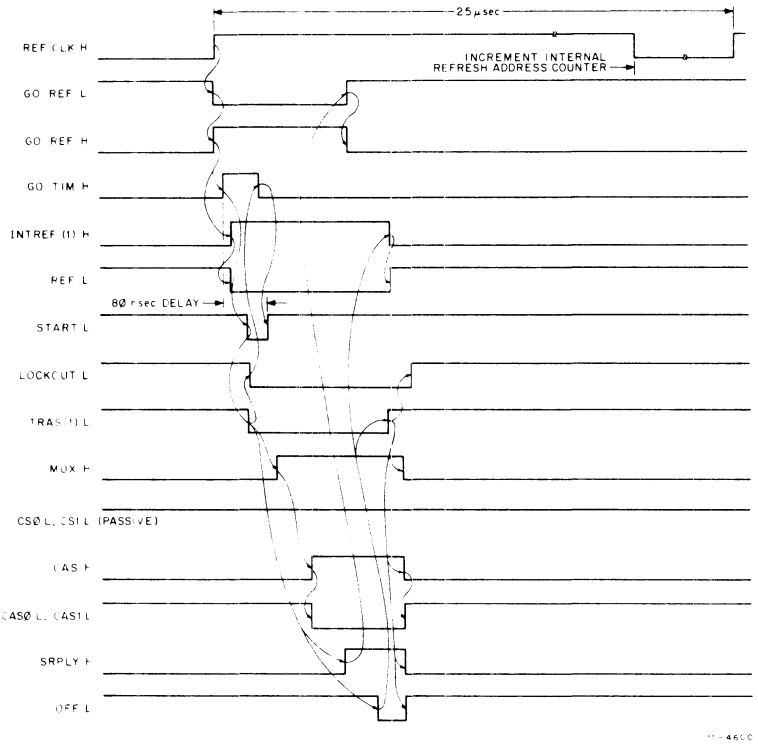


Figure 10 MSV11-CD Internal Refresh Sequence

refresh and row address strobe flip-flops; REF L, TRAS (1) L, LOCKOUT L, MUX H, CAS H, SRPLY H, and OFF L signals go to their passive states.

The internal refresh counter is incremented by the trailing edge of REF CLK H prior to the next internal refresh operation. Hence, each successive internal refresh operation uses the next sequential row address.

When a memory read or write operation is initiated just prior to the refresh operation, and the read or write cycle is still in progress, the leading edge of GOTIM H clocks the passive (low) GO REF H signal into the internal refresh flip-flop; INTREF (1) H remains reset for the duration

of the memory cycle. The refresh operation will not be enabled until LOCKOUT L and FRPLY (1) L go passive (high) at the end of the read or write cycle, enabling a new GOTIM H signal. If this condition occurs, the leading edge of the new GOTIM H signal clocks the active (high) GO REF F signal into the internal refresh flip-flop, and the refresh operation continues as described previously.

When the external refresh mode is selected, jumper W7 is removed. CLK EN H goes low, and the internal refresh cycle flip-flop cannot be set by the 25 μs clock signal. CLK EN L goes high, enabling one input to the LAT EXT REF L gate.

An external refresh cycle is initiated by the bus master asserting BREF L; EXT REF H goes high. The bus master places the refresh row address on the BDAL 1–6 L lines and asserts BSYNC L. BSYNC L produces the active (low) LATCH L signal that latches the 6-bit address in the address latch (Figure 4), and the EXT REF H signal (Figure 9), producing the active (high) LAT EXT REF H signal. This signal is gated with CLK EN L, producing the LAT EXT REF L signal and forcing an active BSEL H signal in the addressing logic. Thus, the MSV11-CD is addressed and enabled for the refresh operation. The external refresh signal sequence is shown in Figure 11.

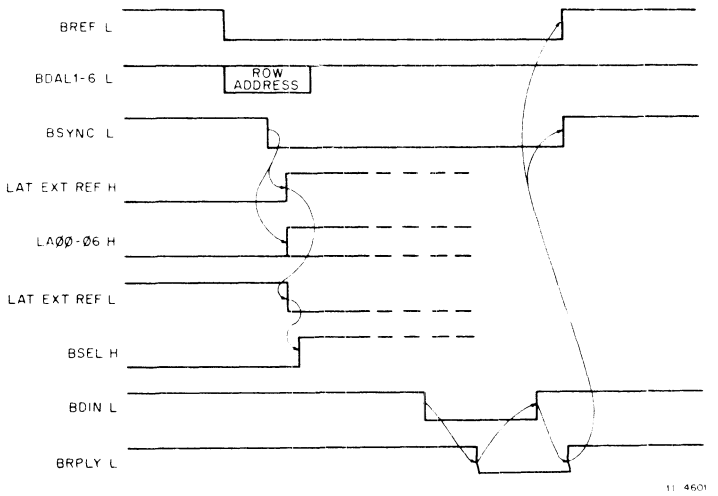


Figure 11 MSV11-CD External Refresh Signal Sequence

The refresh operation continues as described for a memory read operation, except the active REF L signal (produced by the active LAT EXT REF H signals) inhibits a BRPLY L signal, as described for the internal refresh operation. If the MSV11-CD must reply during the external refresh bus transaction, jumper W6 is removed; REF L will not inhibit the reply circuit and BRPLY L will be generated. Only one MOS memory module in a system is required to reply to the refresh bus transactions. The module that should reply is the module with the slowest access time relative to the bus master device. This module is generally the module located the greatest electrical distance on the LSI-11 bus from the bus master device controlling the refresh operation.

Charge Pump Circuit

The charge pump circuit (Figure 12) provides the −5 V power for the MOS memory array integrated circuits. The input power source for this circuit is +12 V. An oscillator circuit, running at approximately 40 kHz, produces a square-wave drive signal to the rectifier circuit. Q2 switches the ground alternation for the charge pump capacitors, reducing the switching current requirement for the oscillator circuit. The rectifier output is −10 V (approximately). The −5 V output is zener-diode regulated. Note that this circuit eliminates the need for backplane power other than the standard +5 V and +12 V. The circuit remains active when battery backup power is used.

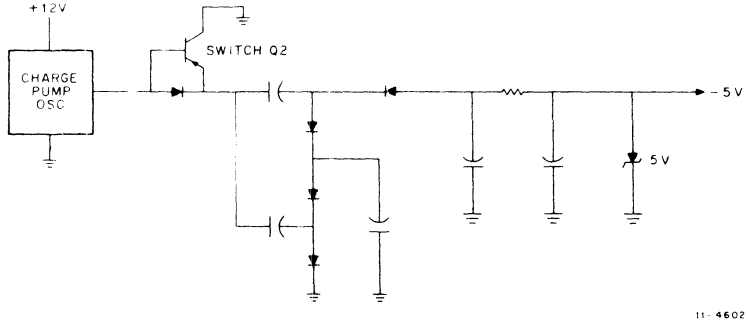


Figure 12 MSV11-CD Charge Pump Circuit

MSV11-D, -E MEMORY

GENERAL

All MSV11-D and MSV11-E memory modules plug into any LSI-11 bus. There are eight versions of this module and they are listed below.

Model	Memory Capacity	Module	Parity Bits
MSV11-DA	4K by 16 bits	M8044-A	No
MSV11-DB	8K by 16 bits	M8044-B	No
MSV11-DC	16K by 16 bits	M8044-C	No
MSV11-DD	32K by 16 bits	M8044-D	No
MSV11-EA	4K by 18 bits	M8045-A	Yes
MSV11-EB	8K by 18 bits	M8045-B	Yes
MSV11-EC	16K by 18 bits	M8045-C	Yes
MSV11-ED	32K by 18 bits	M8045-D	Yes

NOTE

K = 1024 (e.g., 4K = 4096).

Memory storage is provided by either 4K by 1 bit or 16K by 1 bit integrated circuits, depending on model. The integrated circuits are dynamic metal oxide semiconductor (MOS) types that the processor can access during read and write operations. Memory contents are volatile; that is, when operating power is lost, memory data is lost. However, memory contents can be protected during system power failures by supplying battery backup power.

FEATURES

- On-board memory refresh is provided, eliminating the need for refresh signals on the LSI-11 bus.
- The system memory address space to which the module will respond is user-configured via switches contained on the module. An address can start at any 4K bank boundary ranging through the 0–128K address range.
- Memory modules perform DATI, DATO, DATOB, DATIO, and DATIOB bus cycles according to LSI-11 bus protocol.
- No special power is required. Only the normal +5 V and +12 V present on the LSI-11 backplane are necessary. An on-board charge pump circuit produces the necessary –5 V operating voltage for the memory integrated circuits.

- Jumpers allow the user to implement battery backup power.
- Memory access is disabled when "bank 7" is addressed (BBS7 L is asserted) or when "external" memory refresh bus cycles are in progress. The lower 2K of bank 7 can be enabled by a user-installed jumper. (Bank 7, the upper 4K system address space, is normally reserved for peripheral device addressing.)

SPECIFICATIONS

Identification

MSV11-DX	M8044-X
MSV11-EX	M8045-X (X = A,B,C,D)

Size: Double

Power

	Supply Voltage	Typical Operating Power	Typical Standby Power
MSV11-DA,-DC (4K or 16K)	+5 V system power +5 V battery backup +12 V system power or battery backup	1.7 A 0.7 A 0.34 A	1.7 A 0.7 A 0.06 A
MSV11-DB,-DD (8K or 32K)	+5 V system power +5 V battery backup +12 V system power or battery backup	1.7 A 0.7 A 0.37 A	1.7 A 0.7 A 0.08 A
MSV11-EA,-EB (4K or 16K)	+5 V system power +5 V battery backup +12 V system power or battery backup	2.0 A 1.0 A 0.38 A	2.0 A 1.0 A 0.06 A
MSV11-EC,-ED (8K or 32K)	+5 V system power +5 V battery backup +12 V system power or battery backup	2.0 A 1.0 A 0.41 A	2.0 A 1.0 A 0.09 A

Bus Loading

AC	2
DC	1

Operational

MSV11-D

Bus Cycle Type	Access Time (ns) Typ	Max	Notes	Cycle Time (ns) Typ	Max	Notes
DATI	210	225	1,2	500	520	1,4
DATO(B)	100	110	1,2	545	565	1,5
DATIO(B)	630	650	1,3	1075	1100	1,6

MSV11-E

Bus Cycle Type	Access Time (ns) Typ	Max	Notes	Cycle Time (ns) Typ	Max	Notes
DATI	250	265	1,2	500	520	1,4
DATO(B)	100	110	1,2	545	565	1,5
DATIO(B)	670	690	1,3	1115	1140	1,6

All Models

Refresh cycle time (7) 575 ns typ., 600 ns max.

NOTES

1. All operating speeds are in nanoseconds and are based on memory not busy and no refresh arbitration. Refresh arbitration adds 100 ns typical (120 ns maximum) to access and cycle times. Refresh conflicts add 575 ns typical (600 ns maximum) to access and cycle times.

2. Access times are defined as internal SYNC H to REPLY H with minimum times (25 or 50 ns) from SYNC H to DIN H or DOUT H. The DATO(B) access and cycle times assume a minimum 50 ns from SYNC H to DOUT H at bus receiver outputs. For actual LSI-11 bus measurements, 150 ns should be added to DATO(B) times, i.e., access time (typical) = 100 + 150 = 250 ns.

3. Access times are defined as internal SYNC H to REPLY H [DATO(B)] with minimum time (25 ns) from SYNC H to DIN H, and minimum time (350 ns) from RPLY H (DATI) asserted to DOUT H asserted.

4. Cycle times are defined as internal SYNC H to LOCKOUT L negated.

5. Cycle times are defined as internal SYNC H to LOCKOUT L negated with minimum time (50 ns) from SYNC H to DOUT H.

6. Cycle times are defined as internal SYNC H to LOCKOUT L [DATO(B)] with minimum times (25 ns) from SYNC H to DIN H and minimum time (350 ns) from RPLY H (DATI) asserted to DOUT asserted.

7. Refresh cycle time is defined as internal REF REQ L to LOCKOUT L negated.

CONFIGURATION

General

Configuring the MSV11-D or MSV11-E will alter its operation for a specific system application. The following items can be configured.

1. Select the starting address for the contiguous memory contained on the module

2. Battery backup power

3. Enable/disable 2K word portion of bank 7

NOTES

1. If the MSV11-D or MSV11-E memory module is installed in a system that contains a KD11-F processor module etch revision C or D, CS revision H2 or earlier, BDAL16 L and BDAL17 L bus lines (AC1 and AD1, respectively) must be terminated. An REV11-A, TEV11, or BCV1B cable set will also accomplish this termination.

2. Each MSV11-D or -E module contains two factory-installed wire-wrap jumpers that select memory size (4K, 8K, 16K, or 32K); these jumper configurations normally should not be changed.

Address Selection

The MSV11-D or MSV11-E address can start at any 4K bank boundary. The address configured is the starting address for the contiguous portion of memory (4K, 8K, 16K, or 32K) contained on the module. Set the switches, located as shown in Figure 1, to the desired starting address as listed in Table 1. The upper 4K address space is normally reserved for peripheral device and register addresses.

Factory-configured modules will not respond to bank 7 addresses. In special applications that permit the use of the lower 2K portion of bank 7 for system memory, enable the lower 2K portion of bank 7 by removing the jumper from wire-wrap pins 1 and 3 and connecting a new jumper from 1 to 2.

Battery Backup Power

The MSV11-D and MSV11-E modules are factory-configured with the power jumpers installed for normal system power. In this configuration, the memory and refresh logic are powered from the normal bus backplane power. The modules are designed so that the dc power required to support them during a backup period is minimized. The jumpers are provided to allow the user to disconnect the memory and refresh logic from the normal bus power and connect it to a separate battery source. The user can configure the jumpers, shown in Figure 1, for battery backup operation as follows:

W2, W3 Remove to separate the module from the bus-powered backplane.

W4, W5 Insert to connect the battery power to the memory and refresh logic.

To use the MSV11-D or MSV11-E modules in a battery backup system, the battery or source must be capable of supplying the following:

	MSV11-D (1 Module)	**MSV11-E (1 Module)**
+5 Vdc ± 3%	0.7 A	1.0 A
+12 Vdc ± 5%	0.37 A	0.41 A max

These voltages must remain within ±3% of the bus voltage at all times and not vary more than ±3% during the transition to or from the battery.

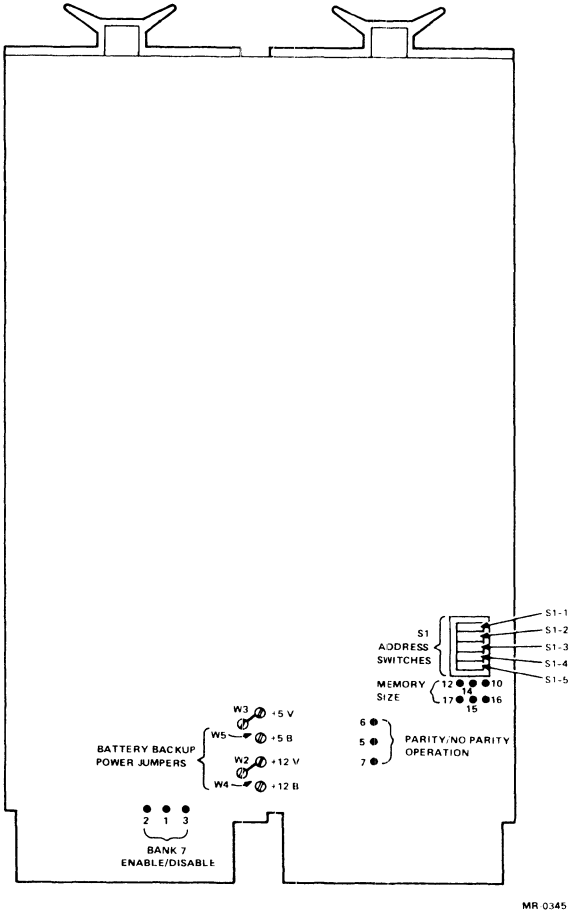


Figure 1 MSV11-D, MSV11-E Switch and Jumper Locations

Table 1 MSV11-D, MSV11-E Addressing Summary

Starting Address	Switch Settings					Memory Bank(s) Selected			
	S1-1	S1-2	S1-3	S1-4	S1-5	-DA, -EA	-DB, -EB	-DC, -EC	-DD, -ED
0	C	C	C	C	C	0	0–1	0–3	0–7
20000	C	C	C	C	O	1	1-2	1-4	1-10
40000	C	C	C	O	C	2	2-3	2-5	2-11
60000	C	C	C	O	O	3	3-4	3-6	3-12
100000	C	C	O	C	C	4	4-5	4-7	4-13
120000	C	C	O	C	O	5	5-6	5-10	5-14
140000	C	C	O	O	C	6	6-7	6-11	6-15
160000	C	C	O	O	O	7	7-10	7-12	7-16
200000	C	O	C	C	C	10	10-11	10-13	10-17
220000	C	O	C	C	O	11	11-12	11-14	11-20
240000	C	O	C	O	C	12	12-13	12-15	12-21
260000	C	O	C	O	O	13	13-14	13-16	13-22
300000	C	O	O	C	C	14	14-15	14-17	14-23
320000	C	O	O	C	O	15	15-16	15-20	15-24
340000	C	O	O	O	C	16	16-17	16-21	16-25
360000	C	O	O	O	O	17	17-20	17-22	17-26
400000	O	C	C	C	C	20	20-21	20-23	20-27
420000	O	C	C	C	O	21	21-22	21-24	21-30
440000	O	C	C	O	C	22	22-23	22-25	22-31
460000	O	C	C	O	O	23	23-24	23-26	23-32
500000	O	C	O	C	C	24	24-25	24-27	24-33
520000	O	C	O	C	O	25	25-26	25-30	25-34
540000	O	C	O	O	C	26	26-27	26-31	26-35
560000	O	C	O	O	O	27	27-30	27-32	27-36
600000	O	O	C	C	C	30	30-31	30-33	30-37

Table 1 MSV11-D, MSV11-E Addressing Summary (Cont)

Starting Address	Switch Settings					Memory Bank(s) Selected			
	S1-1	S1-2	S1-3	S1-4	S1-5	-DA, -EA	-DB, -EB	-DC, -EC	-DD, -ED
620000	O	O	C	C	O	31	31-32	31-34	X
640000	O	O	C	O	C	32	32-33	32-35	X
660000	O	O	C	O	O	33	33-34	33-36	X
700000	O	O	O	C	C	34	34-35	34-37	X
720000	O	O	O	C	O	35	35-36	X	X
740000	O	O	O	O	C	36	36-37	X	X
760000	O	O	O	O	O	37	X	X	X

NOTES

1. Switch settings

   C = ON
   O = OFF

2. Bank 7 cannot be selected as factory-configured; however, the user can enable the lower 2K portion of bank 7 for use.

3. X = Do not use.

4. Rocker switch positions are defined by pressing the desired side of the rocker, not by the red line on the opposite side of the rocker.

One MSV11-E module draws approximately 7 W when operating in the battery backup mode. A typical backup system that is 30% efficient with a 2.5 ampere-hour battery will support each module for approximately 2 hours. When used in a PDP-11/03 system, or equivalent, no additional cooling of the module is required during the backup period, if the room temperature is maintained to less than 32° C (90° F).

Parity

One jumper is factory-installed for nonparity (MSV11-D) or parity (MSV11-E) operation, depending on model. Do not reconfigure this jumper. Standard jumper configurations are listed below for reference purposes. Refer to the functional description section on parity for recommended implementation.

All MSV11-D models: Jumper installed from pin 7 to pin 5
All MSV11-E models: Jumper installed from pin 6 to pin 5

Memory Size

Two jumpers are factory-installed to configure addressing logic for memory size (number and type of memory integrated circuits). Do not reconfigure these jumpers. Standard jumper configurations are listed below for reference purposes.

	Jumpers (Two Installed)	
Models	**Memory Range Pins**	**Memory Select Pins**
MSV11-DA,-EA	From 17 to 15	From 17 to 14
MSV11-DB,-EB	From 17 to 15	From 12 to 14
MSV11-DC,-EC	From 16 to 15	From 16 to 14
MSV11-DD,-ED	From 16 to 15	From 10 to 14

FUNCTIONAL DESCRIPTION

General

Logic functions and circuits that comprise MSV11-D and MSV11-E memory modules are shown in Figure 2. Both types of memory modules are identical, with the exception that MSV11-E models include parity logic; MSV11-D models do not include parity.

Memory Array

The memory array is the main function contained on the module. Depending on model, the module will contain 16 or 32 dynamic random access memory (RAM) integrated circuits (ICs); MSV11-E models include an additional two or four RAM ICs, depending on model, as part of the parity logic. All RAM ICs will be identical types for a given model.

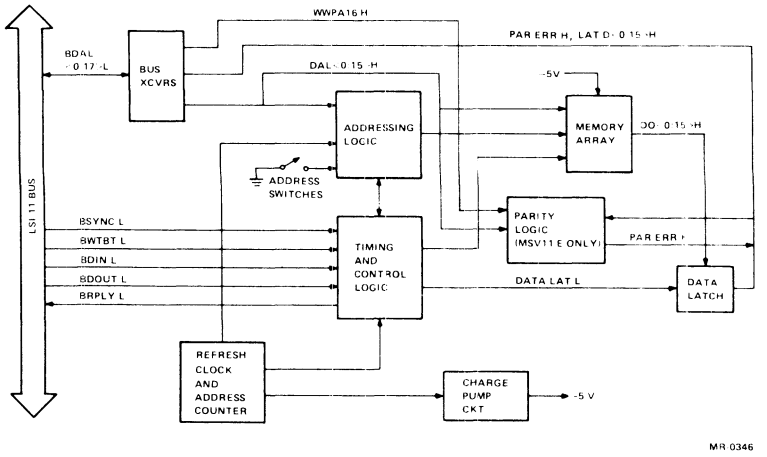


Figure 2 MSV11-D and MSV11-E Logic Functions

Two types are used: 4K by 1 bit and 16K by 1 bit. The number and type of RAMS used are listed for each memory model as follows.

Model	RAM IC Type	Qty RAM ICs in Memory Array	Qty RAM ICs in Parity Logic
MSV11-DA	4K X 1	16	None
MSV11-DB	4K X 1	32	None
MSV11-DC	16K X 1	16	None
MSV11-DD	16K X 1	32	None
MSV11-EA	4K X 1	16	2
MSV11-EB	4K X 1	32	4
MSV11-EC	16K X 1	16	2
MSV11-ED	16K X 1	32	4

The memory array is organized as shown in Figure 3. As previously listed, either 16 or 32 memory ICs comprise the memory array. Models that include only 16 ICs are organized with 8 ICs in the high byte and 8 ICs in the low byte of the low range array shown on the figure. Models that include 32 ICs include the 16 ICs described for the 16-IC models, plus an additional 16 ICs for the high and low bytes of the high range array. Row address strobe (RAS0 L and RAS1 L) control signals, produced by the addressing logic, select the appropriate low or high range

array. Write byte (WTBT1 L and WTBT0 L) control signals are produced by the addressing logic during a memory write operation to select the addressed byte (DATOB bus cycle); during a word write operation (DATO bus cycle), WTBT L is high and selects both bytes.

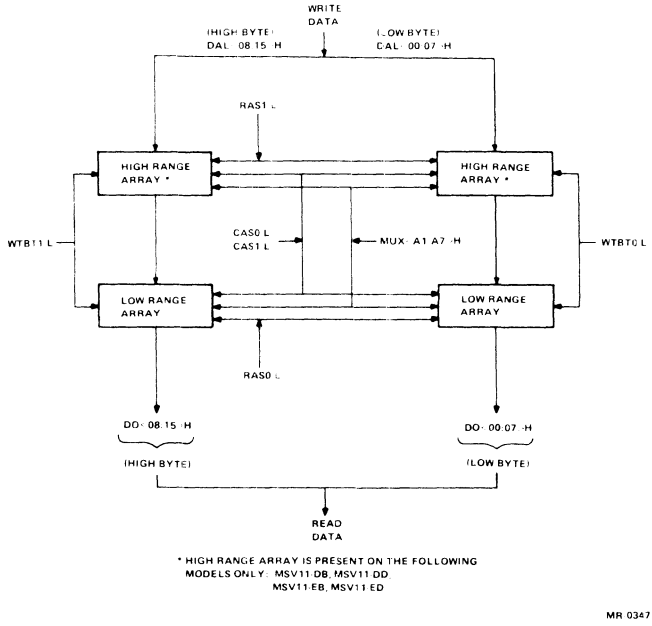


Figure 3 Memory Array

Fourteen address bits are required for 16K by 1 bit RAM ICs, and 12 address bits are required for 4K by 1 bit RAMs. The required 12- or 14-bit address is multiplexed over 6 or 7 address lines [MUX (A1:A7)H] to all RAM ICs that comprise the memory array. Addressing is controlled by column address strobe (CAS0 L and CAS1 L) and row address strobe (RAS0 L and RAS1 L) signals.

Addressing Logic

Addressing logic (Figure 4) receives addresses from the LSI-11 bus and produces address bits and control signals when the received address is for a memory location on the module. The user configures a starting

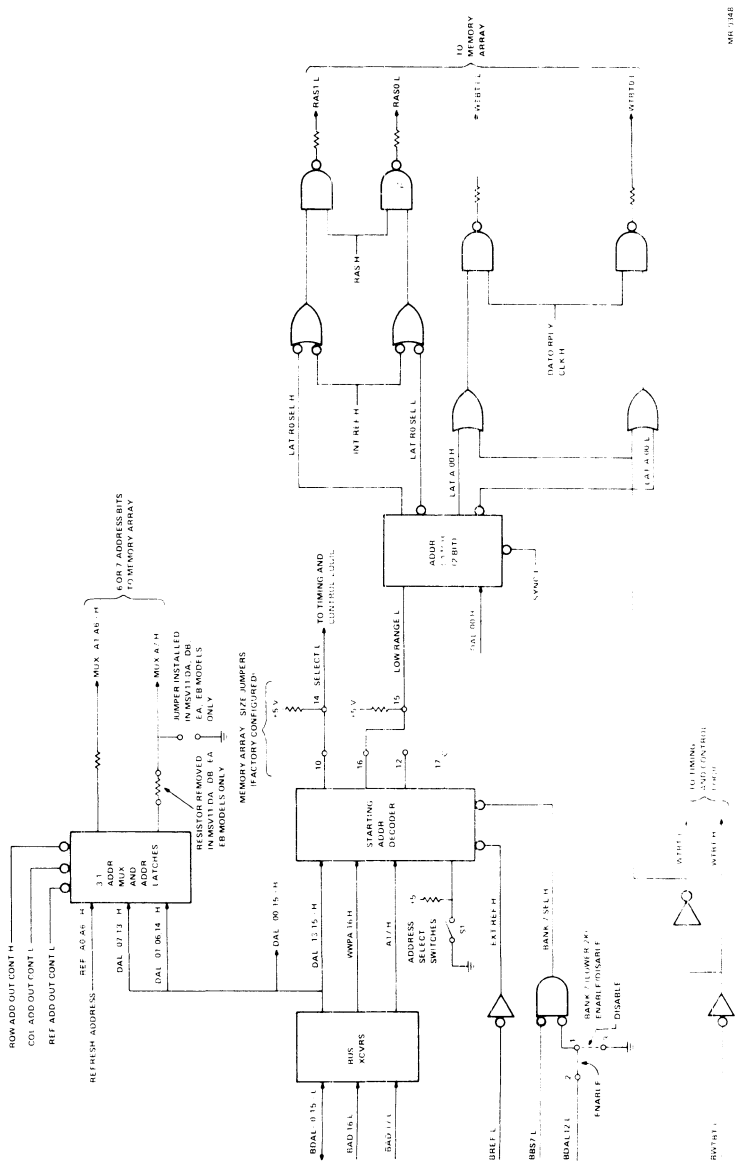


Figure 4 Addressing Logic

address (described in Table 1) that defines the lowest address in the module's range. When an address is received that resides in the module's user-configured range, SELECT L goes active. SELECT L is produced by decoding address bits DAL (13:15) H and the starting address configured by S1–S5. Memory array size jumpers select the appropriate SELECT L and LOW RANGE L decoder ROM outputs, depending on MSV11-D or MSV11-E model; these jumpers are factory-configured and normally should not be changed. SELECT L initiates the memory cycle in the timing and control logic. LOW RANGE L controls selection of RAS0 L or RAS1 L signals that select the low range array for all models, or the high range array when addressed on MSV11-DB, -DD, -EB, and -ED models.

The starting address decoder is always inhibited during external refresh operations; EXT REF H goes low during normal memory access operations.

The upper 4K address space in all systems is normally reserved for peripheral devices. However, the user can enable the use of the lower 2K portion of bank 7 by installing a jumper. When bank 7 is not enabled, BBS7 L is inverted by a bus receiver producing BANK 7 SEL H; the high signal inhibits the starting address decoder ROM and no active outputs are produced. When the lower 2K portion of bank 7 is enabled, a jumper on the input of the BBS7 L bus receiver is reconfigured to inhibit the bus receiver when BDAL 12 L is high (the lower 2K portion). Thus, BANK 7 SEL H will go high only when an address resides in the upper 2K portion of bank 7 and inhibits memory address decoding.

MSV11-D and MSV11-E models will not respond to external refresh signals, only to "on-board" refresh described in the paragraph entitled "Memory Refresh." When the externally generated BREF L signal is asserted, EXT REF H goes high and inhibits the starting address decoder ROM.

Timing and Control Logic

Circuits comprising timing and control logic are shown in Figure 5. Signal sequences for DATI, DATO(B), DATIO(B), and refresh cycles are shown in Figures 6 through 9, respectively.

The major portions of timing and control functions are contained in the timing and refresh arbitration logic (Figure 5). Basic timing for any memory cycle is produced by a tapped delay line and appropriate gating logic. Additional logic functions arbitrate refresh cycles, produce control signals for the memory array, addressing logic, and parity logic functions, and generate appropriate BRPLY L signals during any memory access operation.

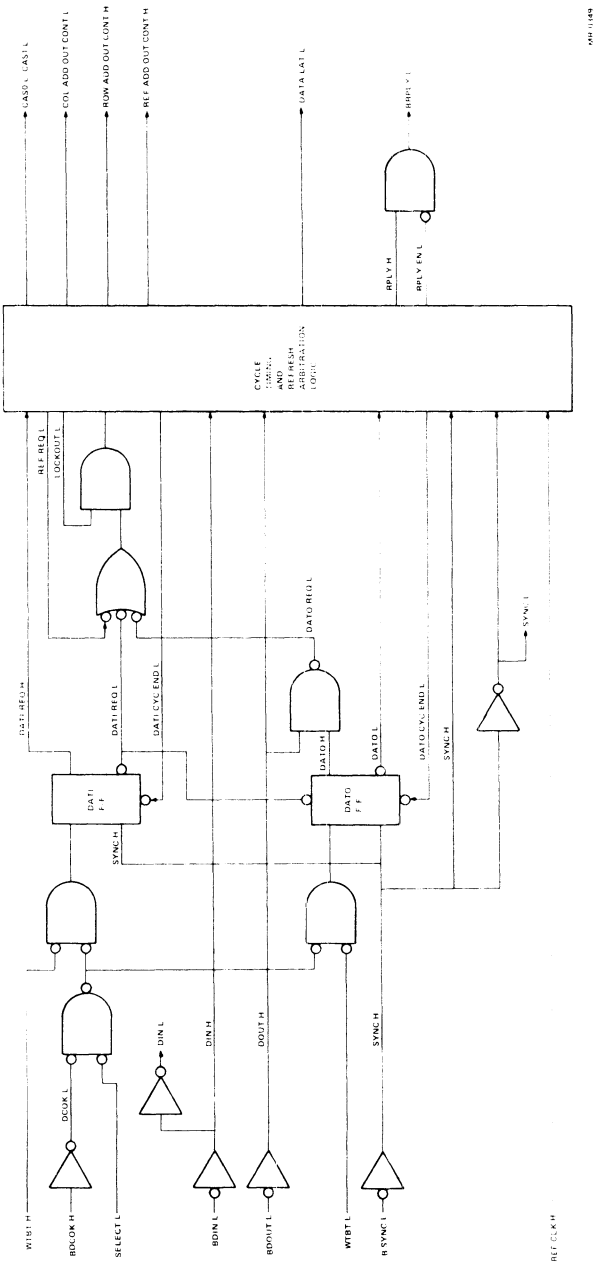


Figure 5 Timing and Control Logic

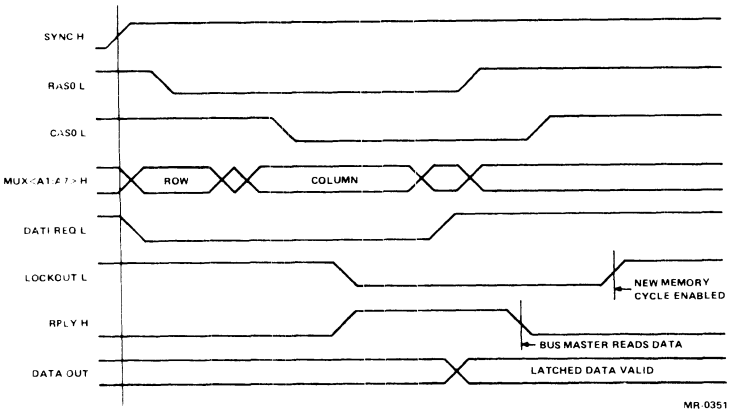


Figure 6 DATI Signal Sequence

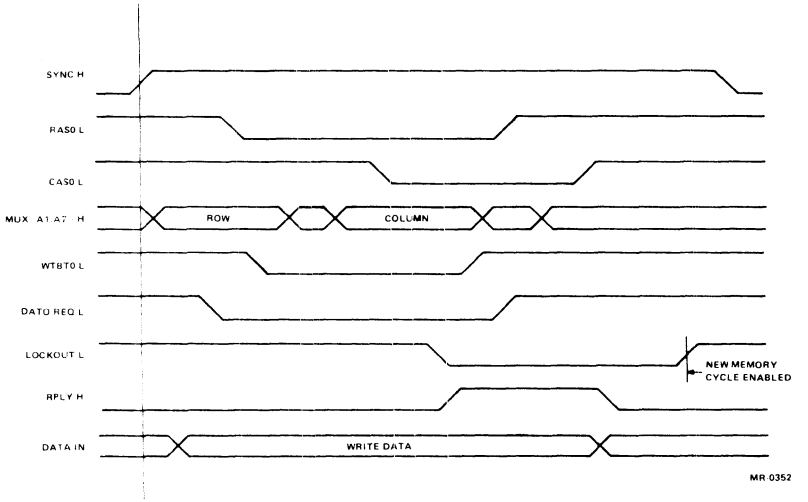


Figure 7 DATO(B) Signal Sequence

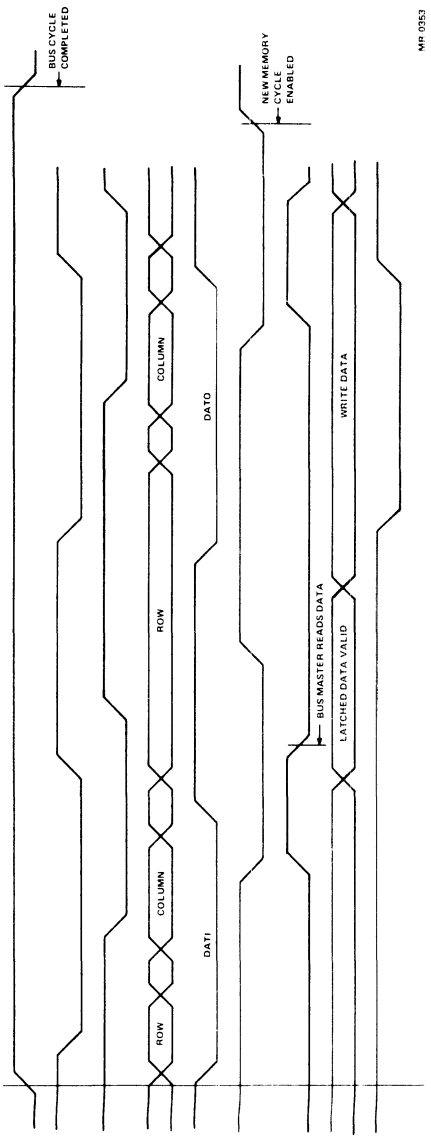


Figure 8 DATI0(B) Signal Sequence

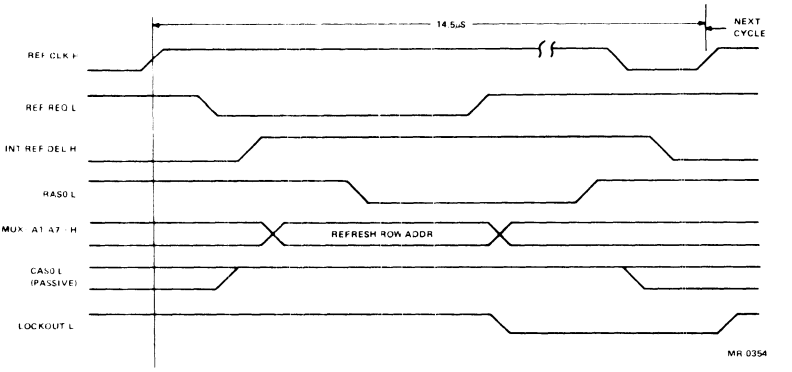


Figure 9 Memory Refresh Signal Sequence

A memory cycle (other than refresh) is initiated by the active SELECT L signal produced by addressing logic. The leading edge of SYNC H clocks either the DATI or DATO flip-flop to the set state, depending on the state of WTBT H and WTBT L; these two signals, produced by the LSI-11 bus BWTBT L signal, go active during the addressing portion of the cycle only when a DATO(B) cycle is in progress; DATO H enables DATA REQ L when DOUT H goes active (high). The appropriate DATI REQ L or DATO REQ L signal is ORed with REF REQ L, producing a high signal that initiates the timing sequence.

If a refresh cycle is in progress when the DATI, DATO(B), or DATIO(B) cycle is initiated, the refresh operation is first completed before continuing the memory access operation; LOCKOUT L goes active during any cycle timing sequence and inhibits the new request from starting another cycle until the present cycle has been completed. However, if a memory access cycle is initiated (addressing portion completed) and a refresh cycle request occurs, refresh arbitration logic delays the start of the memory access cycle approximately 100 ns. If a refresh conflict occurs (refresh wins), the refresh cycle will be first completed and add approximately 575 ns to the DATI or DATO(B) cycle time. If memory has been accessed (LOCKOUT L goes passive), a refresh cycle can be initiated although the bus cycle "handshaking" may not have been completed.

A DATIO(B) bus cycle is similar to a DATI cycle followed by a DATO(B) cycle; however, only the addressing portion of the cycle prior to the DATI portion occurs, according to LSI-11 bus protocol.

Write-byte operations (DATOB or the DATOB portion of DATIOB cycles) are controlled by the bus BWTBT L signal and the addressing logic. The timing and control functions are exactly the same for write byte or write word operations.

Memory Refresh

Memory refresh request logic is shown in Figure 10. A 14.5 μs refresh clock operates the refresh request time to allow completion of 128 refresh cycles during any 2 ms period. A refresh address counter increments once on each refresh cycle, producing the current refresh row address. Sequential row addresses are thus refreshed, completing all 128 rows within 2 ms for 16K by 1 bit memory integrated circuits, or 64 rows within 1 ms for 4K by 1 bit memory integrated circuits.

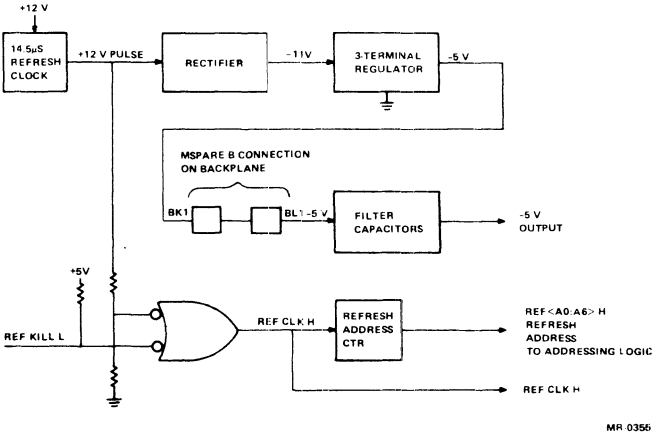


Figure 10 Refresh Logic and Charge Pump Circuit

Charge Pump Circuit

The charge pump circuit (Figure 10) produces −5 Vdc for the memory array. Input power is obtained from the +12 V system or battery backup power applied via the refresh clock. The resulting 12 V 14.5 μs refresh clock pulse is applied to a rectifier circuit which produces a −11 Vdc (approximately) output. A 3-terminal regulator then produces the required regulated −5 Vdc.

Note that the –5 V is applied to the filter capacitors via MSPAREB backplane pins. This is done for manufacturing test purposes. These pins are connected on all LSI-11 backplanes as shown on the figure. If nonstandard backplanes (user-supplied) are used, be certain that these pins are connected.

MSV11-E Parity Logic

MSV11-E parity logic functions are shown in Figure 11. The basic functions include a parity generator for memory write data, a 2-bit memory array, a parity detector, and a latch circuit. The parity generator produces two parity bits, one for each main memory byte. Address and control signal (not shown) lines are identical to those applied to the main memory array. When any main memory location is read, the corresponding

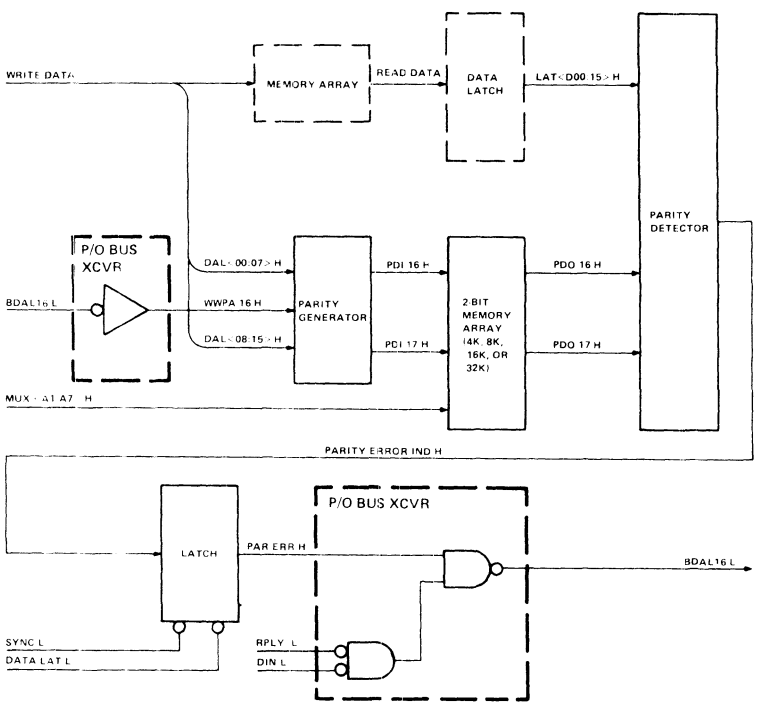


Figure 11 Parity Logic

parity memory location is read. Parity bits are checked by the parity detector and the result is stored in the output latch. If a parity error is detected (PAR ERROR IND H is active), PAR ERR H is gated onto the BDAL 16 L bus line. The processor reads the error during the memory read (DATI) cycle and responds accordingly.

MSV11-E memory modules respond to bus master devices by delaying BRPLY L assertion to accommodate the parity generator and parity detector logic. This timing is jumper-selected (factory-configured) and should not be changed.

Parity logic functions are tested when running memory diagnostics by writing incorrect parity bits. The processor forces this condition during a DATO(B) cycle by asserting BDAL 16 L during the output data transfer portion of the bus cycle. BDAL 16 L is received, inverted to produce "write wrong parity" (WWPA 16 H), and applied to the parity generator, forcing it to store incorrect parity bits. The error is then detected by subsequent memory read cycles.

LSI-11 processors do not support the parity implementation used on the MSV11-E. However, the user may implement logic to use the PAR ERR signal that is gated onto the BDAL 16, and to assert it for testing the parity function. A recommended method could be a module that clocked BDAL 16 on the trailing edge of DIN. Any time BDAL 16 is asserted, a parity error has occurred. The user can then cause an interrupt, increment a counter, etc. Note that the instruction execution cannot be aborted under this scheme, as is the normal procedure when detecting a parity error.

REV11-A DMA REFRESH, BOOTSTRAP/TERMINATOR
REV11-C DMA REFRESH, BOOTSTRAP

GENERAL

The REV11-A DMA refresh, bootstrap/terminator module consists of DMA refresh circuits, a bootstrap ROM, and 120-ohm termination circuits. The REV11-C is similar to the REV11-A, but does not have the 120-ohm termination circuits.

FEATURES

- Dynamic MOS memory refresh
- ROM programs for booting paper tapes, RXV11 floppy disks, and RKV11 cartridge disks
- ROM diagnostics for CPU and memory
- 120-ohm LSI-11 bus terminations (REV11-A only)

SPECIFICATIONS

Identification	M9400-YA (REV11-A) M9400-YC (REV11-C)
Size	Double
Power	+5 V ± 5% at 1.64 A (REV11-A) +5 V ± 5% at 1.0 A (REV11-C)
Bus Loads	
AC	2.2
DC	1

FUNCTIONAL DESCRIPTION

General

The REV11 modules provide the following functional operations: DMA refresh for volatile semiconductor memories; bootstrap programs for paper tape, the RXV11 floppy disk system, and the RKV11 cartridge disk system CPU and memory diagnostics; and 120-ohm terminations required for the LSI-11 bus lines. Only the REV11-A has the terminations

DMA Refresh Logic

General – DMA refresh logic consists of the three main functions shown in Figure 1. Arbitration logic requests the I/O bus once every 30 μs (approx) and completes the required DMA signal sequence with the processor. When it becomes bus master, it enables the bus control logic to execute a single refresh BSYNC L/BDIN L bus transaction, simultaneously refreshing one row in all dynamic MOS memory chips contained in the system. The refresh address logic places a 6-bit memory chip "row" address on the BDAL 1–6 lines during the addressing portion of the I/O bus cycle. Once the cycle has been completed, the row address is incremented by one for the next refresh cycle, and the I/O bus is released. The actual refresh transaction for one row address takes approximately 1.2 μs. Each dynamic MOS memory chip contains 64 row addresses. Hence, the DMA refresh logic is capable of refreshing all dynamic MOS memory contained in the system within the required 2 ms (maximum) period (i.e., 64 rows X 30 μs between refresh bus cycles = 1.92 ms).

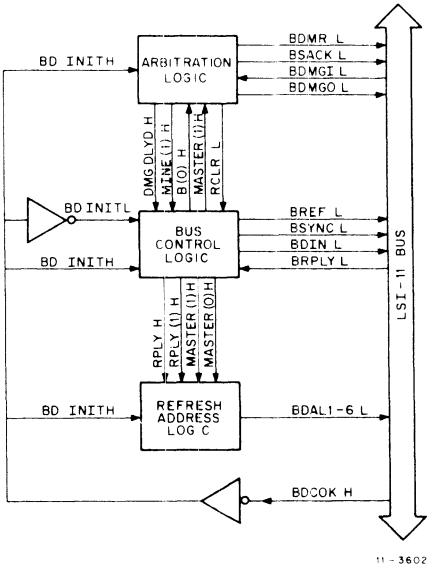


Figure 1 DMA Refresh Logic

Arbitration Logic – Arbitration logic is shown in Figure 2; timing is shown in Figure 3. The DMA refresh sequence is initiated once every 30 μs by a clock oscillator. GRAB BUS H is the clock output signal. It is inverted and gated with a ground (enable) signal, supplied via refresh disable jumper W2, to produce the REQ H signal. REQ H clocks the DMR flip-flop to the set state, producing active R PENDING (1) H and BDMR L signals. The processor arbitrates the DMA request and responds by asserting the daisy-chained BDMGI L signal when the present bus cycle is completed. BDMGI L is received and inverted, producing the active DMGR H signal. The leading edge of this signal clocks the active R PENDING (1) H signal into the Mine flip-flop, causing it to go the set state. MINE (1) H goes high and MINE (0) H goes low, inhibiting the BDMGO L signal logic.

When not requesting the bus for a refresh bus transaction, the arbitration logic passes BDMGI L signals to its BDMGO L output so that the daisy-chained signal continuity is maintained to the lower priority device requesting the bus. The high MINE (0) H signal enables generation of a delayed BDMGO L signal. The 100 ns delay ensures that the Mine flip-flop has sufficient time to go to the set state, if the DMA refresh option is requesting the I/O bus.

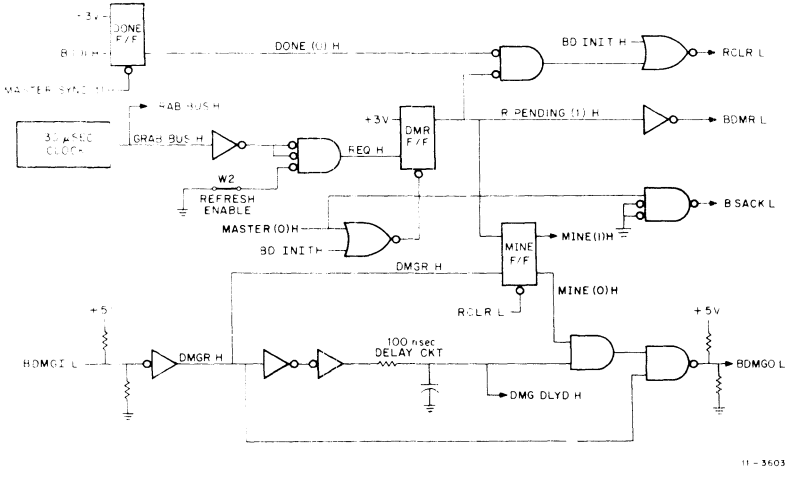


Figure 2 Arbitration Logic

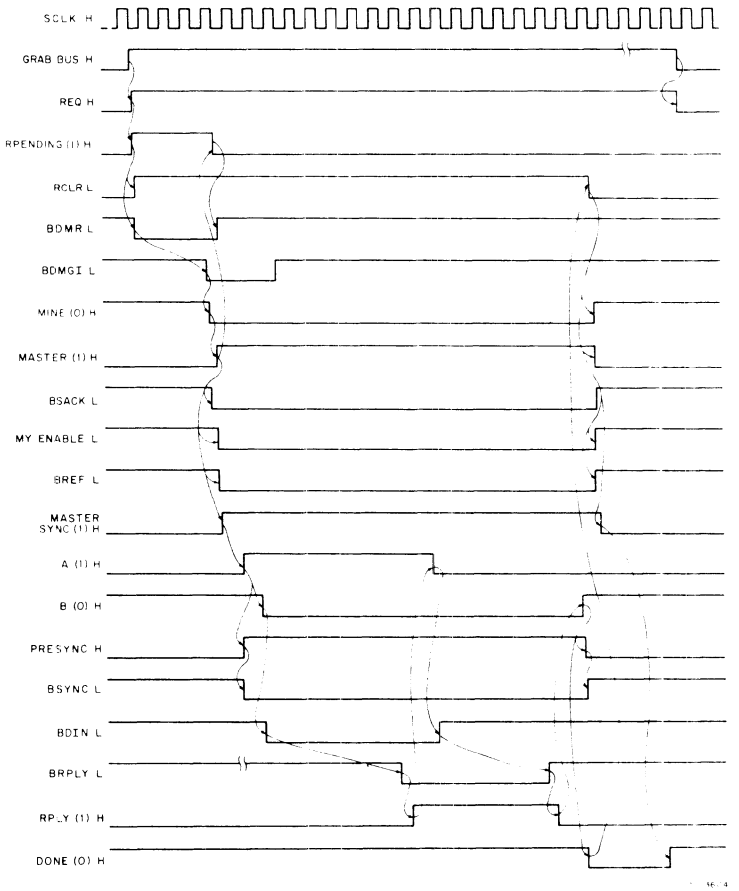


Figure 3 DMA Refresh Logic Signal Sequence

Bus Control Logic – The bus control logic operation is initiated when the arbitration logic asserts the MINE (1) H and DMG DLYD H signals. These signals are gated with passive SYNC H and RPLY H signals to produce the MCLK H signal, as shown in Figure 4. MCLK H clocks the master flip-flop to the set state; MASTER (1) H goes high and MASTER (0) H goes low.

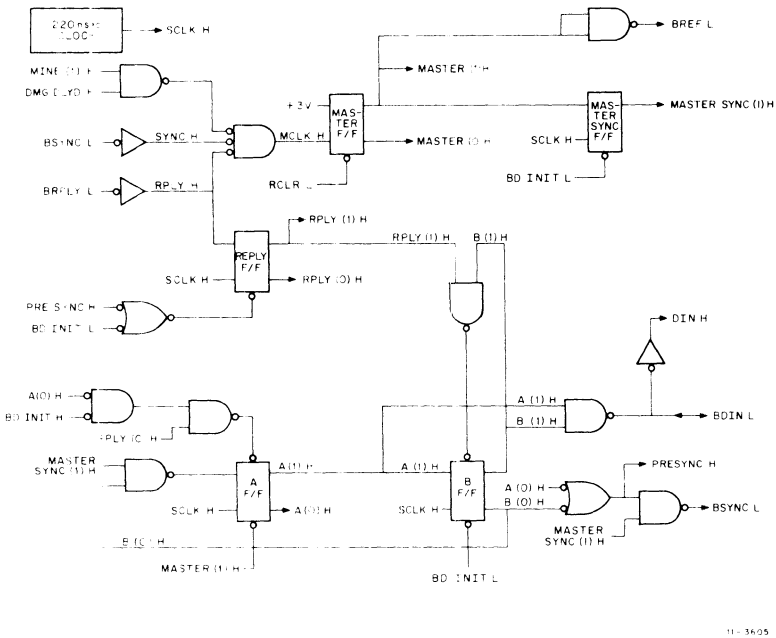


Figure 4 Bus Control Logic

The active MASTER (1) H signal is applied to the arbitration logic (Figure 2) where it generates an active BSACK L signal. The active BSACK L signal informs the processor that a DMA device has become bus master, and the DMA grant sequence is completed. MASTER (1) H also clears the Mine flip-flop; R PENDING (1) H goes low, negating BDMR L and enabling the RCLR L logic. (RCLR L is generated later in the sequence when the done flip-flop becomes set.)

MASTER (1) H is inverted, producing the active BREF L signal (Figure 4). BREF L causes all dynamic MOS memories contained in the system to be simultaneously addressed during the refresh bus transaction, and it remains active for the duration of the refresh operation. MASTER (1) H is applied to refresh address logic where it produces the MY ENABLE L signal. This signal enables low byte BDAL (0–7) bus drivers, and row address bits are placed on the BDAL bus.

The sequence of operations involving the bus control logic is controlled by sequence flip-flops A and B. (Note that the A flip-flop is shown

inverted.) Operations are synchronized by the positive-going leading edge of the 220 ns clock SCLK H signal, as shown in Figure 3. On the SCLK H leading edge following the active MASTER (1) H signal, the master-sync flip-flop clocks to the set state, producing the active MASTER SYNC (1) H signal. The MASTER SYNC (1) H and B (0) H signals are gated to produce a low signal that clocks sequence flip-flop A to the set state on the following SCLK H pulse. The RPLY (0) H signal is initially high since the refresh bus transaction with system memory has not been completed. Thus, the high RPLY (0) H, passive (low) BDINIT H, and A (0) H signals are gated, producing a low signal that keeps the A flip-flop set until the RPLY (0) H signal goes low. The low A (0) H signal is ORed with B (0) H to produce the PRE SYNC H signal. PRE SYNC H and the active MASTER (1) H signal are gated by the BSYNC L bus driver, causing that bus signal to become asserted.

On the third SCLK H leading edge, the B sequence flip-flop clocks to the set state, producing the high B (1) H and low B (0) H signals. B (1) H and A (1) H are gated by the BDIN L bus driver, causing that signal to become asserted. Bus control logic remains in this state until system memory responds to the refresh transaction by asserting BRPLY L. (This may occur one or more SCLK H signals later, depending on system delays.)

BRPLY L is received and inverted, producing RPLY H. On the next leading edge of SCLK H, the reply flip-flop clocks to the set state, and high RPLY (1) H and low RPLY (0) H signals are produced. The low RPLY (0) H signal inhibits the A sequence flip-flop clear gate, and the flip-flop clocks to the reset state on the following SCLK H pulse. A (1) H goes low, inhibiting the BDIN L bus driver, and terminating that signal. RPLY (1) H and B (1) H are ANDed to produce a low signal which presets the B sequence flip-flop. This prevents resettling the B flip-flop as long as RPLY (1) H is in the active state.

System memory responds to the passive BDIN L signal by terminating the BRPLY L signal. On the next SCLK L pulse, the reply flip-flop clocks to the reset state; RPLY (1) H goes low and RPLY (0) H goes high. The following SCLK L pulse then clocks the B sequence flip-flop to the reset state and B (1) H goes passive; PRE SYNC H and BSYNC L go to the passive states.

Low R PENDING (1) H and DONE (0) H signals are gated to produce the active (low) RCLR L signal (Figure 2) which clears the Mine flip-flop; BSACK L and MINE (0) H signals go high. RCLR L also clears the master flip-flop in the bus control logic (Figure 4), causing BREF L to go passive and MY ENABLE L in the refresh address logic (Figure 5) to go passive, inhibiting the BDAL bus drivers. On the next SCLK H pulse, MASTER SYNC (1) H goes passive (Figure 4), and the refresh bus transaction is

completed. The passive MASTER SYNC (1) H signal resets the done flip-flop, enabling the next refresh operation.

Refresh Address Logic – Refresh address logic is shown in Figure 5. A 6-bit binary counter produces the six row address bits that are placed on the BDAL bus during the addressing portion of the refresh bus transaction. The low MASTER (0) H signal enables the counter output bits during the operation. Upon completing the transaction, RPLY (1) H goes passive, inhibiting the CK L gate; the CK L signal goes high, incrementing the 6-bit binary counter by one count. Hence, on each successive refresh operation, a new row address is used.

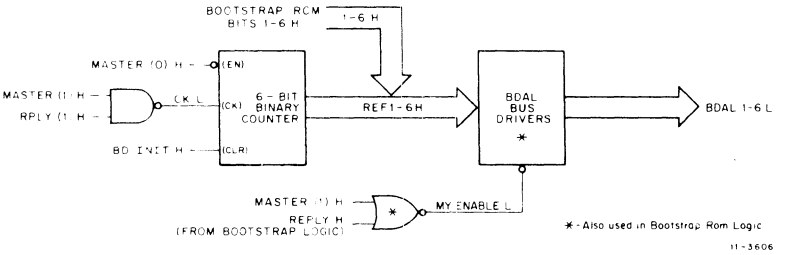


Figure 5 Refresh Address Logic

Initialization – DMA refresh logic initialization is controlled by the BDCOK H signal. Initialization occurs only during power-up or power-down conditions (when BDCOK H is in the low passive state). All flip-flops (except the done flip-flop) are initialized by either the BD INIT H (inverted-passive BDCOK H), BD INIT L (inverted BD INIT H), or RCLR L (gated BD INIT H) signals.

Bootstrap ROM/Diagnostic

Addressing – The module includes a 512 X 16-bit ROM array that is addressed in two 256-word segments. These address segments are reserved for REV11 options and reside in the upper 4K address bank, normally used for peripheral device addresses. The reserved addresses range from 165000–165776 and 173000–173776. A power-up mode, which will cause the processor to access ROM location 173000 upon power-up, is jumper-selectable on the processor module.

Circuits associated with bootstrap ROM logic are shown in Figure 6. Wired inputs to an address comparator circuit reserve the ROM

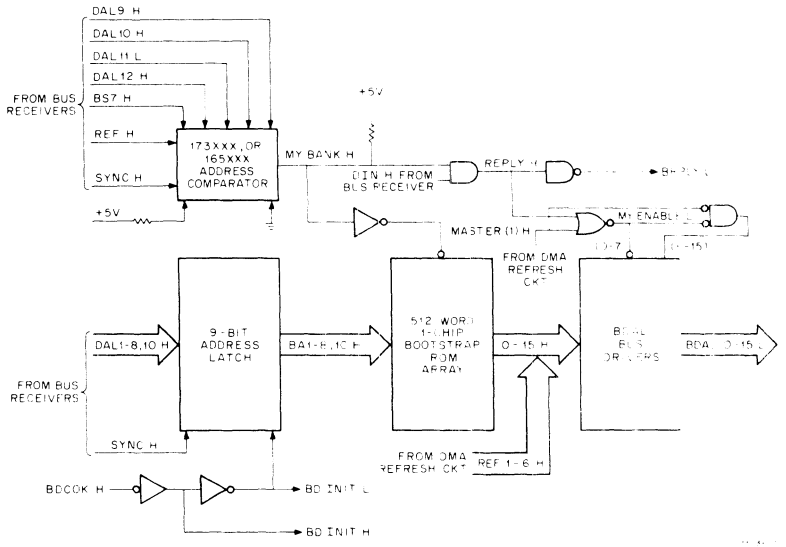


Figure 6 Bootstrap ROM Logic

addresses. The address comparator responds to any of the reserved addresses during the addressing portion of a bus I/O cycle by generating an active MY BANK H signal. MY BANK H is ANDed with DIN H to produce a BRPLY H signal when the ROM word is read by the processor. MY BANK M is also inverted and applied to the ROM array chip enable inputs.

DAL1-8 H and DAL10 H address bits are stored in the 9-bit address latch on the leading-edge of SYNC H. The stored BA1-8 H and BA10 H address bits select the desired word location to be read within the two 256-word address segment detected by the address comparator.

Data Transfer – After the addressing portion of the bus DATI cycle has been completed, the ROM 0-15 H data becomes available on the BDAL bus driver inputs. Note that the ROM array consists of four 512 X 4-bit ICs. Hence, the four 4-bit outputs comprise the 16-bit LSI-11 word. MY ENABLE L strobes the 16-bit word onto the I/O bus in response to the DIN H signal. The processor then receives the data, terminates BDIN L, and the bootstrap ROM logic responds by terminating BRPLY L and inhibiting the BDAL bus drivers.

Initialization – The bootstrap ROM logic is initialized only when BDCOK H goes false. This condition occurs during a power failure and produces active BD INIT H and BD INIT L signals. These signals clear the 9-bit address latch and circuits contained in the DMA refresh logic. The option does not respond to the LSI-11 bus BINIT L signal.

Terminations (REV11-A Only)
Each bus signal line terminates with two resistors as shown in Figure 7. These termination resistors are generally contained in a 16-pin, dual-in-line package which is identical to an IC package. Each package contains 14 termination pairs. The values used are shown in the figure. Daisy-chained grant signals are terminated and jumpered. BIAKI L is jumpered (with etch) to BIAKO L, and BDMGI L is connected to BDMGO L via factory-installed jumper W1.

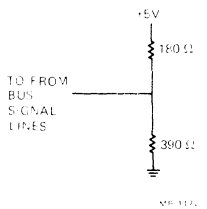


Figure 7 Typical 120-Ohm Bus Termination

USING REV11-A AND REV11-C COMMANDS

General – The REV11 hardware option contains programs stored in read-only memory. The normal starting address for the programs is 173000. When started at this location, the program that is executed is a non-memory modifying processor test. If no errors are detected, the program outputs a dollar-sign ($) for display on the console device. This character is the prompt character for the operator to enter a command.

The starting address can be entered and program operation started either manually, using the console ODT go command, or automatically during power-up. Automatic operation is accomplished by selecting power-up mode 2 by appropriately configuring jumpers on the processor module. The normal power-up response for this mode results in the console device displaying the $ prompt character instead of the @ console ODT prompt character.

Unsuccessful execution of the non-memory modifying processor test program results in the $ prompt character not being displayed. Instead, the program hangs (branch to self) when a sequence of instructions does not execute properly, or the processor halts due to a double bus error; a halt normally results in the console terminal displaying the PC contents (the address of the halt +2), followed by the console ODT prompt character @.

REV11-A and REV11-C Command Set – Once the $ prompt character is displayed, the operator can enter one of the commands described in Table 1. Note that in the command examples, characters printed by the program are shown underlined; characters not underlined are entered by the operator. Command inputs to the program can either be upper- or lowercase characters. If an invalid command is entered following the $ prompt character, the program responds by displaying ? after the invalid command and a new $ prompt character on a new line. For example, program response to the invalid "XJ" command is shown below:

$ XJ ?

$

NOTE

The <CR> function in Table 1 represents the nonprintable character "carriage return" that is recognized as an execute command.

Table 1 REV11 ROM Program Commands

Command	Function
OD	ODT (Halt). This allows the operator to examine and/or alter memory and register locations via the console device. Control can be returned to the REV11 program by entering the ODT P (proceed) command if the PC has not been altered, and the console device will display the $ prompt character. If the PC has been altered, the operator can start program execution by entering the starting address 165006 and the G (go) commands as follows: @ 165006G $ The processor responds by displaying the $ prompt character on a new line and another REV11 command can be entered.

Table 1 REV11 ROM Program Commands (Cont)

Command	Function
XM<CR>	Memory diagnostic program. After successfully completing the diagnostic, the prompt character ($) is displayed on the console device. Errors are indicated by the following displays on the console device. 1. 173732 @ This is an address test error. The expected (normal) data is in R3 and the invalid data is in the memory location pointed to by R2. If desired, continue diagnostic program execution by entering the ODT P command. 2. 173756 @ This is a data test error. The expected (normal) data is stored in R3 and the invalid data is in the memory location pointed to by R2. If desired, continue diagnostic program execution by entering the ODT P command. 3. 000010 @ A time-out trap has occurred in testing memory locations outside of the first (lowest) 4K memory. 4. nnnnnn @ A time-out trap has occurred in testing memory locations within the first 4K memory. The nnnnnn displayed is an indeterminate number.

Table 1 REV11 ROM Program Commands (Cont)

Command	Function
	The actual test consists of an address test and a data test. The address test first writes all memory locations with addresses; it then reads and verifies the addresses. The data test consists of two parts. An "all 1s" word is first walked through all memory locations, which are initially 0. The second part consists of walking an "all 0s" word through all memory locations which are all 1s.
XC<CR>	Processor diagnostic program. This is a memory-modifying instruction test. Successful execution of the diagnostic program results in the prompt character ($) being displayed on the console device. Errors are indicated by: 1. The program halting when an instruction sequence is not correctly executed 2. The program halting in the trap vector area for various traps.
AL<CR>	Absolute loader program, normal (absolute address) loading operation. Entering AL<CR> specifies that a paper tape is to be loaded via the console device (CSR address = 177560). However, another device can be specified by entering the appropriate CSR address. For example, to load paper tapes in absolute loader format via a device whose CSR address is 177550, enter the following command $ AL177550<CR> The program responds by first executing the memory-modifying CPU instruction test and memory test (refer to the XC and XM commands). Successful test execution results in execution of the absolute loader program.

Table 1 REV11 ROM Program Commands (Cont)

Command	Function
	A successful program load is indicated by one of the following three things. 1. The console device displays: 165626 @ 2. The loaded program automatically starts execution. 3. Absolute loader errors are: • Checksum error, with the program halting and producing the following display: 165534 @ • Program halts in the trap vector area for traps other than a time-out trap. • Time-out trap occurs, causing the display of $ on a new line on the console device. This program can be restarted without first executing the diagnostic programs. This is accomplished as follows. 1. Load R4 with 165414 (AL starting address). 2. Load the highest available memory address into R5. (For example, if the system contains 4K of read/write memory, load R5 with 17776.) 3. Start the program at 165242.

Table 1 REV11 ROM Program Commands (Cont)

Command	Function
AR<CR>	Absolute loader program, relocated loading operation. When this command is entered, the memory modifying CPU instruction test and memory test are automatically first executed (refer to the XC and XM commands), followed by the absolute loader program. Successful execution of the tests results in the program halting with the following console display: 165412 @ The operator must then enter the appropriate "software switch register" contents in R4. To select relocated loading, which uses an address (bias) contained in the software switch register, enter the following commands: @ R4/ xxxxxx nnnnnn<CR> @ P The value nnnnnn is a relocation value selected by the operator as directed in the *PDP-11 Paper Tape Software Handbook* (DEC-11-XPTSA-B-D). Observe that the least significant "n" value entered must be an odd number; this sets the software switch register (R4) bit 0 to a logical 1, selecting the relocated loading mode. Note that the program being loaded must be in position independent code (PIC) format for relocated loading. When large programs are contained on more than one tape, the program halts at the end of the first tape. Install the second tape in the reader and enter a "1" in R4 using the ODT command shown below; resume loading by entering the P command. @ R4/xxxxxx 1 <CR> @ P

Table 1 REV11 ROM Program Commands (Cont)

Command	Function
	The six octal digits (xxxxxx) are the present contents of R4. Entering a value of 1 selects relocated loading for the next program tape, starting at the address following the end of the previous load operation. The P command allows the absolute loader program execution to continue the loading process once the software switch register value has been entered. A successful program load is indicated when the loaded program automatically starts execution, or the console device displays: 165626 @ Absolute loader errors are as described for the AL command. This program can be restarted without first executing the diagnostic programs. This is accomplished as follows. 1. Load R4 with 165406 (AR starting address). 2. Load the highest available memory address in R5. (For example, if the system contains 4K of read/write memory, load R5 with 17776.) 3. Start the program at 165242.
DX<CR> or DXn<CR>	RXV11 floppy disk system bootstrap. Entering the DX<CR> command starts the memory-modifying CPU instruction test and memory test execution. (See the XC and XM commands.) Successful test execution results in execution of the bootstrap program for disk drive 0, the system disk. Otherwise, specify the drive number (n) as 0 (drive 0) or 1 (drive 1).

Table 1 REV11 ROM Program Commands (Cont)

Command	Function
	Floppy disk bootstrap errors are:
	1. The program halts and the console device displays 165316 @ indicating that the device done flag in the RXV11 interface was not set within the required time (approx. 1.3 seconds). The bootstrap can be restarted by entering the P command; the $ is then displayed on the console device and the bootstrap command can be entered.
	2. The program halts and the console displays: 165644 @ indicating that a bootstrap error occurred. The RXV11 error register contents are stored in R2. By examining the contents of R2 and using the information in this handbook on the RXV11, the exact nature of the error can be determined. Examine the contents of R2 (nnnnnn) as follows: @ R2/nnnnnn<CR> @ P $ After examining R2, the bootstrap can be restarted by the P command; enter the desired bootstrap command immediately after the $ prompt character.

Table 1 REV11 ROM Program Commands (Cont)

Command	Function
	3. The program halts in the trap vector for traps; a time-out trap returns the program to the $ prompt character. If a time-out trap occcurs first, check for proper system cable connections and device interface module installation. Then, attempt to successfully bootstrap the system by again entering the desired bootstrap command. The bootstrap for disk drive 0 (DX) can be started without first executing the diagnostic programs. This is accomplished as follows. 1. Load R4 with 165264 (the DX bootstrap starting address). 2. Start the program at 165242.
DK<CR> or DKn<CR>	RKV11-D disk drive system bootstrap. Entering the DK command starts the memory-modifying CPU instruction test and memory test execution. (See the XC and XM commands.) Successful test execution results in execution of the bootstrap program for disk drive 0, the system disk. Otherwise, specify the drive number n as 0 (drive 0), 1 (drive 1), or 2 (drive 2). Disk bootstrap errors are: 1. The program halts and the console device displays: 165724 @ indicating that the device done flag in the RKV11-D interface was not set within the required time (approx. 1.3 seconds). The bootstrap can be started by entering the P command; the $ is then displayed on the terminal and the bootstrap command can be entered.

Table 1 REV11 ROM Program Commands (Cont)

Command	Function
	2. The program halts and the console displays 165644 @ indicating that a bootstrap error occurred. The RKV11-D error register contents are stored in R2. By examining the contents of R2 and using the information contained in the RKV11-D option description, the nature of the error can be determined. Examine the contents of R2 (nnnnnn) as follows: @R2/nnnnn<CR> @P $ After examining R2, the bootstrap can be restarted by the P command; enter the desired bootstrap command immediately after the $ prompt character. 3. The program halts in the trap vector for traps; a time-out trap returns the program to the $ prompt character. If a time-out trap occurs first, check for proper system cable connections and device interface module installation. Then, attempt to successfully bootstrap the system by again entering the desired bootstrap command.

RKV11-D RK05 DISK DRIVE CONTROLLER

GENERAL

The RKV11-D option consists of an RK05 disk drive controller, an LSI-11 bus interface module, and an RK05-J disk drive. The controller and the RK05-J disk drive form a mass storage system. Up to eight RK05-J or four RK05-F disk drives can be used with one RKV11-D controller. The RKV11-D/RK05 system is block-oriented but is capable of transferring from 1 to 2^{16} consecutive data words without reinitiation or processor intervention. The data transfers occur from the RKV11-D to the system memory by direct memory access (DMA), which does not require processor interruption and operates at maximum bus bandwidth.

The RKV11-D is housed in a rack-mountable, 48.2 cm (19-in) wide cabinet that is 8.9 cm (3-1/2 in) high. This cabinet houses four controller modules and an H780 power supply. A double-height bus control module plugs into the LSI-11 bus and provides the RKV11-D/LSI-11 interface. A sixth module terminates the RK05 drive bus (DR bus) at the last used RK05 disk drive. Each RK05 drive requires an M7700 module (Rev J or later), and a backpanel (Rev A or later). The RKV11-D is cabled to the first RK05 disk drive with a pair of 120-ohm, 40-conductor flat cables (70-09026-02). Two BC05L cables are used to connect the RKV11-D to the LSI-11 bus controller module. Eight versions of the RKV11-D system are available.

Option No.	Voltage	Controller	RK05-J	Cabinet*
RKV11-AA	115 V/60 Hz	Yes	Yes	No
RKV11-AB	230 V/60 Hz	Yes	Yes	No
RKV11-BA	115 V/50 Hz	Yes	Yes	No
RKV11-BB	230 V/50 Hz	Yes	Yes	No
RKV11-DE	115 V/60 Hz	Yes	Yes	Yes
RKV11-DF	230 V/60 Hz	Yes	Yes	Yes
RKV11-DH	115 V/50 Hz	Yes	Yes	Yes
RKV11-DJ	230 V/50 Hz	Yes	Yes	Yes

*The cabinet is an H967-M cabinet, 127.0 cm (50 in) tall, that provides 106.7 cm (42 in) of rack-mountable area (48.2 cm, 19 in). The RK05-J and the RKV11-D controller occupy 35.6 cm (14 in) of the rack area.

FEATURES

- 2.5 million byte storage is available in the RK05-J cartridge disk.
- 5 million byte storage is available in the RK05-F fixed disk.
- 20 million byte storage is available per system.

RKV11-D

- Up to eight RK05-J disk drives can be used with one RKV11-D controller.
- DMA data can be transferred to and from the LSI-11 bus.
- RK05-J and RK05-F disk drives can be operated from the same RKV11-D controller.
- RKV11-D controller can be mounted in a standard 48.2 cm (19 in) equipment rack, along with the disk drives.
- The RKV11-D controller has a self-contained power supply and its own status indicators.
- Only one double-height module slot of the LSI-11 bus is used.
- The LSI-11 bus is not extended.

SPECIFICATIONS

LSI-11 Bus Module

Identification	M7269
Size	Double
Power	+5 V ± 5% at 1.8 A
Bus Loads	
AC	1.9
DC	1

RKV11-D Controller

Input Voltage	
RKV11-DA	100–127 Vac, 50/60 Hz ± 1 Hz
RKV11-DB	200–254 Vac, 50/60 Hz ± 1 Hz
Input Power	140 W max
Power Supply	H780
Line Protection	
115 Vac	5 A fast blow fuse
230 Vac	2.5 A fast blow fuse

LSI-11 bus backplane signal from RKV11-D power supply	BPOKH (power supply AC LO) BDCOKH (Bus DC LO)
Module Complement	
M7254	Control/Status
M7255	Disk Control
M7256	Data Paths
M7268	Bus Adapter
M930	Drive Bus Terminator
M7269	Bus Control
Cables	Two 40-conductor flat 70-09026-02 (to first RK05 drive)
	Two 40-conductor flat BC05L (to LSI-11 bus interface)

CONFIGURATION

General

The RKV11-D/RK05 disk drive system can be configured with up to eight RK05-J disk drives daisy-chained on the drive bus (DR bus). Each disk drive must have an M7700 module of revision J or later. The M7700 module has a rotary switch that defines the logical disk drive DR bus position. The first disk drive on the DR bus is normally set to switch position 1 on the M7700 module and is designated as disk drive 0. The second disk drive would then be designated as drive 1 (switch position 2), and so on, up to the eighth disk drive (switch position 8). This configuration (Figure 1) may be varied as DR bus length allows. The maximum length of the DR bus is 15 m (50 ft). The DR bus must be terminated with the M930 module at the last RK05 on the bus.

Module Jumpers

The M7269 module has jumpers to configure the interrupt vector and device register addresses. The M7256, M7255, and M7254 modules have jumpers to configure certain RK05 disk drive functions. The jumpers on the M7269 module have been factory-configured for an interrupt vector of 220_8 and device addresses of 177400_8 through 177416_8. These addresses are the normal user addresses and should not be altered. Figure 2 shows the jumper locations for the interrupt vector and device address jumpers on the M7269 module. The interrupt vector and device address word formats are shown in Figures 3 and 4 and described in Table 1. Figures 5, 6, and 7 show the locations of the jumpers on the M7256, M7255, and M7254 modules, respectively.

These jumpers should not be changed by users using only RK05 disk drives on the REV11-D controller. For details on these module jumpers, refer to Field Maintenance Print Set MP00223. There are no jumpers on the M7268 module.

Table 1 Standard Assignments

Description	Mnemonic	Read/ Write	M7269 Module Address
Registers			
Drive Status	RKDS	R	177400
Error	RKER	R	177402
Control/Status	RKCS	R/W	177404
Word Count	RKWC	R/W	177406
Bus Address/Current Memory Address	RKBA	R/W	177410
Disk Address	RKDA	R/W	177412
Unused			177414
Data Buffer	RKDB	R (PIO)	177416
Interrupt			
Interrupt Vector	–	–	220

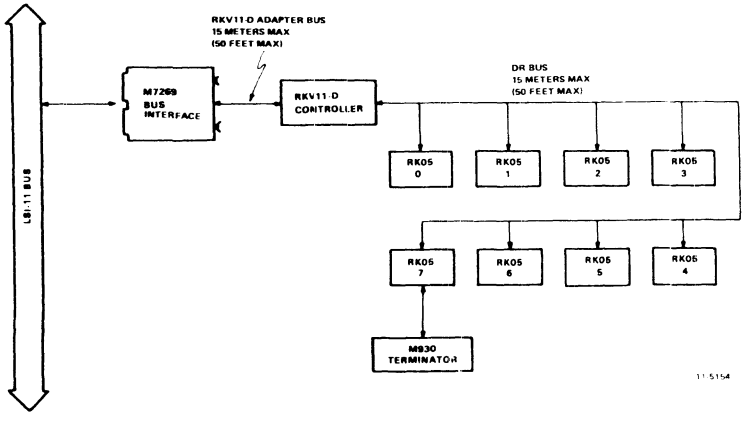


Figure 1 RKV11-D/RK05 System Configuration

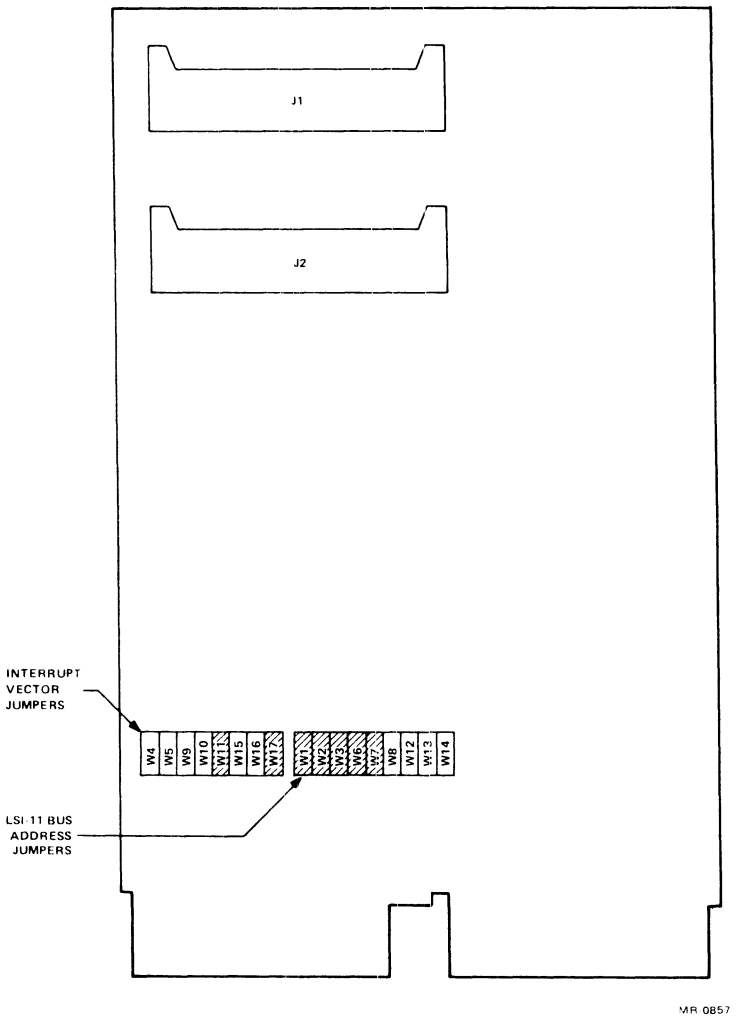


Figure 2 M7269 Module Jumpers

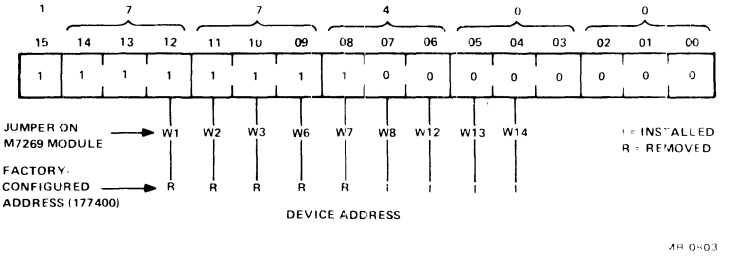


Figure 3 M7269 Device Address Format

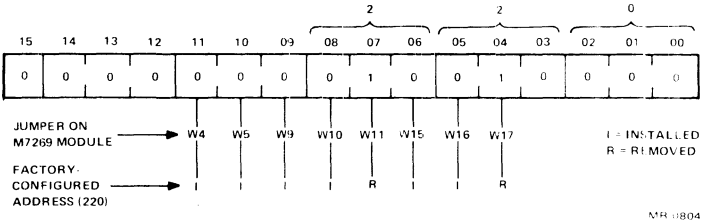
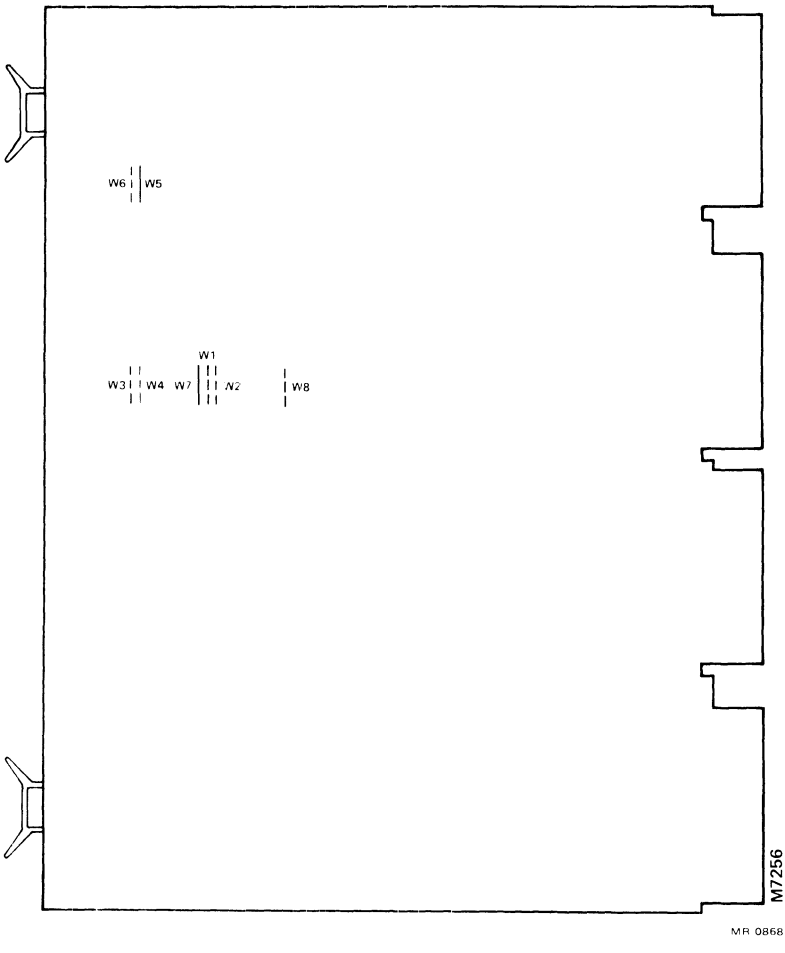
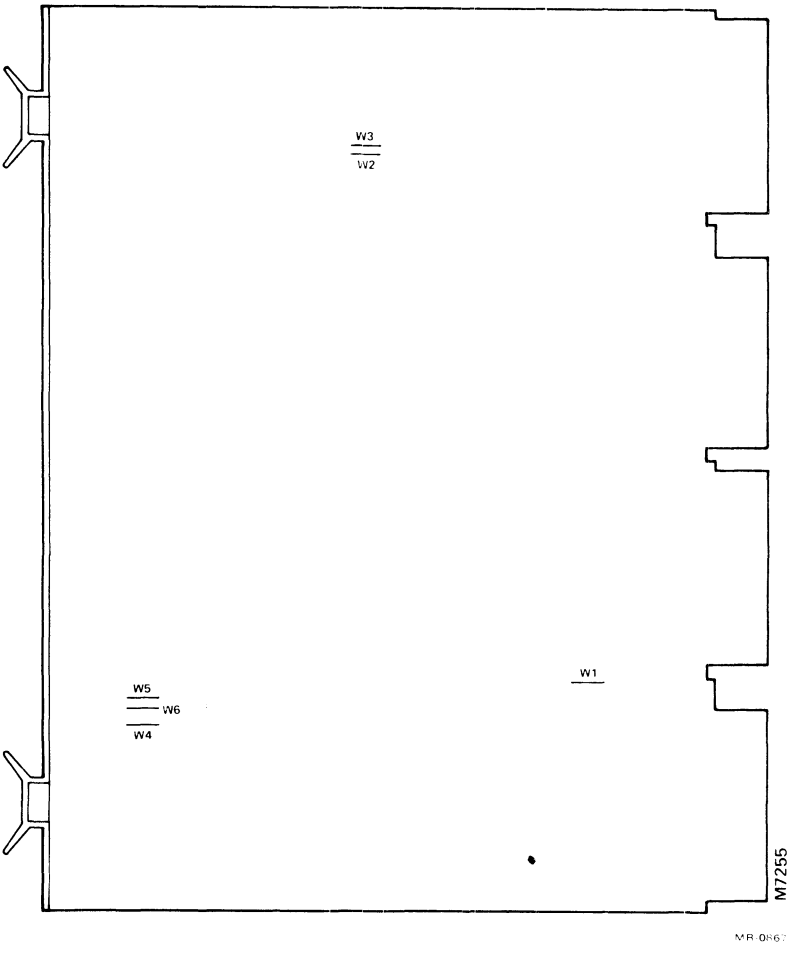


Figure 4 M7269 Interrupt Vector Format



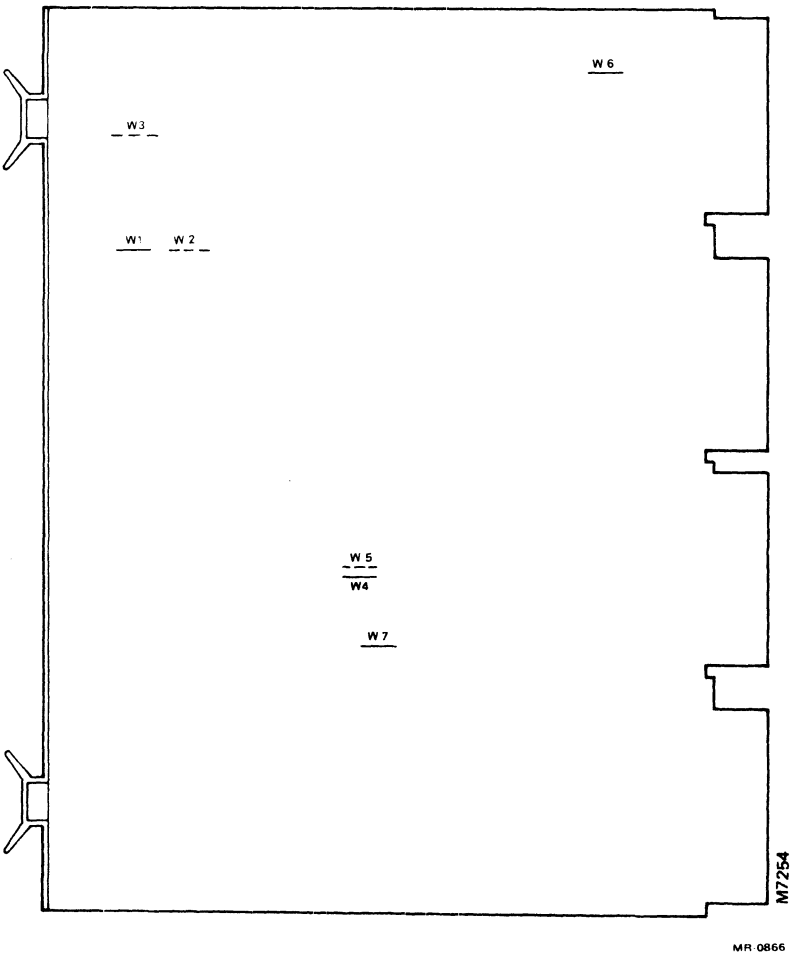
Factory Configuration:
W1, W3, W4, W6, W8 – REMOVED
W2, W5, W7 – INSTALLED

Figure 5 M7256 Jumper Locations and Configuration



Factory Configuration:
W1, W2, W6 – INSTALLED
W3, W4, W5 – REMOVED

Figure 6 M7255 Jumper Locations and Configuration



Factory Configuration:
W1, W4, W6, W7 – INSTALLED
W2, W3, W5 – REMOVED

Figure 7 M7254 Jumper Locations and Configuration

Module Utilization

Of the six modules supplied with the RKV11-D, four are installed in the RKV11-D controller backplane as shown in Figure 8. The M930 terminator module is plugged into the last RK05 disk drive on the DR bus, and the M7269 module is plugged into the LSI-11 bus. The M7269 is a double-height module. The RKV11-D is a DMA device. Priority of DMA devices on the LSI-11 bus is determined by the devices' electrical distance from the processor. The DMA device closest to the processor has the highest DMA priority.

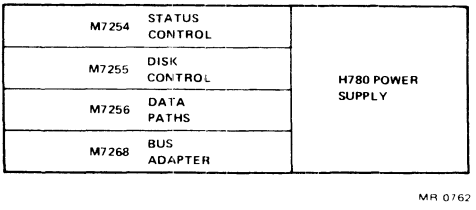


Figure 8 RKV11-D Module Utilization

Cabling

The RKV11-D is supplied with two BC05L cables which connect the M7269 LSI-11 bus control module to the M7268 bus adapter module. The BC05L cables are connected from J1 to J1 and from J2 to J2 on each module (Figures 2 and 9). Two 70-09026-02 cables are also supplied. These cables are connected from J3 and J4 on the M7268 module (Figure 9) to the RK05 M993-YA module.

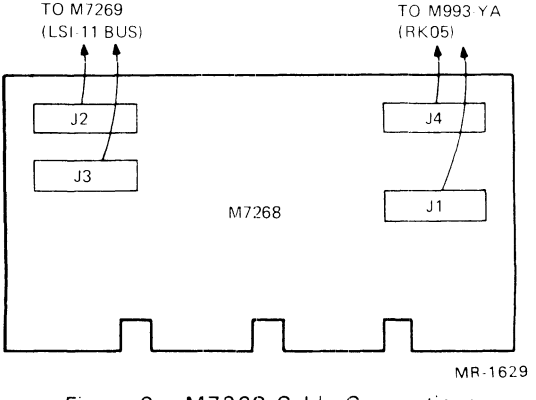


Figure 9 M7268 Cable Connections

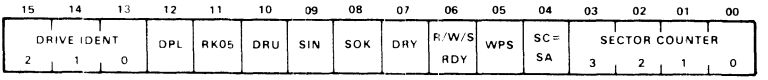
Registers

The RKV11-D contains seven 16-bit programmable registers that provide software interface to the LSI-11 bus. These registers are addressable from the processor and are listed in Table 2. The formats for these registers are shown in Figures 10 through 16. Bit descriptions are in Tables 3 through 9.

Table 2 RKV11-D Addressable Registers

Register Name	Mnemonic	Address*
RKV11-D Drive Status Register	RKDS	177400
RKV11-D Error Register	RKER	177402
RKV11-D Control/Status Register	RKCS	177404
RKV11-D Word Count Register	RKWC	177406
RKV11-D Bus Address Register (Current Memory Address)	RKBA	177410
RKV11-D Disk Address Register	RKDA	177412
RKV11-D Data Buffer Register	RKDB	177416

*Address 177414 is unused.



NOTE

This register is a read-only register, and contains the selected drive status and current sector address.

Figure 10 Drive Status Register (RKDS) – Address 177400

Table 3 Drive Status Register Bit Descriptions

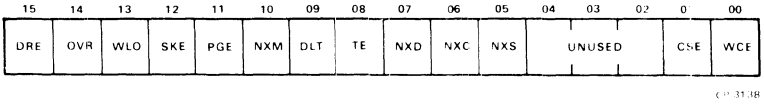
Bit	Name	Description
0–3	SC (Sector Counter)	These four bits are the current sector address of the selected drive. Sector address 0 is defined as the sector following the sector that contains the index pulse.

Table 3 Drive Status Register Bit Descriptions (Cont)

Bit	Name	Description
4	SC=SA (Sector Counter Equals Sector Address)	Indicates that the disk heads are positioned over the disk address currently held in the sector address register.
5	WPS (Write Protect Status)	Sets when the selected disk is in the write-protected mode.
6	R/W/S RDY (Read/Write/Seek Ready)	Indicates that the selected drive head mechanism is not in motion, and that the drive is ready to accept a new function.
7	DRY (Drive Ready)	Indicates that the selected disk drive complies with the following conditions: a. The drive is properly supplied with power. b. The drive is loaded with a disk cartridge. c. The disk drive door is closed. d. The LOAD/RUN switch is set to RUN. e. The disk is rotating at a proper speed. f. The heads are properly loaded. g. The disk is not in a DRU (bit 10 of RKDS) condition.
8	SOK (Sector Counter OK)	Indicates that the sector counter operating on the selected drive is not in the process of changing, and is ready for examination. If this bit is not set, the sector counter is not ready for examination and a second attempt should be made.

Table 3 Drive Status Register Bit Descriptions (Cont)

Bit	Name	Description
9	SIN (Seek Incomplete)	Indicates that due to some unusual condition, the seek function cannot be completed. Can be accompanied by RKER 15 (drive error). Cleared by a drive reset function.
10	DRU (Drive Unsafe)	Indicates that an unusual condition has occurred in the disk drive, and it is unable to properly perform any operations. Reset by setting the RUN/LOAD switch to LOAD. If, when the switch is returned to RUN, the condition recurs, an inoperative drive can be assumed, and corrective maintenance procedures should begin. Can be accompanied by RKER 15 (drive error).
11	RK05 (RK05 Disk On Line)	Always set to identify the selected disk drive as RK05.
12	DPL (Drive Power Low)	Sets when an attempt is made to initiate a new function, or if a function is actively in process when the control senses a loss of power to one of the disk drives. Can be accompanied by RKER 15 (drive error). Reset by a BUS INIT or a control reset function.
13–15	ID (Identification of Drive)	If an interrupt occurs as the result of a hardware poll operation, these bits will contain the binary representation of the logical drive number that caused the interrupt.



NOTE
This is a read-only register.

Figure 11 Error Register (RKER) – Address 177402

Table 4 Error Register Bit Descriptions

Bit	Name	Description
0	WCE (Write Check Error)	Indicates that an error was encountered during a write check function as a result of a faulty bit comparison between disk data and memory data. Clears upon the initiation of a new function. This is a soft error condition.
1	CSE (Checksum Error)	Sets while performing a read function as a result of a faulty recalculation of the checksum. Cleared upon the initiation of any new function. This is a soft error condition.
2–4	Unused	
	NOTE The remaining bits of the RKER are all hard errors, and are cleared only by a BUS INIT or a control reset function.	
5	NXS (Nonexistent Sector)	Indicates that an attempt was made to a sector address greater than 13_8.
6	NXC (Nonexistent Cylinder)	Indicates that an attempt was made to initiate a transfer to a cylinder address greater than 312_8.

Table 4 Error Register Bit Descriptions (Cont)

Bit	Name	Description
7	NXD (Nonexistent Disk)	Indicates that an attempt was made to initiate a function on a nonexistent drive.
8	TE (Timing Error)	Indicates that a loss of timing pulses for at least 5 μs has been detected.
9	DLT (Data Late)	Sets during a write or write check function when the multibuffer file is empty and the operation is not yet complete. Sets during a read function when the multibuffer file is filled and the operation is not yet complete.
10	NXM (Nonexistent Memory)	Sets if memory does not respond with a RPLY within 20 μs of the time when the RKV11-D becomes bus master during a DMA sequence. Because of the speed of the RK05 disk drive, it is possible that NXM will be accompanied by RKER 9 (data late).
11	PGE (Programming Error)	Indicates that RKCS 10 (format) was set while initiating a function other than read or write.
12	SKE (Seek Error)	Sets if the disk head mechanism is not properly positioned while executing a normal read, write, read check, or write check function. The control checks 16 times before flagging this error. A simple jumper change will force the control to check just once.
13	WLO (Write Lockout Violation)	Sets if an attempt is made to write on a disk that is currently write-protected.

Table 4 Error Register Bit Descriptions (Cont)

Bit	Name	Description
14	OVR (Overrun)	Indicates that, during a read, write, read check, or write check function, operations on sector 13_8, surface 1 of cylinder address 312_8 were finished, and the RKWC has not yet overflowed. This is essentially an attempt to overflow out of a disk drive.
15	DRE (Drive Error)	Sets if a function is either initiated or in process, and: a. One of the drives in the system senses a loss of either ac or dc power, or b. The selected drive is not ready, or is in some error condition.

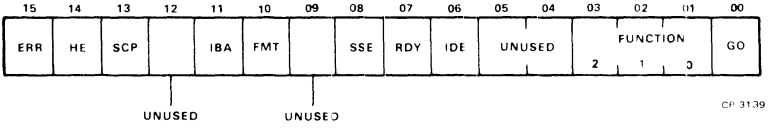


Figure 12 Control/Status Register (RKCS) – Address 177404

Table 5 Control/Status Register Bit Descriptions

Bit	Name	Description
0	GO	This bit can be loaded by the operator and causes the control to carry out the function contained in bits 1–3 of the RKCS (functions). Remains set until the control actually begins to respond to GO, which may take from 1 μs to 3.3 ms, depending on the current operation of the selected disk drive (to protect the format structure of the sector). Write-only bit.

Table 5 Control/Status Register Bit Descriptions (Cont)

Bit	Name	Description
1–3	Function	The function register, or function bits, are loaded with the binary representation of the function to be performed by the control when a GO command is initiated. These bits are loaded by the program and cleared by BUS INIT. The binary codings are as follows. **Bit** **3 2 1 Operation** 0 0 0 Control reset 0 0 1 Write 0 1 0 Read 0 1 1 Write check 1 0 0 Seek 1 0 1 Read check 1 1 0 Drive reset 1 1 1 Write lock Read/write bits.
4, 5	Unused	**NOTE** The RKV11-D uses these bits. Since the LSI-11 bus structure has no provision for extended addressing, no connection is made to the bus from these bits on the RKV11-D. They will respond as two unused read/write bits in the status register, but like the RKV11-D they will increment should the RKBA overflow.
6	IDE (Interrupt on Done Enable)	When set, causes the control to issue a bus request and interrupt to vector address 220 if: a. A function has completed activity. b. A hard error is encountered. c. A soft error is encountered and bit 8 of the RKCS (SSE) is set. d. RKCS 7 (RDY) is set and GO is not set. Read/Write bit.

Table 5 Control/Status Register Bit Descriptions (Cont)

Bit	Name	Description
7	RDY (Control Ready)	Indicates that the control is ready to perform a function. Set by INIT, a hard error condition, or by the termination of a function. Cleared by GO being set. Read-only bit.
8	SSE (Stop on Soft Error)	If a soft error is encountered when this bit is set: a. All control action will stop at the end of the current sector if RKCS 6 (IDE) is reset, or b. All control action will stop and a bus request will occur at the end of the current sector if RKCS 6 (IDE) is set. Read/write bit.
9	Unused	
10	FMT (Format)	FMT is under program control, and must be used only in conjunction with normal read and write functions. Used to format a new disk pack or to reformat any sector erased due to control or drive failure. Alters the normal write operation under which the header is rewritten each time the associated sector is rewritten; the head position is not checked for proper positioning before the write. Alters the normal read operation in that only one word, the header word, is transferred to memory per sector. For example, a 3-word read function in format mode will transfer header words from three consecutive sectors to three consecutive memory locations for software checking. Read/write bit.

Table 5 Control/Status Register Bit Descriptions (Cont)

Bit	Name	Description
11	IBA (Inhibit Incrementing the RKBA)	Inhibits the RKBA from incrementing during a normal transfer function. This allows data transfers to occur to or from the same memory location throughout the entire transfer operation. Read/write bit.
12	Unused	
13	SCP (Search Complete)	Indicates that the previous interrupt was the result of some previous seek or drive reset function. Cleared at the initiation of any new function. Read-only bit.
14	HE (Hard Error)	Sets when any of RKER 5–15 are set. Stops all control action, and processor reaction is dictated by RKCS 6 (IDE), until cleared, along with RKER 5–15, by INIT or a control reset function. Read-only bit.
15	ERR (Error)	Sets when any bit of the RKER sets. Processor reaction is dictated by RKCS 6 and RKCS 8 (IDE and SSE). Cleared if all bits in the RKER are cleared. Read-only bit.

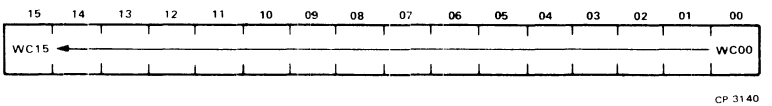


Figure 13 Word Count Register (RKWC) – Address 177406

Table 6 Word Count Register Bit Descriptions

Bit	Name	Description
0–15	WC00–WC15	The bits in this register contain the 2's complement of words to be affected or transferred by a given function. The register increments by one after each word transfer. When the register overflows (all WC bits go to zero), the transfer is complete and RKV11-D operation is terminated at the end of the present disk sector. However, only the number of words specified in the RKWC are transferred.

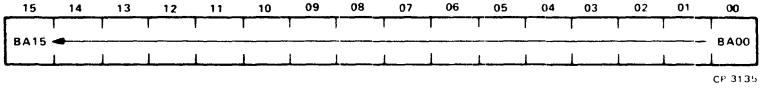


Figure 14 Bus Address Register (RKBA) – Address 177410

Table 7 Bus Address Register Bit Descriptions

Bit	Name	Description
0–15	BA00–BA15	The bits in this register contain the bus address to or from which data will be transferred. The register is incremented by two at the end of each transfer. Read/write bit.

NOTE

This register will not respond to commands while the controller is busy. Therefore, RKDA bits are loaded from the bus data lines only in the control ready (bit 7 of the RKCS) state, and are cleared by BUS INIT and control reset. The RKDA is incremented automatically at the end of each disk sector.

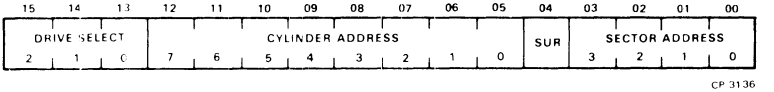


Figure 15 Disk Address Register (RKDA) – Address 177412

Table 8 Disk Address Register Bit Descriptions

Bit	Name	Description
0–3	SA (Sector Address)	Binary representation of the disk sector to be addressed for the next function. The largest valid address (or number) for the sector address is 13_8.
4	SUR (Surface)	When active, enables the lower disk head so that operation is performed on the lower surface; when inactive, enables the upper disk head.
5–12	CYL ADDR (Cylinder Address)	Binary representation of the cylinder address currently being selected. The largest valid address or number for the cylinder address is 312_8.
13–15	DR SEL (Drive Select)	Binary representation of the logical drive number currently being selected.

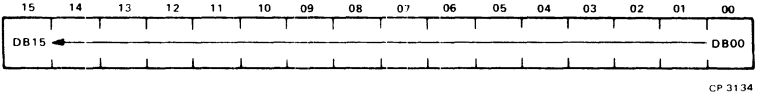


Figure 16 Data Buffer Register (RKDB) – Address 177416

Table 9 Data Buffer Register Bit Descriptions

Bit	Name	Description
0–15	BD00–DB15	The bits of this register work as a general data handler in that all information transferred between the control and the disk drive must pass through this register. Loaded from the bus only while the RKV11-D is bus master during a DMA sequence. Read-only PIO

PROGRAMMING

Data Format

Data is stored on the disk cartridge in groups of 12 sectors per track. Each of the 12 disk sectors contains 256_{10} words and is defined by physical sector marks. These sector marks generate a sector pulse that is passed from the disk drive to the controller. A similar physical disk mark, called an index mark, defines the starting point for the sequence of sectors. The sector which follows a sector containing the index mark is defined as sector 0. All of the sectors are formatted identically in five parts: preamble (terminated with a sync bit), header, data, checksum, and postamble (Figure 17).

PREAMBLE	SYNC BIT	HEADER	DATA	CHECKSUM	POSTAMBLE
15$_{10}$ WORDS OF ZEROES	"1"	CYLINDER ADDRESS (1 WORD)	256$_{10}$ (400$_8$) WORDS	SECTOR CHECKSUM (1 WORD)	1 WORD OF ZEROES

CP-3133

Figure 17 Sector Data Format

The preamble and postamble areas of a sector serve as boundaries before and after the information major states (header, data, and checksum) to ensure compatibility between disk drives at the cartridge level despite variations in sector pulse positioning. (Refer to the *RK05 Disk Drive Maintenance Manual*, EK-RK5JF-MM-001.)

The preamble consists of 15_8 words of zeros, adequate to guarantee that RD GATE will turn on during a known zero data field under all conditions. The disk drive head then waits for the first "1" to occur (sync bit) and begins to read with the header word. During a write function, the sync bit is automatically written by hardware following the 15_8 words of zeros.

The header area of a sector consists of a single word containing the cylinder address from RKDA 5–12. Before a data transfer function is performed, the header word is read and checked against the cylinder address portion of the RKDA to ensure that the disk drive heads are positioned at the proper cylinder. The write function always rewrites the header on the disk, using the cylinder address portion of the RKDA. The sector format for a raw (unformatted) cartridge is written under program control in conjunction with RKCS 10 (FMT).

The data area consists of 256_{10} data words. These words, like all of the words in each area of the sector, are 16 bits long.

The checksum area of a sector consists of a single word that is the checksum of all 256 data words. This checksum is compared by the controller to the checksum that it calculates itself whenever a write, check, read, or read check function is performed within a given sector. For a write function, the controller calculates a checksum and writes it on the disk cartridge following the last data word.

Short portions (less than 256 data words) of a sector may be read or written as long as this short sector is the last sector of the data transfer. When a short sector is written, the remainder of a sector is automatically written with zeros. The write check function may be performed on a short sector as long as the number of words write checked is equal to the number of words previously written into the sector. Because the read check function is essentially a parity check, it must be performed on a whole-sector basis only.

Program Interrupts

A program interrupt is initiated by an interrupt request, which can only occur if RKCS 6 (IDE) is set. Six hardware conditions can generate an interrupt request to the processor.

1. The occurrence of a hard error condition (RKCS 14)

2. The presence of a soft error condition (RKCS 8 and either RKER 00 or RKER 01 is set)

3. Completion of transfer of the designated number of words

4. The acceptance (address acknowledge) of a seek or drive reset function by the selected disk drive, freeing the controller for hardware polling or a new function

5. The initiation of a write lock function on a disk drive, indicating that the controller is free to perform a new function

6. The completion of hardware polling (RKCS 13, SCP), indicating that the disk drive in the drive ID bits of the RKDS has completed a seek or drive reset function (RKDS 6, R/W/S RDY).

Because of the format structure of the RKV11-D, any interruption of the write function cannot be tolerated until the end of the current sector, as it would result in what would be essentially an unformatted disk cartridge. As a result, outside intervention is inhibited until the current sector is completed, including control reset functions and processor initialize (BUS INIT) signals. This means that such functions as control reset, seek, and write lock, which take only a few microseconds to initiate, can take as long as 3.3 ms if initiated during a write function. For this reason, seek, drive, reset, and write lock functions cause an interrupt as soon as the function is initiated, provided RKCS 6 (IDE) is set.

Timing Considerations

RKV11-D timing is a consideration in the performance of overlapping seek or drive reset functions, because these functions can be initiated on free disk drives while previous seek or drive reset functions are in process on other disk drives. Thus, up to eight disk drives can be performing a seek or drive reset function simultaneously. The hardware poll logic of the disk control module generates an interrupt when a disk drive has completed the seek or drive reset function (RKDS 6, R/W/S RDY set). When a seek or drive reset function has been initiated on the disk drive (address acknowledge), an interrupt request occurs if RKCS 6 (IDE) is set. This process normally requires 1 μs but may range up to 3.3 ms, if an attempt is made to abort a write function. Head movement, however, may take as long as 80 ms, after which a second interrupt (RKCS 13, Search Complete) occurs (if IDE is set). In the interval between these two events, the selected disk drive is busy moving its heads but the controller is free to perform any RKV11-D function on any other available disk drive. Once a disk drive has begun moving its head mechanism, only a drive reset function can stop it. An attempt to perform any other function on a disk drive whose heads are in motion results in a hard error condition.

The data transfer functions (read, write, read check, and write check) all begin with an automatic "implied" seek. This allows the user of a single disk drive system to ignore the seek function completely and initiate data transfer functions directly. The hardware poll logic is initiated only for seek and drive reset functions and not for the "implied" seek portion of data transfer functions.

Power-Fail

An RKV11-D system contains a number of power supplies, each with its own circuitry for detection of a power failure:

1. The central processor and other computer-related supplies
2. The RKV11-D box
3. The RK05 disk drives.

If the power to the entire system is interrupted, a variety of events can occur depending on which of the system supplies first senses a power loss, the worst of which is the abortion of the function currently in process in the RKV11-D. Also, if a write function was in process at the time of the failure, the sector being written at the time of the power loss may contain erroneous but readable data. All of the RK05 drives will unload their heads, and no data or format on any disk drive will be lost.

If one or more of the computer-related supplies should malfunction, the program being executed is interrupted and a power-down sequence occurs in the computer. The result is the same as a system power failure except that the RK05 disk drives do not unload their heads. No data or format on any disk drive will be lost.

If the RKV11-D power supply malfunctions, the result is the same as a system power failure except that the computer and its parts will continue to operate. Because no dc power is available to the RKV11-D, no interrupt or error condition will occur to notify the computer that a failure has occurred. In most cases the RKV11-D controls the system disk, and this sort of malfunction would "hang" the software in the computer. The same unreportable error occurs if any of the computer-related power supplies has a similar malfunction.

An RKV11-D power supply malfunction is easily identified both physically and logically. Physically the "DC ON" LED on the power supply console will extinguish, and all the disk drives will unload their heads. Logically, all RKV11-D addressable registers contain all zeros.

If any of the RK05 disk drives senses a loss of ac or dc power, no new functions can be initiated. If an ac power loss is sensed and a function is in progress, the current sector will finish properly, and the next sector pulse will unload the heads, setting bit 15 RKER (DRE). If a malfunction occurs and a dc power loss occurs, the function is aborted; and, if writing, the sector being written may be logically damaged and in need of reformatting before it can be used again. Bit 15 RKER (DRE) and bit 12 RKDS (DPL) are set.

RKV11 Boot Programs

The following boot program can be used to boot an RKV11/RK05 system from drive unit 0.

```
@1000/000000          12700<LF>
001002    000000      177406<LF>
001004    000000      12710<LF>
001006    000000      177400<LF>
001010    000000      12740<LF>
001012    000000      5<LF>
001014    000000      105710<LF>
001016    000000      100376<LF>
001020    000000      5007<CR>
@1000G
```

The following boot program is used to boot an RKV11/RK05 system from an RK05 disk drive with unit numbers 1 through 7.

```
@1000/000000          12700<LF>
001002    000000      177406<LF>
001004    000000      12760<LF>
001006    000000      (unit)<LF>*
001010    000000      4<LF>
001012    000000      12700<LF>
001014    000000      177406<LF>
001016    000000      12710<LF>
001020    000000      177400<LF>
001022    000000      12740<LF>
001024    000000      5<LF>
001026    000000      105710<LF>
001030    000000      100376<LF>
001032    000000      5007<CR>
@1000G
```

*Unit No.	Contents
1	20000
2	40000
3	60000
4	100000
5	120000
6	140000
7	160000

NOTES

<LF> = Line Feed
<CR> = Carriage Return
Starting address = 1000

This program may also be used to boot an operating system from any RK05 when the system does not contain a hardware bootstrap module or contains a defective bootstrap module.

```
;R0 = drive number in bits 15, 14, 13; all others are zero.
;R1 = 177404 (= RKCS Address)

001000 000005 START: RESET
001002 010061        MOV    R0,6(R1)     ;LOAD RKDA
001004 000006
001006 012761        MOV    #-256.2(R1);LOAD RKWC = -256
001010 177400
001012 000002
001014 012711        MOV    #5,(R1)      ;LOAD READ & GO
001016 000005
001020 105711  1$    TSTB   (R1)         ;TEST READY
001022 100376        BPL    1$           ;AWAIT READY
001024 005007        CLR    PC           ;FORCE PC TO
                                         ABSOLUTE ZERO
```

Oscillating Seek Program

This program aids in checking servo signals and performing head alignment. Load the program into memory using the hardware ODT feature and select the desired drive, cylinder, and surface addresses. The program will then cause the drive to seek back and forth between the cylinder addresses contained in the high and low bytes of R0. If both bytes of R0 contain the same cylinder address, the drive will stay at that cylinder.

Equivalent Track Addresses

Decimal	Octal
0	0
4	4
64	100
85	125
105	151
125	175
202	312

```
;R0 = two cylinder addresses, one in each byte
;R1 = 177404 (RKCS address)
;R2 = drive number in bits 15, 14, 13; surface number in bit 4; all
others are zero.
```

```
001000 000005 START: RESET
001002 010003 LOOP:  MOV    R0, R3      ;R3 = CYLINDER
                                         ADDRESS
001004 042703        BIC    #377,R3     ;MASK FOR SINGLE
                                         ADDRESS
001006 000377
001010 000241        CLC
001012 006003        ROR    R3
001014 006003        ROR    R3          ;POSTION ADDRESS
001016 006003        ROR    R3
001020 010361        MOV    R3,6(R1)    ;LOAD CYLINDER
                                         ADDRESS
001022 000006
001024 050261        BIS    R2,6(R1)    ;LOAD DRIVE SURFACE
                                         ADDRESS
001026 000006
001030 012711        MOV    #11,(R1)    ;LOAD SEEK & GO
001032 000011
001034 105711 1$:    TSTB   (R1)
001036 100376        BPL    1$          ;AWAIT READY
001040 032737        BIT    #100,RKDS   ;AWAIT R/W/S RDY
001042 000100
001044 177400
001046 001774 2$:    BEQ    2$
001050 000300        SWAB   R0          ;POSITION SECOND
                                         ADDRESS
001052 000753        BR     LOOP
```

Format Program – This program allows the user to format an unformatted disk on any disk pack in the system. Any information formerly contained in the disk is lost, and the entire disk is filled with the contents of memory address 000000. When the program halts, check the contents of the RKER register (177402). It will contain 000100 if the format was successfully completed. If this register contains any other data, the format did not complete successfully.

```
;R0 = drive number in bits 15, 14, 13; all others are zero.
;R1 = 177404 (= RKCS)
001000 000005 START: RESET
001002 010061        MOV    R0,6(R1)    ;RKDA = DRIVE
                                         NUMBER
001004 000006
001006 005161 LOOP:  OM     2(R1)       ;RKWC = -1
001010 000002
001012 012711        MOV    #6003,(R1)  ;LOAD WRITE FORMAT,
                                         IBA + GO
001014 006003
001016 105711        TSTB   (R1)        ;READY?
001020 100376 1$     BPL    1$          ;AWAIT READY
001022 005711        TST    (R1)        ;ERROR?
001024 100370        BPL    LOOP        ;IF NOT, LOOP
001026 000000        HALT
```

FUNCTIONAL DESCRIPTION

General

The RKV11-D disk drive controller is implemented on five functional modules as shown in Figure 18. The paragraphs which follow provide a brief description of each module.

M7254 Control/Status Module

The M7254 module initiates the programmable functions of the RKV11-D and monitors logic status conditions by means of a programmable control/status register (RKCS), word count register (RKWC), and error register (RKER).

The RKCS receives function and control information from the LSI-11 bus, and implements it by initiating and directing RKV11-D functions, generating interrupt requests, and monitoring RKV11-D status information, which it transmits to the data paths module (M7256).

The RKWC receives data transfer word count information from the LSI-11 bus, is incremented for each word of data that is transferred, and overflows (word count overflow, WC OVF) to indicate the end of non-processor request (NPR) transfers.

The RKER provides error status information to the RKCS control logic and to the programmer.

M7255 Disk Control Module

The M7255 module controls the functions of the RK05 disk drive according to commands received from the M7254 status control.

The DR bus conveys disk drive status information to the drive, and includes control signals DR DC LO, ADD ACK, ILLEGAL ADD, LAST SECTOR, DR BUS RD CLK, and DR BUS RD DATA. CLK from the M7255 disk control is the WT CLK for a write function, or the DSK RD CLK from the selected disk drive for read, read check, or write check functions.

M7256 Data Paths Module

The M7256 module control bidirectional data flow (read or write) between a selected disk drive and the LSI-11 bus. It also controls the flow of data within the RKV11-D and contains the programmable disk address register (RKDA) and the bus address register (RKBA).

For a read function, the M7255 disk control supplies serial data from a selected disk drive to an in-buffer shift register on the M7256 module.

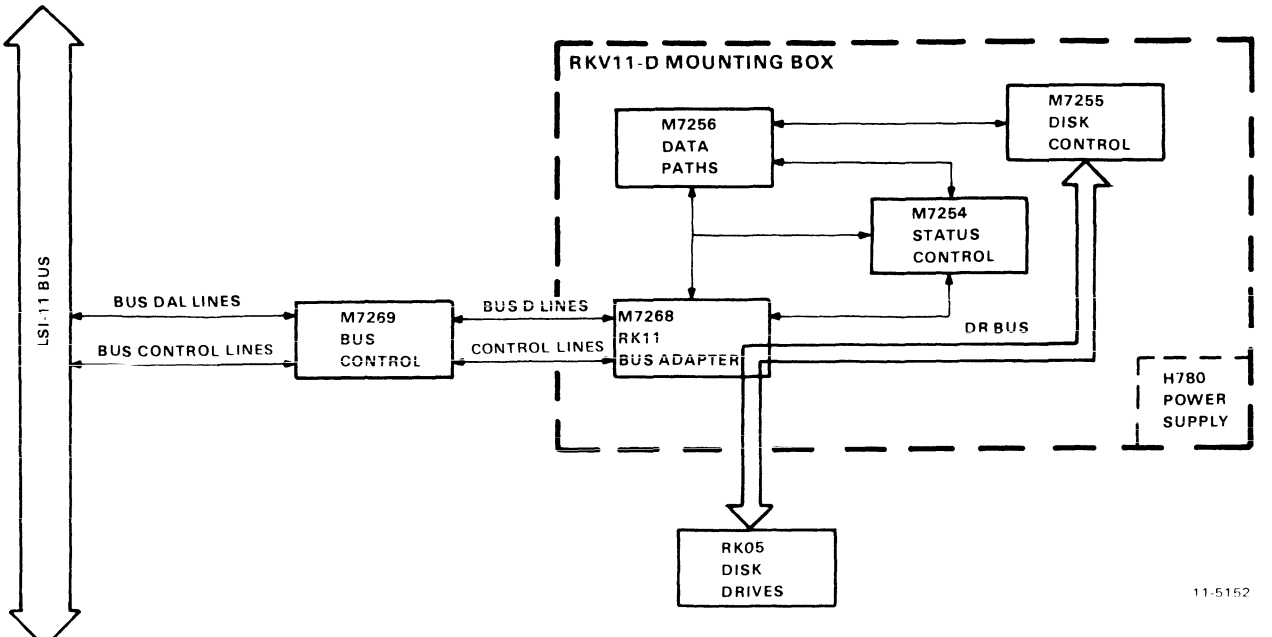


Figure 18 RKV11-D Controller, Functional Block Diagram

When a data word is complete, it is parallel-loaded into one of four word locations in a 4-word file. From the file, the data is loaded into the M7256 data buffer register (RKDB) for transfer to the LSI-11 bus. The data word is then multiplexed to the M7268 RK11 bus adapter, and from there transferred to the M7269 bus control module and placed onto the bus. The word transfer is a DMA transfer. Meanwhile, subsequent data words are transferred from the RKDB in-buffer to other locations in the 4-word file. During a read check function, the 4-word file is not used.

M7268 RKV11 Bus Adapter Module

The M7268 module contains no logic. This module is a connector module that has four 40-pin connectors. These connectors and the two 70-09026-02 cables and the two BC05L cables provide the mechanical interface between the RK05 disk drive and the RKV11-D, and between the LSI-11 bus (via the M7269 module) and the RKV11-D.

M7269 Bus Control Module

The M7269 module is the RKV11-D's interface to the LSI-11 bus. This module contains bus transceivers for interfacing to the bus, device address decoders, and interrupt vector generation logic. Two BC05L cables connect the M7269 module to the M7268 module.

Selectable Functions

Through software control, the RKV11-D can perform four control functions (control reset, seek, drive reset, and write lock) and four data transfer functions (write, read, write check, and read check). The hardware poll feature enables more than one disk drive to perform multiple seek or drive reset functions simultaneously. The RKV11-D also initiates an interrupt sequence on the LSI-11 bus in response to any of six interrupt conditions.

The data transfer functions (read, write, read check, and write check) all begin with an automatic "implied" seek operation. This allows the user of a single disk drive system to ignore the seek function completely and initiate data transfer functions directly. The hardware poll logic is initiated only for seek and drive reset functions and not for the "implied" seek portion of data transfer functions.

Control Reset – The control reset function initializes all internal registers and flip-flops and clears all of the bits of the seven programmable registers except RKCS 7 (READY), which it sets, and RKDS 0 through 11, which are not affected. Disk drive operation is only affected indirectly, as a result of RKV11-D logic being cleared.

Control reset serves as an effective "abort," because it terminates all controller action; however, care should be taken during a write operation as the abort does not occur until completion of the current sector. If a control reset function is used to abort a function in process to allow a high-priority user access to a disk drive, that drive must first be checked for head motion (indicated by RKDS 6, read/write/seek ready). If the function is initiated before the heads have stopped, a hard error results, after which a drive reset function must be performed on that drive before it can be used again.

Seek Function – For a seek function, the RKV11-D directs the selected disk drive to move its head mechanism to the cylinder address specified by RKDA 5–12. When this portion of a seek has been initiated, the controller returns to the ready state (RKCS 7). If the specified cylinder address is greater than 312_8, the function is aborted and bit 6 (non-existent cylinder) of the RKER is set. RKCS 6 (IDE) then determines the program reaction.

The selected disk drive completes the seek function by moving its head mechanism to the desired cylinder, whereupon RKDS 6 (R/W/S RDY) is set. The time required to initiate a seek function is normally 1 μs but may range up to 3.3 ms if an attempt is made to abort a write function. Head movement may take up to a maximum of 80 ms.

Drive Reset Function – For a drive reset function, the controller directs the selected disk drive to move its head mechanism to cylinder address 000 and reset all active error status lines. To the controller, the drive reset function is the same as a seek function, even to the manner in which the hardware poll logic is used; however, a drive reset function can take much longer than a seek function to execute. The time required to complete a drive reset function depends on the physical position of the head mechanism at the time the function is initiated and therefore may take a maximum of 2 seconds.

Write Lock Function – The write lock function write-protects a selected disk drive until the condition is overridden by operation of the corresponding WT PROT (write protect) switch on the disk drive (refer to *RK05 Disk Drive Maintenance Manual*, EK-RK5JF-MM-001). The disk drive is automatically write-enabled when power is first applied or when the disk drive RUN/LOAD switch is set to RUN.

Write Function – For a write function, the controller automatically performs an "implied" seek operation. When that is completed, the next header word is read and checked for correct cylinder identification (cylinder address). If the header is correct, the controller begins the write operation when the sector counter (RKDA 0–3) equals the sector address (RKDS 0–3), hereafter referred to as SC = SA (RKDS 4).

A preamble consisting of 15 words of zeros is written, followed by a sync bit. Then the header word is rewritten automatically, followed immediately by the data words for the sector. As the data words pass through the controller, a one-word checksum word is calculated and automatically written after the last sector data word, followed by one word of zeros for the postamble. If the cylinder address is incorrect, the controller makes 16 attempts to establish the correct cylinder address before the function is aborted, setting RKER 12 (seek error). (Compatibility with the RK11-C, which makes only one attempt, may be achieved by cutting a jumper on the status control module.)

An RKWC overflow at any time from the start of the write function stops the DMA data transfers and sets RKCS 7 (RDY) at the end of the current sector. If the RKWC has not overflowed at the end of a given sector, the function is continued at the next contiguous sector; however, if the last sector of the disk cartridge is transferred without RKWC having overflowed, then RKER 14 (OVR) is set

Read Function – For a read function, the controller automatically performs an "implied" seek operation. When that is completed, the controller waits for SC = SA then reads and checks the header word. If the cylinder address is correct, the controller continues reading the sector, and DMA transfers the data words onto the LSI-11 bus. If the cylinder address is initially incorrect, the controller makes 16 attempts (jumper-selectable to one) to establish the correct cylinder address before the function is aborted, setting RKER 12. As the data words of a sector pass through the controller, a 1-word checksum word is calculated and compared with the checksum read from the disk drive. If there is a discrepancy between the two checksums, RKER 1 (checksum error) is set, and the controller reaction is determined by RKCS 6 (IDE) and RKCS 8 (SSE). An RKWC overflow at any time from the start of the read function stops the DMA data transfers and sets RKCS 7 (RDY) at the end of the current sector. If the RKWC has not overflowed at the end of the given sector, the function is continued at the next sector.

Write Check Function – The write check function is used to compare the contents of memory to the contents of a continuous block of data on a disk cartridge. The controller automatically performs an "implied" seek operation, just as for a write function and then reads and checks the next header word. If the cylinder address is correct, the controller waits for SC = SA, then begins reading the rest of the sector (data and checksum) while performing DMA transfers for each data word. Each data word from the disk drive is compared, bit by bit, with memory data from the LSI-11 bus. The disk drive checksum, in turn, is compared with the checksum calculated by the controller. If any bit is found to be in error, RKER 0 (write check error) is set. Controller reaction is then determined

by RKCS 6 (IDE) and RKCS 8 (SSE). The write check function may be performed on a short sector (less than 256 data words) as long as the number of words write-checked is equal to the number of words previously written into the sector.

Read Check Function – The read check function is identical to a normal read function, except that no DMA data transfers occur. Only the checksum is calculated and compared with the checksum read from the disk drive. This function enables the program to know beforehand if a given block of data is readable and error free. Because the read check is essentially a parity check, it must be performed on a whole-sector basis only.

Hardware Poll – The controller is capable of permitting any or all disk drives to perform a seek or drive reset function simultaneously. The hardware poll feature in the disk control module identifies the logical disk drive in RKDS 13–15 (ID) for any disk drive that has completed a seek or drive reset function. This poll causes an interrupt if RKCS 6 (IDE) is set, the controller is in the ready state (RKCS 7 set), and the controller is not already attempting to initiate an interrupt from some other function. If two or more disk drives complete a seek or drive reset function simultaneously, the controller interrupts once for each disk drive and identifies each in turn to the RKDS. In this situation, the processor interrupt level must be raised in order to shut off interrupts, or a second interrupt will occur immediately after the first, causing the interrupt service routine to be interrupted. Similarly, back-to-back interrupts will also result from directing the heads to a cylinder at which they are already positioned, with the first interrupt coming from the initiation of a seek function and the second coming from notification from the hardware poll that the heads are already at the desired address.

Disk Drive

The RK05 is a moving head disk drive that uses RK03-KA disk cartridges for data storage. Data is stored on both sides of the disk by a pair of movable heads, which are always positioned over opposing surfaces of the same cylinder. Each side of the disk contains 203_{10} tracks, each of which contains 12_{10} sectors capable of storing 400_8 or 256_{10} data words.

The sector format consists of 15_8 words of preamble terminating in a sync bit followed by a 1-word header, 400_8 data words, a 1-word checksum, and one word of postamble. A sector pulse indicates the beginning of each sector. The index pulse occurs during the last sector, and the sector following the index pulse is sector 0.

The DR bus has up to eight disk drives connected in daisy-chain fashion, each of which can be write-protected either by an RKV11-D controller write lock function or by manual intervention.

On a disk cartridge, the upper surface is defined as surface 0 and is active when RKDA 4 (SUR) is clear. If a data transfer requires an overflow from surface 0, SUR is set automatically, and surface 1 (the lower surface of the cartridge) is activated at sector 0. If a data transfer requires an overflow from surface 1, the RKV11-D automatically moves the disk drive heads to the next cylinder, checks the header word to verify head positioning, and resumes the data transfer at sector 0 of surface 0. Attempting this cross-cylinder operation from surface 1 of the last cylinder will result in an error condition (RKER 14).

For more detailed information on the disk drive operation and the related power supply, refer to the *RK05 Disk Drive Maintenance Manual* (EK-RK5JF-MM-001). That manual also contains a complete description of the DR bus lines.

RLV11 RL01 DISK DRIVE CONTROLLER

GENERAL

The RLV11 option is designed to interface RL01 disk drives with the LSI-11 bus. The RLV11 controller can only be used in an H9273-A type backplane (PDP-11/03L or BA11-NE), which incorporates the LSI-11 bus in slot AB and an interboard bus in slot CD. The 2-card controller can interface up to four RL01 disk drives for a complete system. The RLV11 option consists of two quad size boards, an RL01 disk drive, and all the necessary cables.

The RL01 disk drive is a random access, mass storage system that stores data in fixed-length blocks on a preformatted disk cartridge. Each drive can store 5.24 million bytes and a complete system can store up to 21 million bytes. The RLV11 transfers data to and from the LSI-11 bus using direct memory access (DMA) techniques. This allows data transfers to occur without any processor interruptions and at the bus bandwidth speed.

FEATURES

- 5.24 million bytes per RL01 disk drive; 21 million bytes per system
- Up to four RL01 disk drives can be used with one RLV11 controller
- Universal power supply, 110/220 V, 50/60 Hz
- Bootstrap provided on BDV11
- Mounts in a PDP-11/03L system, BA11-N expansion box, or H9273-A backplane
- DMA transfers to and from the LSI-11 bus at 256K words per second
- 256K word silo buffer that eliminates late data errors on normal reads and writes

SPECIFICATIONS

LSI-11 Bus Modules

Identification	M8013 M8014
Size	Two quads
Power	+5 Vdc ± 5% at 6.5 A +12 Vdc ± 3% at 1 A
Bus Loads	
AC	3.2
DC	1

RL01 Disk Drive

Data Organization	256 bytes per sector 40 sectors per track 256 tracks per surface 256 cylinders per cartridge 2 surfaces per cartridge
Formatted Capacity	10,240 bytes per track 20,480 bytes per cylinder 5.24M bytes per cartridge 21M bytes per controller
Recording Density	125 tracks/in 3725 bits/in (max)
Recording Method	MFM
Performance	
Peak Transfer Rate	3.9 μs per word 512.5K bytes per second
Head Positioning Time	15 ms track-to-track 55 ms average 100 ms maximum
Rotational Latency	12.5 ms average
Operating Environment	
Temperature Range	10° to 40° C (50° to 104° F) at sea level
Relative Humidity	
Without Condensation	10 to 90%
Max. Wet Bulb	28° C (82° F)
Altitude	Up to 240 m (8000 ft) at max. temperature of 36° C (96° F)
Heat Dissipation	150 W (600 Btu/hr)
Operation	
Start Time	50 seconds
Stop Time	30 seconds
Rotational Speed	2400 rev/min

Power	
Drive	Single-phase
Start Current/Running Current	5 A/1.6 A max., 110 V, 50/60 Hz 2.5 A/0.85 A max., 230 V, 50/60 Hz
Mechanical Drive	
Size	48 cm wide X 63.4 cm deep X 27 cm high (19 in wide X 25 in deep X 10.5 in high)
Weight	33.75 kg (75 lb)
Mounting	RETMA standard 48.26 cm (19 in) rack-mounted on slides (provided). Recommended maximum height from floor is 18.9 cm (48 in) Stand-alone cabinets for expansion (standard option) available
Cartridge	2 data surfaces Embedded servo Top loading
Cable Lengths	
Standard	
Power	3.05 m (10 ft)
Controller to Drive	3.05 m (10 ft)
Drive to Drive	3.05 m (10 ft)
Optional	
Drive Cables	6.96, 12.19, 18.29 m (20, 40, 60 ft)

NOTE

Maximum physical length from controller to last drive should be 30.48 m (100 ft).

CONFIGURATION

General

All software control of the RLV11 controller is performed by means of four device registers. These registers are assigned addresses and can be read or written (as required) under software control. DIGITAL software requires that the device addresses are within the range of 160000 to 177777. This device address is preset at the factory to 174400. The address can be changed by setting the rocker switches designated "bus address switches" in Figure 1. These switches are used to assign a specific address to the control/status register (CSR) and the remaining registers will be assigned the next three addresses as shown in Table 1. A logical 1 is represented when the switch is placed to the ON position. Figure 2 shows the switch positions for the factory set address. The M8014 module must be located immediately after the M8013 module on the LSI-11 bus priority chain.

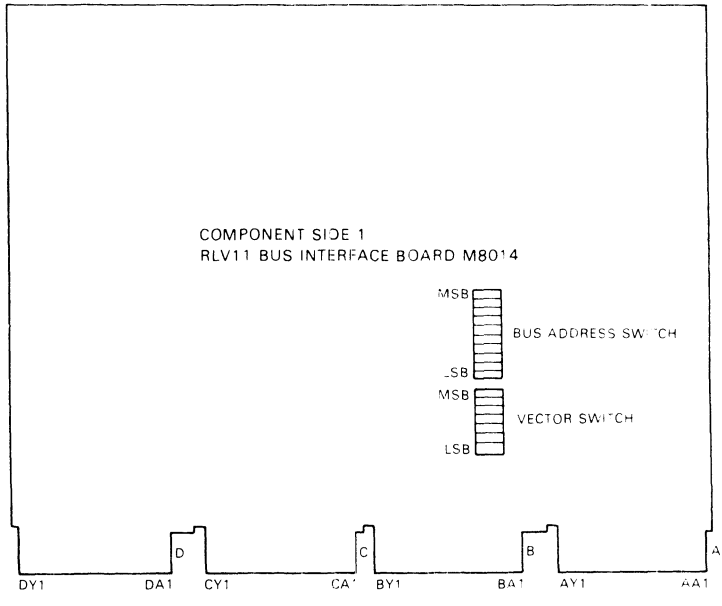


Figure 1 RLV11 Bus Interface Module (M8014)

Table 1 Standard Assignments

Description	Mnemonic	Read/ Write	Address
Registers			
Control/Status	CSR	R/W	174400
Bus Address	BAR	R/W	174402
Disk Address	DAR	R/W	174404
Multipurpose	MPR	R/W	174406
Interrupts			
Interrupt vector			160

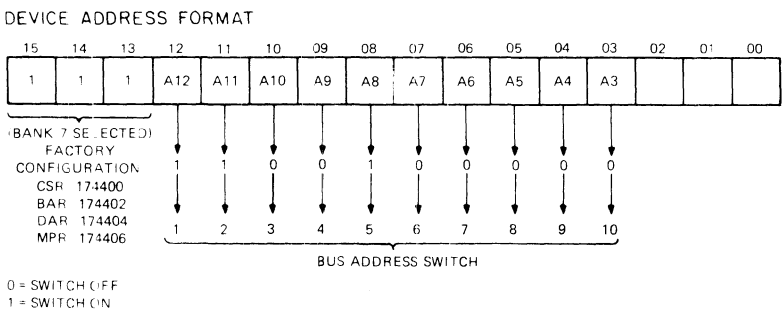


Figure 2 RLV11 Device Address Format

The interrupt vectors are allocated memory locations from 0–774. The recommended interrupt vector for the RLV11 is 160 and is preset at the factory for this vector. The user may set the rocker switches designated "vector switches" in Figure 1 for any vector within the allocation. A logical 1 is presented when the switch is placed to the ON position. Figure 3 shows the switch positions for the factory set address.

Jumpers

There are four jumpers (W1 to W4) installed on the M8013 printed circuit board as shown in Figure 4. These jumpers are installed in the factory and are used as described in Table 2.

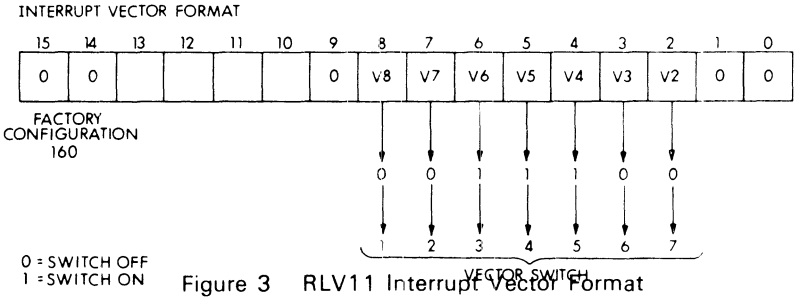


Figure 3 RLV11 Interrupt Vector Format

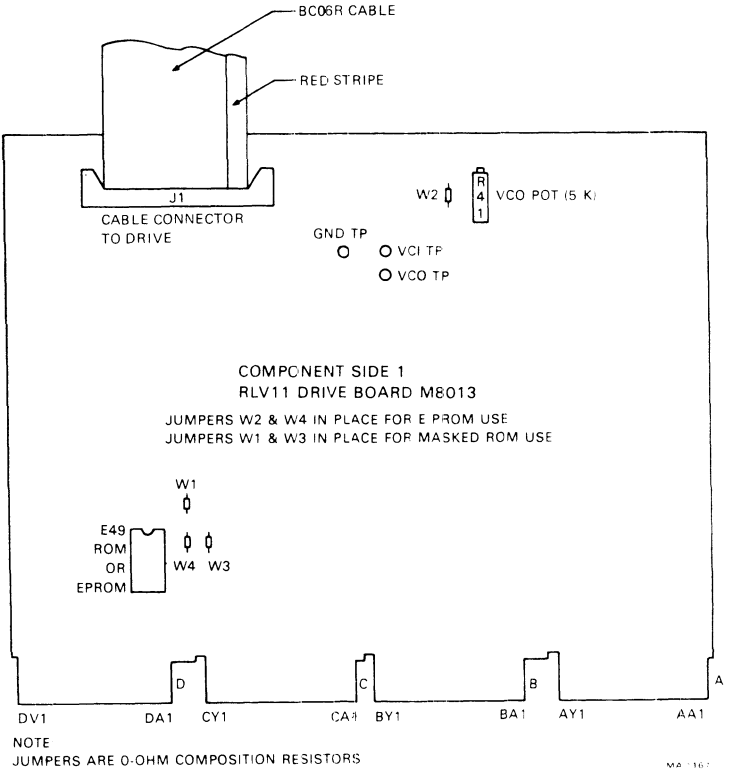


Figure 4 RLV11 Drive Module (M8013)

Table 2 M8013 Jumpers

Jumper	Definition
W1	Used with masked ROMs
W2	Used with EPROMs
W3	Used with masked ROMs
W4	Used with EPROMs

Masked ROMs W1, W3 – These jumpers are installed when using masked ROMs in E49. Jumpers W2 and W4 are removed.

EPROMs W2, W4 – These jumpers are installed when using EPROMs in E49 Jumpers W1 and W3 are removed.

Registers

Control/Status Register (CSR) – The control/status register (Figure 5) is a 16-bit, word-addressable register with a standard address of 174400. Bits 1 through 9 can be read or written; the other bits can only be read. The bit functions are described in Table 3.

When the LSI-11 bus is initialized (BINIT L), bits 1–6 and 8–13 are cleared, and bit 7 is set. Bit 0 is set whenever the selected drive is in the ready condition; otherwise the bit is cleared. Bit 14 is cleared as long as there is no drive error; otherwise the bit is set and remains set until the drive error is corrected or the drive error is cleared by a get status command with drive reset (bit 3) set. Bit 15 is set only when there is a drive or controller error (bits 10–14).

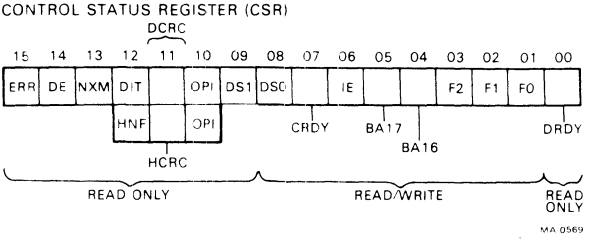


Figure 5 Control/Status Register

Table 3 CSR Word Format

Bit	Name	Description
0	DRDY (Drive Ready)	When set, this bit indicates that the selected drive is ready to receive a command or supply valid read data. The bit is cleared when a seek operation is initiated and set when the seek operation is completed
1–3	F2–F0 (Function Code)	These bits are set by software to indicate the command to be executed:

F2	F1	F0	Command	Octal Code
0	0	0	Maintenance Mode	0
0	0	1	Write Check	1
0	1	0	Get Status	2
0	1	1	Seek	3
1	0	0	Read Header	4
1	0	1	Write Data	5
1	1	0	Read Data	6
1	1	1	Read Data Without Header Check	7

Command execution starts when CRDY (bit 7) of the CSR is cleared by software. In a sense, then, bit 7 can be considered a negative GO bit.

4, 5	BA16, BA17 (Bus Address Extension Bits)	Two upper order bus address bits. Read and written as bits 4 and 5 of the CSR, they function as address bits 16 and 17 of the BAR.

Table 3 CSR Word Format (Cont)

Bit	Name	Description
6	IE (Interrupt Enable)	When this bit is set by software, the controller is allowed to interrupt the processor at the assertion of CRDY. This occurs at the normal or error termination of a command. Once an interrupt request is posted in the LSI bus, it is not removed until serviced even if IE is cleared.
7	CRDY (Controller Ready)	When cleared by software, this bit indicates that the command in bits 1–3 is to be executed. Software cannot set this bit because no registers are accessible while CRDY is 0.
8, 9	DS0, DS1 (Drive Select)	These bits determine which drive will communicate with the controller via the drive bus.
10	OPI (Operation Incomplete)	When set, this bit indicates that the current command was not completed within the OPI timer period.
11	DCRC (Data CRC) or HCRC (Header CRC)	If OPI (bit 10) is cleared and bit 11 is set, the CRC error occurred on the data (DCRC). If OPI (bit 10) is set and bit 11 is also set, the CRC error occurred on the header (HCRC). **NOTE** Cyclic redundancy checking is done only on the desired header. It is performed on the first and second header words, even though the second header word is always 0.
12	DLT (Data Late) or HNF Error (Header Not Found)	When OPI (bit 10) is cleared and bit 12 is set, it indicates that a data late condition occurred on a read without header check operation. The FIFO was more than half full and the controller was unable to transfer the next sequential sector.

Table 3 CSR Word Format (Cont)

Bit	Name	Description
		When OPI (bit 10) is set and bit 12 is also set, it indicates that a time-out occurred while the controller was searching for the correct sector to read or write (no header compare).
13	NXM (Non-Existent Memory)	When set, this bit indicates that during a DMA data transfer, the memory location addressed did not respond within 10 μs.
14	DE (Drive Error)	This bit is buffered from the drive error interface line. When set, it indicates that the selected drive has flagged an error, the source of which can be determined by executing a get status command. One way to clear the drive error is to reset the drive error register (e.g., by setting bit 3 of the get status command word).
15	ERR (Composite Error)	When set, this bit indicates that one or more of the error bits (bits 10–14) is set. When an error occurs, the current operation terminates and an interrupt routine is initiated if the interrupt enable bit (bit 6 of the CSR) is set

At the beginning of each controller command, error bits 10–13 are automatically cleared. At the completion of each controller command, bit 7 is automatically set. (Bit 7 is also set if an error is detected during command execution.)

The functions of control/status register bits 1–3 are described in the following paragraphs.

Maintenance Function (0) – The maintenance command provides a means of exercising the controller logic circuits to test whether the major data paths and data storage functions are operating. This command is used during the diskless diagnostic routine to detect controller malfunctions or to establish a level of confidence in controller operations.

The first circuitry tested is the microsequencer wait and branch logic, followed by branch conditions WCOFLW and MISMATCH. Upon successful completion of this test, the DAR is incremented by 1. This is used as a trace feature to show in which test a failure occurred.

The next circuit element to be tested is the silo (first-in/first-out buffer). A microsequencer routine is initiated to transfer 256 words of data from memory into the silo and then back to memory again. This exchange is performed under DMA control and again the DAR is incremented by 1 (which is the original DAR + 3).

Next a test word previously loaded into the disk address register (DAR) is sequenced through the controller data path and cyclic redundancy checking (CRC) logic to end up in the silo. The resultant silo word is in the form of the CRC of the test word.

The DAR is then incremented by one and the test word + 1 is sequenced through the same data paths and CRC to become the second silo word. This second silo word is in the form of the CRC of the test word + 1. The DAR is then incremented by one again.

Finally, to exercise the silo serial output stage, this second silo word is shifted out of the silo and sequenced through the same data paths and CRC circuit another time before coming to rest in the silo again. It now becomes the new second silo word and has the form of the CRC of the test word + 1. The DAR is then incremented by one again.

The results of this exercise are two adjacent data blocks in memory, two test words residing in the silo, and the test word + 3 residing in the DAR.

The silo buffer contains 255 words and each data block in memory occupies 256 locations.

The two words residing in the silo can be accessed via the multipurpose register. The first word is a test of the data paths. The second word is a test of the data paths plus the silo serial output stage. These words are read into memory and software monitored for malfunctions.

Write Check (1) – The write check command compares the data in the memory buffer to the data on the disk. Write check functions the same as a read, except the data transfer is from the memory.

Get Status Function (2) – The get status command initiates a microsequencer routine that shifts a drive command word from the controller to a selected drive. This word is a status request word that asks the drive to return information concerning its current operation and error status. If the reset bit in the status request is set, the drive will first clear all soft errors (those no longer present) before sending back drive status. When the drive sends back its status word, it is stored in the controller silo to await later access through the multipurpose register.

One prerequisite for issuing the get status command is a knowledge that the controller is in the ready state. It is important to note that the drive does not have to be ready (for example, during a seek or when in the load state) to issue a get status command.

The only programming prerequisite is that the status request word be loaded first into the disk address register before issuing the get status command.

Seek Function (3) – The seek command initiates a microsequencer routine that shifts a drive command word from the controller DAR to the drive. This drive command word contains head positioning information that includes the cylinder distance to be moved, the direction of movement, and the head to be selected for the next data transfer operation. Once this positioning information is received by the drive, the heads seek to the new track location.

There are several prerequisites for issuing a seek command. First, the present location must be known and this is available from the read header function. Once this is known, then the software must calculate the cylinder difference information needed by the drive to reposition the heads. Then before issuing the seek command, the software must know that the controller is in the ready state.

The only programming prerequisite is to load the disk address register with the head positioning information prior to issuing the seek function.

Read Header Function (4) – The functions of the read header command are to read the first header encountered on the selected drive and to store the three header words in the silo. These are header WD1 which contains the cylinder address, head select, and sector; header WD2, which contains all zeros; and header WD3, which contains the header CRC. One or more header words can then be extracted from the silo by reading the MPR. Extracting the first header word alone provides sufficient head positioning information to permit software calculation of cylinder difference for a subsequent seek operation to a new track address.

The only prerequisite for issuing the read header command is a knowledge that the controller is in the ready state.

Write Data Function (5) – The write data command initiates a microsequencer routine that enables the controller DMA circuitry. The controller eventually becomes LSI-11 bus master and data words are loaded into the silo. When the drive is ready, header information is continually read off the disk and compared with the first sector address stored in the DAR. Once a header match is found, the silo data is written on the disk in successive sectors until the word counter overflows. For partial sector writes, the remaining sector area is filled with 0s.

There are two prerequisites for the write data command. The first is that the heads must already be located at the correct track. This implies issuing a seek command if necessary. Also, the software must know that the controller is in the ready state before issuing a command.

Read Data Function (6) – The read data command initiates a controller microsequencer routine that reads successive headers off the disk and compares them against the first sector address in the DAR. When a header match is found, disk data is transferred into the silo and out to the LSI-11 bus under DMA control. The data transfer ends when the word counter overflows.

There are two prerequisites for the read data command. The first is that the heads must be located at the correct track. This implies issuing a seek command if necessary. The second is that software must know that the controller is ready to accept a command.

Read Without Header Check Function (7) – This command allows the recovery of data if the headers become unreadable. If header not found (HNF) or header CRC (HCRC) errors are encountered on a particular sector, then data is not recoverable by the standard read data command.

To convert this data, a seek command must be issued if the heads are not already located on the track where the bad sector is. Then the sector preceding the bad sector must be located by performing successive read header commands. Finally a read header without header check command can be issued within 300 μs to recover the next sector if the controller is ready.

Bus Address Register (BAR) – The bus address register (Figure 6) is a 16-bit, word-addressable register with an address of 174402. Bits 0 through 15 can be read or written; bit 0 should normally be written as 0. Expansion bits 16 and 17 are programmable via bits 4 and 5 of the CSR.

The bus address register indicates the memory location involved in the DMA data transfer during a read or write operation. The contents of the BAR are automatically incremented by 2 as each word is transferred between system memory and controller.

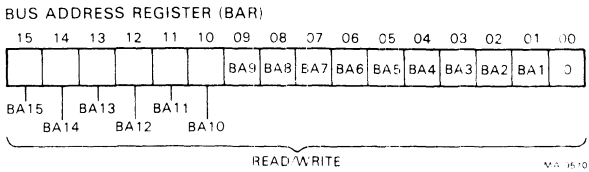


Figure 6 Bus Address Register

Clearing of the BAR is accomplished by executing a BUS INIT.

Disk Address Register (DAR) – The disk address register is a 16-bit, read/write, word-addressable register with an address of 174404. Its contents can have one of three meanings, depending on the function being performed. Clearing of this register is accomplished by executing a BUS INIT.

DAR During a Seek Command – To perform a seek function, it is necessary to provide address difference, head select, and head directional information to the selected drive as indicated in Figure 7. The word format is described in Table 4.

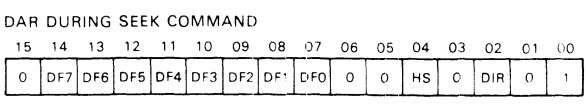


Figure 7 DAR Seek Command

Table 4 DAR Seek Command Word Format

Bit	Name	Description
0	MRKR (Marker)	Must be a 1.
1		Must be a 0, indicating to the drive that a seek command is being requested and that the remaining bits in the register will contain the seek specifications.

Table 4 DAR Seek Command Word Format (Cont)

Bit	Name	Description
2	DIR (Direction)	This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 7–14).
3		Must be a 0.
4	HS (Head Select)	Indicates which head (disk surface) is to be selected. Set = lower, clear = upper.
5, 6		Reserved
7–14	DF (07:00) (Cylinder Address Difference	Indicates the number of cylinders the heads are to move on a seek.
15		Must be a 0.

DAR During Read or Write Data Command – For a read, write, or write check operation, the DAR is loaded with the address of the first sector to be transferred. Thereafter, as each adjoining sector is transferred, the DAR is automatically incremented by 1 (Figure 8). If the DAR increments to the nonexistent sector address (50_8), an OPI time-out will occur. The word format is described in Table 5.

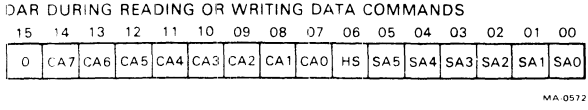


Figure 8 DAR Read/Write Data Command

Table 5 DAR Read/Write Data Command Word Format

Bit	Name	Description
0–5	SA (5:0) (Sector Address)	Address of one of the 40 sectors on a track. (Octal range is 0 to 47.)
6	HS (Head Select)	Indicates which head (disk surface) is to be selected. Set = lower; clear = upper.
7–14	CA (7:0) (Cylinder Address)	Address of one of the 256 cylinders. (Octal range is 0 to 377.)
15		Must be a 0.

DAR During a Get Status Command – After the get status command is deposited in the CSR, it is the DAR's responsibility to get the command transferred to the drive. Therefore, the DAR must also be programmed along with the CSR to do the get status command.

For a get status command, the DAR register bits must be programmed as shown in Figure 9; the word format is described in Table 6.

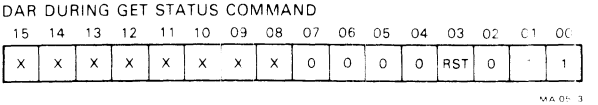


Figure 9 DAR Get Status Command

Table 6 DAR Get Status Command Word Format

Bit	Name	Description
0	MRKR (Marker)	Must be a 1.

Table 6 DAR Get Status Command Word Format (Cont)

Bit	Name	Description
1	GS (Get Status)	Must be a 1, indicating to the drive that its status word is being requested. At the completion of the get status command, the drive status word is read into the controller multipurpose (MP) register (output stage of FIFO). With this bit set, bits 8–15 are ignored by the drive.
2		Must be a 0.
3	RST (Reset)	When this bit is set, the drive clears its error register of soft errors before sending a status word to the controller.
4–7		Must be a 0.
8–15		Not used.

Multipurpose Register (MPR) – The MPR is two registers bearing the same base address. When writing into that location, the word counter accepts the data. When reading from that location, the FIFO output buffer provides the data.

MPR During a Get Status Command – When a get status command is executed and a status word is returned to the controller, the MPR (FIFO output stage) format is as shown in Figure 10 and described in Table 7.

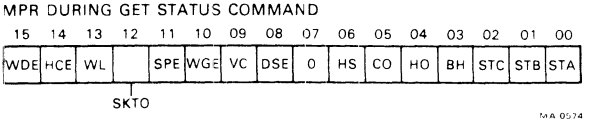


Figure 10 MPR Status Word

Table 7 MPR Status Word Format

Bit	Name	Description
0–2	State (C:A)	These bits define the state of the drive: **C B A** 0 0 0 Load State 0 0 1 Spin up 0 1 0 Brush cycle 0 1 1 Load heads 1 0 0 Seek track counting 1 0 1 Seek linear mode (lock on) 1 1 0 Unload heads 1 1 1 Spin down
3	BH (Brush Home)	Asserted when the brushes are not over the disk.
4	HO (Heads Out)	Asserted when the heads are over the disk.
5	CO (Cover Open)	Asserted when the cover is open or the dust cover is not in place
6	HS (Head Select)	Indicates the currently selected head
7		Reserved. Will be 0
8	DSE (Drive Select Error)	Indicates multiple drive selection is detected.
9	VC (Volume Check)	VC is set every time the drive goes into load heads state. This asserts a drive error at the controller but not on the front panel. VC is an indication that program does not really know which disk is present until it has read the serial number and bad sector file. (The disk might have been changed while the heads were unloaded.)

Table 7 MPR Status Word Format (Cont)

Bit	Name	Description
10	WGE (Write Gate Error)	Indicates the drive sensed that write gate was asserted when sector pulse was asserted, or write gate was set with the drive not ready, or the drive was write-locked.
11	SPE (Spin Error)	Indicates the spindle is not reaching speed in the required time, or over speeding.
12	SKTO (Seek Time Out)	Indicates the heads did not come on track in the required time during a seek command.
13	WL (Write Lock)	Indicates write lock status of selected drive.
14	HCE (Head Current Error)	Indicates write current was detected in the heads when write gate was not asserted.
15	WDE (Write Data Error)	Indicates write gate was asserted but no transitions were detected on the write data line.

MPR During a Read Header Command – When a read header command is executed, three words will be stored in the multipurpose register (FIFO output buffer). The first header word will contain sector address, head select and cylinder address information. The second word will contain all 0s. The third word will contain the header CRC information. All three words are readable by the main program (Figure 11).

MPR During Read/Write Data Commands – When transferring data via DMA, the MPR functions as a word counter and is loaded by the program with the 2's complement of the number of words to be transferred. It is then incremented by 1 by the controller as each word is transferred. The reading or writing operation generally is terminated when the word counter overflows. The word counter can keep track of from one data word to the full 40-sector count of 5120 data words (decimal). The

maximum number of words that can be transferred in a single operation is limited by the number of sectors available to be written in the track (Figure 12). The word counter format is described in Table 8

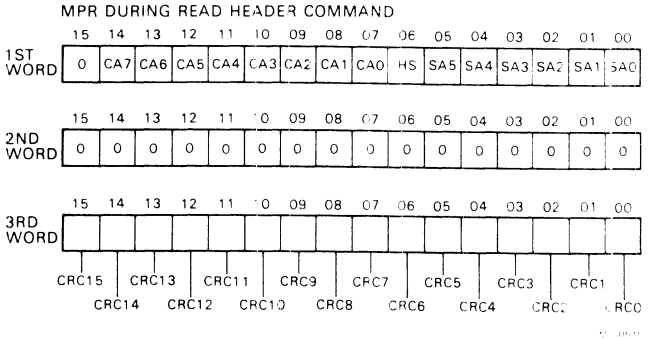


Figure 11 MPR Three Header Words

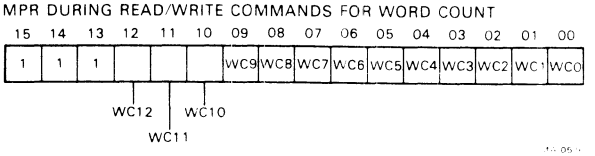


Figure 12 MPR Used as Word Counter

Table 8 MPR Word Counter Format

Bit	Name	Description
0–12	WC (12:0) (Word Count)	2's complement of total number of words to be transferred.
13–15		Must be a 1 for word count in correct range.

Operator Controls and Indicators
The following switches and indicators are located on the RL01 front bezel

1. RUN/STOP switch with LOAD indicator light
2. UNIT SELECT switch with READY indicator light
3. FAULT indicator light
4. WRITE PROTECT switch WRITE PROTECT indicator light

Power ON/OFF control is via a rear panel circuit breaker switch which is normally left in the ON position. Operation of this circuit breaker switch will not damage the drive in any way.

RUN/STOP Switch with LOAD Indicator – The RUN/STOP switch is a push/push alternating action switch which, when depressed, energizes the spindle motor. When released, it de-energizes the spindle motor provided the heads are not loaded and the brushes are retracted. If the heads are loaded, it causes the heads to unload and then de-energizes the spindle motor.

The switch contains mechanical memory. In the event of main power disruption and subsequent restoration, the drive will cycle up if the switch is in the depressed state.

The LOAD indicator is lit whenever the spindle is stopped, heads home, brushes home, and the spindle motor is not energized. A cartridge can be loaded when this indicator is lit.

UNIT SELECT Switch with READY Indicator – The UNIT SELECT switch is a cam-operated switch which is actuated by inserting a numbered cam button. The numbered cam button is such that the drive logic will recognize the drive address code corresponding to the unit select number on the cam button. The numbered indicator lights to indicate the condition identified as heads loaded and locked on a cylinder, drive ready for read or write operations.

FAULT Indicator – The FAULT indicator is lit whenever a fault or error condition occurs in the drive.

WRITE PROTECT Switch with WRITE PROTECT Indicator –The WRITE PROTECT switch is a push/push alternating action switch. When depressed, it sets the drive in write protect mode. If the drive is in the process of writing at the time that the switch is depressed, writing will continue until write gate is negated at the next sector pulse. The WRITE PROTECT indicator will not be illuminated until the write protect function is enabled. Removal of write protect will occur immediately upon the deactivation of the WRITE PROTECT switch.

I/O Transfer Operations

There are three kinds of I/O transfers that are used to interface the processor with the RLV11 controller. They are programmed I/O transfers, DMA transfers, or interrupt-driven transfers.

Programmed I/O transfers are executed by single- or double-operand PDP-11 instructions. By including the device's address as the effective source or destination address, the user specifies the transfer as an input or output operation. Programmed I/O allows information to be transferred between the RLV11 addressable registers and LSI-11 memory locations and processor registers. The transfer of each word requires the execution of a PDP-11 instruction.

DMA transfers, on the other hand, require only a few programmed I/O transfers to set control information. Then a large block of data can be moved to or from memory without any support from the processor. DMA transfers are the fastest method of transferring data between memory and a device. They can occur between processor bus cycles and do not alter processor status in any way. Blocks of data can be moved at speeds that are not limited by processor instruction execution via the DMA transfer mode. The read and write data in the controller FIFO is received and transmitted under DMA control.

Interrupt-driven transfers allow the processor to continue a programmed operation without waiting for the controller to become ready. When the controller becomes ready, it interrupts the processor's background program sequence and causes execution of the controller's service routine. After the controller's service routine has been executed, the background program is restored and program execution resumes at the point where it was interrupted.

Programmed I/O Transfers – Every processor instruction requires one or more I/O operations. The first operation required is a data input transfer (DATI), which fetches an instruction from memory at the location addressed by the program counter. This operation is called a DATI bus cycle. If the controller is referenced, additional DATI, or data output transfer (DATO) bus cycles are required.

Writing Controller Registers – When writing the controller registers, the CPU is the bus master and the controller is the slave. The initial DATI fetch cycle is followed by a DATO cycle.

Reading Controller Registers – When reading the controller registers, the CPU is bus master and the controller is the slave. The processor performs a DATI cycle to obtain the data from the RLV11 registers. The DATI cycle is a result of a processor programmed instruction which addresses the controller registers.

DMA I/O Transfers – Direct memory access (DMA) is used to transfer data between the controller FIFO and memory without program control. The processor can service DMA requests between bus cycles. Upon receiving BDMR requests from the bus, the processor sets up the conditions for a DMA transfer by granting bus mastership to the BDMG priority daisy-chain. If a high-priority device is requesting bus mastership, it will receive it and inhibit passage of the processor's grant, regardless of other lower priority requests. If it is not requesting bus mastership, it will pass the processor's BDMGO through other non-requesting devices to the one that is requesting. In practice, the disk controller is the highest priority device after memory in the system.

Once the controller is bus master and memory is the slave, DMA transfers can occur without processor intervention. The DMA protocol circuit limits transfers to four words at a time to allow other devices to be serviced and to prevent interference with the memory refresh cycle. After a time-out of 4 μs, if the processor is bus master, the controller can reassert mastership and continue the transfer with another four words.

Interrupt-Driven I/O Transfers – Interrupts are requests made by the controller that cause the processor to temporarily suspend its present program sequence to execute the controller service routine. The controller can interrupt the processor only when its interrupt control circuit is enabled. This circuit is enabled by an interrupt enable (IE) bit in the control/status register. A program must set this bit before an interrupt request can be issued.

An interrupt vector associated with the RLV11 controller is located in the controller interface/control logic. This vector is an address pointer that allows automatic entry into the controller service routine without device polling. The vector is switch-selectable in the range 0–774.

The controller requests interrupt service by asserting BIRQ L. The processor acknowledges the interrupt request by asserting BDIN L followed by BIAKO L. The first device on the bus receives this daisy-chained signal at its BIAKI L input. If it is not requesting service, it passes the signal via its BIAKO L output to the next device, and so on, until the requesting device receives the signal. The requesting device responds by asserting BRPLY L and placing its interrupt vector on the data/address bus lines BDAL (0:15) L. Automatic entry to the service routine is then executed by the processor.

Bus Signal Timing

Diagrams illustrating the bus timing requirements between the processor and the RLV11 controller, given in general master/slave device terms, may be found in the *Microcomputer Processors Handbook* published by Digital Equipment Corporation.

FUNCTIONAL DESCRIPTION

General

The RLV11 controller was designed to interface the RL01 disk drives to the LSI-11 bus. One RLV11 controller can support up to four RL01 disk drives. The controller consists of two quad height modules that plug directly into an LSI-11 backplane assembly. The backplane should be structured as an H9273 (slots AB are LSI-11 bus and slots CD are an interboard bus). (Refer to the section on H9273 backplanes in Chapter 4.)

The M8014 module contains all the LSI-11 bus-related circuits. Items such as the bus control circuits, bus transceivers and decoders, programmable registers, and the FIFO circuits are located on this module. The bus control function consists of the register protocol, interrupt control, operation incomplete timer, direct memory access, and nonexistent memory timer. The bus transceiver circuits transmit and receive both data and address information on the bus. The programmable registers consist of the control status, bus address word counter, disk address, and the multipurpose register. The FIFO circuits are a first in-first out memory that can store up to 256 16-bit data words.

The M8013 module contains all the controller timing and sequence logic and the data formatting circuits necessary to read and write on the disk. The microsequencer logic decodes the function command and proceeds to the address of the routine associated with the command. The write precompensation logic encodes the data into modified frequency modulation and precompensates the data for peak shifting effects. The cyclic redundancy checker is used to detect errors and compute CRC on a write operation. The data source selector allows the multiplexing of the data under control of the microsequencer. The header compare circuits compare the first header word received from the data separator with the serial disk address word coming from the disk address register.

The major functional sections of the RLV11 controller are shown in Figure 13. The processor controls the RL01 disk drives indirectly by means of the RLV11 controller. The controller has four registers: the bus address register (BAR), disk address register (DAR), control/status register (CSR), and a multipurpose register (MPR). Of these four registers, the CSR is always written last because it initiates the microsequencer operation. These registers can be addressed like any other memory location.

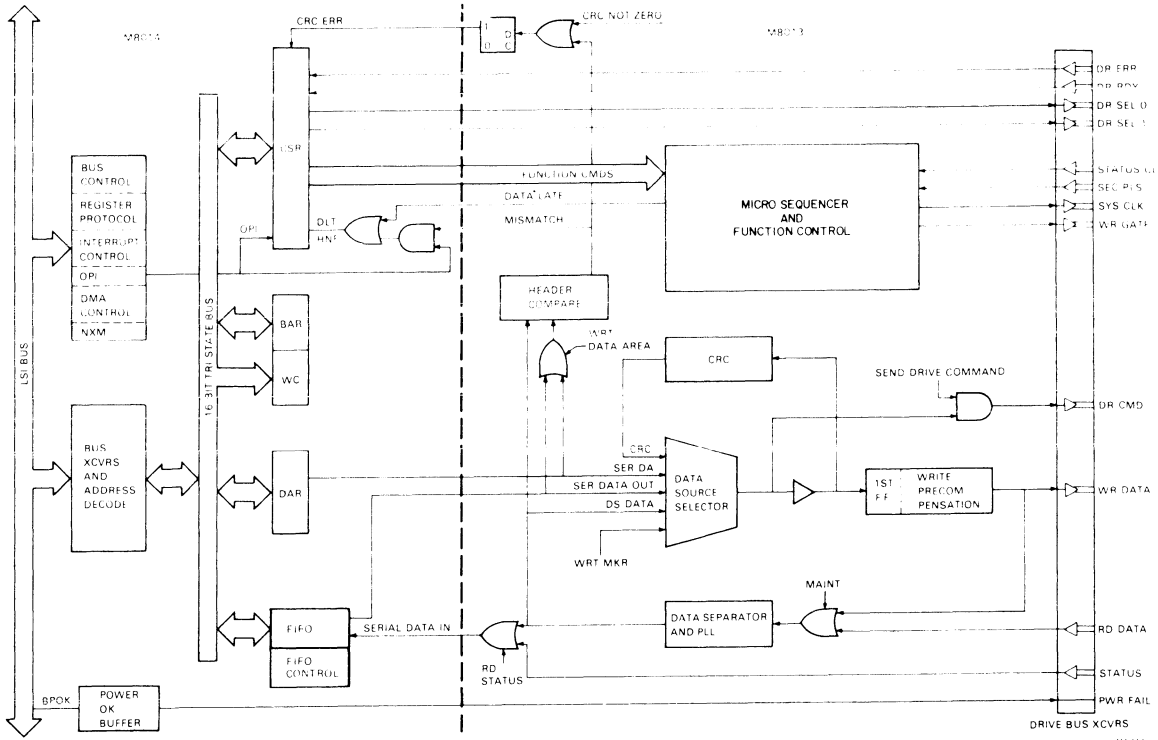


Figure 13 RLV11 Controller Simplified Block Diagram

To issue a function command, the processor places the address and data onto the LSI-11 bus in a multiplexed fashion. The RLV11 controller decodes the information and channels it to the appropriate register. Once the desired function command is written into the control/status register, it begins the microsequencer routine. The control microsequencer goes through a different routine for each of the eight possible command functions. These routines manipulate the data formatting circuits to format the data properly. Included in the data formatting function is an error detection feature that uses cyclic redundancy checking (CRC).

The data buffer (silo) is a data storage element used primarily when reading or writing the RL01K disk under DMA control. It is a FIFO memory that can store up to 256 words of data. The data buffer also performs data conversion functions. It converts parallel data coming off the LSI-11 bus into the serial form that can be written onto the disk. When performing a read operation, it reverses the direction of data flow and converts the serial disk data back into its parallel form.

Bus Control Functions

The bus control block consists of five separate functional units

- Register Protocol Circuit – This circuit selects the controller register to be read or written and supplies the required control signals for loading and reading.

- Interrupt Control Circuit – This circuit sends out a bus interrupt request to the processor when the controller has completed a command operation and the interrupt enable bit is set. It also passes or blocks the processor interrupt acknowledge along the priority daisy-chain and produces control signals for the generation of RPLY and vector data.

- OPI Circuit – This circuit is the operation incomplete (OPI) timer. This timer is initiated upon issuing a controller command. If the command sequence is not completed within the 490 ms nominal OPI time-out period, an OPI error bit is set in the control/status register. The controller ready bit is also set and the processor receives an interrupt request if enabled.

- DMA Control Circuit – The direct memory access (DMA) circuit coordinates the timing of the controller FIFO during DMA data exchanges with memory.

- NXM Circuit – The nonexistent memory (NXM) circuit is a timer used when the controller is attempting to read or write from memory. It is initialized by the bus SYNC signal and gives the memory device 10 μs to reply to a controller data in (DIN) or data out (DOUT) signal. If the

reply (BRPLY) is not received within 10 μs, the NXM error bit is set in the CSR. NXM time-out can also occur because of a failure at the controller or drive.

Bus Transceivers

These circuits transmit and receive both data and address information on the bus. The address decoder circuit compares each incoming address with the controller's preset base address. When a match is found, the register protocol circuit is enabled.

Programmable Registers

Control/Status Register (CSR) – The CSR is a holding register for command control information such as drive select, function to be performed, interrupt enable, and extended address bits. It also indicates drive ready and error conditions.

Bus Address Register (BAR) – The BAR contains the 16-bit memory address to which the next DMA transfer is to be made. It is incremented by two under control of the DMA control circuit at the end of each DMA transfer.

Disk Address Register (DAR) – The DAR contains the next sector address where data is to be read or written on the disk. It is incremented by one at the end of each sector read or written. The DAR is also used to store drive command information that is sent to the drive during a seek or get status operation.

Multipurpose Register (MPR) – The MPR is not a single physical entity like the other registers. It consists of two separate registers, the word counter and the FIFO output buffer, both bearing the same base address.

When writing the MPR, the data word is loaded into the word counter (WC) register. The WC register contains the number of data words remaining to be transferred under DMA control. The WC register is incremented by 1 under control of the DMA control circuit at the end of each DMA transfer.

When reading the MPR, the data word is read from the FIFO output buffer. After a read header command, it contains the header words. After a get status, it contains disk drive status.

FIFO

The FIFO is a first-in/first-out silo-type memory element that can store up to 256 data words. When full, it holds two sectors of data. A FIFO serializer circuit converts the FIFO parallel data into the serial form needed for writing to the disk. Similarly, the serial data read from the disk is converted to parallel form through the same serializer circuit.

The FIFO contents can be recovered by reading the current data word in the MPR. For example, to recover three FIFO words requires three successive readings of the MPR. During disk read and write operations, the FIFO is emptied and filled under control of the DMA logic.

Microsequencer Logic
The microsequencer first decodes the function command by using three function bits to point to an address in its sequencer ROM. There it finds a routine that corresponds to the command issued. It then proceeds to generate the timing and control signals needed to channel the incoming or outgoing data through all its various paths within the controller.

Write Precompensation
This circuit performs two major functions. It encodes digital data into its MFM form, and it precompensates this data for peak shifting effects.

MFM encoding is a magnetic recording technique used by the RL01 drive. A flux reversal is written on the disk in a center of a bit cell to represent a logical 1. To represent two successive logical 0s, a flux reversal is written at this common cell boundary. This recording technique guarantees at least one flux reversal for every two cell bits.

One of the problems associated with magnetic recording is a phenomenon called peak shift. Adjacent flux reversals on a track appear to be displaced from where they were written. To offset peak shift, the precompensation logic is used to displace the encoded data pulses in the opposite direction as the expected peak shift before they are written.

Data Separator
The data separator circuit makes use of a phase-locked loop oscillator to detect and decode incoming MFM disk data into its digital logical representation. It also generates the timing signals used by the microsequencer to control the read data operations.

CRC Circuit
The cyclic redundancy checker (CRC) is an error-detection circuit. For any data written on the disk, a code is generated in the CRC circuit by an internal algorithm. The code is then appended onto the end of each header or sector in the form of a CRC word. When this header or sector is read from the disk, the data is channeled through the CRC circuit. Any errors introduced into the data or its CRC word are detected and a CRC error bit is set in the CSR.

Data Source Selector
This circuit allows the multiplexing of different data sources under the control of the microsequencer. There are five different sources of data: CRC data, serial disk address data, serial FIFO output data, data separator (DS) data, and the write marker pulse.

Header Compare Circuit

The function of the header compare circuit is to compare the fist header word coming from the data separator with the serial disk address word coming from the DAR This compare is done serially on a bit-by-bit basis. If any pair of bits is not identical, a mismatch signal is generated. At the end of a compare, the result is available to the microsequencer.

RXV11 FLOPPY DISK OPTION

GENERAL

The RXV11 floppy disk option is a random access mass memory device that stores data in fixed-length blocks on a preformatted flexible diskette. Each diskette can store and retrieve up to 256K 8-bit bytes of data. The RXV11 system is rack-mountable and consists of an interface module, an interface cable, and either a single or dual RX01 floppy disk drive.

The interface module converts the RX01 I/O bus to the LSI-11 bus structure. It controls the RX01 interrupts to the processor, decodes device addresses for register selection, and handles the data interchange between the RX01 and the processor. Power for the interface module is supplied by the LSI-11 bus.

The RXV11 floppy disk system is available in the configurations described in Table 1.

Table 1 RXV11 Configurations

System	Disk Drive	Line Voltage*
RXV11-AA	Single drive system	115 V/60 Hz
RXV11-AC	Single drive system	115 V/50 Hz
RXV11-AD	Single drive system	230 V/50 Hz
RXV11-BA	Dual drive system	115 V/60 Hz
RXV11-BC	Dual drive system	115 V/50 Hz
RXV11-BD	Dual drive system	230 V/50 Hz

*50 Hz versions are available in voltages of 105, 115, 220, and 240 Vac by field-pluggable conversion. Refer to the *RX01/RX8/RX11 Floppy Disk System Maintenance Manual* for complete input power modification details.

FEATURES

- Compact disk system
- Stores/retrieves 256K 8-bit bytes of data
- Rack mountable
- Available with either single or dual disk drive
- Available for 115 or 230 Vac, 50 or 60 Hz
- Can be converted (50 Hz version) for 105, 115, 220, or 240 Vac operation

RXV11

SPECIFICATIONS

Module	
Identification	M7946
Size	Double
Power	+5 V ± 5% at 1.5 A
Bus loads	
AC	1.8
DC	1
Drive	
Identification	RX01
Size	46.3 cm w × 28.7 cm h × 53.3 cm d (19 in w × 10.5 in h × 21 in d)
Recommended Service Clearance (front and rear)	55 cm (22 in)
AC Power	4 A at 115 Vac; 2 A at 230 Vac (dual drive)
Cable Included	BC05L-15 (15 ft)
Drive Performance	
Capacity (8-bit bytes)	
Per diskette	256,256 bytes
Per track	3,328 bytes
Per sector	128 bytes
Data transfer rate	
Diskette to controller buffer	4 μs/data bit 250K bits/s)
Buffer to RXV11 interface	2 μs/bit (500 K bits/s)
RXV11 interface to LSI-11 I/O bus	18 μs/8-bit byte (<50K bytes/s)
Track-to-track move	10 ms/track maximum
Head settle time	20 ms maximum

Rotational speed	360 rpm ÷ 2.5%; 166 ms/rev nominal
Recording surfaces per disk	1
Tracks per disk	77 (0–76) or ($0–114_8$)
Sectors per track	26 (1–26) or ($0–32_8$)
Recording technique	Double frequency
Bit density	3200 bits/in at inner track
Track density	48 tracks/in
Average access	488 ms, computed as follows:

Seek	Settle	Rotate	Total
(77 tks/2) × 10 ms	+ 20 ms	+ (166 ms/2)	= 488 ms

Environmental Characteristics

Temperature

RX01, operating	15° to 32° C (59° to 90° F) ambient; maximum temperature gradient = –6.7° C/ hr (20° F/hr)
RX01, nonoperating	–35° to +60° C (–30° to +140° F)
Media, nonoperating	–35° to +52° C (–30° to +125° F)

NOTE

Media temperature must be within operating temperature range before use.

Relative humidity

RX01, operating	25° C (77° F) maximum wet bulb 2° C (36° F) minimum dew point 20% to 80% relative humidity
RX01, nonoperating	5% to 98% relative humidity (no condensation)
Media, nonoperating	10% to 80% relative humidity
Magnetic field	Media exposed to a magnetic field strength of 50 oersteds or greater may lose data.

System Reliability	
Minimum number of revolutions/track	1 million/media (head-loaded)
Seek error rate	1 in 10^6 seeks
Soft read error rate	1 in 10^9 bits read
Hard read error rate	1 in 10^{12} bits read

NOTE

The above error rates only apply to media that is properly cared for. Seek error and soft read errors are usually attributable to random effects in the head/media interface, such as electrical noise, dirt, or dust. Both are called "soft" errors if the error is recoverable in ten additional tries or less. "Hard" errors cannot be recovered. Seek error retries should be preceded by an initialize

CONFIGURATION

General

The factory jumper locations on the M7946 interface module are shown in Figure 1. Note that two styles of modules are used: one style (etch Rev B) has machine inserted jumpers; the other (etch Rev C) has wire-wrap jumpers. All M7946 interface modules are configured and shipped with preselected register addresses and vectors as shown in Figure 2. The control/status register (RXCS) address is 177170, and the data buffer register (RXDB) address is 177172. The interrupt vector is 264_8. As supplied, the factory-configured jumpers are for the normal addresses used with DIGITAL software. However, in applications where more than one RXV11 system is required, appropriate register addresses and vectors may be configured by installing or removing jumpers. A second RXV11 system would normally be assigned register addresses 177174 (RXCS) and 177176 (RXDB), with an interrupt vector of 270_8 (Table 2).

Register Descriptions

Command and Status Register (RXCS) (177170) – The format for the RXCS register is shown in Figure 3. Bit descriptions are presented in Table 3. Loading the RXCS register while the RX01 is not busy and with bit 0 = 1 will initiate a function described in Table 3.

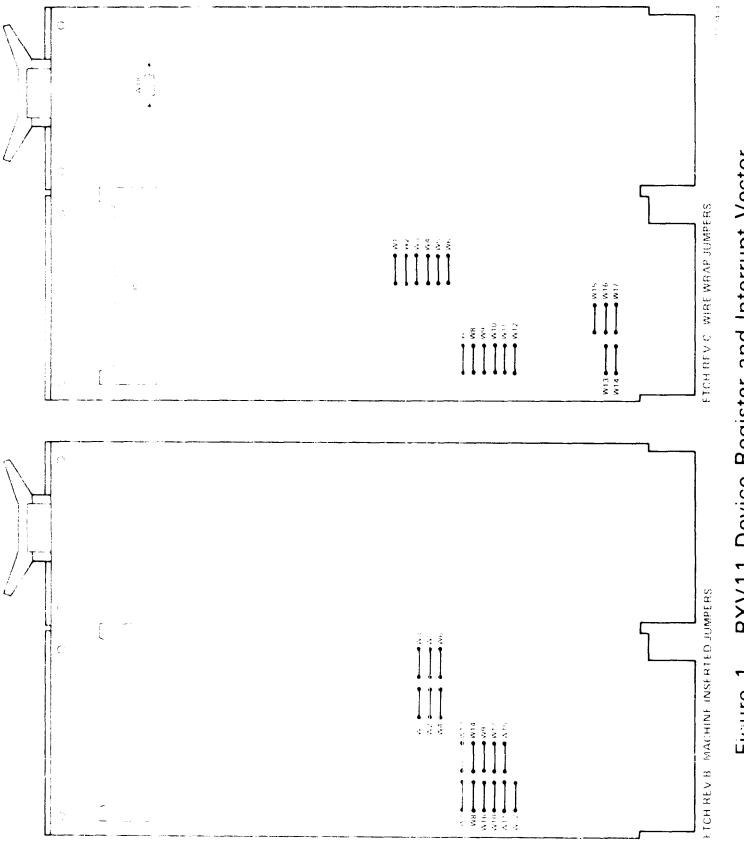


Figure 1 RXV11 Device Register and Interrupt Vector Jumper Locations

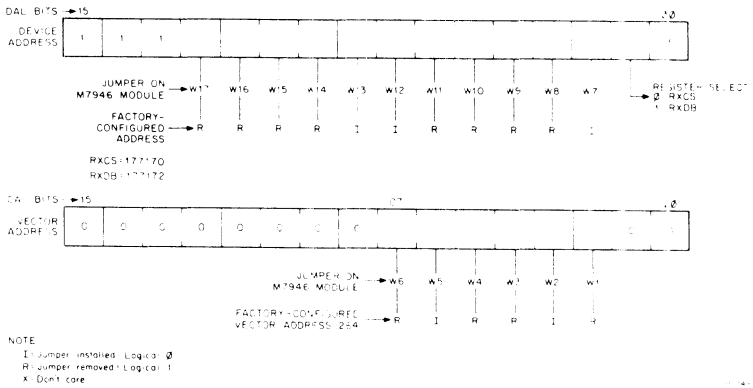


Figure 2 Device Register Address and Interrupt Vector

Table 2 Standard Assignments

Description	Mnemonic	Read/ Write	First Module Address	Second Module Address
Registers				
Control/Status	RXCS	R/W	177170	177174
Data Buffer	RXDB	R/W	177172	177176
Interrupt				
Function Complete	Done	--	264	270

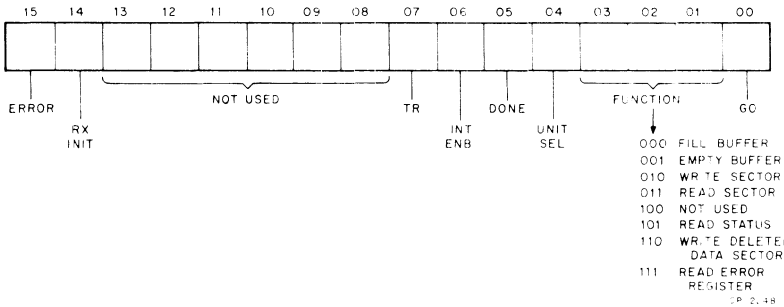


Figure 3 RXCS Format

Table 3 RXCS Bit Descriptions

Bit	Description
0	Go. Initiates a command to RX01. This is a write-only bit.
1–3	Function Select. These bits code one of the eight possible functions described in detail within this section. These are write-only bits.
4	Unit Select. This bit selects one of the two possible disks for execution of the desired function. This a write-only bit.
5	Done. This bit indicates the completion of a function. Done will generate an interrupt when asserted if interrupt enable (RXCS bit 6) is set. This is a read-only bit.
6	Interrupt Enable. This bit is set by the program to enable an interrupt when the RX01 has completed an operation (done). The condition of this bit is normally determined at the time a function is initiated. This bit is cleared by the LSI-11 bus initialize (BINIT L) signal, but it is not cleared by the RXV11 initialize bit (RXCS bit 14). This is a read/write bit.
7	Transfer Request. This bit signifies that the RXV11 needs data or has data available. This is a read-only bit.
8–13	Unused.
14	RXV11 Initialize. This bit is set by the program to initialize the RXV11 without initializing all of the devices on the LSI-11 bus. This is a write-only bit. **CAUTION** 1. Loading the lower byte of the RXCS will also load the upper byte of the RXCS. 2. Setting this bit (BIS instruction) will not clear the interrupt enable bit (RXCS bit 6). Upon setting this bit in the RXCS, the RXV11 will negate done and move the head position mechanism of drive 1 (if two are available) to track 0. Upon completion of a successful initialize, the RX01 will zero the error and status register, set initialize done, and set RXES bit 7 (DRV RDY) if unit 0 is ready. It will also read sector 1 of track 1 on drive 0.

Table 3 RXCS Bit Descriptions (Cont)

Bit	Description
15	Error. This bit is set by the RX01 to indicate that an error has occurred during an attempt to execute a command. This read-only bit is cleared by the initiation of a new command or by setting the initialize bit. When an error is detected, the RXES is automatically read into the RXDB.

Data Buffer Register (RXDB) (177172) – This RX01 interface register serves as a general-purpose data path between the RX01 and the interface. It may represent one of five RX01 registers according to the protocol of the command function in progress. The RX01 registers include RXDB, RXTA, RXSA, RXES, and RXER; each is described below.

This register is read/write if the RX01 is not in the process of executing a command; that is, it may be manipulated without affecting the RX01 subsystem. If the RX01 is actively executing a command, this register will only accept data if RXCS bit 7 (TR) is set. In addition, valid data can only be read when TR is set.

CAUTION

Violation of protocol in manipulation of this register may cause permanent data loss.

RX Data Buffer (RXDB) (Figure 4) – All information transferred to and from the floppy media passes through this register and is addressable only under the protocol of the function in progress.

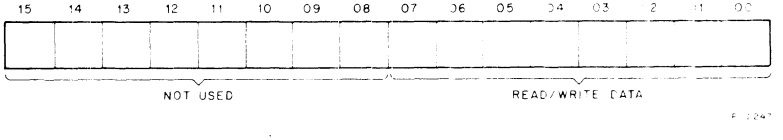


Figure 4 RXDB Format

RX Track Address (RXTA) (Figure 5) – This register is loaded to indicate on which of the 114_8 tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.

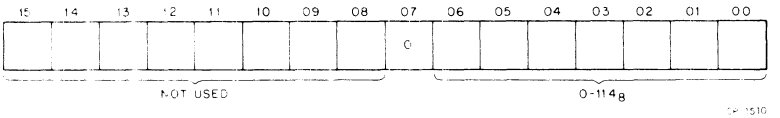


Figure 5 RXTA Format

RX Sector Address (RXSA) (Figure 6) – This register is loaded to indicate on which of the 32_8 sectors a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.

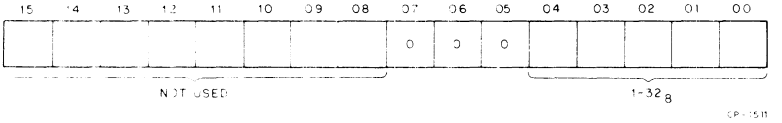


Figure 6 RXSA Format

RX Error and Status (RXES) (Figure 7) – This register contains the current error and status conditions of the drive selected by bit 4 (unit select) of the RXCS. This read-only register can be addressed only under the protocol of the function in progress. The RXES is located in the RXDB upon completion of a function. Table 4 lists the RXES bit descriptions.

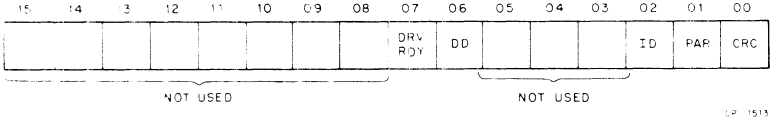


Figure 7 RXES Format

Table 4 RXES Bit Descriptions

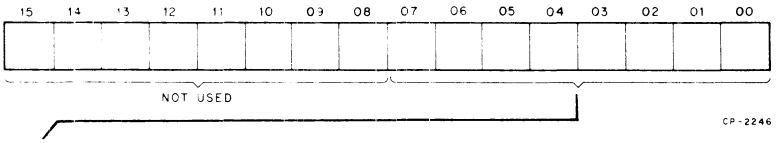
Bit	Description
0	CRC Error. A cyclic redundancy check error was detected as information was retrieved from a data field of the diskette. The RXES is moved to the RXDB, and error and done are asserted.
1	Parity Error. A parity error was detected on command or on address information being transferred to the RX01 from the LSI-11 bus interface. A parity error indication could mean that there is a problem in the interface cable between the RX01 and the interface. Upon detection of a parity error, the current function is terminated; the RXES is moved to the RXDB, and error and done are asserted.
2	Initialize Done. This bit is asserted in the RXES to indicate completion of the initialize routine, which can be caused by RX01 power failure, system power failure, or programmable or LSI-11 bus initialize.
3–5	Unused.
6	Deleted Data Detected. During data recovery, the identification mark preceding the data field was decoded as a deleted data mark.
7	Drive Ready. This bit is asserted if the unit currently selected exists, is properly supplied with power, has a diskette installed correctly, has its door closed, and has a diskette up to speed.

NOTES

The drive ready bit is only valid when retrieved via a read status function or at completion of initialize when it indicates status of drive 0.

If the error bit was set in the RXCS but error bits are not set in the RXES, then specific error conditions contained in the RXER can be accessed from the RXDB via a read error register function.

RX Error (RXER) (Figure 8) – This register is located in the RX01 and contains specific RX01 error information. This information is normally accessed when RXCS error bit 15 is set but RXES error bits 0 and 1 are not set. This is a read-only register.



Octal Code	Error Code Meaning
010	Drive 0 failed to see home on initialize.
020	Drive 1 failed to see home on initialize.
030	Found home when stepping out 10 tracks for INIT.
040	Tried to access a track greater than 77.
050	Home was found before desired track was reached.
060	Self-diagnostic error.
070	Desired sector could not be found after looking at 52 headers (2 revolutions).
110	More than 40 μs and no SEP clock seen.
120	A preamble could not be found.
130	Preamble found but no I/O mark found within allowable time span.
140	CRC error on what was thought to be a header.
150	The header track address of a good header does not compare with the desired track.
160	Too many tries for an IDAM (identifies header).
170	Data AM not found in allotted time.
200	CRC error on reading the secotr from the disk. No code appears in the ERREG.
210	All parity errors.

Figure 8 RXER Format

Function Codes

Data storage and recovery on the RXV11 system is accomplished by careful manipulation of the RXCS and RXDB registers according to the strict protocol of individual functions. The penalty for violation of protocol can be permanent data loss. Each of the functions are encoded and written into RXCS bits 1–3, as shown in Figure 3. Programming protocol for each function is described below.

Fill Buffer (000) – This function is used to fill the RX01 buffer with 128 8-bit bytes of data from the host processor. Fill buffer is a complete function in itself; the function ends when the buffer has been filled. The contents of the buffer can be written onto the diskette by means of a subsequent write sector function, or the contents can be returned to the host processor by an empty buffer function.

RXCS bit 4 (unit select) does not affect this function, since no diskette drive is involved. When the command has been loaded, RXCS bit 5 (done) is negated. When the TR bit is asserted, the first byte of data may be loaded into the data buffer. The same TR cycle will occur as each byte of data is loaded. The RX01 counts the bytes transferred; it will not accept less than 128 bytes and will ignore those in excess. Any read of the RXDB during the cycle of 128 transfers results in invalid read data.

Empty Buffer (001) – This function is used to empty the internal buffer of the 128 data bytes loaded from a previous read sector or fill buffer command. This function will ignore RXCS bit 4 (unit select) and negate done.

When TR sets, the program may unload the first of 128 data bytes from the RXDB. Then the RXV11 again negates TR. When TR resets, the second byte of data may be unloaded from the RXDB, which again negates TR. Alternate checks on TR and data transfers from the RXDB continue until 128 bytes of data have been moved from the RXDB. Done sets, ending the operation and initiating an interrupt if RXCS bit 6 (interrupt enable) is set. RXES contents are moved to the RXDB where they can be read.

NOTE

The empty buffer function does not destroy the contents of the sector buffer.

If the deleted data address mark was detected, the control will assert RXES bit 6 (DD). As data enters the sector buffer, a CRC is computed, based on the data field and CRC bytes previously recorded. A non-zero residue indicates that a CRC error has occurred. The control sets RXES bit 0 (CRC error) and RXCS bit 15 (error). The RXV11 ends the operation by moving the contents of the RXES to the RXDB, sets done, and initiates an interrupt if RXCS bit 6 (interrupt enable) is set.

Read Status (101) – The RXV11 will negate RXCS bit 5 (done) and begin to assemble the current contents of the RXES into the RXDB. RXES bit 7 (drive ready) will reflect the status of the drive selected by RXCS bit 4 (unit select) at the time the function was given. All other RXES bits will reflect the conditions created by the last command. RXES may be sampled when RXCS bit 5 (done) is again asserted. An interrupt will occur if RXCS bit 6 (interrupt enable) is set.

NOTE

The average time for this function is 250 ms. Excessive use of this function will result in substantially reduced throughput.

Write Sector with Deleted Data (110) – This operation is identical to function 010 (write sector) with the exception that a deleted data address mark precedes the data field instead of a standard data address mark.

Read Error Register Function (111) – The read error register function can be used to retrieve explicit error information contained in the RXER when RXCS error bit 15 is set. The function is initiated, and bits 0–6 of the RXES are cleared. Out is asserted and done is negated. The controller then generates the appropriate number of shift pulses to transfer the specific error code from the RXER to the interface register and completes the function by asserting done. The RXDB program can then read the error code to determine the type of failure that occurred (Figure 8).

NOTE

Care should be exercised in the use of this function since, under certain conditions, erroneous error information may result.

Power Fail – There is no actual function code associated with power fail. When the RX01 senses a loss of power, it will unload the head and abort all controller action. All status signals are invalid while power is low.

When the RX01 senses the return of power, it will remove done and begin a sequence to:

1. Move drive 0 head position mechanism to track 0.

2. Clear any active error bits.

3. Read sector 1 of track 1 of drive 0 into the sector buffer.

4. Set RXES bit 2 (initialize done) after which done is again asserted.

5. Set drive ready of the RXES according to the status of drive 0.

Write Sector (010) – This function is used to locate a desired track and sector and write the sector with the contents of the internal sector buffer. The initiation of this function clears bits 0, 1, and 6 of RXES (CRC error, parity error, and deleted data detected) and negates done.

When TR is asserted, the program must first move the desired sector address into the RXDB, which will negate TR. When TR is again asserted, the program must move the desired track address into the RXDB, which will negate TR. If the desired track is not found, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (error), assert done, and initiate an interrupt if RXCS bit 6 (interrupt enable) is set.

TR will remain negated while the RX01 attempts to locate the desired sector. If the RX01 is unable to locate the desired sector within two diskette revolutions, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (error), assert done, and initiate an interrupt if RXCS bit 6 (interrupt enable) is set.

If the desired sector is successfully located, the RXV11 will write the 128 bytes stored in the internal buffer followed by a 16-bit CRC character that is automatically calculated by the RX01. The RXV11 ends the operation by asserting done and initiating an interrupt if RXCS bit 6 (interrupt enable) is set.

NOTES

The contents of the sector buffer are not valid data after a power loss has been detected by the RX01. The write sector function, however, will be accepted as a valid function, and the random contents of the buffer will be written, followed by a valid CRC.

The write sector function does not destroy the contents of the sector buffer.

Read Sector (011) – This function is used to locate a desired track and sector and transfer the contents of the data field to the μCPU controller sector buffer. The initiation of this function clears bits 0, 1, and 6 of RXES (CRC error, parity error, deleted data detected) and negates done.

When TR is asserted, the program must first move the desired sector address into the RXDB, which will negate TR. When TR is again

asserted, the program must move the desired track address into the RXDB, which will negate TR.

If the desired track is not found, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (error), assert done, and initiate an interrupt if RXCS bit 6 (interrupt enable) is set.

TR and done will remain negated while the RX01 attempts to locate the desired track and sector. If the RX01 is unable to locate the desired sector within two diskette revolutions after locating the presumably correct track, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (error), assert done, and initiate an interrupt if RXCS bit 6 (interrupt enable) is set.

If the desired sector is successfully located, the control will attempt to locate a standard data address mark or a deleted data address mark. If either mark is properly located, the control will read data from the sector into the sector buffer.

There is no guarantee that information being written at the time of a power failure will be retrievable. However, all other information on the diskette will remain unaltered.

One method of aborting a function is through the use of RXCS bit 14 (RXV11 initialize); however, this will not clear the interrupt enable bit (RXCS bit 6). Another method is through the use of the system initialize signal that is generated by the PDP-11 RESET instruction, the console ODT Go command, or system power failure.

PROGRAMMING

General

The RXV11 is controlled by the processor by two registers located on the M7946 interface module. These registers, shown in Figure 9, are the command status register (RXCS) and a multipurpose data buffer register (RXDB). These registers can be read or loaded by program instructions that refer to the device addresses. For programming details and instructions, refer to the RXV11 User's Manual.

The RX01 has a read/write data buffer that can contain one full sector (128 8-bit bytes) of diskette data. This buffer and other RX01 registers are also shown in Figure 9. The program has direct access to the RXCS and RXDB only. Access to the RX01 registers is through the RXDB. Read and write data transfers always require two steps. When writing data, the program first fills the buffer with write data via program transfers with the RXDB. Once the buffer is filled, the program issues a write

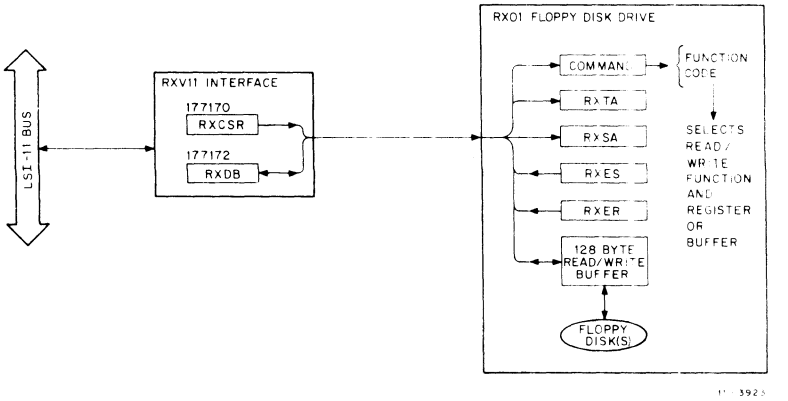


Figure 9 RXV11 System Register Functions

sector command via the RXCS and the buffer's contents are written to the diskette. During a read operation, the diskette data is first read into the buffer. The program then reads the data via the RXDB.

Restrictions and Programming Pitfalls – A set of restrictions and programming pitfalls for the RXV11 is presented below.

1. Depending on how much data handling is done by the program between sectors, the minimum interleave of two sectors may be used, but to be safe a 3-sector interleave is recommended.

2. If an error occurs and the program executes a read error register function (111), a parity error may occur for that command. The error status would not be for the error in which the read error register function was originally required.

3. The DRV SEL RDY bit is present only at the time of a read status function (101) for both drives, and after an initialize, depending on the status of drive 0.

4. It is not required to load the drive select bit into the RXCS when the command is fill buffer (000) or empty buffer (010).

5. Sector Addressing: 1–26 (*No sector 0*)
   Track Addressing: 0–76

6. A power failure causing the recalibration of the drives will result in a done condition, the same as finishing the reading of a sector. However, during a power failure, RXES bit 2 (initialize done) will set. Checking this bit will indicate a power-fail condition.

7. Excessive usage of the read status function (101) will result in drastically decreased throughput, because a read status function requires between one and two diskette revolutions or about 250 ms to complete.

Error Recovery – There are two error indications given by the RXV11 system. The read status function will assemble the current contents of the RXES, which can be sampled to determine errors. The read error register function can also be used to retrieve explicit error information from the RXER.

A list of error codes associated with the RXER is shown in Figure 8.

NOTE

A read status function is not necessary if the DRV RDY bit is not going to be interrogated, because the RXES is in the interface register at the completion of every function.

Programming Examples

Read Data/Write Data – Figure 10 presents a program for implementing a write, write deleted data, or a read function, depending on the function code that is used. The first instructions set up the error retry counters PTRY, CTRY, and STRY. The instruction RETRY moves the command word for a write, write deleted data, or read into the RXCS.

The set of three instructions beginning at the label 1$ moves the sector address to the RXV11 after transfer request (TR), which is bit 7, has been set. The three instructions beginning at the label 2$ move the track address to the RXV11 after TR has been set. The group of instructions beginning at the label 3$ looks for the done flag to set and checks for errors.

An error condition, indicated by bit 15 setting, is checked beginning at ERFLAG. If bit 0 is set, a CRC error has occurred, and a branch is made to CRCER. If bit 1 is set, a parity error has occurred, and a branch is made to PARER. If neither of the above bits is set, a seek error is assumed to have occurred and a branch is made to SEEKER, where the system is initialized. In the case of a write function, the sector buffer is refilled by a JMP to FILLBUF. In the case of a read function, a JMP is made to EMPBUFF.

```
                                        .ABS
                                    ;PROGRAMMING EXAMPLES FOR THE RX11/RX01 FLEXIBLE DISKETTE
                                    ;
                                    ;THE FOLLOWING IS THE RX11 STANDARD DEVICE ADDRESS AND VECTOR ADDRESS
                                    ;
          177170                    RXCS=177170                     ; COMMAND STATUS REGISTER
          177172                    RXDB=177172                     ; DATA BUFFER REGISTER
          177172                    RXSA=177172                     ; SECTOR ADDRESS REGISTER
          177172                    RXTA=177172                     ; TRACK ADDRESS REGISTER
          177172                    RXES=177172                     ; ERROR STATUS REGISTER
                                    ;
                                    ;THE FOLLOWING IS A PROGRAMMING EXAMPLE OF THE PROTOCOL REQUIRED
                                    ;TO WRITE, WRITE DELETED DATA, OR READ AT SECTOR "S" (THE CONTENTS OF PROGRAM
                                    ;LOCATION SECTOR) OF TRACK "T" (THE CONTENTS OF PROGRAM LOCATION TRACK)
                                    ;
000000  012767  177770  000320      START:  MOV #-10, PTRY          ; PARITY RETRY COUNTER
000006  012767  177770  000314              MOV #-10, CTRY          ; CRC RETRY COUNTER
000014  012767  177770  000310              MOV #-10, STRY          ; SEEK RETRY COUNTER
                                    ;
                                    ;WRITE, WRITE DELETED DATA, OR READ
                                    ;
                                    ; BITS 4 THRU 1 OF PROGRAM LOCATION COMMAND CONTAIN THE FUNCTION
                                    ;
                                    ; BIT 4 = 1 MEANS UNIT 1 ( = 0 MEANS UNIT 0)
                                    ;
                                    ; BITS 3 THRU 1 IS THE COMMAND ( 4 = WRITE, 14 = WRITE DELETED DATA, 6 = READ)
                                    ;
000022  016767  000306  177140      RETRY:  MOV COMMAND, RXCS       ; UNIT + (WRITE, WRITE DELETED DATA, OR READ)
                                    ;
                                    ;WAIT FOR THE TRANSFER REQUEST FLAG THEN TRANSFER THE SECTOR ADDRESS
                                    ;
000030  105767  177134              1$:     TSTB RXCS               ; TEST FOR THE TRANSFER REQUEST FLAG
000034  001775                      BEQ 1$                          ; BEQ UNTIL THE TRANSFER REQUEST FLAG SETS
000036  116767  000274  177126      MOVB SECTOR, RXSA               ; LOAD SECTOR ADDRESS
                                    ;
                                    ;WAIT FOR THE TRANSFER REQUEST FLAG THEN TRANSFER THE TRACK ADDRESS
                                    ;
000044  105767  177120              2$:     TSTB RXCS               ; TEST FOR THE TRANSFER REQUEST FLAG
000050  001775                      BEQ 2$                          ; BEQ UNTIL THE TRANSFER REQUEST FLAG SETS
000052  116767  000262  177112      MOVB TRACK, RXTA                ; LOAD TRACK ADDRESS
                                    ;
                                    ;THE SECTOR AND TRACK ADDRESSES HAVE BEEN TRANSFERRED TO THE RX01
                                    ;
                                    ;WAIT FOR THE DONE FLAG AND CHECK FOR ANY ERRORS
                                    ;
                                    ;IF THE FUNCTION HAS COMPLETED SUCCESSFULLY (NO ERROR FLAG) THEN HALT
                                    ;
```

Figure 10 Write/Write Deleted Data/Read (Sheet 1 of 3)

```
000060  032767  000040  177102  3$:     BIT #DONEBIT, RXCS      ; TEST FOR THE DONE FLAG
000066  001774                          BEQ 3$                  ; BEQ UNTIL THE DONE FLAG SETS
000070  005767  177074                  TST RXCS                ; TEST FOR THE ERROR FLAG
000074  001001                          BNE ERFLAG              ; BNE IF AN ERROR HAS OCCURED
000076  000000                          HALT                    ; OK - COMPLETED
                                ;THE ERROR FLAG IS SET
                                ;
                                ;THE CONTENTS OF THE RXES IS THE ERROR STATUS
                                ;
                                ;IF THE RXES BITS 1 AND 0 = 0 THEN SOME TYPE OF SEEK ERROR OCCURED
                                ;IF THE RXES BIT 0 = 1 THEN A CRC ERROR HAS OCCURED
                                ;IF THE RXES BIT 1 = 1 THEN A PARITY ERROR HAS OCCURED
                                ;
000100  032767  000003  177064  ERFLAG: BIT #3, RXES            ; TEST FOR CRC AND PARITY ERRORS
000106  001414                          BEQ SEEK                ; NOT A PARITY OR CRC [MUST] BE A SEEK
000110  032767  000002  177054          BIT #2, RXES            ; TEST FOR PARITY ERROR
000116  001404                          BEQ CRC                 ; NOT A PARITY ERROR [MUST] BE A CRC
                                ;
                                ;A PARITY ERROR HAS OCCURED
                                ;
                                ;INCREMENT AND TEST THE PARITY ERROR RETRY COUNTER PROGRAM LOCATION " PTRY "
                                ;
                                ;AND RETRY THE " COMMAND " UNTIL THE PARITY ERROR RECOVERS
                                ;
                                ;OR UNTIL THE PTRY COUNTER OVERFLOWS TO 0
                                ;
000120  005267  000202                  INC PTRY
000124  001336                          BNE RETRY               ; RETRY THE COMMAND
000126  000000                          HALT                    ; HARD PARITY ERROR
                                ;
                                ;A CRC ERROR HAS OCCURED
                                ;
                                ;INCREMENT AND TEST THE CRC ERROR RETRY COUNTER PROGRAM LOCATION " CTRY "
                                ;
                                ;AND RETRY THE COMMAND UNTIL THE CRC ERROR RECOVERS
                                ;
                                ;OR UNTIL THE CTRY COUNTER OVERFLOWS TO 0
                                ;
000130  005267  000174          CRC:    INC CTRY
000134  001332                          BNE RETRY               ; RETRY THE COMMAND
000136  000000                          HALT                    ; HARD CRC ERROR
```

Figure 10 Write/Write Deleted Data/Read (Sheet 2 of 3)

```
 91                                     ;THE ERROR FLAG IS SET
 92                                     ;
 93                                     ;THE ERROR IS [NOT] A PARITY ERROR AND IS [NOT] A CRC ERROR
 94                                     ;
 95                                     ;THEREFORE IT MUST BE A SEEK ERROR
 96                                     ;
 97                                     ; (STATE OF RXCS BITS 0 AND 1 ARE 0)
 98                                     ;
 99  000140  012767  340000  177022     SEEK:   MOV #INIT, RXCS         ; INITIALIZE
100                                     ;
101                                     ;INCREMENT AND TEST THE SEEK ERROR RETRY COUNTER PROGRAM LOCATION " STRY "
102                                     ;
103                                     ;AND RETRY THE COMMAND UNTIL THE SEEK ERROR RECOVERS
104                                     ;
105                                     ;OR UNTIL THE CTRY COUNTER OVERFLOWS TO 0
106                                     ;
107  000146  005267  000160                    INC STRY
108  000152  001323                            BNE RETRY               ; RETRY THE COMMAND
109  000154  000000                            HALT                    ; HARD SEEK ERROR
```

Figure 10 Write/Write Deleted Data/Read (Sheet 3 of 3)

In each of the PAR, CRC, and SEEK routines, the command sequence is retried ten times by decrementing the respective retry counter. If an error persists after ten tries, it is a hard error. The retry counters can be set up to retry as many times as desired.

NOTE

A fill buffer function is performed before a write function, and an empty buffer function is performed after a read function.

Empty Buffer Function – Figure 11 shows a program for implementing an empty buffer function. The first instruction sets the number of error retries to ten. The address of the memory buffer is placed in register R0, and the empty buffer command is placed in the RXCS. Existence of a parity error is checked starting at instruction 3$. If a parity error is detected, the empty buffer command is loaded again. If an error persists for ten retries the error is considered hard.

If no error is indicated, the program looks for the transfer request (TR) flag to set. The error flag is retested if TR is not set. Once TR sets, a byte is moved from the RXV11 sector buffer to the core locations of BUFFER. The process continues until the sector buffer is empty and the done bit is set

Fill Buffer Function – Figure 12 presents a program to implement a fill buffer function It is very similar to the empty buffer example.

Bootstrapping the RXV11

The RXV11 bootstrap loader program loads the system monitor from disk into system memory. No system operation can occur until the monitor is contained in system memory. Bootstrapping ("booting") the system can be accomplished via a hardware-implemented bootstrap in the REV11-A, REV11-C, or the BDV11 option, or it can be entered and executed via the console device.

When a bootstrap option is not included in the system, the operator must enter a bootstrap program via the console device. Place the processor in the Halt mode and proceed as shown below; observe that underlined characters are printed by the processor and non-underlined characters are entered by the operator

```
160                                     ;THE FOLLOWING IS A PROGRAMMING EXAMPLE OF PROTOCOL REQUIRED TO
161                                     ;
162                                     ;EMPTY THE  SECTOR BUFFER OF 128 8-BIT BYTES
163                                     ;
164  000242  012767  177770  000056     EENTRY: MOV #-10, PTRY          ; 8 TRYS TO EMPTY THE SECTOR BUFFER
165  000250  012700  000342             ESETUP: MOV #BUFFER, R0         ; PROHGRAMS DATA BUFFER
166  000254  016767  000054  176706             MOV COMMAND, RXCS       ; ISSUE THE COMMAND
167                                     ;
168                                     ;WAIT FOR A TRANSFER REQUEST FLAG BEFORE TRANSFERRING DATA TO THE PROGRAMS
169                                     ;
170                                     ;DATA BUFFER FROM THE RX01 SECTOR BUFFER
171                                     ;
172                                     ;WAIT FOR A DONE FLAG TO INDICATE THE COMPLETION OF THE EMPTY BUFFER COMMAND
173                                     ;
174                                     ;PRIOR TO TESTIN G THE ERROR FLAG
175                                     ;
176  000262  105767  176702             ELOOP:  TSTB RXCS               ; TEST FOR TRANSFER REQUEST FLAG
177  000266  001014                             BNE EMPTY               ; BNE IF TRANSFER REQUEST FLAG IS SET
178  000270  032767  000040  176672             BIT #DONEBIT, RXCS      ; TEST FOR DONE FLAG
179  000276  001771                             BEQ ELOOP               ; BEQ UNTIL THE DONE FLAG SETS
180                                     ;
181                                     ;THE DONE FLAG IS SET
182                                     ;
183                                     ;TEST FOR ANY ERRORS (ONLY ERROR POSSIBLE IS A PARITY ERROR)
184                                     ;
185  000300  005767  176664                     TST RXCS
186  000304  001001                             BNE 1$
187  000306  000000                             HALT                    ; NO ERRORS = OK = COMPLETE
188                                     ;
189                                     ;INCFEMENT AND TEST THE PARITY ERROR RETRY PROGRAM LOCATION " PTRY "
190                                     ;
191                                     ;AND RETRY THE COMMAND UNTIL THE ERROR RECOVERS
192                                     ;
193                                     ;OR UNTIL THE PTRY CUNTER OVERFLOWS TO 0
194                                     ;
195  000310  005267  000012             1$:     INC PTRY
```

Figure 11 Empty Buffer (Sheet 1 of 2)

```
000314  001355                  BNE ESETUP              ; RETRY TO EMPTY THE SECTOR BUFFER
000316  000000                  HALT                    ; HARD PARITY ERROR
                        ;
                        ;THE TRANSFER REQUEST FLAG IS SET
                        ;
                        ;TRANSFER DATA TO THE PROGRAM  DATA BUFFER FROM THE RX01 SECTOR BUFFER
                        ;
000320  116730  176646  EMPTY:  MOVB RXDB, @(R0)+
000324  000756                  BR ELOOP

                        ;THE FOLLOWING 3 PROGRAM LOCATIONS ARE THE ERROR RETRY COUNTERS
                        ;
000326  000000          PTRY:   0                       ; PARITY ERROR RETRY COUNTER
000330  000000          CTRY:   0                       ; CRC ERROR RETRY COUNTER
000332  000000          STRY:   0                       ; SEEK ERROR RETRY COUNTER
                        ;
                        ;PROGRAM LOCATION " COMMAND " CONTAINS THE COMMAND TO BE ISSUED VIA THE LCO IOT
                        ;
                        ;WRITE (4), WRITE DELETED DATA (14), OR READ (6), OR EMPTY BUFFER (2)
                        ;
000334  000000          COMMAND:        0               ; 4, 14, 6, OR 2 + (GO BIT 1 = 1)
                        ;
                        ;PROGRAM LOCATION " SECTOR " CONTAINS THE SECTOR ADDRESS (1 TO 32 OCTAL)
                        ;
000336  000000          SECTOR: 0                       ; 1 TO 32 OCTAL
                        ;
                        ;PROGRAM LOCATION " TRACK " CONTAINS THE TRACK ADDRESS (0 TO 114 OCTAL)
                        ;
000340  000000          TRACK:  0                       ; 0 TO 114 OCTAL
                        ;
                        ;PROGRAM EQUIVALENTS
                        ;
                000040  DONEBIT=40
                040000  INIT=40000
                000342  BUFFER=.
                000542          .=BUFFER+200
                000001          .END
```

Figure 11 Empty Buffer (Sheet 2 of 2)

```
111                                     ;THE FOLLOWING IS A PROGRAMMING EXAMPLE OF THE PROTOCOL REQUIRED TO
112                                     ;
113                                     ;FILL THE SECTOR BUFFER WITH 128 8-BIT BYTES
114                                     ;
115                                     ; NOTE: THE DATA TO FILL THE SECTOR BUFFER CAN BE ASSEMBLED IN CORE IN THE
116                                     ;       EVEN ADDRESSES BYTES OF 128 WORDS OR IN BOTH BYTES OF 64 WORDS
117                                     ;
118  000156  012767  177770  000142   ENTRY: MOV #-10, PTRY          ; 8 TRYS TO FILL THE SECTOR BUFFER
119  000164  012700  000342            SETUP: MOV #BUFFER, R0         ; PROGRAMS DATA BUFFER
120  000170  016767  000140  176772           MOV COMMAND, RXCS       ; ISSUE THE COMMAND
121                                     ;
122                                     ;WAIT FOR A TRANSFER REQUEST FLAG BEFORE TRANSFERRING DATA FROM THE PROGRAMS
123                                     ;
124                                     ;DATA BUFFER TO THE RX01 SECTOR BUFFER
125                                     ;
126                                     ;WAIT FOR A DONE FLAT TO INDICATE THE COMPLETION OF THE FILL BUFFER COMMAND
127                                     ;
128                                     ;PRIOR TO TESTING THE ERROR FLAG
129                                     ;
130  000176  105767  176766            LOOP:  TSTB RXCS               ; TEST FOR TRANSFER REQUEST FLAG
131  000202  001414                           BEQ FILL                ; BEQ IF TRANSFER REQUEST FLAG SET
132  000204  032767  000040  176756           BIT #DONEBIT, RXCS      ; TEST FOR THE DONE FLAG
133  000212  001771                           BEQ LOOP                ; BEQ UNTIL THE DONE FLAG SETS
134                                     ;
135                                     ;THE DONE FLAG IS SET
136                                     ;
137                                     ;TEST FOR ANY ERRORS (ONLY ERROR POSSIBLE IS A PARITY ERROR)
138                                     ;
139  000214  005767  176750                   TST RXCS
140  000220  001001                           BNE 1$
141  000222  000000                           HALT                    ; NO ERRORS = OK = COMPLETE
142                                     ;
143                                     ;INCREMENT AND TEST THE PARITY ERROR RETRY PROGRAM LOCATION " PTRY "
144                                     ;
145                                     ;AND RETRY THE COMMAND UNTIL THE ERROR RECOVERS
146                                     ;
147                                     ;OR UNTIL THE RTRY COUNTER OVERFLOWS TO 0
```

Figure 12 Full Buffer (Sheet 1 of 2)

```
148                                             ;
149  000224  005267  000076                     1$:     INC PTRY
150  000230  001355                                     BNE SETUP               ; RETRY TO FILL THE SECTOR BUFFER
151  000232  000000                                     HALT                    ; HARD PARITY ERROR
152                                             ;
153                                             ;THE TRANSFER REQUEST FLAG IS SET
154                                             ;
155                                             ;TRANSFER DATA FROM THE PROGRAMS DATA BUFFER TO THE RX01 SECTOR BUFFER
156                                             ;
157  000234  113067  176732                     FILL:   MOVB @(R0)+, RXDB       ; PROGRAMS DATA BUFFER IS 64 WORDS IN LENGTH
158  000240  000756                                     BR LOOP
```

Figure 12 Full Buffer (Sheet 2 of 2)

RXV11

Full Length Version	Abbreviated Version (DRIVE 0 ONLY)
@1000/000000 12702 <LF>	
001002/000000 1002n7 <LF>*	@1000/000000 5000 <LF>
001004/000000 12701 <LF>	001002/000000 12701 <LF>
001006/000000 177170 <LF>	001004/000000 177170 <LF>
001010/000000 130211 <LF>	001006/000000 105711 <LF>
001012/000000 1776 <LF>	001010/000000 1776 <LF>
001014/000000 112703 <LF>	001012/000000 12711 <LF>
001016/000000 7 <LF>	001014/000000 3 <LF>
001020/000000 10100 <LF>	001016/000000 5711 <LF>
001022/000000 10220 <LF>	001020/000000 1776 <LF>
001024/000000 402 <LF>	001022/000000 100405 <LF>
001026/000000 12710 <LF>	001024/000000 105711 <LF>
001030/000000 1 <LF>	001026/000000 100004 <LF>
001032/000000 6203 <LF>	001030/000000 116120 <LF>
001034/000000 103402 <LF>	001032/000000 2 <LF>
001036/000000 112711 <LF>	001034/000000 770 <LF>
001040/000000 111023 <LF>	001036/000000 0 <LF>
001042/000000 30211 <LF>	001040/000000 5007 <CR>
001044/000000 1776 <LF>	
001046/000000 100756 <LF>	
001050/000000 103766 <LF>	
001052/000000 105711 <LF>	
001054/000000 100771 <LF>	
001056/000000 5000 <LF>	
001060/000000 22710 <LF>	
001062/000000 240 <LF>	
001064/000000 1347 <LF>	
001066/000000 122702 <LF>	
001070/000000 247 <LF>	
001072/000000 5500 <LF>	
001074/000000 5007 <CR>	

*n = 4 for Unit 0
n = 6 for Unit 1
<LF> = Line Feed
<CR> = Carriage Return

FUNCTIONAL DESCRIPTION

General

This overall system block description covers all hardware components in the RXV11 option. A detailed description is included for the M7946 interface module only. Refer to the *RX01/RX8/RX11 Floppy Disk System Maintenance Manual* for detailed descriptions of hardware contained in the RX01 floppy disk drive.

RXV11 System Block Diagram

The RXV11 floppy disk system consists of four elements (Figure 13):

1. Drive mechanics, which include actuators and transducers (up to two per controller)

2. Read/write electronics, which interface drive mechanics to the μCPU controller
3. μCPU controller, which includes all control logic

4. M7946 interface, which interfaces the LSI-11 bus to the RX01.

There are three levels of data transmission in the floppy disk system (Figure 13):

1. The LSI-11 bus for data transmission between the RXV11 interface module and the processor

2. The RX01 data bus for data transmission between the RX01 μCPU controller and the RXV11 interface module (BC05L-15 interface cable)

3. The disk drive interface (M7946) for data and control information transmission between the read/write electronics and the RX01 μCPU controller.

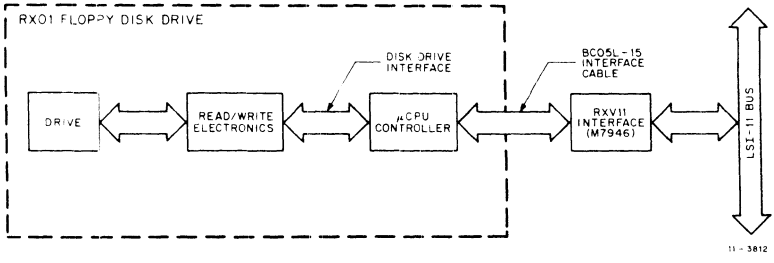


Figure 13 RXV11 System Block Diagram

In addition to the data transmission signals, analog signals between the read/write electronics and mechanical drive control head motion and sense diskette speed and position.

M7946 Interface Signals
Connector J1 on the RXV11 interface module (M7946) provides the interface for the following RX01 signals as shown in Figure 14.

RX INIT L – The RX01 responds to RX INIT L by negating DONE L and moving the head position mechanism of both drives (if two are available) to track 0. The RX01 will also read sector 1 of track 1 of drive 0 and then assert RX DONE L (without error) to indicate successful completion of the initialize function.

RX DONE L – The RX01 asserts RX DONE L to indicate that no RX01 function is in progress. Initiating any function will cause RX DONE L to go false for the duration of that function. Attempting to initiate any function other than initialize while RX DONE L is false is illegal and may result in an error.

RX RUN L – The RXV11 interface asserts RX RUN L to initiate command or data transfers between the interface module and the RX01 μCPU controller. If asserted when RX DONE L is asserted, the byte transferred from the RXV11 interface module to the RX01 is treated as a command. If asserted while RX DONE L is negated, a command is being executed and the byte transferred is considered to be read or write data, sector or track address, or error and status information.

RX OUT L – The RX01 μCPU controller controls this signal to inform the RXV11 interface module of the direction in which it is prepared to transfer a byte. When asserted (low), the direction of serial data transmission is from the RX01 to the RXV11 interface module. When not asserted (high), serial data transmission is from the RXV11 interface module to the RX01. RX OUT L is never asserted when RX DONE L is asserted; when RX DONE L is asserted, the transfer is a command byte from the RXV11 interface module to the RX01. RX INIT L, when asserted, causes RX OUT L to become negated.

RX TRANS REQ L – RX TRANS REQ L, used with RX RUN L and RX OUT L signals, comprise the basic control signal interface between the RX01 and the RXV11 interface module. The RX01 asserts this signal after receiving a new command to indicate that it is ready to receive an address or data byte, or it is ready to output an error status byte or data to the RXV11 interface. Note that this signal is not asserted to initiate a command byte; it is asserted by the RX01 to request transfer of each non-command byte during the execution of a command.

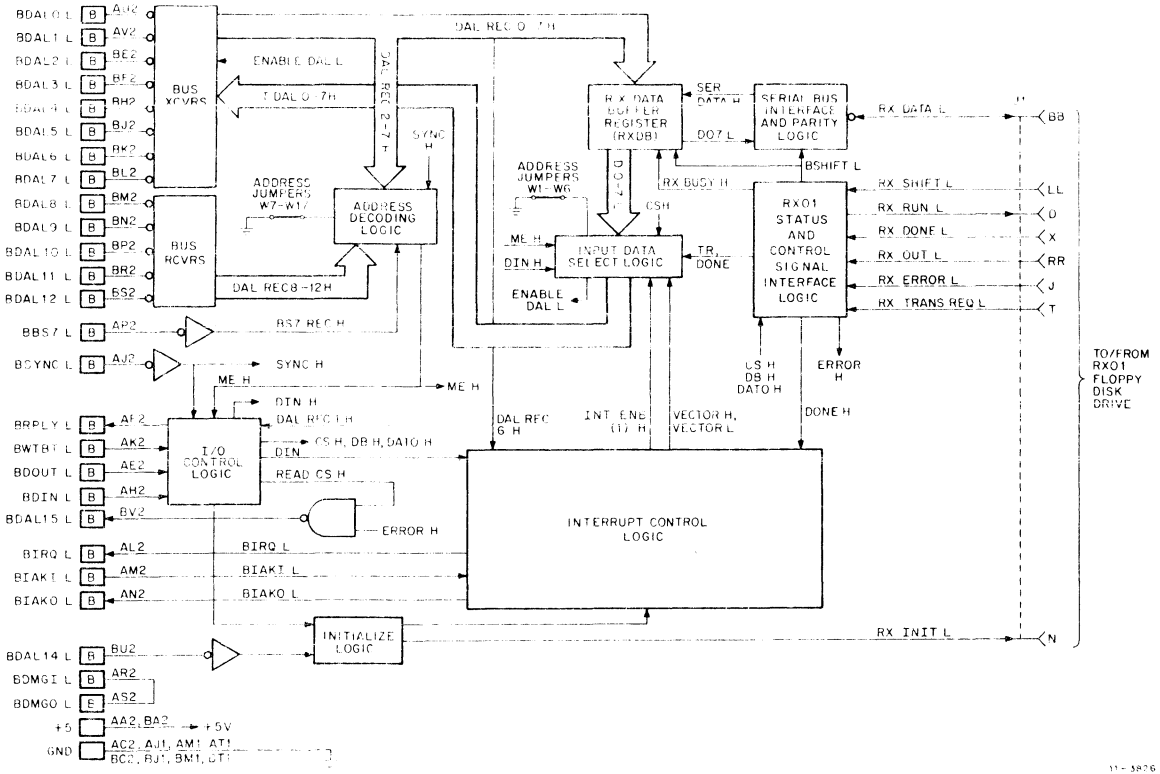


Figure 14 M7946 Interface Module (Logic Block Diagram)

RX DATA L – RX DATA L is the bidirectional serial data line over which all command and data bytes are transferred.

RX SHIFT L – RX SHIFT L is a series of pulses generated by the RX01 which serially shift commands and data into or out of the RXV11 interface module. Pulse width is 200 ns (nominal); pulses occur at 1 μs intervals (nominal).

RX ERROR L – The RX01 asserts this signal when an error is detected. An error results in the RX01 sending RXES information to the RXV11 interface and aborting the present operation; RX DONE L is then asserted. This signal is cleared either by the RXV11 interface asserting RX INIT L or by sending a new command to the RX01.

8/12 BITS L – This signal is not used in RXV11 systems; it is terminated in RX01.

TEV11 TERMINATOR

GENERAL

The TEV11 terminator module provides 120-ohm termination circuits as shown in Figure 1.

SPECIFICATIONS

Identification	M9400-YB
Size	Double
Power	+5 Vdc ± 5% at 0.54 A
Bus Loads	
AC	0
DC	0

FUNCTIONAL DESCRIPTION

General

Each bus signal line terminates with two resistors as shown in Figure 2. These termination resistors are generally contained in a 16-pin, dual-in-line package which is identical to an IC package. Each package contains 14 termination pairs. The values used are shown in the figure. Daisy-chained grant signals are terminated and jumpered. BIAKI L is jumpered to BIAKO L and BDMGI L is connected to BDMGO L via factory-installed jumper W1.

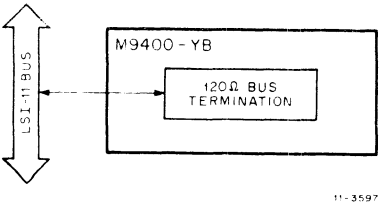


Figure 1 TEV11 Functions

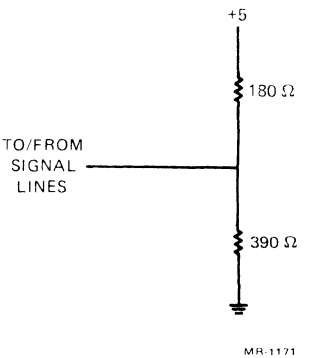


Figure 2 Typical 120-Ohm Bus Termination

CHAPTER 3

USING PROMs

3.1 GENERAL

This chapter contains specific instructions for programming, loading, and erasing MRV11-AC and MRV11-BC PROMs. Instructions are also included for using the QJV11 PROM formatter program. The QJV11 program reads binary object program paper tapes and produces PROM listings and paper tapes for use with automatic PROM loaders.

NOTE

MRV11-AC and MRV11-BC PROMs are used on MRV11-AA and MRV11-BA PROM module options. These options are described in Chapter 2.

3.2 PROGRAMMING NOTES

Generally, programs or data that can be read from read/write memory can also be read from MRV11-AC PROMs. However, special care is required when using the MTPS instruction and KEV11 option EIS instructions. These instructions are listed below.

Mnemonic	Octal Code	Function
MTPS	1064SS	Move byte to PS
MUL	070RSS	Multiply
DIV	071RSS	Divide
ASH	072RSS	Shift arithmetically
ASHC	073RSS	Arithmetic shift combined

These instructions, when executed, fetch source operands via the DATIO bus cycle, rather than the DATI bus cycle. Hence, fetching a source operand from a PROM location will result in a bus error (time-out) because the processor will attempt to write into the addressed location after fetching the operand.

There are two ways to avoid this potential problem. One involves the MRV11-BA UV PROM module (refer to the MRV11-BA option description in Chapter 2) because it has the capability to reply to a DATIO bus cycle although the write operation will not actually "write into" PROM. When configured to reply to DATIO cycles, the above list of instructions can be executed from PROM. However, precautions must be taken if a module that is configured to reply to DATIO cycles is used in any system

running DIGITAL software or bootstraps. Most DIGITAL software, such as RT-11, determines memory size by attempting to write into a location within the memory. If a time-out occurs, it is ensured that no RAM memory is present at that location. PROM memory will normally time-out, as it will not reply to a write cycle. When the MRV11-BA is configured to reply to write cycles, DIGITAL software will assume RAM is present and attempt to write data into it. When the software tries to write data into a PROM, the resultant errors will probably "crash" the system. Therefore any MRV11-BA module used with DIGITAL software or bootstraps must not be configured to reply to DATIO cycles.

The second way to avoid this potential problem is to include separate MOVe instructions within the program. First, MOVe the source operand from the PROM location to a general register or a location in read/write memory. The MTPS or appropriate EIS instruction is then executed using the general register or the read/write temporary (TEMP) location as the source operand.

Two examples are shown below using general register R4 and memory location TEMP as the source operand.

1. Using a general register:

```
MOV NEWPS,R4        ;MOVE SOURCE OPERAND FROM PROM
                    ;TO TEMPORARY (GENERAL) REGISTER.
MTPS R4             ;MOVE NEWPS TO PS
```

2. Using a temporary read/write memory location:

```
MOV CONS,TEMP       ;MOVE SOURCE OPERAND FROM PROM
                    ;TO TEMPORARY LOCATION IN
                    ;READ/WRITE MEMORY.
MUL R1,TEMP         ;MULTIPLY THE CONTENTS OF R1 BY THE
                    ;CONSTANT IN TEMP.
```

When programming MRV11-AC PROMs for use as an RT-11 bootstrap, use 256 X 4 PROMs. This will allow the MRV11-AA address to be configured in the 173000–173776 range. Processor module power-up mode 2 can then be used for automatically bootstrapping RT-11 during system turn-on. Avoid using 512 X 4 PROMs in this application. If 512 X 4 PROMs are used, the MRV11-AA will respond in the 172000–173776 address range and the RT-11 Editor (EDIT.SAV) cannot run properly. This problem exists because the Editor tests for a peripheral device (the VT11) in the 172000–172776 address range. The problem can be avoided by using 256 X 4 PROMs, as described.

3.3 LOADING AND INSTALLING PROMs

3.3.1 General

Loading (blasting, burning, or programming) PROMs is the process where the binary information is stored in the PROM locations. This is a process that must be carefully executed as directed by the appropriate PROM loader manufacturer's instructions.

The procedures for loading and installing PROMs for use in MRV11-AA and MRV11-BA applications are somewhat different. Refer to Paragraph 3.3.2 for the procedures applicable to PROMs used in the MRV11-AA. Similar procedures are included for the MRV11-BA in Paragraph 3.3.3.

3.3.2 MRV11-AA Procedures

3.3.2.1 PROM Types – Basically, two general types of PROMs can be used in the MRV11-AA module: 512 X 4 bit and 256 X 4 bit. The MRV11-AA module contains sockets for installation of up to 32 PROMs. Only the types listed in this chapter are recommended; the particular pinning and I/O levels for the devices listed are fully compatible with the MRV11-AA addressing and data interface. Note that PROMs are always used in multiples of four, comprising the 16-bit word format. Hence, a minimum configuration of four PROMs will comprise either a 256 X 16 or 512 X 16 read-only memory function. Recommended types are listed in Table 3-1.

Table 3-1 MRV11-AA PROM Types

Manufacturer or Source	512 4-Bit PROMs	256 4-Bit PROMs
Digital Equipment Corporation	MRV11-AC*	—
Intersil	IM5624	IM5623
Signetics	82S131*	82S129
MMI	6306	6301

*These parts are identical.

3.3.2.2 Word Format – Each PROM word, when read by the processor, is stored in four 4-bit slices in four separate PROMs. Each word is simultaneously addressed and produces its respective 4-bit portion of the 16-bit word that is read. For example, consider the CMPB instruction shown in Figure 3-1. Its machine code, using the addressing modes shown, is 121343_8 or 1010001011100011_2. The binary bits are stored in PROMs numbered from 1 to 4. Output pins, as indicated, will yield the read data bits for this instruction when addressed.

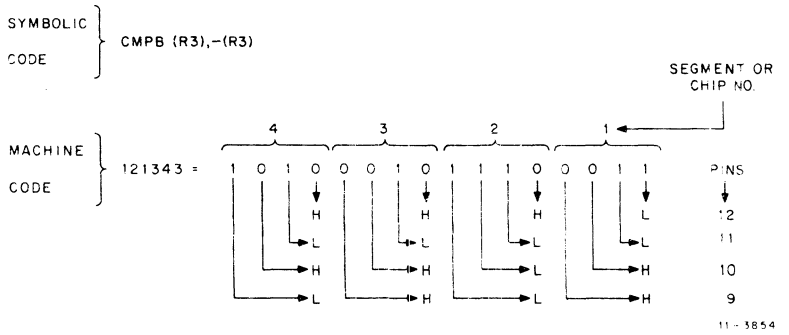


Figure 3-1 MRV11-AA Data Format

Since the word format is contained in four 4-bit slices (one slice in each PROM), the user must load each PROM with successive memory locations. This information can be generated manually—an error-prone, time-consuming process—or it can be generated automatically using the optional QJV11 PROM formatter program, described later.

3.3.2.3 Addressing – PROMs, when installed in the MRV11-AA module, are addressed by low-active address bits. When loading PROMs, the user must be careful that the correct addressing technique is used. An example of this addressing technique, relative to PROM pins, is provided in Table 3-2. Note that 256 X 4 bit and 512 X 4 bit PROMs are addressed in exactly the same manner, except for pin 14, which is A8 in the 512 X 4 bit part, and CE in the 256 X 4 bit part. Also note that LSI-11 bus address bit 0 (DAL0 L) is not used in this application since all read operations are 16-bit word bus transfers.

Table 3-2 MRV11-AA PROM Addressing

Address*		8	7	6	5	4	3	2	1	←Address (DAL) Bits
Octal	Binary	14	1	2	3	4	7	6	5	←PROM Chip Pins
0	000000000	H	H	H	H	H	H	H	H	
2	000000010	H	H	H	H	H	H	H	L	
4	000000100	H	H	H	H	H	H	L	H	
6	000000110	H	H	H	H	H	H	L	L	
10	000001000	H	H	H	H	H	L	H	H	
12	000001010	H	H	H	H	H	L	H	L	Actual
14	000001100	H	H	H	H	H	L	L	H	Logic
16	000001110	H	H	H	H	H	L	L	L	Levels
20	000010000	H	H	H	H	L	H	H	H	Required
⋮										(256_{10} Locations)
774	111111100	L	L	L	L	L	L	L	H	
776	111111110	L	L	L	L	L	L	L	L	

*Address bit 0 is not used; hence, only even-numbered addresses are shown.

The optional QJV11 PROM formatter program addresses PROMs in the manner described.

The MRV11-AA address word format for 512 X 4 and 256 X 4 PROM applications is shown in Figure 3-2. Note that BDAL0 is not used in the address word format; BDAL1 corresponds to PROM chip address bit A0. The 4K bank select bits and 2K segment select bit (256 X 4 PROM applications only) are jumper-configured on the MRV11-AA module.

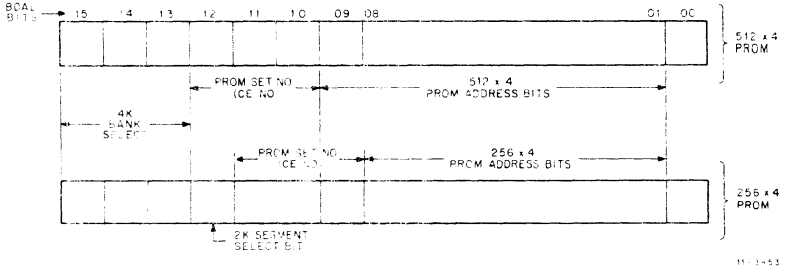


Figure 3-2 MRV11-AA Address Word Format

3.3.2.4 Installing PROMs – After PROMs are properly programmed, loaded, and verified, they can be installed on the properly configured MRV11-AA module (as described in Chapter 2). Refer to Figure 3-3 for proper location of PROMs. Observe that PROMs are always installed in sets of four—one for each segment. Segment and set numbers correspond to those indicated in the QJV11 PROM listing output.

An addressing summary for PROM sets as arranged by physical locations (CE numbers marked on the MRV11-AA module) is provided in Table 3-3.

Table 3-3 MRV11-AA PROM Addressing Summary

	512 × 4 PROMs			256 × 4 PROMs		
	Address Range			Address Range		
Set No.	Decimal	Octal	Physical Location	Decimal	Octal	Physical Location
0	0–511	0–11777	CE0	0–255	0–777	CE0
1	512–1023	2000–13777	CE1	256–511	1000–1777	CE4
2	1024–1545	4000–15777	CE2	512–767	2000–2777	CE1
3	1546–2047	6000–17777	CE3	768–1023	3000–3777	CE5
4	2048–2557	10000–11777	CE4	1024–1279	4000–4777	CE2
5	2560–3071	12000–13777	CE5	1280–1545	5000–5777	CE6
6	3072–3583	14000–15777	CE6	1546–1791	6000–6777	CE3
7	3584–4095	16000–17777	CE7	1792–2047	7000–7777	CE7

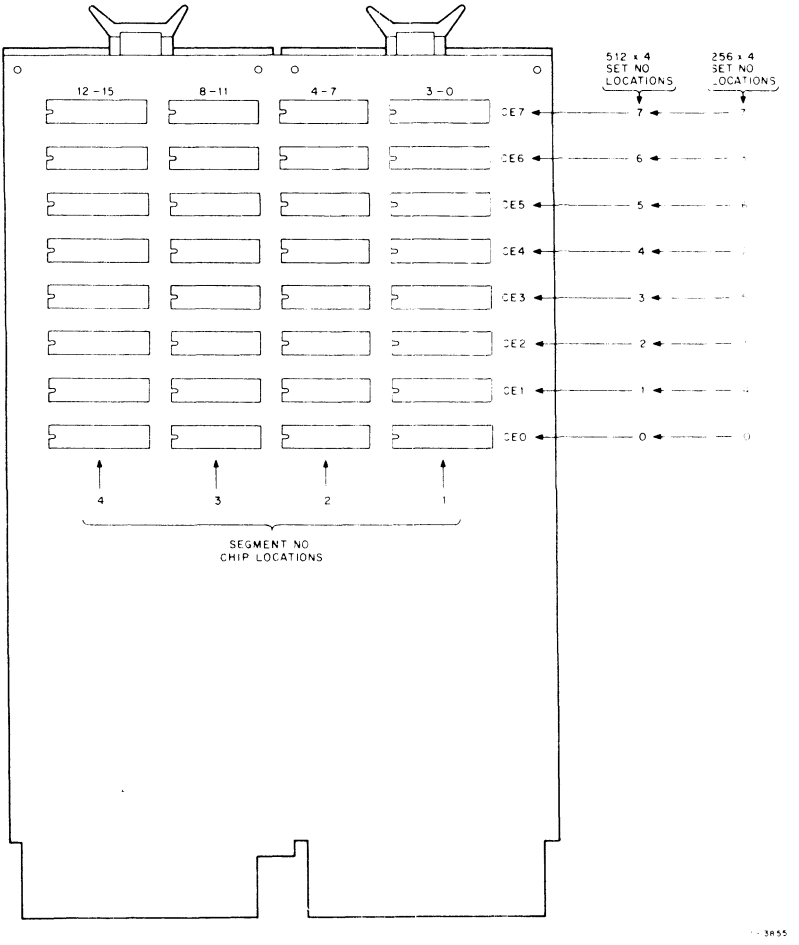


Figure 3-3 PROM Set and Segment Positions on the MRV11-AA Module

3.3.3 MRV11-BA Procedures

3.3.3.1 Data Word Format – Each PROM word, when read by the processor, is stored in two bytes in two separate PROMs. Each word is simultaneously addressed and produces its respective 8-bit portion of the 16-bit word that is read. Since the word format is contained in two 8-bit bytes (one byte in each PROM), the user must load each PROM with successive memory locations. This information can be generated manually or it can be generated using the optional QJV11 PROM formatter program described later.

3.3.3.2 Addressing – PROM integrated circuits, when installed in the MRV11-BA module, are addressed by high-active address bits. When loading PROMs, the user must be careful that the correct addressing technique is used. An example of this addressing technique, relative to PROM pins, is provided in Table 3-4. Note that LSI-11 bus address bit operations are 16-bit word bus transfers.

3.3.3.3 Installing PROMs – PROMs should be installed in the MRV11-BA sockets shown in Chapter 2 (MRV11-BA Option Description). PROMs are normally installed starting with the first 1K locations (E28 and E29). Check PROM size jumpers to ensure that they agree with the number of PROMs installed. A so, be sure to install the low byte and high byte PROMs in appropriate sockets.

3.3.3.4 Erasing PROMs – PROMs can be erased by exposure to ultraviolet light at a wavelength of 2537Å. The recommended integrated light (light intensity X exposure time) is 10 W-s/cm^2. The lamp is normally placed approximately 2.54 cm (1 in) away from the PROM to be erased and turned on for a period of time. The time required can be determined empirically or refer to typical times recommended by PROM integrated circuit manufacturers. Typical times may vary from 10 to 30 minutes (approximately).

3.4 PROM FORMATTING USING THE QJV11 PROGRAM

3.4.1 General

The QJV11 PROM formatter program is a paper tape software option that greatly reduces the work required for coding binary patterns for individual PROM chips. Object tapes punched in absolute loader format are the input to the program. QJV11 will produce and verify PROM tapes and listings for PROMs for use in the MRV11-AA and MRV11-BA, and PROMs in other configurations for special user applications.

3.4.2 Loading QJV11

QJV11 is supplied on punched paper tape in absolute loader format. Load the program using the absolute loader program (DEC-11-UABLB-A-PO) or the REV11-A or REV11-C AL (absolute loader) command.

Table 3-4 MRV11-BC PROM Addressing

Address*		10	09	08	07	06	05	04	03	02	01	←Address Bits	
Octal	Binary	22	23	1	2	3	4	5	6	7	8	←PROM Pins	
0	0000000000	L	L	L	L	L	L	L	L	L	L		
2	0000000001	L	L	L	L	L	L	L	L	L	H		
4	0000000010	L	L	L	L	L	L	L	L	H	L		
6	0000000011	L	L	L	L	L	L	L	L	H	H	Actual	
10	0000000100	L	L	L	L	L	L	L	H	L	L	Logic	
12	0000000101	L	L	L	L	L	L	L	H	L	H	Levels	
14	0000000110	L	L	L	L	L	L	L	H	H	L	Required	
.												(1024_{10} Locations)	
.													
.													
3776	1111111111	H	H	H	H	H	H	H	H	H	H		

*Bus address bit 0 is not used; hence, only even-numbered addresses are shown.

Hardware requirements include 8K read/write memory (minimum), and either a high-speed paper tape reader (CSR address = 177550) or a low-speed reader (Teletype®) used as the console terminal (CSR address = 177560). QJV11 is self-starting; when it has been correctly loaded, the program automatically starts and the initial message shown in Figure 3-4 is displayed. QJV11 is now ready to receive specific input parameters.

```
PROM V01-00

ENTER AN OCTAL VALUE IN RESPONSE TO QUESTIONS
WHICH REQUIRE A NUMERIC RESPONSE. TYPE 'Y' FOR
YES AND 'N' OR NOTHING FOR NO. TERMINATE ALL
RESPONSES WITH A <CR> (CARRIAGE RETURN).
RUBOUT MAY BE USED TO DELETE ONE CHARACTER AT
A TIME BEFORE <CR> IS TYPED. CTRL/U MAY BE
USED TO DELETE THE ENTIRE RESPONSE. CTRL/O
MAY BE TYPED TO TURN OFF OUTPUT TO THE
TERMINAL.                                          } Initial Message

HOW MANY WORDS ARE IN A PROM? 1000
HOW MANY BITS ARE IN A PROM WORD? 4
HOW MANY PROMS ARE USED IN PARALLEL? 4
ARE THE DATA BITS INVERTED? N
ARE THE ADDRESS LINES INVERTED? Y
HOW MANY BYTES ARE IN THE AREA TO BE
OUTPUT? 20000
WHAT IS THE STARTING ADDRESS OF THE AREA TO
BE OUTPUT? 0
IS YOUR INPUT/OUTPUT DEVICE ON THE HIGH SPEED
READER/PUNCH? Y
READY INPUT, TYPE <CR> WHEN READY. <CR>           } Input Parameters

DO YOU WISH TO PUNCH TAPES? Y
DO YOU WANT TO VERIFY A TAPE? N
DO YOU WANT A LIST OF THE PROM CONTENTS? Y
DO YOU WANT IT ON A LINE PRINTER? Y
DO YOU WISH TO MAKE ANOTHER TAPE? N               } QJV11 Operation
```

Figure 3-4 QJV11 Program Execution (for 512 X 4 PROMs)

3.4.3 Entering Parameters

QJV11 requires certain inputs that must be supplied for each PROM loading session. The dialogue between the QJV11 user and the program is as shown in Figure 3-4 for 512 X 4 PROMs (to be used in the MRV11-AA PROM module); a similar example for 1K X 8 PROMs (for use in the MRV11-BA module) is shown in Figure 3-5.

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```
ENTER AN OCTAL VALUE IN RESPONSE TO QUESTIONS
WHICH REQUIRE A NUMERIC RESPONSE. TYPE 'Y' FOR
YES AND 'N' OR NOTHING FOR NO. TERMINATE ALL
RESPONSES WITH A <CR> (CARRIAGE RETURN).
RUBOUT MAY BE USED TO DELETE ONE CHARACTER AT
A TIME BEFORE <CR> IS TYPED. CTRL/U MAY BE
USED TO DELETE THE ENTIRE RESPONSE. CTRL/O
MAY BE TYPED TO TURN OFF OUTPUT TO THE
TERMINAL.                                          Initial Message

HOW MANY WORDS ARE IN A PROM? 2000
HOW MANY BITS ARE IN A PROM WORD? 10
HOW MANY PROMS ARE USED IN PARALLEL? 2
ARE THE DATA BITS INVERTED? N
ARE THE ADDRESS LINES INVERTED? N
HOW MANY BYTES ARE IN THE AREA TO BE
OUTPUT? 20000                                      Input Parameters
WHAT IS THE STARTING ADDRESS OF THE AREA TO
BE OUTPUT? 0
IS YOUR INPUT/OUTPUT DEVICE ON THE HIGH SPEED
READER/PUNCH? Y
READY INPUT, TYPE <CR> WHEN READY. <CR>

DO YOU WISH TO PUNCH TAPES? Y
DO YOU WANT TO VERIFY A TAPE? Y
READY INPUT, TYPE <CR> WHEN READY. <CR>            QJV11 Operation
DO YOU WANT A LIST OF THE PROM CONTENTS? Y
DO YOU WANT IT ON A LINE PRINTER? N
```

Figure 3-5 QJV11 Program Execution (for 1K X 8 PROMs)

The first parameter to be entered is the number of words (locations) in a PROM. The parameter is requested in the form of a question at the end of the initial message. Operator response to QJV11 requests in Figures 3-4 and 3-5 are underlined. Refer to Table 3-5 for a list of valid parameter inputs for specific applications.

When reading source tapes for MRV11-AA programs that are not greater than 4K, only a single pass of the source tape is required, the QJV11 source buffer is 4K words (4096 X 16 bits). However, longer programs will require one additional pass for each 4K word buffer storage. The appropriate portion of the program is read into the buffer when reading the source tape as specified by the "STARTING ADDRESS OF THE AREA TO BE OUTPUT." Hence, the starting addresses shown in Table 3-5 are applicable for both multiple-pass programs to specify the starting address for that pass and programs that do not reside in the first 4K of system memory (addresses 0–17776).

Table 3-5 QJV11 Input Parameters

Parameter	MRV11-AA Applications		MRV11-BA Applications	Special Applications
	512 × 4 PROMs	256 × 4 PROMs	1K × 8 PROMs	
No. words in a PROM (N_8)	1000	400	2000	Any integer power of two (2000 max.)
No. bits in a PROM word (N_8)	4	4	10	1, 2, 4, or 10 (8_{10})
No. PROMs used in parallel	4	4	2	Any number; however, No. bits × No. PROMs must not exceed 20 (16_{10}).
Are data bits inverted	N	N	N	N or Y
Are addr. lines inverted	Y	Y	N	N or Y
How many bytes in the area to be output (N_8)	20000	10000	20000	Any integer power of two (20000 max.)
Starting Address	0, 20000, 40000, 60000, 100000, etc.	0, 10000, 20000, 30000, 40000, etc.	0, 20000, 40000, 60000, 100000, etc.	Any integer multiple of the no. of bytes in the area to be output.
I/O device on the H.S. reader/punch	Y or N	Y or N	Y or N	Y or N

The final input to QJV11 is the source program to be loaded into the PROMs. The program must be in absolute loader format. Place the source tape in the tape reader. Press the RETURN key (shown as <CR> in program examples) on the console device to initiate tape reading.

3.4.4 QJV11 Operation

3.4.4.1 General – Once the input parameters and source program have been entered, QJV11 is ready to output tapes or listings, or to verify tapes. Operation is simple: respond to QJV11 questions by typing Y or N to indicate the operation(s) desired. The Y answers cause the appropriate QJV11 function to execute immediately. The examples shown in Figures 3-4 and 3-5 do not contain the PROM program listing because the separate line printer was selected for the listing. (QJV11 assumes a line printer CSR address = 177514.) If the line printer was not selected, the listing would appear immediately below the listing request.

3.4.4.2 PROM Paper Tape Formats – The QJV11 output tape is punched with as many segments as there are PROMs to be loaded for a particular application. A segment contains the information necessary for loading one PROM. Since multiple PROMs are normally required for the 16-bit PDP-11 word format, either two segments (MRV11-BA applications) or four segments (MRV11-AA applications) are required, comprising a set. Therefore, the minimum-size QJV11 output would occur when programming a single set of two PROMs for the MRV11-BA or four PROMs for the MRV11-AA.

The tape is punched for MRV11-AA applications as shown in Figure 3-6. Special alternate punched frames (16 total) identify that a PROM set follows. This area is followed by 32 frames with all frames punched (377_8), followed by an unpunched frame (0). The first data frame follows immediately after the unpunched frame.

This frame contains the low-order four bits of the 16-bit PROM word at the lowest address (0) in this PROM set; the bits are read over BDAL0–3 bus lines. Successive frames contain 4-bit slices, each representing the 4-bit contents of PROM location. A frame is punched for each of the 256 or 512 locations in the PROM segment. Frames are punched in high-active PROM address sequence rather than LSI-11 bus address sequence. (LSI-11 bus address bits are inverted; hence, PROMs are programmed starting at the highest bus address or lowest PROM location address.)

The punched tape for MRV11-BA applications will differ from the MRV11-AA type. Instead of the first data frame containing four bits, this frame contains the low-order eight bits of the 16-bit PROM word at the lowest address (0) in this PROM set; the bits are read over BDAL (0:7) bus lines. Successsive frames contain 8-bit bytes, each representing the

8-bit contents of a PROM location. A frame is punched for each of the 1K locations in the PROM segment. Frames for MRV11-BA applications are punched in high-active PROM address sequence.

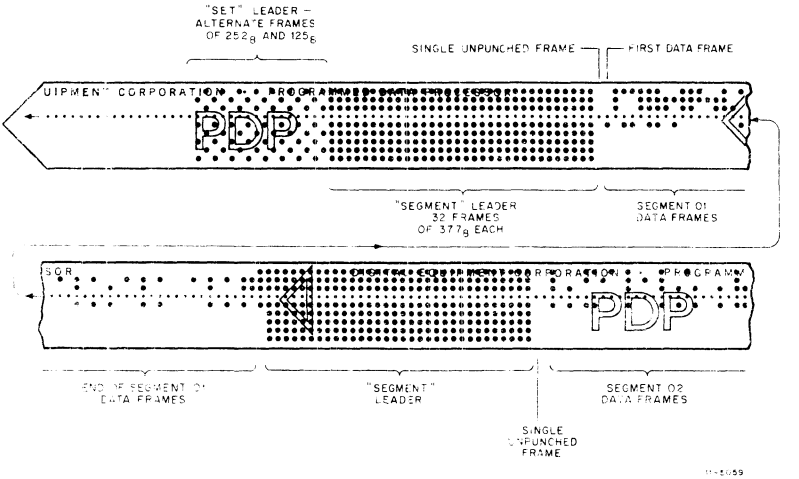


Figure 3-6 QJV11 PROM Tape Format for MRV11-AC Applications

3.4.4.3 Verifying Tapes – Tapes punched by QJV11 can be verified by comparing the punched tape with the QJV11 source buffer contents. Respond to the "DO YOU WANT TO VERIFY A TAPE?" request by typing Y <CR>. The program responds with "READY INPUT, TYPE <CR> WHEN READY." Place the tape in the reader and press the RETURN key on the console device.

If an error is found, the program responds with "ERROR VERIFYING TAPE." When an error is found, it is necessary to punch another tape. If errors are not found, the program responds with "DO YOU WANT A LIST OF THE PROM CONTENTS?"

3.4.4.4 QJV11 PROM Listing Formats – Sample portions of PROM listings for MRV11-AA and MRV11-BA applications are shown in Figures 3-7 and 3-8, respectively. The listings are organized by sets. Each set contains the successive PROM addresses, octal and binary codes for each of the PROM sets, the system memory address obtained from the absolute loader format source tape, and the octal content of the 16-bit PROM word.

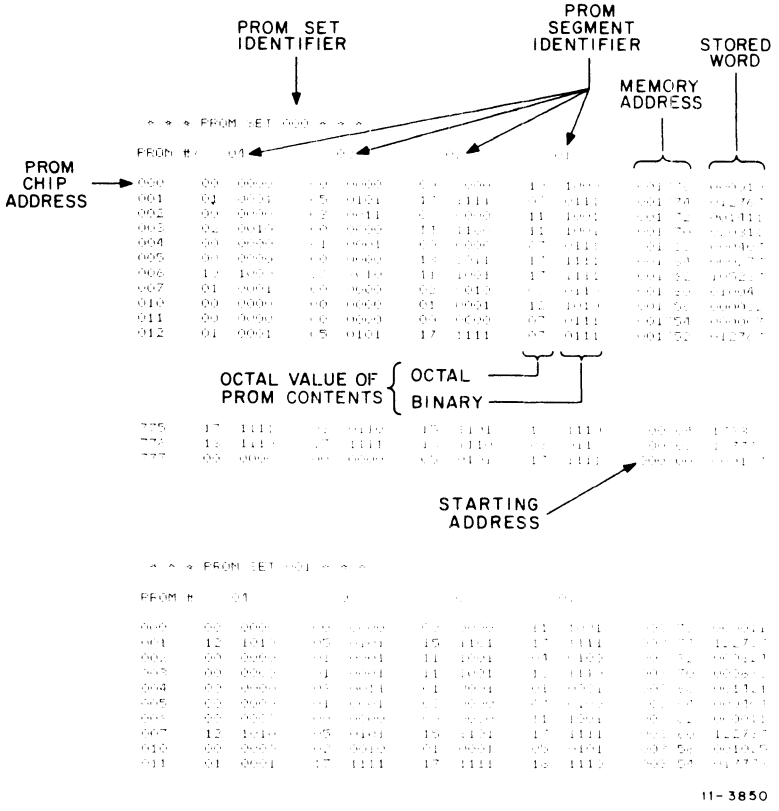


Figure 3-7 QJV11 PROM Listing Format for MRV11-AA Applications

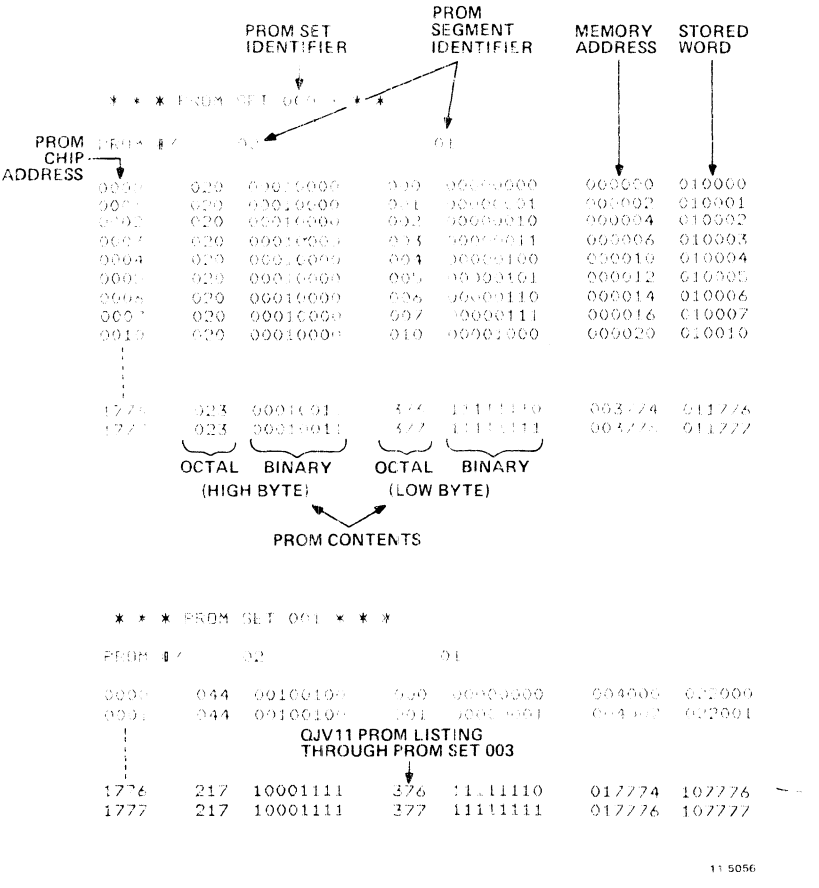


Figure 3-8 QJV11 PROM Listing Format for MRV11-BA Applications

3.4.4.5 Using QJV11 PROM Tapes – PROM tapes can be used with automatic PROM loaders, such as those manufactured by DATA I/O Corporation and PRO-LOG Instruments Corporation. Refer to documentations supplied with the PROM loader for the procedure for using the PROM tapes generated by QJV11.

CHAPTER 4

HARDWARE OPTIONS

4.1 INTRODUCTION

This chapter contains detailed descriptions, specifications, and installation and operation information for LSI-11 bus hardware options. This chapter is organized into several subgroups as follows:

- Backplanes
- Enclosures
- Cabinets
- Wire-Wrappable Modules
- Power Supply
- Cables and Connectors

General information for options contained within each subgroup is summarized in Table 4-1. The option designation is printed on the top of each page to assist in locating a specific option.

Table 4-1 Hardware Option Summary

Option	Description	Remarks
	Backplanes	
H9270	A 4 X 4 (four rows of four slots each) backplane with card guide assembly. LSI-11 bus in rows A-B and C-D.	Accepts 8 double-height modules or 4 quad-height modules or combinations of both.
H9273-A	A 9 X 4 (nine rows of four slots each) backplane with card guide assembly. LSI-11 bus in rows A-B only. Special interconnect bus in rows C-D.	Accepts double-height or quad-height modules.
H9281	A 2-slot backplane available in 4-, 8-, or 12-slot options.	Accepts double-height modules only.
DDV11-B	A 9 X 6 (nine rows of six slots each) backplane. LSI-11 bus in rows A-B and C-D. Rows E-F are unbussed except for +5 V and ground.	Accepts 18 double-height or 9 quad-height modules or combinations of both.

Table 4-1 Hardware Option Summary (Cont)

Option	Description	Remarks
	Enclosures	
H909-C	A 13.3 cm (5.25 in) high, 48.3 cm (19 in) wide enclosure which can be mounted in a 48.3 cm (19 in) rack or as a stand-alone. Accommodates the DDV11-B backplane or a 9 X 6 system mounting unit or houses non-standard mounting arrangement.	Includes cooling fan, cord guide, cable restraints, front bezel, and connector block
BA11-M	A 8.9 cm (3.5 in) high, 48.3 cm (19 in) wide expansion box which can be mounted in 48.3 cm (19 in) rack.	Includes H9270 backplane, H780 power supply, blank front panel or bezel, and cooling fan.
BA11-N	A 13.2 cm (5.19 in) high, 48.3 cm (19 in) wide mounting box which can be mounted in a 48.3 cm (19 in) rack.	Includes H9273-A backplane, H786 power supply, H403-A ac input panel, blank front panel or bezel, and cooling fan
	Cabinets	
H984-B	A low-profile cabinet with four casters. Provides mounting space for standard 48.3 cm (19 in) panels and enclosures in rack at both front or rear.	Includes distribution panel (115 Vac, 230 Vac)
H9800-A	A low-profile system desk with casters. Provides mounting space for standard 48.3 cm (19 in) panels and enclosures.	Includes distribution panel (115 Vac, 230 Vac)

Table 4-1 Hardware Option Summary (Cont)

Option	Description	Remarks
	Wire-Wrappable Modules	
W9511	LSI-11 bus compatible quad-height module which accepts a variety of IC package types and discrete components. No DIP sockets included.	Includes 40-pin male connector on module.
W9514	Same as the W9511 (above) except with 58 pre-mounted DIP sockets.	Same as above
W9512	Double-height module. No DIP sockets included.	Same as above
W9515	Same as W9512 except with 25 premounted DIP sockets.	Same as above
	Power Supply	
H780	Provides +5 V ± 4%, 18 A (max) and +12 V ± 3%, 3.5 A (max) at 110 Vac and features line-time clock, and power-fail/automatic restart. Available primary power of 115 or 230 Vac and with or without master and slave console.	
	Cables and Connectors	
	Six preassembled cable types are available in a variety of lengths. All consist of an H856 connection on one end. Two BC05L cables are used in both the BCV1B option and the BCV1A option.	

4.2 BACKPLANE OPTIONS

The four backplane options available for the LSI-11 bus are presented in the following paragraphs. They include:

H9270
H9273-A
H9281
DDV11-B

4.2.1 H9270 Backplane

The H9270 consists of an 8-slot backplane with a card guide assembly. This backplane is designed to accept up to eight double-height modules (including processor), four quad modules, or a combination of quad and double-height modules. When used for bus expansion in multiple backplane systems, the H9270 provides space for up to six option modules, plus the required expansion cable connector module(s) and/or terminator module.

Mounting dimensions and possible methods of mounting the H9270 backplane are shown in Figure 4-1. Option positions are shown in Figure 4-2. Slot numbers indicate device interrupt and/or DMA priority in LSI-11 bus systems. The lowest numbered positions receive the highest priority.

Mounting the Backplane

Mounting of the H9270 backplane can be accomplished in any one of three planes, as shown in Figure 4-1.

DC Power Connections

Voltage and Current Requirements – A power supply for a single H9270 backplane LSI-11 system should have the following capacity:

+5 V ± 5% load; 0–18 A static/dynamic
+12 V ± 3% load; 0–2.5 A static/dynamic
+5 ripple: less than 1% of nominal voltage
+12 ripple: less than 150 mV p-p (frequency 5 kHz)

NOTE

Regulation at the H9270 backplane must be maintained to the specifications listed above.

The H780 power supply option provides sufficient dc power and generates the required bus signals. Installation details are included in the H780 power supply description (Paragraph 4.6).

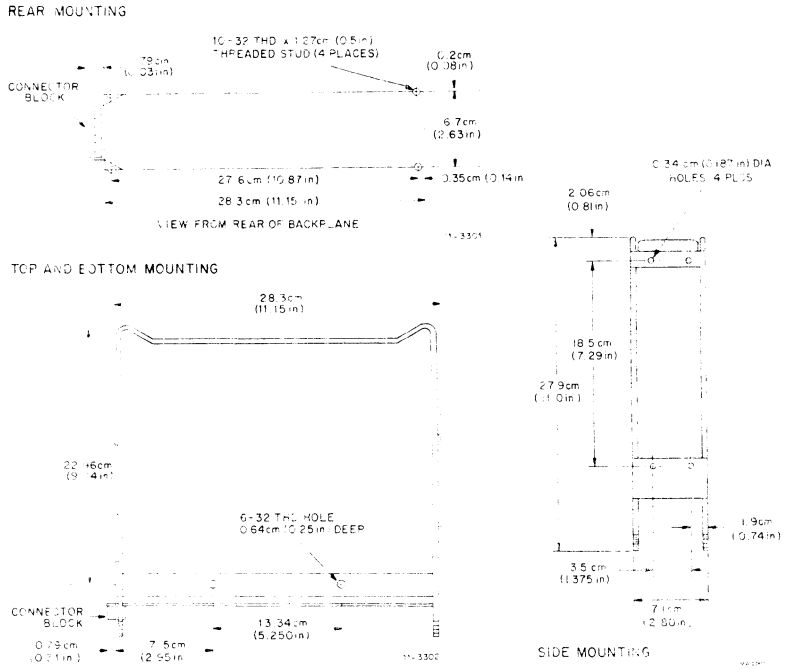


Figure 4-1 Backplane Mounting

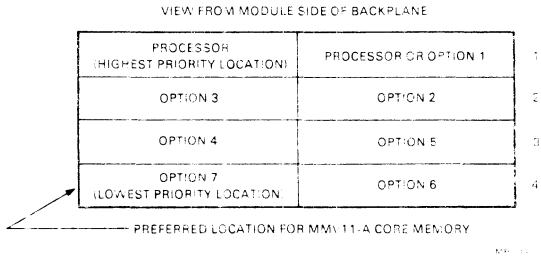


Figure 4-2 H9270 Option Positions

A power supply for a DDV11-B, or a multiple-backplane system using H9270 backplanes, should have the same voltage regulation and ripple specifications as listed for the single H9270 backplane. However, it will be necessary to calculate the actual power requirements, based on individual power requirements for modules used in the system.

Backplane Power Connections – If the H780 power supply option is not used, perform the following steps to connect power to the H9270 backplane (Figure 4-3).

1. Select wire size. (14 gauge is recommended.) Consider load current and distance between the power supply and backplane.

2. For a standard system, connect the applicable wires to the H9270 connector block per Table 4-2.

   For battery backup, remove the jumper between +5 V and +5 B and connect the applicable wires to the H9270 connector block.

3. Connect the ground terminals at the power sources.

4. It is recommended that the backplane frame/casting be electrically connected to system/power supply ground.

The signal connections to the H9270 backplane are shown in Figure 4-4.

Table 4-2 H9270 Backplane Standard Power Connections

Power Source (From)		H9270 Connector Block (To)
+12 V	+12 V	
+5 V	+5 V	Factory
	+5 B	Connected
GND	GND	Factory
GND	GND	Connected
−12 V	−12 V	This voltage is not required. The connection is available for custom interfaces.

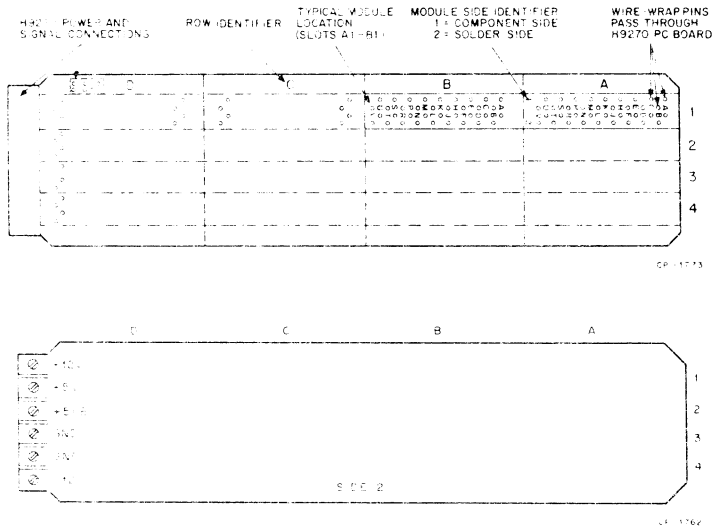


Figure 4-3 H9270 Backplane Terminal Block (Pin Side View Shown)

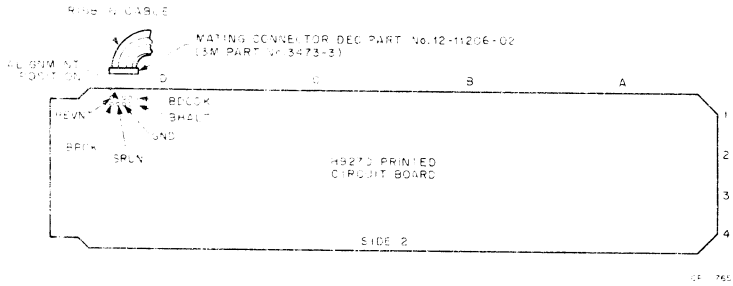


Figure 4-4 H9270 Backplane Signal Connections (Pin Side View Shown)

4.2.2 H9273-A Backplane

The H9273-A backplane logic assembly consists of a 9 X 4 backplane (nine rows of four slots each) and a card frame assembly. The H9273-A backplane logic assembly is shown in Figure 4-5. Power and signals are supplied to the backplane to connectors J7 and J8. These connectors are shown in Figures 4-5, 4-6, and 4-7. Connectors J9 (GND) and J10 (–12 V) are also shown in Figure 4-6.

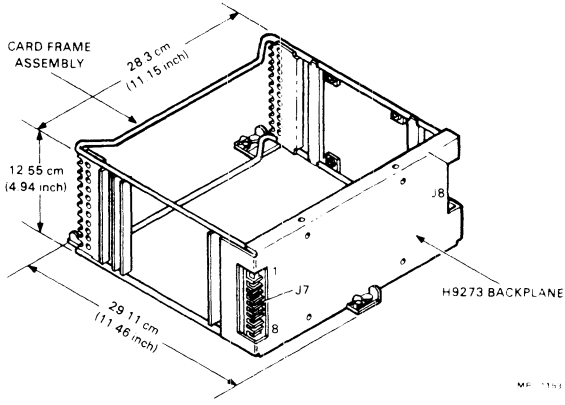


Figure 4-5 H9273-A Backplane Logic Assembly

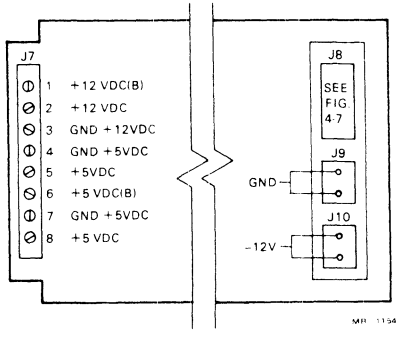


Figure 4-6 H9273-A Power Connections

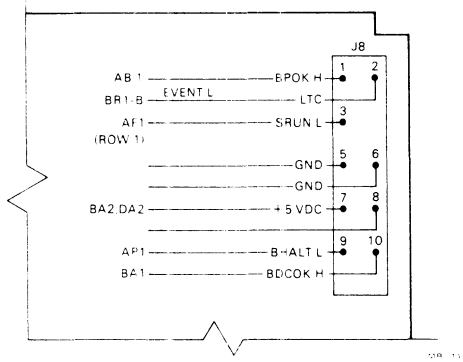


Figure 4-7 H9273-A Signal Connections

The H9273-A backplane is designed to accept both double-height and quad-height modules with the exception of the MMV11-A core memory module. The backplane structure is unique in that it provides two distinct buses: the LSI-11 bus signals (slots A and B) and the CD bus (slots C and D). The connectors that comprise this backplane are arranged in nine rows (Figure 4-8). Each connector has two slots, each of which contains 36 pins, 18 on either side of the slot.

The connectors designated "Connector 1" in Figure 4-8 are wired according to the LSI-11 bus specification. Slots A and B carry the LSI-11 bus signals and are termed the LSI-11 bus slots. The connectors designated "Connector 2" are wired for +5 V and ground, and have no connections to the LSI-11 bus; instead, C- and D-slot pins on side 2 of each row are connected to the C-and D-slot pins on side 1 in the next lower row. Details on the CD interconnection scheme are depicted in Figure 4-9.

Installation

The H9273-A backplane logic assembly is designed to mount into a BA11-N mounting box or equivalent. Refer to the BA11-N mounting box description (Paragraph 4.3.3) for more information.

NOTE

Connector block pins do not extend beyond the H9273-A printed circuit etch card, thus eliminating the possibility of backplane wire-wrapping.

Three jumpers (W1, W2, and W3) are shown in Figure 4-8. Jumper W1 enables the line-time clock when inserted and disables it when removed.

NOTE

Only one BA11-N mounting box in any system may have the line-time clock enabled.

When inserted, jumpers W2 and W3 allow the LSI-11 quad-height CPU to run in row 1. Jumpers W2 and W3 are removed when the backplane is used as an expansion backplane in a system.

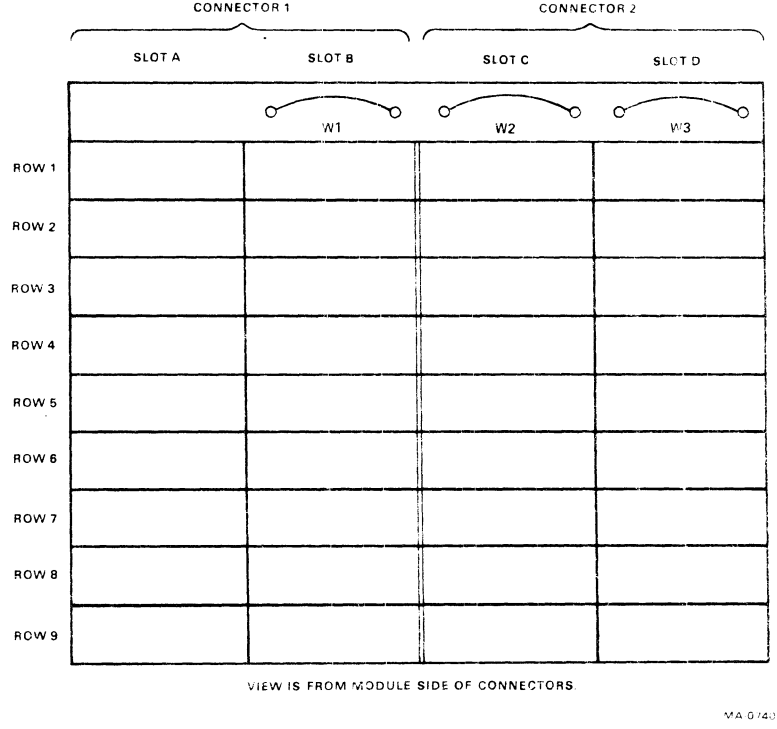


Figure 4-8 H9273-A Backplane Connectors

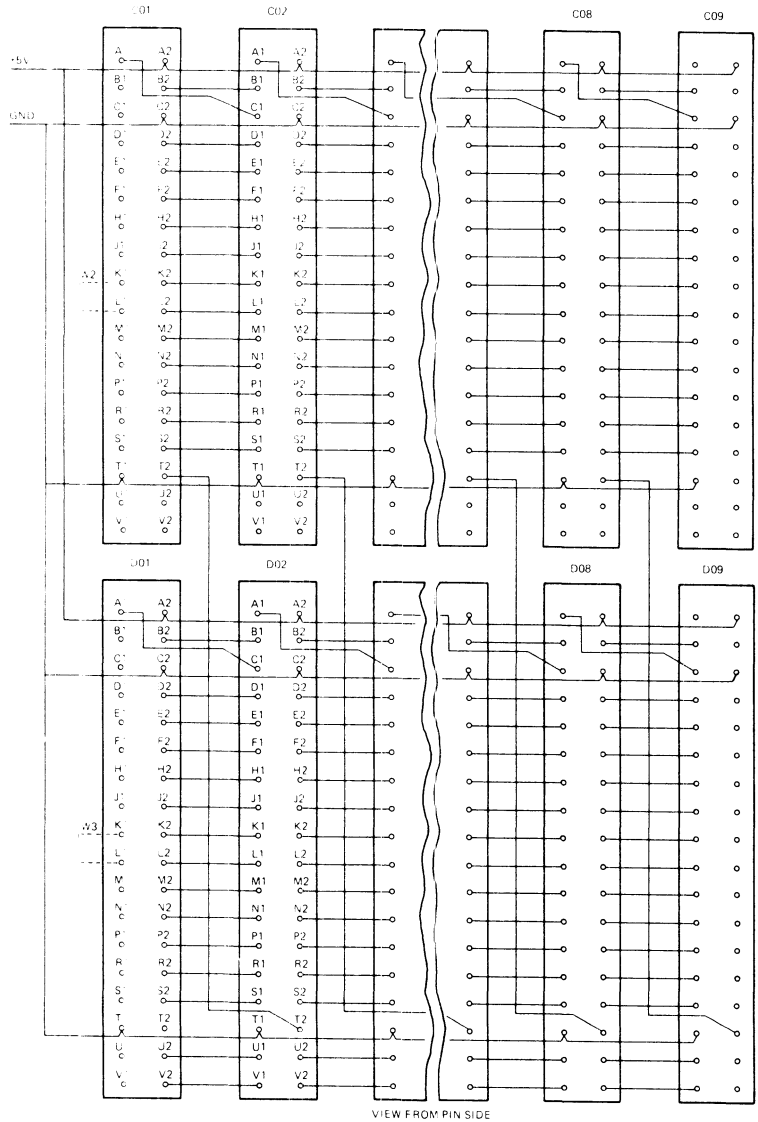


Figure 4-9 C-D Bus Interconnection Scheme

4.2.3 H9281 Backplane

The H9281 backplanes are designed to accept double-height modules only. The H9281 2-slot backplane is available in six options as listed below. These backplanes allow the user to configure compact LSI-11 bus systems that most efficiently utilize available system space.

Backplane Option Designation	Description
H9281-AA	4-module backplane
H9281-AB	8-module backplane
H9281-AC	12-module backplane
H9281-BA	4-module backplane and card cage assembly
H9281-BB	8-module backplane and card cage assembly
H9281-BC	12-module backplane and card cage assembly

The following list presents quad-height options that are too large to be installed in an H9281 backplane.

Backplane Option Designation	Module Number	Description
AAV11-A	A6001	4-channel 12-bit D/A converter
ADV11-A	A0121	16-channel 12-bit A/D converter
DRV11-B	M7950	DMA interface
DUV11-A	M7951	Line interface
DZV11-A	M7957	Asynchronous multiplexer
KWV11-A	M7952	Programmable line-time clock
MMV11-A	H223, G653	Core memory
MSV11-CD	M7955-YD	16K MOS memory
RLV11	M8013 M8014	RL01 controller

Installation

Mounting dimensions for H9281 backplanes are shown in Figures 4-10 and 4-11. The H9281 backplanes can be mounted in any plane. The enclosure in which the backplane is mounted, available system space, and cooling air flow will determine an acceptable backplane position in a particular system.

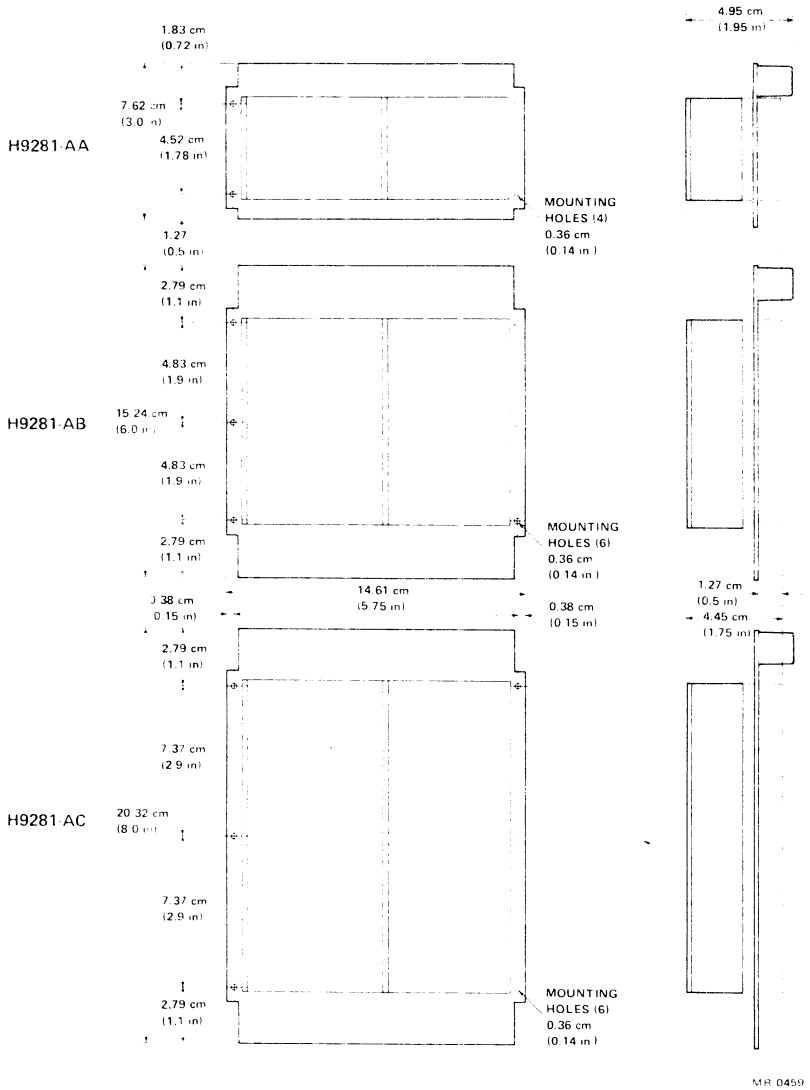
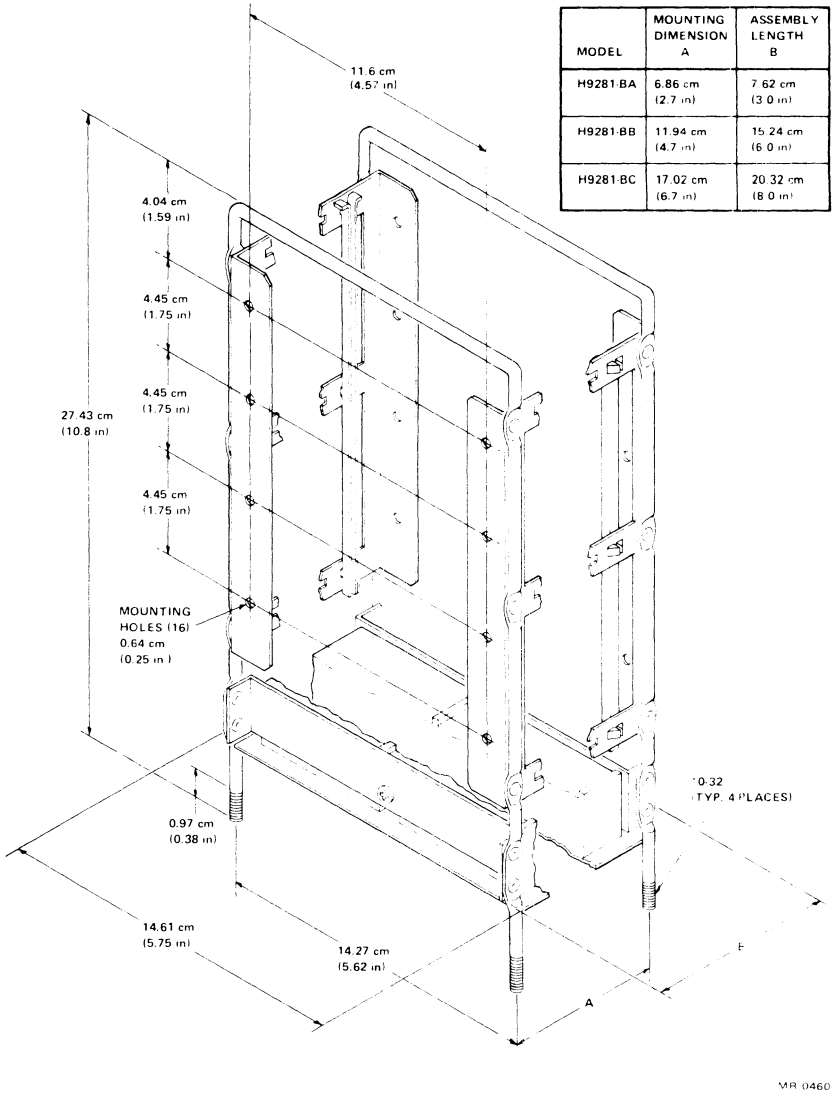


Figure 4-10 H9281-AA, AB, AC Mounting Dimensions



MODEL	MOUNTING DIMENSION A	ASSEMBLY LENGTH B
H9281-BA	6.86 cm (2.7 in)	7.62 cm (3.0 in)
H9281-BB	11.94 cm (4.7 in)	15.24 cm (6.0 in)
H9281-BC	17.02 cm (6.7 in)	20.32 cm (8.0 in)

Figure 4-11 H9281-BA, BB, BC Mounting Dimensions

Connecting System Power

Seven screw terminals are provided on the slot 1 end of the backplane for power connections. Connect system power (and optional battery backup power) as shown in Figure 4-12. Power wiring should be done with a wire gauge appropriate for the total power requirements for options installed in the backplane. The recommended wire size for H9281-AC and -BC backplanes is 12 gauge; 14 gauge is sufficient for other H9281 models.

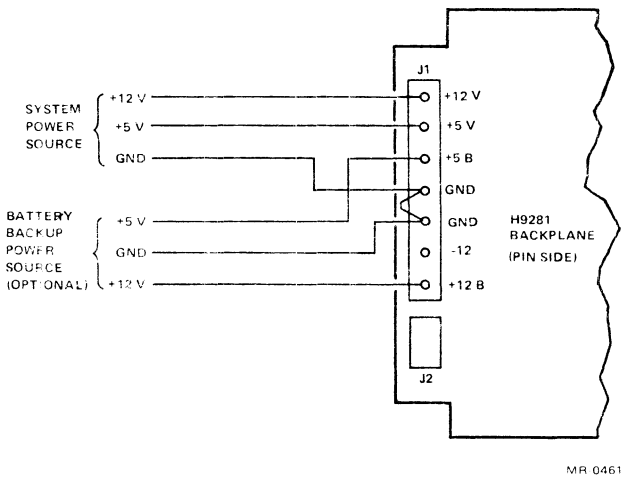


Figure 4-12 H9281 Power Connections

Select a power supply that will meet LSI-11 system power specifications and supply sufficient current for the options comprising the system. The H780 power supply is recommended.

Connecting Externally Generated Bus Signals

Externally generated bus signals can be connected to the H9281 backplane via connector J2. These signals include power sequence signals BPOK H, BDCOK H, BHALT L, and BEVNT L. In addition, the processor-generated SRUN L signal is available via J2 for driving a RUN indicator circuit. J2 connector pins are fully compatible with the H780 model series power supply or the KPV11-A power-fail/line-time clock. Signal connector J2 pinning and signal names are identified in Figure 4-13.

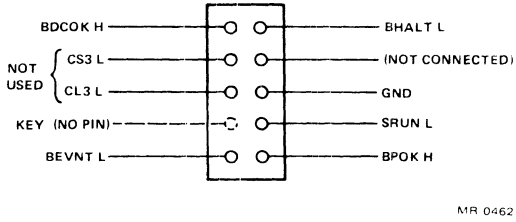


Figure 4-13 H9281 Signal Connections (J2)

Device Priority

All LSI-11 bus backplanes are priority structured. Daisy-chained grant signals for DMA and interrupt requests propagate away from the processor from the first (highest priority device) to successively lower priority devices. Processor module locations and device (option) priorities are shown in Figure 4-14.

Bus Terminations

Backplane models H9281-AB, -BB, -AC, and -BC include 120 Ω bus termination resistors at the electrical end of the bus; therefore, it is not necessary to install a separate 120 Ω bus terminator module in these backplanes.

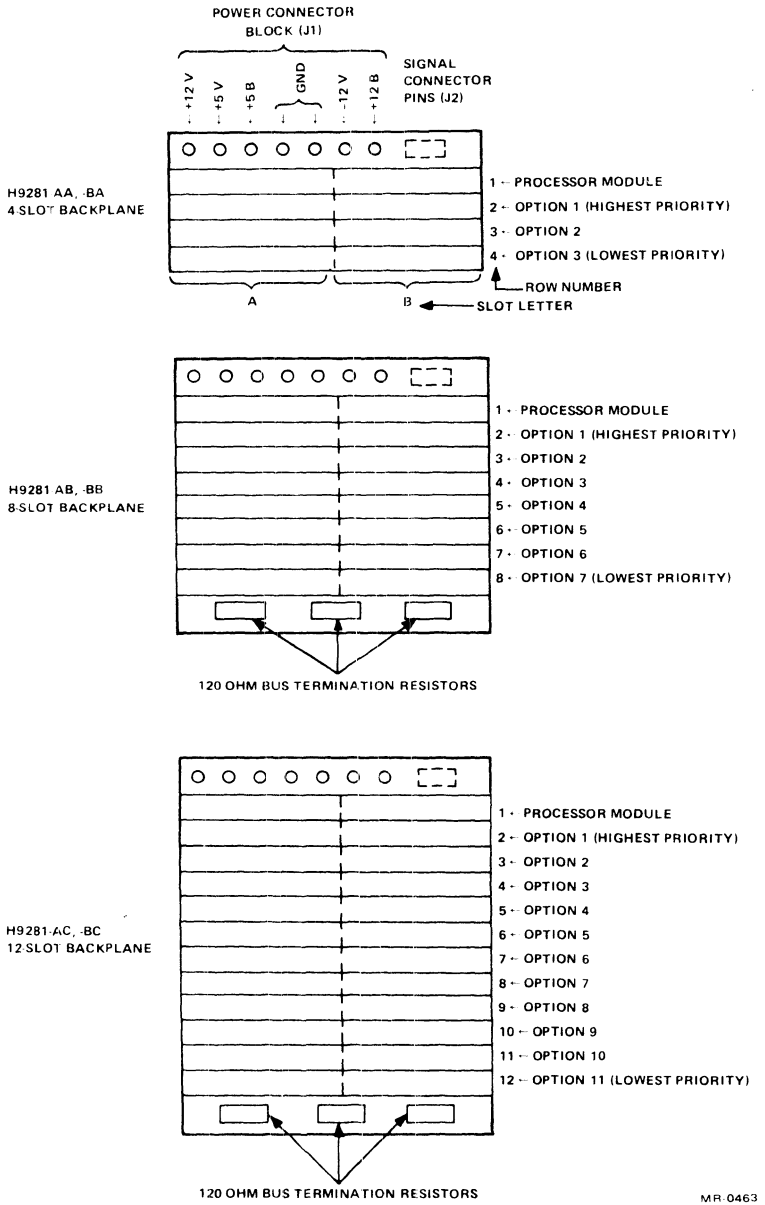


Figure 4-14 H9281 Option and Connector Locations (Module Side)

4.2.4 DDV11-B Backplane

The DDV11-B is an optional LSI-11 bus expansion backplane for use when additional logic space is required. The DDV11-B is a 9 X 6, 54-slot backplane with a 9 X 4 slot section (18 individual double-height or 9 quad-height module slots) prebused specifically for LSI-11 bus signal and power and ground connections. The remaining 9 X 2 slot section is provided with +5 Vdc, GND, and −12 Vdc power connections only; this leaves the remaining pins free for use with any special double-height logic modules to be used in conjunction with the LSI-11 family of modules and bus requirements.

The DDV11-B consists of an H034 system unit mounting frame, six H863 and three H8030 connector blocks, and the etched board bus structure necessary for signal routing. The etched board completely overlays the entire pin side of all connector blocks and is recessed sufficiently to allow wire-wrapping on those same pins with 30 AWG wire

An optional card cage, type H0341, is also available to provide protection against physical damage to modules and to serve as a card guide. This card cage completely surrounds the slot side of the system unit and is shown in Figure 4-15. The DDV11-D can be mounted in the H909-C enclosure.

NOTE

The H909-C includes the H0341 card guide.

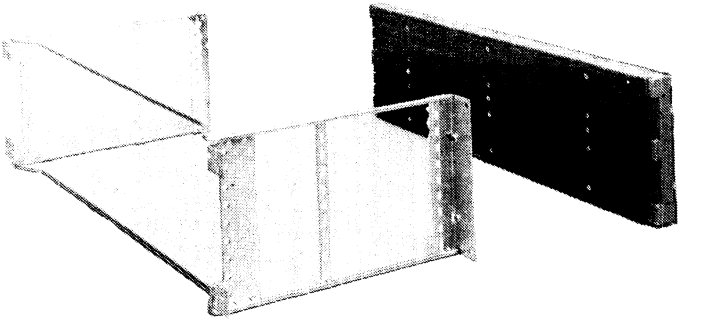


Figure 4-15 DDV11-B with H0341 Card Assembly

Module Slot Assignments

Figure 4-16 shows the slot location assignments of the DDV11-B. Rows A, B, C, and D are dedicated to the LSI-11 bus. Any module which conforms to the LSI-11 bus specifications may be used in this portion of the DDV11-B. The position numbers indicate the bus grant wiring scheme with respect to the processor module. The bus grant signals propagate through the slot locations in the position order shown in Figure 4-16 until they reach the requesting device. Any unused slots must be jumpered to provide bus grant signal continuity or it is recommended that unused locations occur only in the highest position numbered locations.

Rows E and F contain the 18 user-defined slots with power and ground connections provided.

Equipment Supplied

The DDV11-B option is supplied with the following items:

Six H863 connector blocks
Three H8030 connector blocks
Etched board bus structure

Installation

The DDV11-B can be easily mounted on panels or chassis using standard hardware. The overall dimensions of the unit are shown in Figure 4-17. The H034 mounting frame of the DDV11-B is provided with tapped holes and clearance holes to enable the attachment of the system unit.

H0341 Card Assembly Mounting

The H0341 card assembly is supplied with the hardware necessary to mount to the H034 mounting frame. Figure 4-18 shows the method of assembly. Two screws (item 2) and two washers (item 1) are inserted through the clearance holes of the PC board and H034 mounting frame and into the two threaded inserts on each bracket of the card assembly. The card assembly provides nylon guides which help to guide and support the modules installed in the system unit.

DC Power and Power Signal Connections

DC power is supplied to the modules in the DDV11-B through the backplane PC board. The power and ground leads from the external source connect to the 7-position terminal board mounted on the edge of the PC board as shown in Figure 4-17. Any suitable connector terminals, solder or crimp type, may be attached to the power supply leads and inserted under the terminal strip screws. A jumper tab is mounted between the

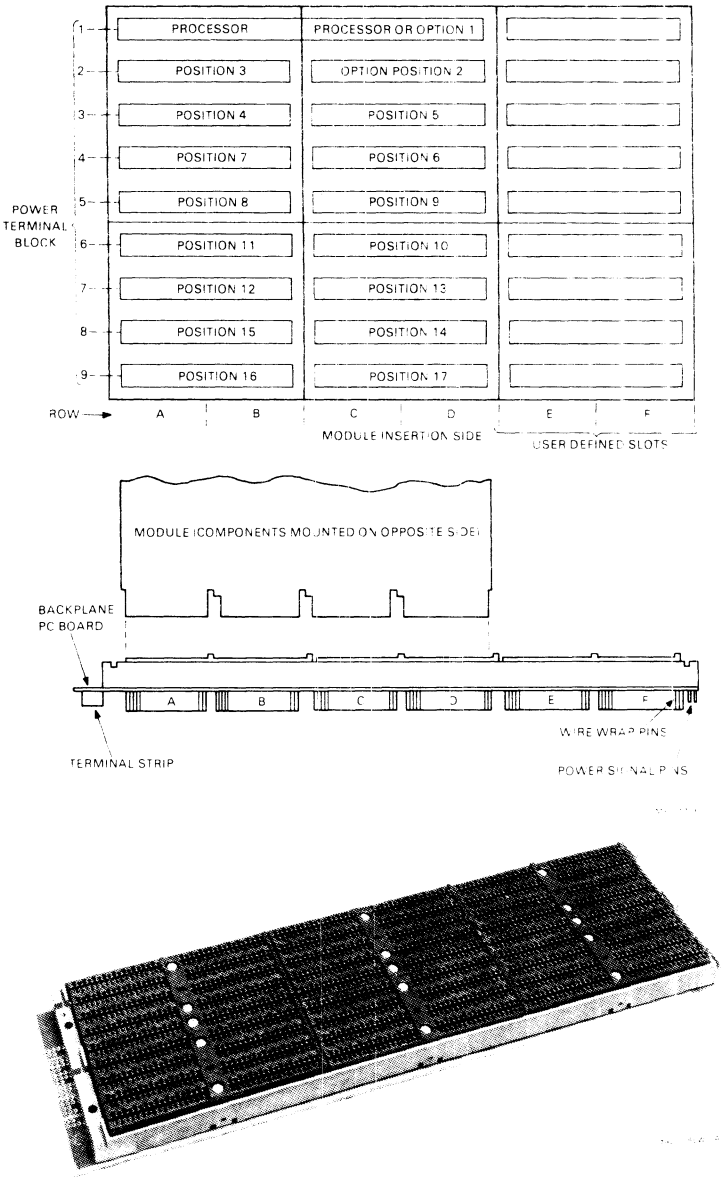


Figure 4-16 DDV11-B Module Installation and Slot Assignments

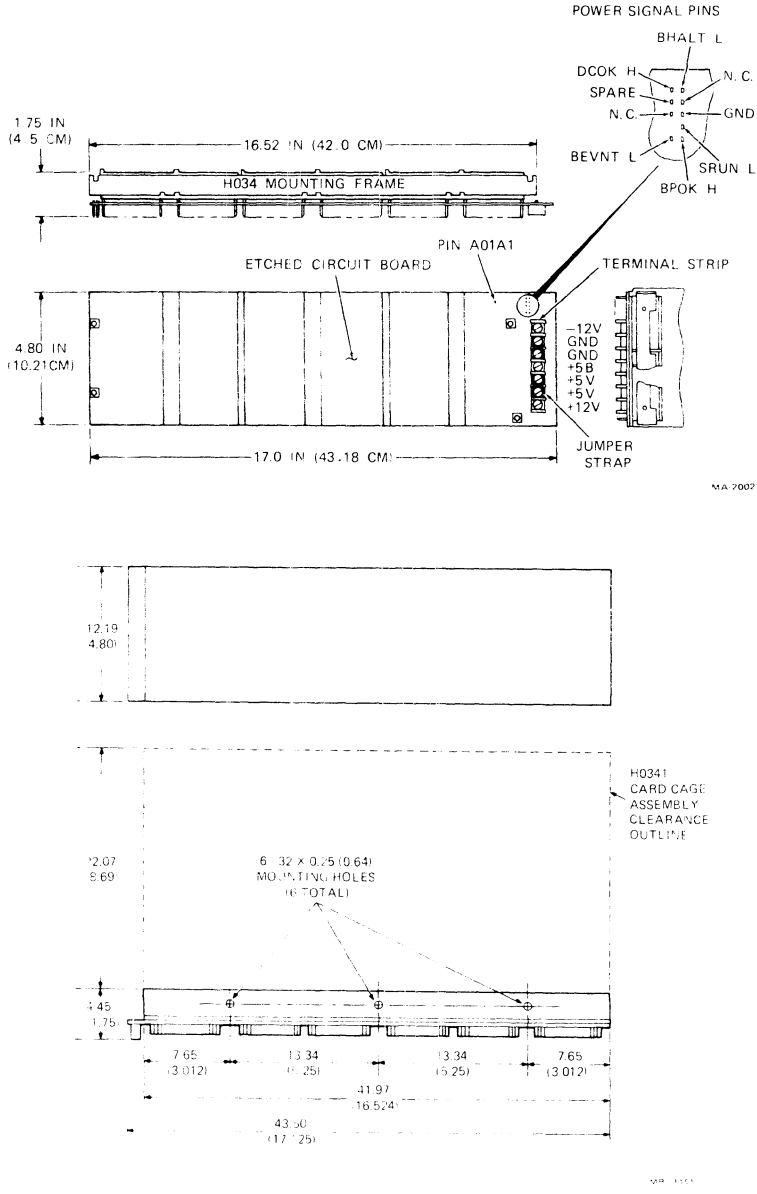


Figure 4-17 DDV11-B Power Wiring and Dimensions

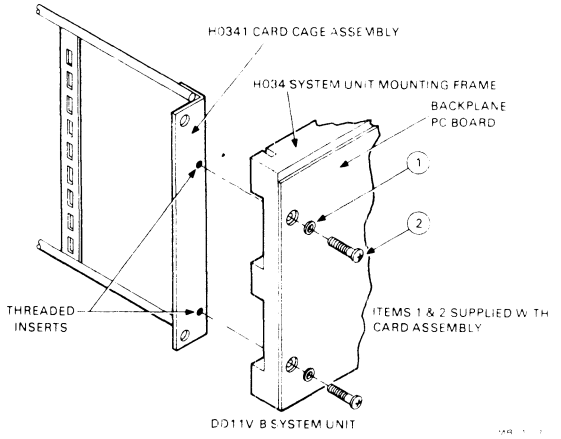


Figure 4-18 H0341 Card Assembly Installation

two +5 V screws and between the two ground (GND) screws on the terminal board. The total current capability of the DDV11-B and the wire sizes required are as follows:

Terminal		Current (Max)	Wire Size (AWG)
+12 V		20 A	14
+5 V	Jumped	40 A	14
+5 V			
+5 B		20 A	
GND	Jumped	40 A	14
GND			
−12 V		20 A	

Figure 4-17 identifies the power signal pins which are located at the opposite end of the backplane PC board from the power terminal strip. A mating female connector (DIGITAL P/N 12-11206-02 or 3M P/N 3473-3) can be inserted over the pins and used to connect the external signals to the backplane.

Backplane Pin Assignments

Table 4-3 lists the backplane pin assignments for the LSI-11 bus signals and dc power and ground connections on the DDV11-B backplane.

Table 4-3 DDV11-B Backplane Pin Assignments

Side Row	2 A&C	1 A&C	2 B&D	1 B&D	2 E	1 E	2 F	1 F
A	+5V	BSPARE 1	+5V	BDCOK H	+5V	BLANK	+5V	BLANK
B	-12V	BSPARE 2	-12V	BPOK H	-12V	BLANK	-12V	BLANK
C	GND	BDAL 17 L	GND	SSPARE 4	GND	BLANK	GND	BLANK
D	+12V	BDAL 16 L	+12V	SSPARE 5	BLANK	BLANK	BLANK	BLANK
E	BDOUT L	SSPARE 1	BDAL2 L	SSPARE 6	BLANK	BLANK	BLANK	BLANK
F	BRPLY L	SSPARE 2	BDAL 3 L	SSPARE 7	BLANK	BLANK	BLANK	BLANK
H	BDIN L	SSPARE 3	BDAL 4 L	SSPARE 8	BLANK	BLANK	BLANK	BLANK
J	BSYNC L	GND	BDAL 5 L	GND	BLANK	BLANK	BLANK	BLANK
K	BWTBT L	MSPARE A	BDAL 6 L	MSPARE B	BLANK	BLANK	BLANK	BLANK
L	BIRQ L	MSPARE A	BDAL 7 L	MSPARE B	BLANK	BLANK	BLANK	BLANK
M	BIAK I L	GND	BDAL 8 L	GND	BLANK	BLANK	BLANK	BLANK
N	BIAK O L	BDMR L	BDAL 9 L	BSACK L	BLANK	BLANK	BLANK	BLANK
P	BBS 7 L	BHALT L	BDAL 10 L	BSPARE 6	BLANK	BLANK	BLANK	BLANK
R	BDMG 1 L	BREF L	BDAL 11 L	BEVNT L	BLANK	BLANK	BLANK	BLANK
S	BDMG 0 L	PSPARE 3	BDAL 12 L	PSPARE 4	BLANK	BLANK	BLANK	BLANK
T	BINIT L	GND	BDAL 13 L	GND	BLANK	GND	BLANK	GND
U	BDAL 0 L	+12B	BDAL 14 L	PSPARE 2	BLANK	BLANK	BLANK	BLANK
V	BDAL 1 L	+5B	BDAL 15 L	+5	BLANK	BLANK	BLANK	BLANK

4.3 ENCLOSURES

Three basic enclosures are available: the H909-C enclosure, the BA11-M expansion box, and the BA11-N mounting box. A detailed description of each, including application and configuration information, is presented in the following paragraphs. The various options available are listed below.

Options	Voltage (V)	Bezel*	Includes	Mounting
H909-C	–	No	Fan and H0341 card guide	–
PDP-11/03-XA	115	Yes	X=E: KD11-F	BA11-MC or BA11-MD
PDP-11/03-XB	230	Yes	X=K: KD11-R	BA11-MC or BA11-MD
PDP-11/03-LC	115	Yes	KD11-R and BDV11-A	BA11-NC or BA11-ND
PDP-11/03-LD	230	Yes	KD11-R and BDV11-A	BA11-NC or BA11-ND
BA11-ME	115	No	Cable to daisy chain	
BA11-MF	230	No	Power supply	
BA11-NE	115	No		
BA11-NF	230	No		

*Including switches.

4.3.1 H909-C General Purpose Logic Enclosure

The H909-C is a general purpose logic box designed to accommodate the DDV11-B backplane or any one of several different standard logic subsystems (Figure 4-19). In addition, with the use of compatible logic frames and connector blocks, it can house custom configured subassemblies. The box features a distinctive front panel that can be drilled for lights and switches as desired by the user. A fan is provided for cooling capability and ample room is reserved for power supply installation.

Specifications

Width	48.25 cm (19 in)
Height	13.33 cm (5.25 in)
Depth	62.86 cm (24.75 in) 70.48 cm (27.50 in) including bezel
Weight	27.21 kg (60 lb)
Mounting Space for Power Supplies	12.7 cm X 15.8 cm X 50.8 cm (5 X 6.25 X 20 in)

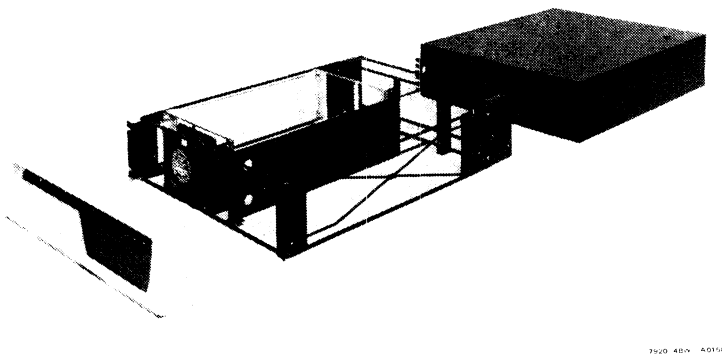


Figure 4-19 H909-C Enclosure

4.3.2 BA11-M Expansion Boxes

The BA11-M expansion box provides a convenient means for expanding LSI-11 bus systems. Each expansion box includes an H9270 LSI-11 bus-structured backplane and an H780 power supply system mounted in an enclosure with a blank front panel.

The BA11-M is shown in Figure 4-20. Mechanical and mounting details are shown in Figures 4-21 and 4-22.

Specifications

Table 4-4 lists significant BA11-M specifications. Refer to Paragraph 4.6 for specifications of the H780 power supply.

Installation

When installing an expansion box to expand from a single to a dual backplane system, the BCV1B bus expansion option and TEV11 bus terminator option (or equivalent) must be used. Install the BCV1B modules and cables as shown in Figure 4-23. The terminator must be installed in the option location in the last box. When installing the BCV1B cable set, disregard any "This side up" labels that may be on the BC05L cables. Ensure that the red line on each cable is toward the center of both modules and that J1 on each board is connected to J1 on the second board and similarly for J2 on both boards. Ensure that the cables have no twists. Carefully fold excess cable as shown in Figure 4-23. Figure 4-24 illustrates proper installation of the BCV1B and TEV11 options.

When expanding from a second to a third backplane, the BCV1A bus expansion option is required, in addition to the items required for expansion to the second backplane.

NOTE

BCV1A and BCV1B cables must differ in length by 121.92 cm (4 ft) (minimum)

The completed installation for a 3-backplane system using the BCV1A option is shown in Figure 4-24. In addition to this option, the BCV1B option is required to connect the first backplane to the second backplane; a 120 Ω bus termination is required in the last option slot in the third backplane.

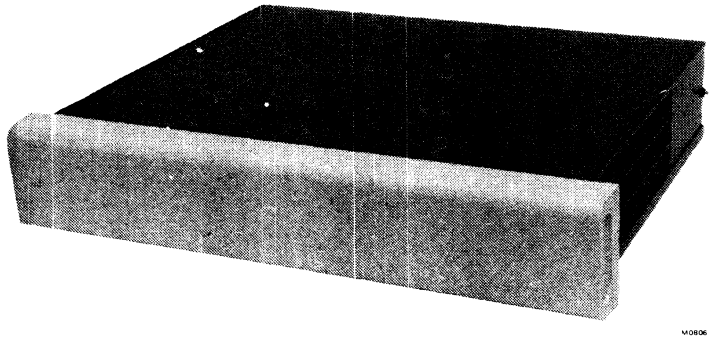


Figure 4-20 BA11-M Expansion Box

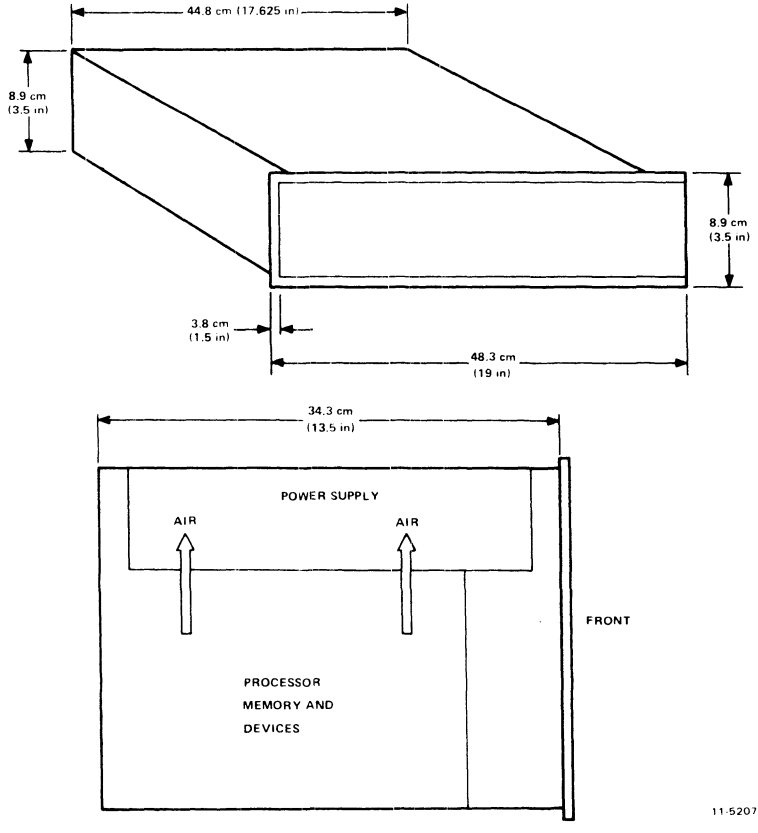


Figure 4-21 BA11-M Assembly Unit

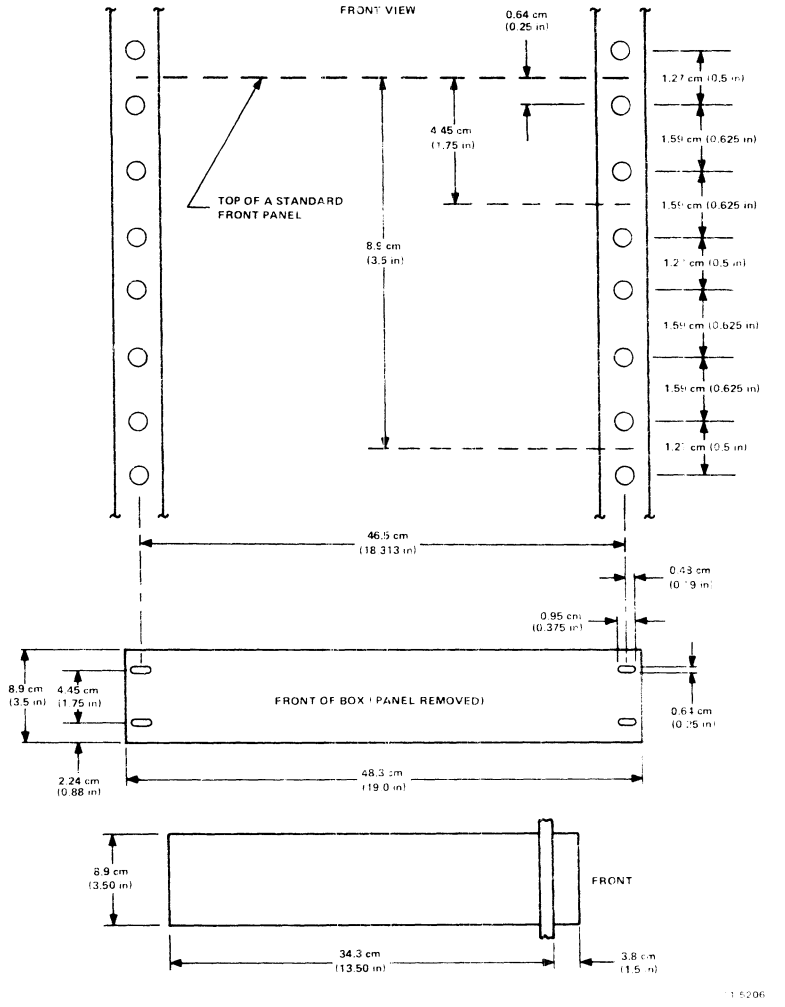


Figure 4-22 BA11-M Cabinet Mounting

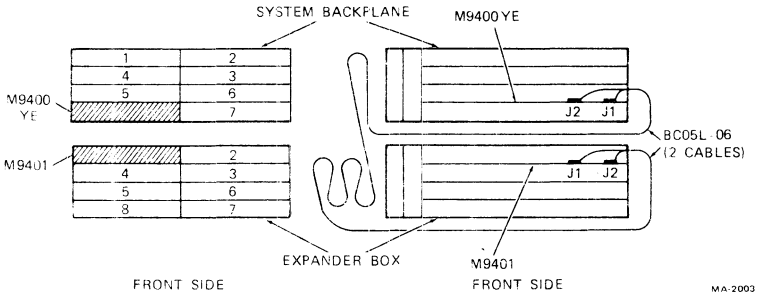


Figure 4-23 BA11-M Expansion Box Interconnections (two-backplane system)

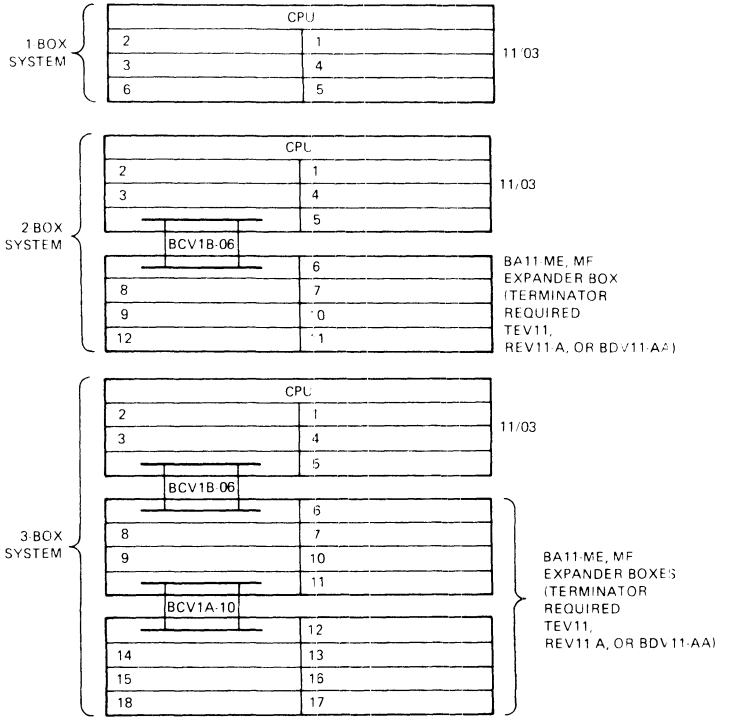
Table 4-4 BA11-M Specifications

Item	Specification
Dimensions (including bezel)	
Width	48.3 cm (19 in)
Height	8.9 cm (3.5 in)
Depth	
Without mounting brackets	34.3 cm (13.5 in)
With mounting brackets	38.1 cm (15.0 in)
Shipping weight	18.1 kg (40 lb)
Operating temperature*	5° to 50° C (41° to 122° F)
Operating humidity	10% to 95%, with a maximum wet bulb temperature of 32° C (90° F) and a minimum dew point of 2° C (36° F)
AC input power	100–127 Vrms, 50 ± 1 Hz or 60 ± 1 Hz, 400 W maximum or 200–254 Vrms, 50 ± 1 Hz or 60 ± 1 Hz, 400 W maximum

*The maximum allowable operating temperature is based on operation at sea level, i.e., at 760 mmHg (29.92 inHg); maximum allowable operating temperature will be reduced by a factor of 1.8° C/1000 m (1.0° F/1000 ft) for operation at higher altitude sites.

Table 4-4 BA11-M Specifications (Cont)

Item	Specification
DC output power	+5 Vdc ± 3%, 0–18 A load (static and dynamic) +12 Vdc ± 3%, 0–3.5 A load (static and dynamic) Maximum output power: 120 W (total)
Recommended circuit breaker rating	15 A at 115 Vac or at 230 Vac



NOTES

1. INCLUDED IN BCV1B BUS EXPANSION OPTION. (CABLES ARE AVAILABLE IN 2, 4, 6, OR 12 FT LENGTHS.)
2. INCLUDED IN BCV1A BUS EXPANSION OPTION. (CABLES ARE AVAILABLE IN 2, 4, 6, OR 12 FT LENGTHS.)
3. INCLUDED IN TEV11 BUS TERMINATOR OPTION.
4. THE LSI-11 BUS IS RESTRICTED TO 15 OPTIONS, MAXIMUM. THESE OPTION SLOTS WOULD ONLY BE USED WHEN PREVIOUS OPTION(S) OCCUPY MORE THAN 1 OPTION LOCATION.
5. BCV1A AND BCV1B EXPANSION CABLES MUST DIFFER IN LENGTH BY 4 FT (MIN).

MA-2000

Figure 4-24 BCV1A Installation

Table 4-5 BA11-N Specifications

Item	Specification
Dimensions (including bezel)	
Width	48.3 cm (19 inch)
Height	13.2 cm (5.19 inch)
Depth	
Without mounting brackets	57.8 cm (22.7 inch)
With mounting brackets	67.96 cm (26.75 in)
Weight (without modules)	20 kg (44 lb)
Operating temperature*	5° to 50° C (41° to 122° F)
Operating humidity	10 to 95%, with a maximum wet bulb temperature of 32° C (90° F) and a minimum dew point of 2° C (36° F)
Input voltage	
BA11-NC/NE	115 Vac
BA11-ND/NF	230 Vac
Input current†	
BA11-NC/NE	12 A max
BA11-ND/NF	6 A max
Circuit breaker rating	15 A at 115 Vac or 230 Vac

*The maximum allowable operating temperature is based on operation at sea level, i.e., at 760 mmHg (29.92 inHg); maximum allowable operating temperature will be reduced by a factor of 1.8° C/1000 m (1.0° F/1000 ft) for operation at higher altitude sites.

†Input current consists of that used by the BA11-N, itself, plus whatever current is supplied via the convenience ac outlet (J3) to an expander box; the total current must be less than the maximum specified.

Table 4-6 BA11-N Power Supply Specifications

Item	Specification
Current rating	5.5 A at 115 Vrms 2.7 A at 230 Vrms
Inrush current	100 A peak, for 1/2 cycle at 128 Vrms or 256 Vrms
Apparent power	630 VA
Power factor	The ratio of input power to apparent power shall be greater than 0.6 at full load and low input voltage.
Output power	+5 Vdc, ±250 mV at 22 A (A minimum of 2 A of +5 Vdc power must be drawn to ensure that the +12 Vdc supply regulates properly.) +12 Vdc, ±600 mV at 11 A
Power-up/power-down characteristics	
Static performance	
Power-up	BDCOK H goes high: 75 Vac BPOK H goes high: 90 Vac
Power-down	BPOK H goes low: 80 Vac BDCOK H goes low: 75 Vac
Dynamic performance	
Power-up	3 ms (min) from dc power within specification or to BDCOK H asserted. 70 ms (min) from BDCOK H asserted to BPOK H asserted.
Power-down	4 ms (min) from ac power off to BPOK H negated. 4 ms (min) from BPOK H negated to BDCOK H negated. 5 μs (min) from BDCOK H negated to dc power as of specifications.

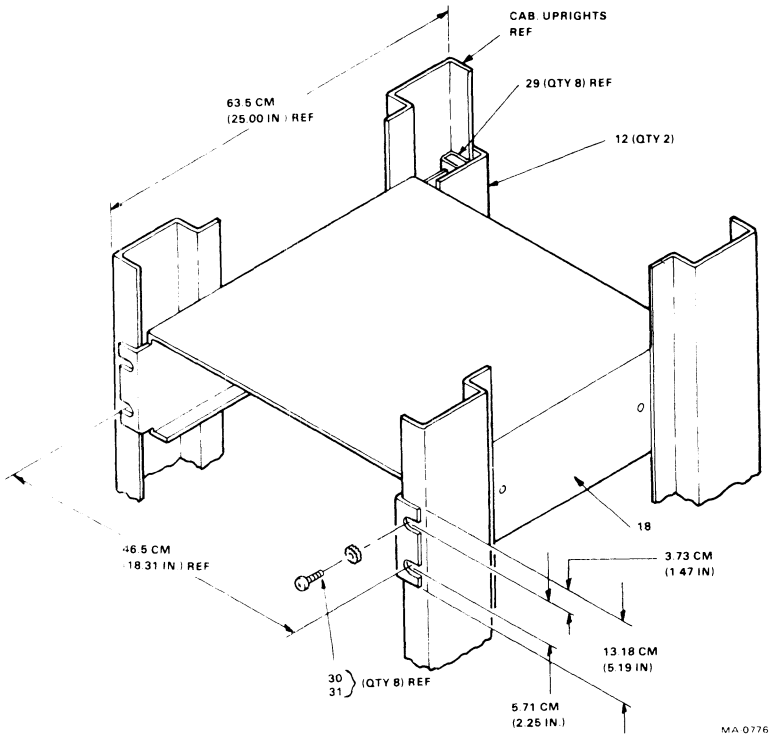


Figure 4-27 BA11-NE and BA11-NF Cover Mounting Dimensions

4. Mount the cover to the front cabinet uprights using four pan head screws (10-32 X 0.62 lg) and four No. 8 lockwashers.

5. Attach the two support brackets to the cover using four Phillips pan head screws (8.32 X 0.38 lg) and four No. 8 lockwashers.

6. Attach the support brackets to the rear cabinet uprights using four Phillips pan head screws (10-32 X 0.62 lg) and four No. 10 flat washers.

7. Slide the unit into the cover. It will be held in place by the spring-button assembly. To slide the unit forward again it will be necessary to release this spring button.

8. If the system is to be moved or shipped, the shipping screw must be replaced

Installing the Logic Box Base in the Cover – Set the rear of the logic box base on the support flanges of the cover and slide the base in until the spring-button assembly engages in the extended position. Take care not to pinch the cables while sliding the base in. Release the spring button and push the base all the way in until it engages in the closed position. Take the following steps to complete the installation.

NOTE

The base being installed is either the main base i.e., the one containing the CPU or an expander base (two expander boxes can be added). Modify the following instructions to suit the kind of base you are installing, e.g., if there is a blank front panel, skip the first half of step 1.

1. Put the AUX switch on the front panel in the OFF position; put the ON/OFF switch on the ac input box in the OFF position.

2. When the AUX switch on the front panel is in the ON position, the two wires of the power controller cable are common. Connect the free end of the cable to the input circuit of the power controller so that the AUX switch controls the application of primary power to the controller. Keep the AUX switch in the OFF position

3. Loosen the cable strain reliefs and open the rear door of the box to install the LSI-11 bus expansion cable assemblies. Two cable assemblies are used. Table 4-7 describes the assemblies and tells where to insert the assembly modules. (Figure 4-28 illustrates module placement.) When inserting the modules, make sure the connectors are on top.

4. Close the rear door; bring the bus cables out under the left strain relief and the communication cables out under the right strain relief. Adjust the strain reliefs so that the cables are held firmly but are not pinched or crushed. Secure the strain reliefs and the rear door. Make sure the cables will not bind when the base is pulled out to the extended position.

Table 4-7 LSI-11 Bus Expansion Cable Assemblies

Assembly	Assembly Composition	Insert Modules In
BCV1B-XX	Two BC05L-XX cables	
	One M9400-YE module	Slots A and B of the first open row after all other LSI-11 bus options have been installed in the main box.
	One M9401 module	Slots A and B of row 1 of expander box 1.
BCV1A-XX	Two BC05L-XX cables	
	One M9400-YD module	Slots A and B of the first open row after all other LSI-11 bus options have been installed in expander box 1.
	One M9401 module	Slots A and B of row 1 of expander box 2.

NOTE

"-X" in the cable assembly number denotes length, which can be 60, 96, 121.92, 182.88, or 304.80 cm (2, 4, 6, or 10 ft). (Each cable of an assembly is the same length.) When both assemblies are used in a system (boxes), the lengths must differ by 121.92 cm (4 ft). To facilitate servicing, the BCV1B cables should be 182.88 cm (6 ft) long, while the BCV1A cables should be 304.80 cm (10 ft) long.

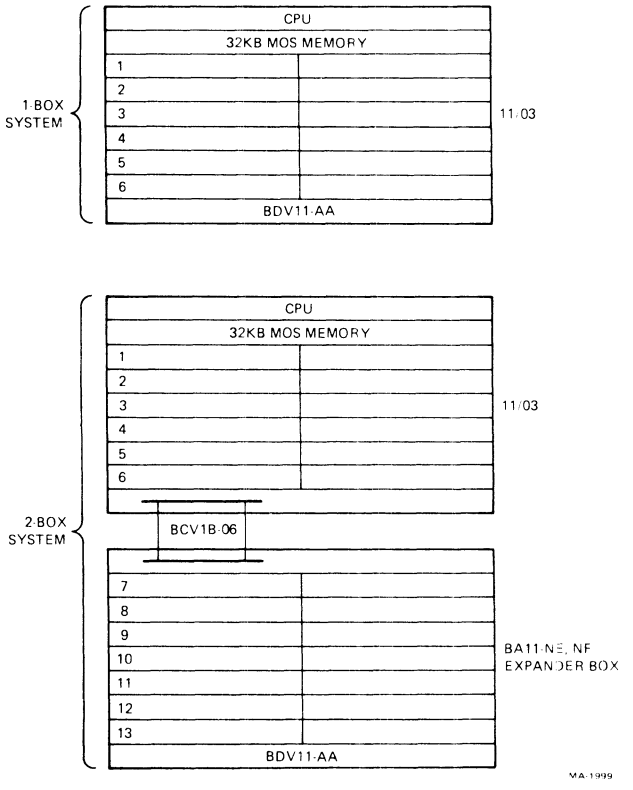


Figure 4-28 Configuring Large Box

4.3.4 Backplane and Module Configuration

LSI-11 bus systems can be classified as either single-backplane or multiple-backplane systems. The electrical characteristics of each system are different; hence, two sets of rules have been devised and must be observed. These rules have their basis in bus loading and power consumption.

Single-Backplane Configuration Rules

1. The LSI-11 bus can support up to 20 ac loads, if unterminated at the end.

2. The terminated bus can support up to 35 ac loads.

3. The bus can support up to 20 dc loads.

4. The amount of current drawn from each power supply should be 70 percent or less of the maximum rated output of the supply.

Multiple-Backplane Configuration Rules

1. No more than three backplanes can be connected together.

2. Each backplane can have no more than 20 ac loads.

3. The total number of dc loads cannot be more than 20.

4. Both ends of the termination line must be terminated with 120 ohms, i.e., the first backplane must have an impedance of 120 ohms, and the last backplane must have a termination of 120 ohms.

5. The cable connecting the first two backplanes (i.e., the main box and expander box 1) must be at least 60.96 cm (2 ft) long. [A 182.88 cm (6 ft) length of cable is recommended for ease of installation.]

6. The cable connecting the backplane of expander box 1 to the backplane of expander box 2 must be at least 121.92 cm (4 ft) longer or shorter than the cable connecting the main box and expander box 1. [A 304.80 m (10 ft) length of cable is recommended for ease of installation.]

7. The combined length of both cables in a 3-backplane system cannot exceed 487.68 m (16 ft).

8. The interbackplane cables must have a characteristic impedance of 120 ohms.

9. The amount of current drawn from each power supply should be 70 percent or less of the maximum output of the supply.

BACKPLANE CONFIGURATION

To configure an LSI-11 bus system, take the following steps.

1. Choose the type of memory (MOS, PROM, or combination) required for the specific application.

2. Select the CPU and memory combination most suited for the application.

3. Select additional memory, interface, and peripheral options required.

4. Count the total number of module positions.

5. Count the total number of bus positions.

6. Choose a backplane configuration that satisfies both the module position requirement, the bus position requirement, and also provides sufficient expansion space.

7. Enter the option names in the backplane positions of the selected configuration.

4.4 CABINETS

Two types of low-profile cabinets are available, the H984 series and the H9800-A.

4.4.1 H984 Series Cabinets (Figure 4-29)

The H984-BA (115 Vac) and the H984-BB (230 Vac) are low-profile cabinets equipped with a walnut-grained, plastic laminate top surface and four ball-type casters mounted on a supporting frame for ease of positioning on solid or carpeted surfaces. The cabinets are a light gray steel enclosure trimmed in flat black to make them compatible with the decor of the modern office or laboratory.

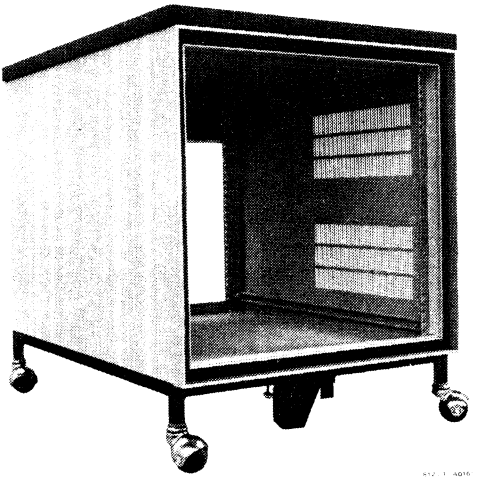


Figure 4-29 H984 Series Cabinet

Each H984 provides mounting space for standard 48.3 cm (19 in) panels or racks at both the front and rear of the unit. Two vertical angles at the front and rear opening of the enclosure contain predrilled holes at EIA spacing. The angles can be laterally positioned within the cabinet to adjust for mounting units with varying depths. Both sides of the steel enclosure contain ventilation ports to allow cooling of the internal components.

A service leg with caster is located beneath the center of the unit and can be easily extended and retracted. The service leg provides stability to the cabinet when slide-mounted chassis are withdrawn from the front of the cabinet. When not in use, the leg retracts into the channel.

A 115 Vac or 230 Vac power distribution panel is supplied with the cabinet and is mounted at the top of the rear opening of the cabinet. The panel can be easily repositioned to accommodate internal chassis when required.

Optional Equipment

Fan Panel Assembly – A fan panel assembly with two enclosed rotary fans is available as an option and provides additional cooling for the electrical components in the cabinet. The assembly is prewired with a cord and male connector which can be inserted into one of the outlets on the power control panel (part of the H984 cabinet). The fan assembly is available for 115 Vac or 230 Vac. The panel is supplied with hardware for mounting.

Black Plastic Front Cover – A flat black, plastic louvered cover panel, 4.45 cm (1.75 in) high, can be used to complete the covering at the front of the H984. The panel slots allow increased air flow through the cabinet.

Blank Connector Panel – The blank connector panel is designed to completely enclose the rear opening of the H984 when the blower fan assembly option is included. This provides a surface for mounting interface cable connectors or cable openings. The panel is supplied with hardware for mounting.

Blank Metal Panel – A light gray blank metal cover panel, 8.9 cm (3.5 in) high, can be ordered to complete the covering at the front of the cabinet. The color is the same as PDP-11/03 front panel and H984 cabinet.

Connector Panel Assembly – A hinged connector, preformed for mounting up to eight cable connectors, encloses the remainder of the H984 rear opening when the fan assembly is included.

Specifications

Dimensions	
Width	59.7 cm (23.50 in)
Depth	71.3 cm (28.06 in)
Height	54.6 cm (21.50 in)
Module enclosure mounting space	Standard 48.3 cm (19 in) EIA
Usable height	61.7 cm (24.28 in)
Usable depth	44.6 cm (17.56 in)
Color	Walnut-grained top surface, light gray side panels, chrome and flat black trim

Description	Part No.	Shipping Weight
Low-Profile Cabinet (115 Vac)	H984-BA	31.8 kg (70 lb)
Low-Profile Cabinet (230 Vac)	H984-BB	31.8 kg (70 lb)
Optional Hardware		
Blower Fan (115 Vac)	70-12438-0	3.6 kg (8 lb)
Blower Fan (230 Vac)	70-12438-1	3.6 kg (8 lb)
Blank Connector Panel (back)	74-17440	2.3 kg (5 lb)
Louvered Cover Panel (front)	12-11474-0	0.45 kg (1 lb)
Blank Metal Cover (front)	H950-NC	1.8 kg (4 lb)
Connector Panel Frame (back)	74-16743	
Connector Panel Assembly (back)	70-12871	

4.4.2 H9800-A Cabinets (Figure 4-30)

The H9800-A is a low-profile systems desk equipped with a walnut-grained plastic laminate top and color coordinated to fit into the modern office decor. The unit is equipped with six ball casters as standard equipment for easy positioning on carpeted surfaces. Also included is a 115 Vac power distribution panel.

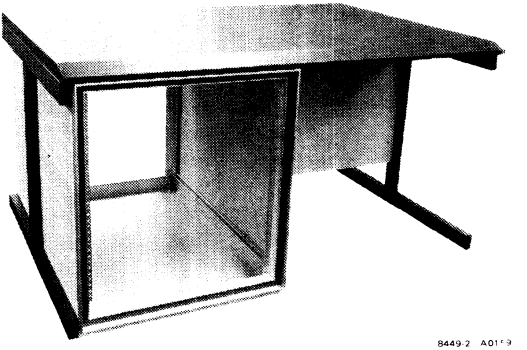


Figure 4-30 H9800-A Cabinet

The H9800-A is constructed of quality materials including a top constructed of 24.9 kg (55 lb) particle board with a dark-walnut plastic laminate. The "module" itself is constructed of 11 and 18 gauge steel with a maximum loading capacity of 181.44 kg (400 lb).

The H9800-A consists of a left-mounted rack enclosure offering 53.3 cm (21 in) of usable height and 73.7 cm (29 in) of usable depth in a standard 48.3 cm (19 in) EIA mount format. The right side offers knee space, a modesty panel, and a convenient work surface ideal for using terminals or typewriters.

Specifications

Dimensions	
Width	121.92 cm (48 in)
Depth	81.28 cm (32 in)
Height	70.1 cm (27.6 in)
Shipping weight	45.36 kg (100 lb)
Module enclosure mounting space	Standard 48.3 cm (19 in) EIA
Usable height	53.3 cm (21 in)
Usable depth (variable)	73.7 cm (29 in)
Color	Walnut-grained top surface, beige side panels, chrome trim

4.5 LSI-11 BUS-COMPATIBLE, WIRE-WRAPPABLE MODULES (W9511, W9512, W9514 AND W9515)

The LSI-11 bus-compatible wire-wrappable modules consist of quad-height and double-height modules (Table 4-8). Two LSI-11 bus-compatible modules are available without DIP sockets. The total IC complement of DIPs that can be installed is listed in Table 4-9. This table allows one pair of holes between each IC package for mounting additional decoupling capacitors. Since the DIPs listed in Table 4-9 are of standard size, additional pairs of holes may be required to allow for mounting oversized ICs.

Table 4-8 LSI-11 Bus-Compatible Modules

Module	Description	Power and Ground Connections
W9511	Quad-height, extended-length, single-width module with extractor handle. No DIP sockets included. One 40-pin male cable connector premounted on board and space for additional 40-pin connector provided.	V_{CC} – AA2, BA2, CA2, DA2 GND – AT1, BT1, CT1, DT1, AC2, BC2, CC2, DC2
W9514	Same as W9511 except with 58 pre-mounted DIP sockets.	Same as W9511
W9512	Double-height, extended-length, single-width module with Flip-Chip handle. No DIP sockets included. One 40-pin male connector premounted on board.	GND – AT1, BT1, AC2, BC2
W9515	Same as W9512 except with 25 pre-mounted DIP sockets.	Same as W9512

WIRE-WRAPPABLE MODULES

Table 4-9 LSI-11 Bus-Compatible Modules (No Sockets)

	IC Capacity (Total)*					
Modules	**6-Pin**	**8-Pin**	**14-Pin**	**16-Pin**	**24-Pin**	**40-Pin**
W9511	152	119	72	61	5	3
W9512	63	53	32	27	5	3

*Standard size ICs (not oversized). Most schemes for mounting decoupling capacitors will reduce the capacity slightly.

Two LSI-11 bus-compatible modules are available with premounted 16-pin DIP sockets. One pair of holes is provided between each DIP socket for mounting additional decoupling capacitors. The total number of sockets mounted on the boards is listed in Table 4-10.

Table 4-10 LSI-11 Bus Compatible Modules (with Sockets)

Module	16-Pin DIP Sockets
W9514	58
W9515	25

The LSI bus-compatible, wire-wrappable modules will accept a variety of IC package types and discrete components. The printed circuit on each board connects the appropriate edge connector pins to the V_{CC} plane on side 2 of the board and the ground plane (GND) on side 1. The remaining edge connector pins terminate to a double row of wire-wrap pins for user-designated functions. The electrical interconnection of the wire-wrap pins can be performed manually or by using automated wire-wrapping techniques. Each of the modules also includes a 40-pin male cable connector to allow an interface cable to be attached to the module logic. The pins of the cable connector are also terminated to a double row of wire-wrap pins. The quad-height module is provided with a space where a 40-pin cable connector (labeled J2) can be inserted by the user. When a connector is not required, additional IC packages can be installed. Each board contains insulated standoffs to maintain the required clearance between adjacent modules and prevent shorting of wire-wrap pins.

IC Package Mounting Area

The total number of IC packages that can be installed on the LSI-11 bus-compatible modules is included in Tables 4-9 and 4-10. Each board without premounted DIP sockets contains a universal area that will accept IC packages with pin centers on 0.76 cm (0.3 in), 1.01 cm (0.4 in), and 1.52 cm (0.6 in). The remaining areas will accept packages with 0.76 cm (0.3 in) pin centers only, except where indicated.

The wire-wrap pins and components are mounted on side 1 of each module. Rows of predrilled holes accept IC packages with pin spacings of 0.76 cm (0.3 in), 1.01 cm (0.4 in), and 1.52 cm (0.6 in). Universal areas on the W9500 series modules are the areas which accept IC packages with standard pin spacings. These areas have four rows of predrilled holes spaced at 0.76, 1.01, and 1.52 cm (0.3, 0.4, and 0.6 in).

The universal area will accept a mixture of 6-, 8-, 14-, 16-, 24-and 40-pin IC packages. The number of pairs of terminals required for each IC package is listed in Table 4-11 and noted in Figures 4-31 and 4-32. This information is used to determine the best configuration when using different size packages in any one universal area. An additional pair of terminals is required when a decoupling capacitor is used.

NOTE

Allow an additional pair of terminals to compensate for the differences in IC package sizes by various manufacturers.

Table 4-11 Terminal Space Requirements

IC Packages	6-Pin	8-Pin	14-Pin	16-Pin	24-Pin	40-Pin
Required pair of terminals	3	4	7	8	12	20
With decoupling capacitor	4	5	8	9	13	21
Oversized IC	5–6	6–7	9–10	10–11	14–15	22–23

WIRE-WRAPPABLE MODULES

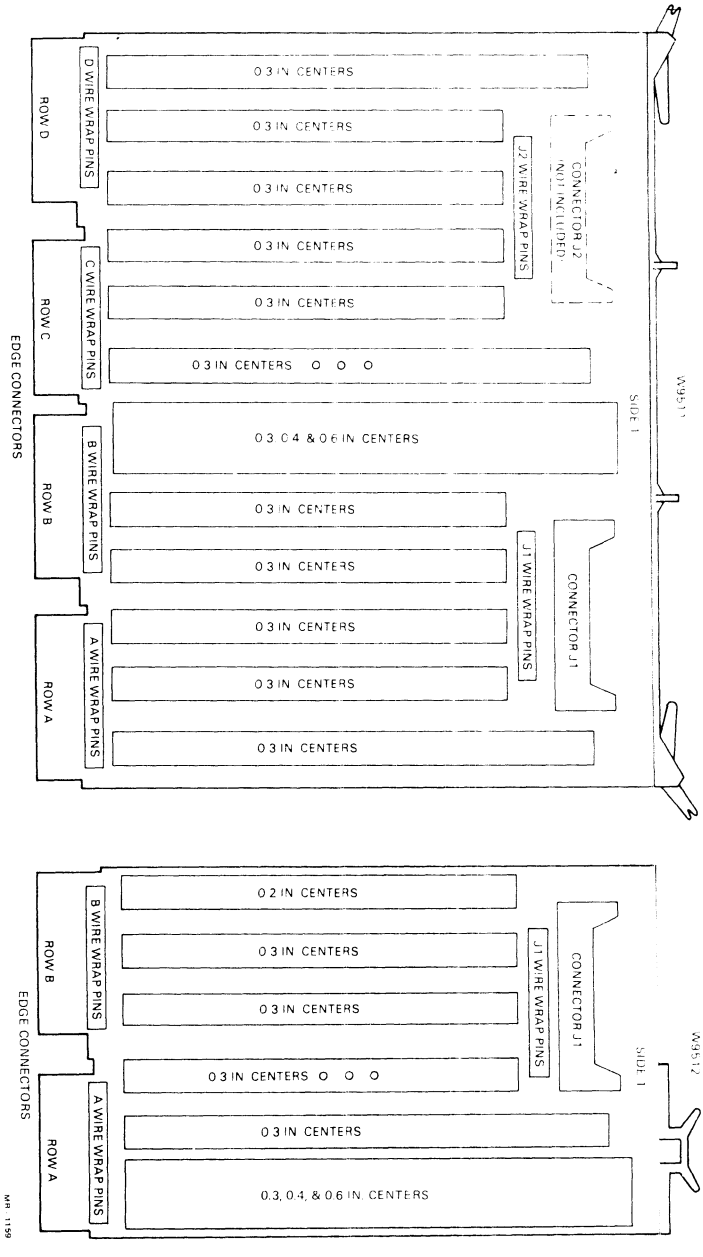


Figure 4-31 LSI-11 Bus-Compatible Modules (No DIP Sockets)

Figure 4-32 LSI-11 Bus-Compatible Modules (With DIP Sockets)

4.6 H780 POWER SUPPLY OPTIONS

Six H780 power supply options are available for use in LSI-11 bus systems. Individual model numbers determine combinations of 115 or 230 Vac (nominal) primary power and selection of master console, slave console, or no console. Models are listed below.

H780 Model No.	Input Power	Console Description	Figure
H780-C	115 V	None	4-33
H780-D	230 V	None	4-33
H780-H	115 V	Master	4-34
H780-J	230 V	Master	4-34
H780-K	115 V	Slave	4-35
H780-L	230 V	Slave	4-35

The H780 master console contains RUN and DC ON indicators for monitoring the processor states, as well as DC ON/DC OFF, LTC ON/OFF, and ENABLE/HALT switches for controlling the processor. The slave console contains only a DC ON indicator for monitoring the status of the slave power supply.

In addition to producing dc operating voltages (+5 V, 18 A and +12 V, 3.5 A) for system components, the H780 power supply automatically sequences BPOK and BDCOK bus signals for proper power-up/power-down operation. The power supply can be used as a stand-alone unit or it can be used with a backplane. Built-in cooling fans provide forced air cooling for the H780, and, when mounted to an H9270 backplane, also provide cooling for the system modules mounted in the backplane. High-frequency, low-voltage switching regulators and a multiplexing scheme provide control of overcurrent, overvoltage, slow voltage buildup, low line voltage, and short-circuit protection.

4.6.1 General

Six H780 power suppply options are available for use in system applications. The six models provide for a choice of input voltage (115 Vac or 230 Vac, nominal), and master console, slave console, or no console. The various models are defined and illustrated in Paragraph 4.6.

All models are used for supplying dc operating voltages to an LSI-11 bus backplane. In addition, each model generates a proper power-up/power-down sequence of BDCOK H and BPOK H LSI-11 bus signals. Master console-equipped and slave console-equipped models can be interconnected to allow control of both supplies from the master console.

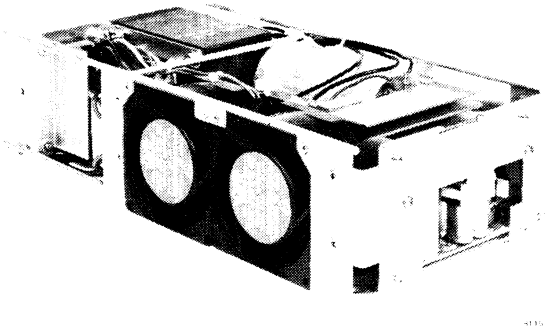


Figure 4-33 H780-C and -D Power Supplies

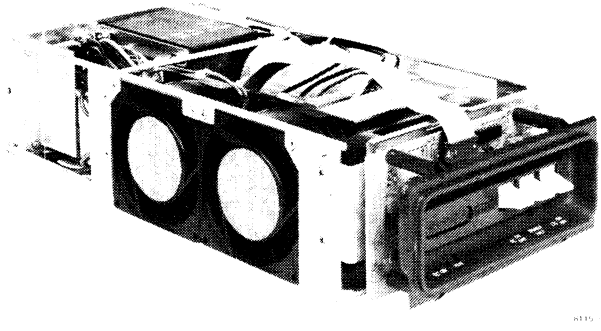


Figure 4-34 H780-H and -J Power Supplies

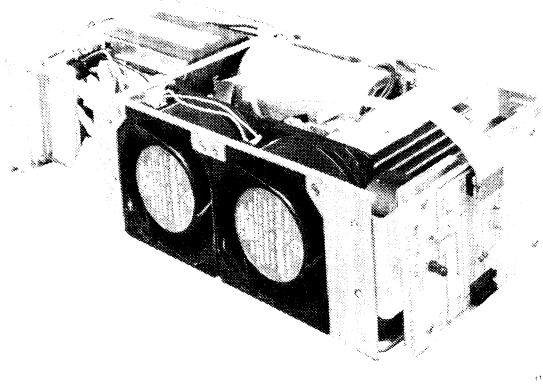


Figure 4-35 H780-K and -L Power Supplies

All H780 models feature:

- +5 V ± 3%, 18 A (maximum) and +12 V ± 3%, 3.5 A (maximum), combined dc power must not exceed 110 W.

- Overcurrent/short-circuit protection – Output voltages return to normal after removal of overload or short. Current limited to approximately 1.2 times the required maximum rating.

- Overvoltage protection – +5 V limited to +6.3 V (approx). +12 V limited to +15 V (approx).

- Line-time clock – A bus-compatible signal is generated by the power supply for the event (line-time clock) interrupt input to the processor. This signal is either 50 or 60 Hz, depending on primary power line frequency input to the power supply.

- Power-fail/automatic restart – Fault detection and status circuits monitor ac and dc voltages and generate bus-compatible BPOK H and BDCOK H signals (respectively) to inform the LSI-11 bus modules of power supply status.

- Fans – Built-in fans provide cooling for the power supply and modules contained in the system backplane.

4.6.2 Specifications

Input Voltage (Continuously – see Note 1)
100–127 Vac (H780-C, -H, -K)
200–254 Vac (H780-D, -J, -L)

Temporary Line Dips Allowed
100% of voltage, 20 ms max

AC Inrush Current
70 A at 127 V, 60 Hz (8.33 ms)
25 A at 254 V, 50 Hz (10 ms)

Input Power (fans included
340 W at full load max
290 W at full load typical

EMI (Emission and Susceptibility)
Per DEC STD 102.7 and VDE N-12 Limits

Input Protection
H780-C, -H, -K (100–127 Vac) fast blow, 5 A fuse
H780-D, -J, -L (200–254 Vac) fast blow, 2.5 A fuse

Hi-Pot
2 kV for 60 seconds from input to output, or input to chassis

Output Power (combinations not to exceed 110 W)
+5 V, 1.5 A – 18 A
+12 V, 0.25 A – 3.5 A

Maximum DC Current Under Fault Conditions
+5 V bus = 28 A
+12 V bus = 9.5 A

+5 V Output		
Total Regulation	5 V ± 3%	
Line Regulation	±0.5%	
Load Regulation	±1.0%	
Stability	0.1%/1000 hours	
Thermal Drift	0.025%/°C	(See Note 2)
Ripple	150 mV p-p (1% for f <3 kHz)	
Dynamic Load Regulation	±1.2% di/dt = 0.5 A/μs ΔI = 5 A	
Noise	1% peak at f > 100 kHz (noise is superimposed on ripple)	
Interaction due to +12 V	± 0.05%	
+12 V Output		
Total Regulation	12 V ± 3%	
Line Regulation	±0.25%	
Load Regulation	±0.5%	
Stability	0.1%/1000 hours	
(See Thermal Drift Note 2)	0.025%/°C above 25°C	
Ripple	350 mV p-p (1% for f <3 kHz)	
Dynamic Load Regulation	±0.8% di/dt = 0.5 A/μs f <500 Hz ΔI = 3 A	
Noise	1% peak f > 100 kHz (noise is superimposed on ripple)	
Interaction due to +5 V	±0.2%	

Overvoltage Protection	
+5 V	6.3 V nominal 5.65 V min 6.8 V max
+12 V	15 V nominal 13.6 V min 16.5 V max

Adjustments

+5 V Output	4.05 V–6.8 V Guarantee range 4.55–5.65 V
+12 V Output	10.6 V–16.5 V Guarantee range 11.7–13.6 V

Controls

Rear Panel	AC ON/OFF switch
Front Console	DC ON/OFF switch HALT/ENABLE switch
(Master only)	LTC ON/OFF switch
Console Indicators	DC ON RUN (Master) Spare (Master only)

Backplane Signals

BPOK H BDCOK H BEVNT L BHALT L	Transmitted
SRUN L	Received (Master only)

Mechanical

Cooling

Two self-contained fans provide (30 ft^3/min) 0.7140 m^3/min air flow.

Size

13.97 cm w × 8.43 cm h × 37.15 cm l
(5-1/2 in w × 3-1/3 in h × 14-5/8 in l)

Weight

5.90 kg (13 lb)

Environmental

Temperature

Ambient	5° to 50° C (41° to 122° F)
Storage	–40° to +70° C (–40° to +158° F)

Humidity

90% maximum without condensation

NOTES

1. Operation from ac lines below 100 V may cause the power supply to overheat because of decreased air flow from the cooling fans.
2. These parameters apply after 5 minutes of warmup and are measured with an averaging meter at the processor backplane terminal block under system loading.

4.6.3 Functional Description

4.6.3.1 General - Figure 4-36 is a block diagram of the H780 power supply. AC line voltage is applied to the two cooling fans and to the power transformer. The transformer has dual primary windings to meet U.S. and European power requirements. A single secondary winding generates a stepped-down ac voltage which is rectified and filtered to produce 26 Vdc (nominal) unregulated. The unregulated 26 Vdc is applied to two 3-terminal regulators which produce −15 V and +5 V for the H780 internal circuits. Unregulated 26 Vdc is also applied to +5 V and +12 V high-frequency, high-efficiency switching regulators. The outputs of the +5 V and +12 V switching regulators supply operating power to the backplane. Each switching regulator circuit is designed for good frequency stability, high noise rejection levels, and excellent load and line regulation. An L-C output filter and a fast-recovery diode are used in each switching regulator circuit. The +5 V switching regulator operates at a frequency from 7 kHz to 12 kHz, while the +12 V switching regulator operates from 8 kHz to 14 kHz. Both switching regulator circuits are protected from overvoltage, overcurrent, and short-circuit outputs. In addition, failsafe short-circuit startup is provided, along with

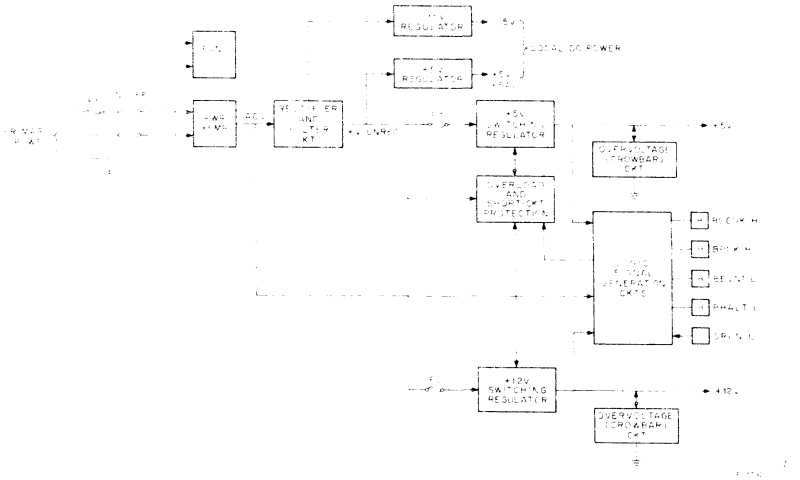


Figure 4-36 H780 Power Supply Block Diagram

protection against a short between the +5 V and +12 V outputs. Logic signal generation circuits within the H780 provide for proper power sequencing of the processor, as well as the generation of the line-time clock (BEVNT L) and power supply status signals. H780-H and -J options are supplied with a console which contains RUN and DC ON indicators for monitoring the processor and power supply states, as well as DC ON/DC OFF, LTC ON/OFF, and ENABLE/HALT switches for controlling the system. The H780-K and -L options have a console which contains only a DC ON indicator. H780-C and -D options have no console panel.

4.6.3.2 Unregulated Voltage and Local Power Circuits – Unregulated voltage and local power circuits provide operating dc power for power supply logic and control circuits, and dc power for the +5 V and +12 V regulator circuits. These circuits are shown in Figure 4-37. AC power is supplied to the H780 via an ac input plug and cable. A toggle switch mounted on the rear of the H780 applies ac power to the power supply. Normally, this switch remains in the ON position, allowing ac power to be controlled by power distribution and control circuits external to the H780. Primary circuit overload protection is provided by a fuse mounted on the rear of the H780.

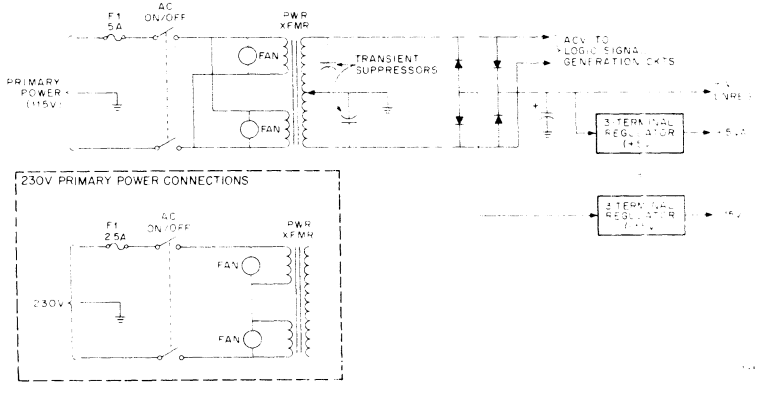


Figure 4-37 Unregulated Voltage and Local DC Power Circuits

Primary power circuits are factory-wired for 115 Vac (H780-C, -H, -K) or 230 Vac (H780-D, -J, -L) operation. Power transformer primary windings and the two fans operate directly from the switched ac power

A single center-tapped secondary winding supplies power for regulator circuits and internal circuit operation. Conventional full-wave rectifiers and a −15 V, 3-terminal regulator IC provide regulated voltage for internal distribution. The rectifiers also provide unregulated +30 V (+V UNREG) for internal distribution and regulator operation. A 3-terminal regulator integrated circuit provides 5 V "+5 A" power for H780 logic and control circuits. The +5 V and +12 V regulators use the same V UNREG voltage for regulation and distribution to the processor modules. AC voltage from one side of the transformer secondary is also routed to the line-time clock (LTC) circuit, which generates a BEVNT L bus signal for a line-time clock processor interrupt. When used with a 60 Hz line frequency, the interrupt occurs at 16.667 ms intervals; a 50 Hz line frequency will produce interrupts at 20 ms intervals.

4.6.3.3 +5 V and +12 V Switching Regulator Circuits – Both +5 V and +12 V regulator circuits receive the +V UNREG input power. The +5 V and +12 V regulator circuits are identical except for component values. Hence, only the basic +5 V regulator is described in detail.

The basic regulator is a switching regulator which operates at approximately 10 kHz. The main controlling element is a 3-terminal regulator which operates at approximately the regulated output voltage level. Basic regulator circuits are shown in Figure 4-38. Note that the ground terminal of the 3-terminal regulator is connected to a circuit that allows adjustment of the terminal voltage over a −0.7 V to +1.5 V range. Hence, the 3-terminal regulator output in the +5 V regulator circuit can range from 4.3 V to 6.8 V (approx).

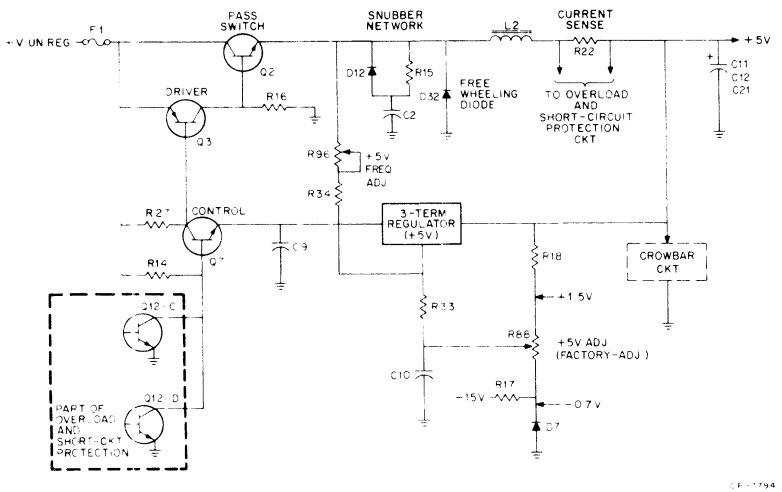


Figure 4-38 Basic Regulator Circuit

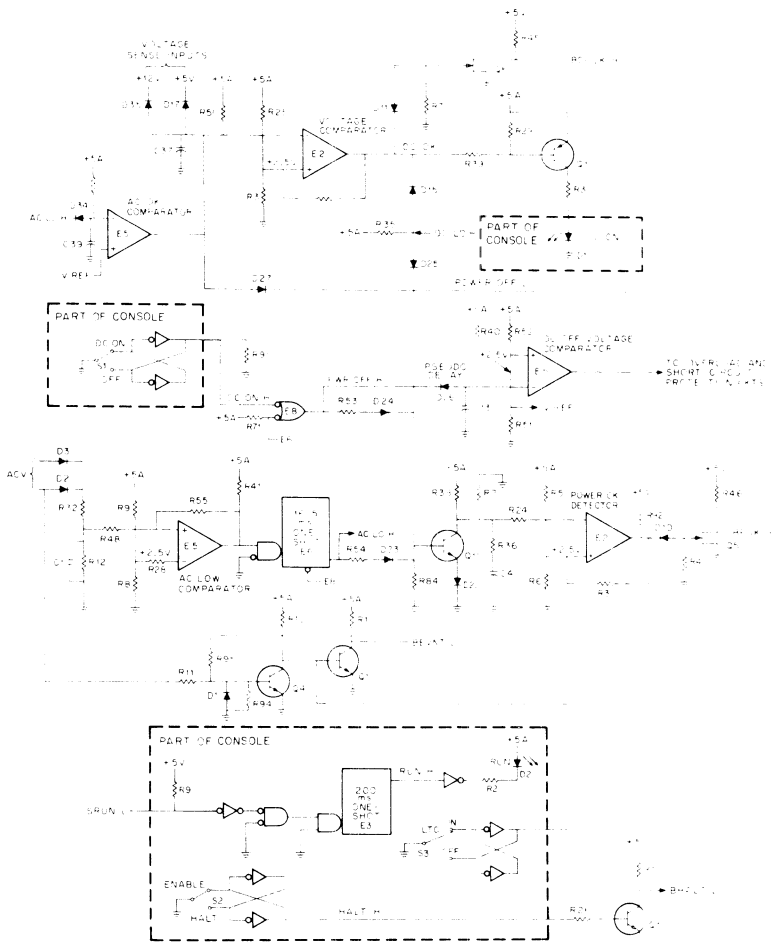


Figure 4-41 Logic Signal Generation Circuits

AC voltage monitor circuits include an ac low comparator, a 16.5 ms delay, and a BPOK H bus driver circuit, which is enabled only when BDCOK H is in the active (dc voltage normal) state. Rectifiers D2 and D3 produce positive-going dc voltage pulses at twice the ac line frequency. R32, R12, and C1 produce nominal +3.9 V (peak) normal line voltage

pulses which are coupled to the noninverting input of the ac low comparator via R48. R8 and R9 produce a +2.5 V reference for the comparator's inverting input. The comparator's normal output is a series of pulses occurring at twice the ac power line frequency. Each positive-going leading edge retriggers the 16.5 ms one-shot, keeping it in the set state. The 16.5 ms one-shot output is diode-ORed with DCOK L via diodes D25 and D23 and PWR OFF H via D24. Normally, the three signals are low and Q11 remains cut off. In this condition, C4 charges to +3.125 V via R36 and R38. This signal is then applied to the power OK comparator's inverting input via R24. Since the noninverting input is referenced to +2.5 V by voltage divider R5 and R6, the comparator's output goes low, biasing off FET Q5. Q5's source voltage then rises toward +5 V via R46, producing the active BPOK H signal. Power-up/power-down sequence timing is shown in Figure 4-42.

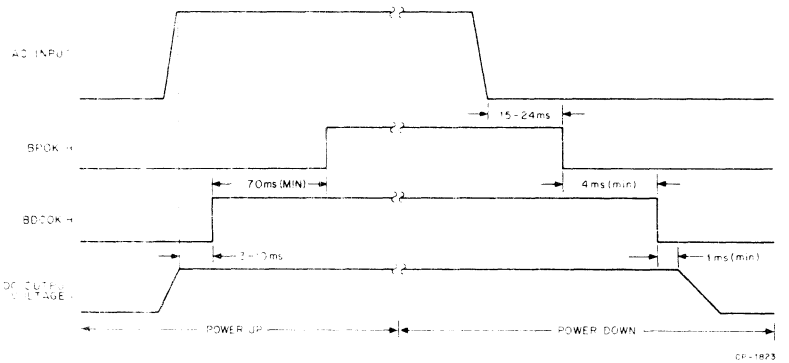


Figure 4-42 Power-Up/Power-Down Sequence

A power failure is first detected when the pulsating dc voltage at the ac low comparator's noninverting input is less than +2.5 V (peak). The comparator's output then remains low, allowing the 16.5 ms one-shot to go out of the retrigger mode. The one-shot resets 16.5 ms after the leading edge of the last valid ac voltage alternation; the 16.5 ms delay is equivalent to a full line cycle (two-alternate) failure. The high one-shot output is then coupled via D23 to the base of Q11, forward-biasing it.

Q11 conducts and rapidly discharges C4; R36 limits peak discharge current.

The low voltage thus produced is less than the +2.5 V reference at the power OK comparator's input, and its output goes high. Q5 then conducts and asserts the BPOK H signal low (power fail). The AC LO H

signal produced by the 16.5 ms one-shot is coupled via D34 to C39 on the inverting input of AC OK comparator E5. When C39's voltage rises above 2.5 V, the comparator's output goes low, turning off the DC ON indicator, negating BDCOK via the dc voltage monitor circuit, and turning off the regulator circuits by asserting POWER OFF L via D27.

When normal power is restored, the 16.5 ms one-shot returns to the retrigger (set) mode. AC LO H goes low and enables the dc voltage monitor and regulator circuits. The low AC LO H signal also removes forward bias from the base of Q11, cutting it off. Its collector voltage then rises as C4 charges at a relatively slow rate. R38 controls the charging rate of C4 and ensures that ac voltage and dc output voltages are normal for approximately 100 ms (70 ms minimum) before BPOK H goes high.

The DC ON/OFF switch simulates a power failure when it is placed in the OFF position. Cross-coupled inverters provide switch debounce protect on and a low (false) DC ON H signal is produced. This signal is inverted to produce a high PWR OFF H signal that is coupled via D26 to the "pseudo delay" circuit, causing a power-fail sequence to occur, and to Q11 via R53 and D24, causing BPOK H to go low (power-fail indication). After a 5–10 ms (approx) "pseudo delay," C13's voltage rises above the dc off voltage comparator's +2.5 V reference (noninverting) input. The comparator's output goes low, asserting POWER OFF L low and turning off the switching regulators. When the DC ON/OFF switch is returned to the ON position, PWR OFF H goes low, rapidly discharging C13. POWER OFF L then goes high and switching regulator operation resumes. Approximately 100 ms later, BPOK H goes high and normal processor operation is enabled. DC ON/OFF circuit timing is shown in Figure 4-43.

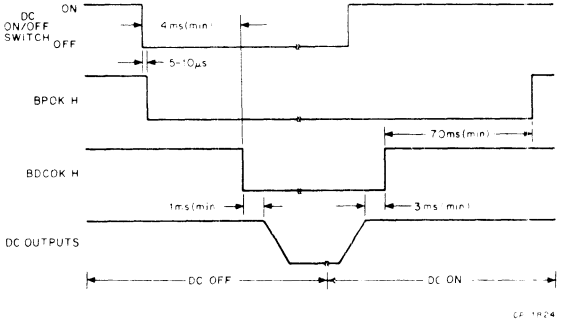


Figure 4-43 DC ON/OFF Circuit Timing

BEVNT L is the bused EVENT line which is normally used for line-time clock interrupts. Q4 is cut off and Q1 is forward-biased during negative alternations of the ac line, producing low-active BEVNT L signals. D1 clips negative alternations and limits Q4's reverse-bias to emitter voltage. The LTC ON/OFF switch must be in the ON position for BEVNT L signal generation. When the LTC function is not desired, the LTC switch is set to the OFF position; CSPARE2 goes low. Q1 remains cut off, and BEVNT L remains passive (high).

The RUN indicator is illuminated whenever the processor is executing programs. SRUN L, a nonbused backplane signal, is a series of pulses which occur at 3–5 μs intervals whenever the processor is in the Run mode. The pulses trigger a 200 ms one-shot on each SRUN L pulse leading edge, keeping it in the retrigger mode. Its high RUN H output signal is then inverted, producing a low signal that turns on the RUN indicator. When the processor is in the Halt mode, SRUN L pulses cease and the 200 ms one-shot resets after the 200 ms delay. The RUN indicator turns off, indicating the Halt mode.

The HALT/ENABLE switch allows the operator to manually assert the BHALT L signal low, causing the processor to execute console ODT microcode. When in the ENABLE position, BHALT L is not asserted, and the Run mode is enabled. Cross-coupled inverters provide a switch debounce function.

4.6.4 H780-C, -D, -H, -J, -K, -L Installation

Installation of an H780 power supply consists of inspecting the unit, connecting a suitable dc power cord, setting up the +5 and +12 Vdc outputs, and connecting the power supply to the system.

4.6.4.1 Differences Between 115 Vac and 230 Vac Power Supplies – The main differences between the 115 Vac H780 power supplies (H780-C, -H, and -K) and the 230 Vac H780 power supplies (H780-D, -J, and -L) are the ac input jumper configuration on the power supply terminal block (TB1), the fuse rating (115 Vac supplies are equipped with a 5 A fast-blow fuse; the 230 Vac supplies have a 2.5 A fast-blow fuse), and the power line RFI filter which is used only on the 230 Vac supplies. Power supplies factory-wired for 115 Vac operation (H780-C, -H, and -K) can be rewired for 230 Vac operation by reconfiguring the jumpers on TB1. However, European users of 115 Vac supplies should not rewire the H780-C, -H or -K for 230 Vac operation as these supplies will not meet the EMI requirements of VDE N-12. On the other hand, the 230 Vac supplies (H780-D, -J, and -L) can be rewired for 115 Vac and used in European countries as well as the U.S. AC wiring configurations for the H780 power supplies are detailed in Paragraph 4.6.4.5.

4.6.4.2 Space Requirements – The H780 power supply occupies a space 13.97 cm wide X 8.43 cm high X 37.15 cm long (5-1/2 in wide X 3-1/3 in high X 14-5/8 in long). Space should be available to the rear of the supply to gain access to the AC ON/OFF toggle switch. H780-H, -J, -K and -L options should be installed to allow for unobstructed viewing and use of the power supply console.

4.6.4.3 Input Power Requirements – The user's ac power source must be capable of providing 340 W (full load) of ac power at 50 ± 1 Hz or 60 ± 1 Hz. No ac power cord is supplied with the H780 options. It is the user's responsibility to provide the proper line cord and ac plug for his particular application. AC power connections to the H780 are detailed in Paragraph 4.6.4.5.

4.6.4.4 Cable Requirements – Three interface cables are supplied with the H780 options to connect the H780 console to the power supply and to connect the H780 to the system backplane. These cables are listed below by type and part number.

Cable	Digital Part No.
DC output cable (connects dc to backplane)	70-11584-0-0
Power supply status cable (logic cable) (connects logic signals to backplane)	70-11411-0K-0
Power supply console cable (connects console to H780)	70-08612-0M-0

Refer to the BA11-N description (Paragraph 4.3.3) for multiple backplane interconnection information.

In addition, if the user is controlling an H780 slave power supply (H780-K or -L) from an H780 master (H780-H or -J), the interface cable between the master and slave is the user's responsibility. This cable can be constructed from 12-conductor ribbon cable and two 16-pin, IC-type male connectors (3M part number 3416). The master/slave cable can be ordered from the nearest Digital Equipment Corporation Sales Office. Cable lengths and part numbers are listed in Table 4-12.

4.6.4.5 Installation Procedure – After unpacking the H780 from the shipping container, inspect the unit and report any damage to the nearest Digital Equipment Corporation Sales Office. Inspect for the following:

1. Damage to the chassis or printed circuit boards

Table 4-12 Master/Slave Interface Cables

Length	DIGITAL Part No.
10.2 cm (4 in)	70-08612-0D
15 cm (6 in)	70-08612-0F
22.9 cm (9 in)	70-08612-0K
27.5 cm (11 in)	70-08612-0M
35.6 cm (14 in)	70-08612-1B
45.7 cm (18 in)	70-08612-1F
124 cm (49 in)	70-08612-4A
61.0 cm (2 ft)	70-08612-02
1.83 m (6 ft)	70-08612-6A
3.05 m (10 ft)	70-08612-10

2. Loose or broken components

3. Damage to the console on the H780-H, -J, -K, or -L

4. Free rotation of the blades on the cooling fans

5. Proper amperage fuse (2.5 A fast-blow for H780-D, -J, and -L; 5 A fast-blow for H780-C, -H, and -K)

6. Proper seating of the fuse

7. Proper seating of the console cable connectors (H780-H, -J, -K, and -L)

8. The presence of the shield covering the terminal block at the rear of the H780.

Connecting AC Line Cord – The H780 power supplies are equipped with a terminal block (Figure 4-44) at the rear. Jumpers on this terminal block configure the supply for 115 Vac or 230 Vac operation (Paragraph 4.6.4.3), while two of the terminal block screws provide a means of connecting ac input power to the H780. A suitable length of No. 16 AWG, 3-conductor, stranded power cord is to be connected to the terminal block as shown in Figure 4-44 (for H780-C, -H, and -K supplies), or Figure 4-46 (for H780-D, -J, and -L supplies). The jumpers shown in Figures 4-45 and 4-46 are factory-installed. However, the jumper configuration can be altered by the user to change the ac input from 115 V to 230 V for the H780-C, -H, and -K, or from 230 V to 115 V for the H780-D, -J, and -L. European users are advised not to operate an H780-C, -H, or -K power supply on a 230 Vac line as these supplies are not

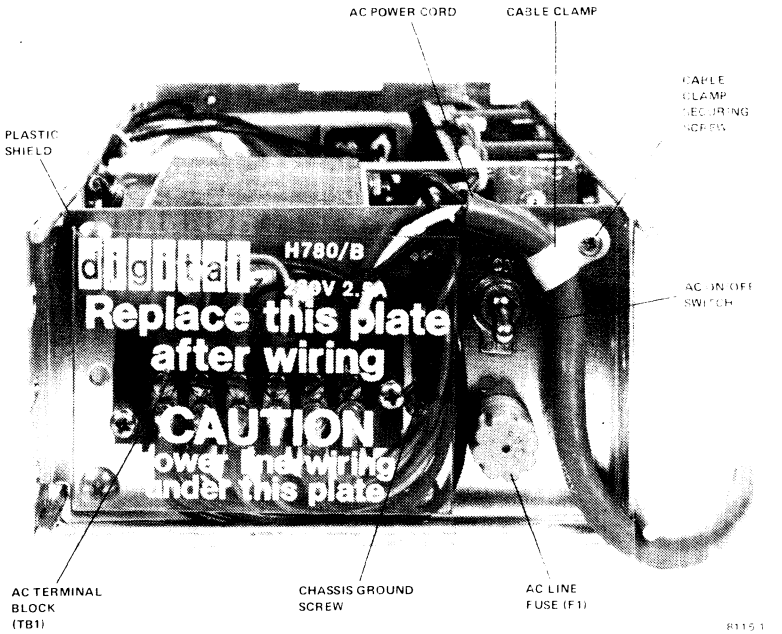


Figure 4-44 AC Terminal Block at Rear of H780

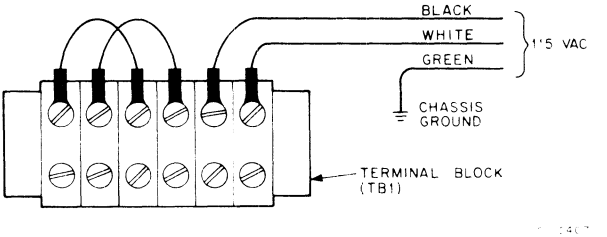


Figure 4-45 H780-C, -H, and -K (115 Vac) AC Terminal Block Wiring Configuration

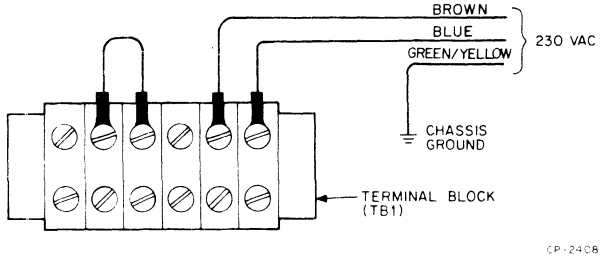


Figure 4-46 H780-D, -J, and -L (230 Vac) AC Terminal Block Wiring Configuration

equipped with a RFI line filter. When installing the ac line cord, remove the plastic shield covering the terminal block (Figure 4-44). Terminals should be crimped or soldered to the power cord wires. Connect the ac phase wires to the terminal block (Figures 4-45 and 4-46) and connect the ac ground wire to the H780 chassis using the Phillips head screw to the right of the terminal block (Figure 4-44). This screw also provides a ground for the RFI filter in the H780-D, -J, and -L supplies by means of a green/yellow wire. Make sure this wire is reconnected to ground when replacing the screw. Be sure to replace the plastic shield over the terminal block after completing the wiring. Route the power cord to the top of the H780 chassis and secure it to the chassis with a suitable strain relief, as shown in Figure 4-44. The upper right screw at the rear of the H780 chassis can be used to anchor a cable clamp. The free end of the power cord should be terminated with a connector which is suitable for the user's requirements.

H780-C and H780-D Stand-Alone Operation – If an H780-C or -D power supply is to be used as a stand-alone supply, a 510 Ω, 1/4 W resistor must be installed between J2-2 and J2-9 on the power supply printed circuit board (Figure 4-47). The 510 Ω resistor provides a pull-up level to an internal power supply gate, thus enabling the +5 V and +12 V outputs. This resistor is not required for the H780-K or -L slave supplies, nor is the resistor required for the H780-H and -J supplies. The resistor can be installed by bending its leads and inserting them into socket J2, or by soldering the resistor across pins 2 and 9 of a 16-pin DIP, IC-type male connector. Pinning for the J2 enable plug is shown in Figure 4-48.

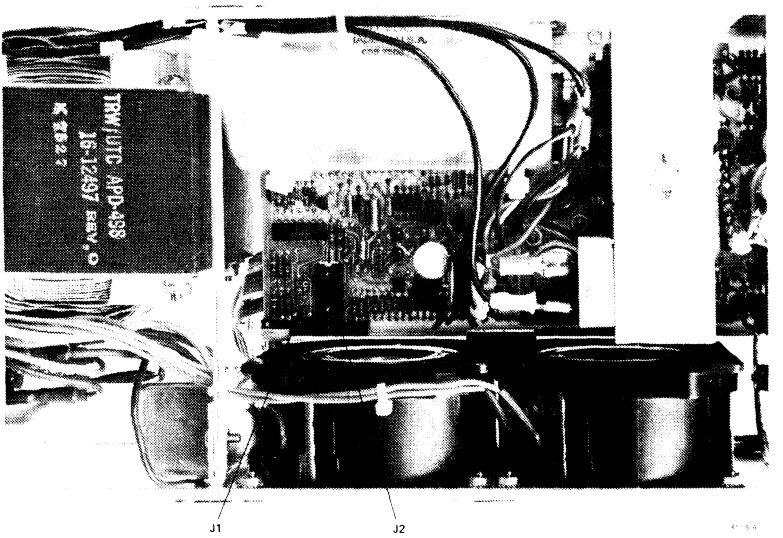


Figure 4-47 Locations of J1 and J2 on Power Supply Board

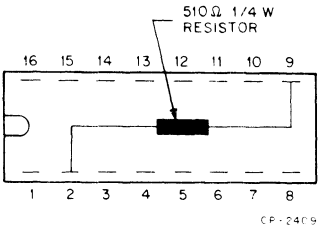


Figure 4-48 H780-C and -D Enable Plug

Initial Power Turn-On – Before connecting the dc output of the H780 to a system, verify the dc output voltages by performing the following procedure.

1. If the H780 is a slave supply (or an H780-C, -D), either connect cable J2 REMOTE of the slave H780 (or J2 on the power supply PC board of H780-C, -D) to the J2 REMOTE connector on the H780 master supply or install a 510 Ω 1/4 W resistor into the slave (Paragraph 4.6.4.5).

2. Connect the H780 to a suitable ac power source.

3. Set the H780 AC ON/OFF switch (Figure 4-44) to ON. The fans in the H780 should operate.

4. On H780-H and -J options, set the console DC ON/OFF switch (Figure 4-57) to ON. The DC ON indicator should light. (For master-slave operation, the DC ON/OFF switch and DC ON indicator are located on the user's master supply. The DC ON indicator on the slave should also light.)

5. Using a DVM, measure the +5 and +12 Vdc outputs at J4 (Figures 4-52 and 4-53) on the H780 PC board (side 2). The +5 V output should not be greater than +5.15 V and the +12 V output should not exceed +12.36 V. Perform the adjustment procedure in Paragraph 4.6.4.7 if the outputs are out of tolerance.

6. Set the master console DC ON/OFF switch to the OFF position.

7. Set the AC ON/OFF switch to the OFF position.

8. Unplug the ac power cord and connect the H780 system.

Mounting an H780 to an H9270 Backplane – The H780 power supply is designed to be mounted to the LSI-11 H9270 backplane. Four holes on the left side of the H780 are equipped with No. 8-32 threaded bosses (Figure 4-49). These holes mate with four holes in the right side of the H9270 backplane frame. Four No. 8-32 X 1/2 inch screws are inserted through the H9270 backplane holes and are threaded into the H780 power supply. The H9270 backplane and the H780 power supply thus become one assembly (Figure 4-50). Figure 4-49 shows the location of the four mounting holes in the H780. The two screws securing the front-chassis partition must be removed. These screws are to be replaced with longer screws (1/2 in) when attaching the H780 to the H9270.

Connecting an H780 to an H9270 Backplane – The H780 power supply is connected to the H9270 by means of two cables. These cables are supplied with the H780. One of these cables is a 25.4 cm (10 in) logic signal cable (DIGITAL part number 70-11411-0K-0), which connects from J1 on the power supply board (Figure 4-47) to connector pins on the H9270 printed circuit board (Figure 4-51). Either end of this cable can be connected to the power supply or the backplane. The other cable is a 30.5 cm (12 in) dc output cable (part number 70-11584-0-0). This cable is terminated at one end with a keyed, 12-pin connector which mates with J4 on side 2 of the H780 power supply board. Figure 4-52 shows the location of J4; Figure 4-53 shows J4 pinning. The remaining end of the dc output cable is terminated with a 6-lug connector strip which is connected to the H9270 backplane terminal block,

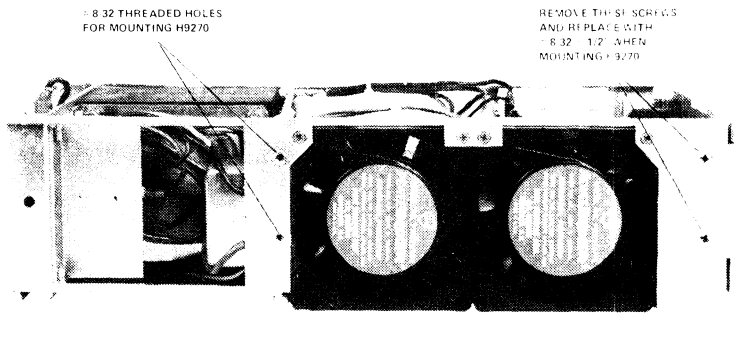


Figure 4-49 Left Side of H780 Showing H9270 Mounting Holes

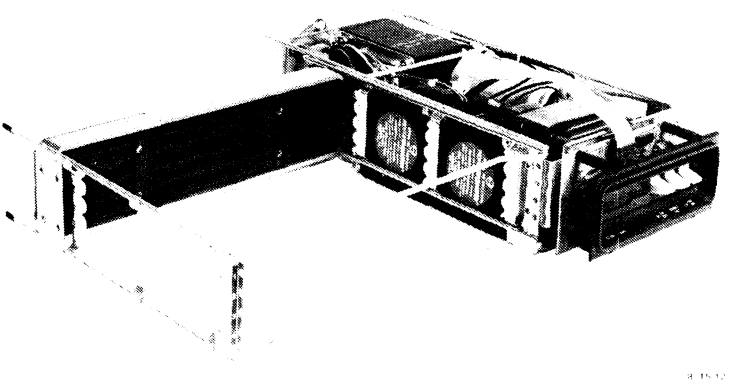


Figure 4-50 H780 Mounted to H9270 Backplane

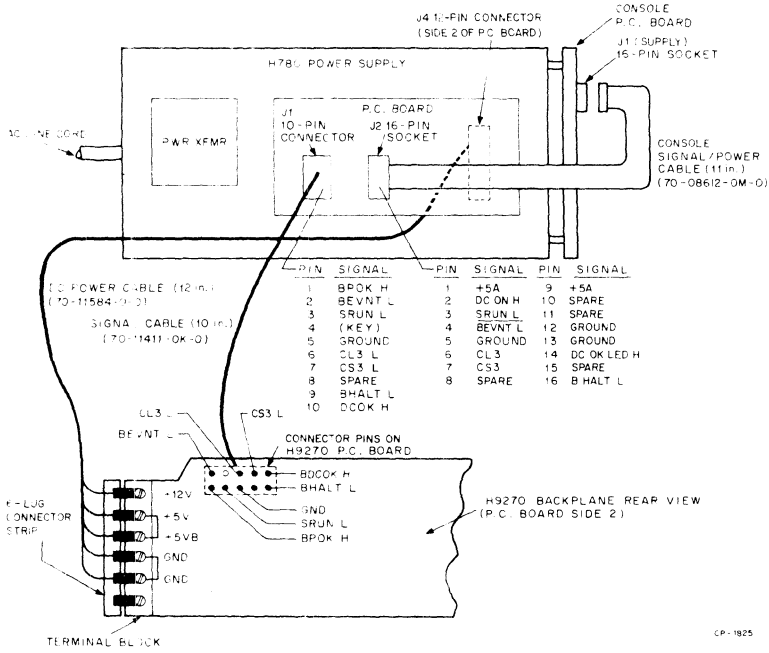


Figure 4-51 H780 to H9270 Backplane Connections

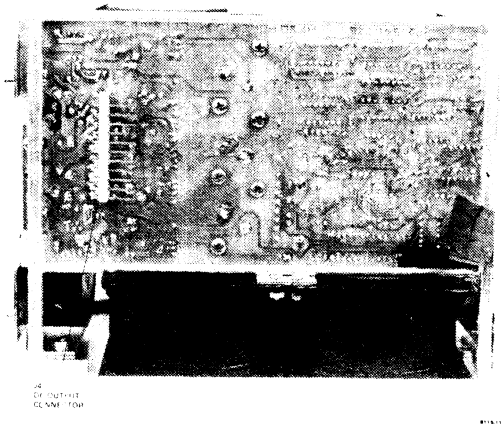


Figure 4-52 Location of H780 DC Output Connector (J4)

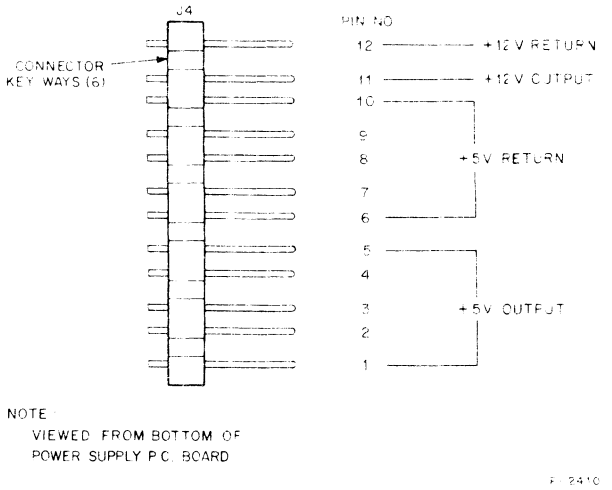


Figure 4-53 Pinning for H780 DC Output Connector (J4)

as shown in Figure 4-51. When connecting the 6-lug connector strip to the H9270 backplane, make sure that the spade lug connectors are facing up. Figure 4-54 shows the dc output cable connected to J4 of the H780. The H780 logic signal and dc output cables are routed toward the rear of the power supply and exit from the supply chassis next to the H9270 backplane terminal block.

H780-H, -J, -K, and -L power supplies have a console that is attached to the H780 and connected to the supply by means of a console signal/power cable (part number 70-08612-0M-0). This cable is factory-installed from J2 on the power supply board (Figure 4-47) to J1 on the console PC board (Figures 4-51 and 4-55).

H780 Master-Slave Connection – An H780-H or -J power supply can be used as a master supply to control an H780-K or -L slave supply. This master-slave arrangement allows the user to power up/power down system expander backplane logic from the master supply console. The slave supply is connected to the master supply by means of the J2 (REMOTE) connector on the master supply console printed circuit board, and J2 (REMOTE) or J3 on the slave power supply console printed circuit board. *The interconnecting cable is the user's responsibility.* Two 16-pin, IC-type male connectors and a suitable length of 16-conductor cable (preferably ribbon type) can be used to construct the interconnecting cable.

Figure 4-55 shows the console printed circuit boards and the locations of the J1 (SUPPLY), J2 (REMOTE), and J3 connectors. J1 is always connected to J2 of the power supply printed circuit board (Figure 4-51) by the console signal/power cable (part number 70-08612-0M-0) which is factory-installed. Pinning for J2 (REMOTE) on the console printed circuit board is shown in Figure 4-56. Pinning for J2 on the power supply printed circuit board is indicated in Figure 4-51.

Connector J3 (Figure 4-55) provides the means of interconnecting boxes in a multiple backplane system. This connector parallels connector J2, so a user can connect J2 on the slave BA11-M to J2 on the master PDP11/03 using the cable supplied with the first BA11-M expansion box, and can connect J3 on the first slave BA11-M to J2 on the second slave BA11-M using the cable supplied with the second BA11-M.

The slave console boards in the early model power supplies did not contain connector J3. Therefore, a single cable containing three DIP plugs (BC03Y-16) should be purchased to interconnect boxes in a multiple backplane system. Each DIP plug is inserted into connector J2 on each box.

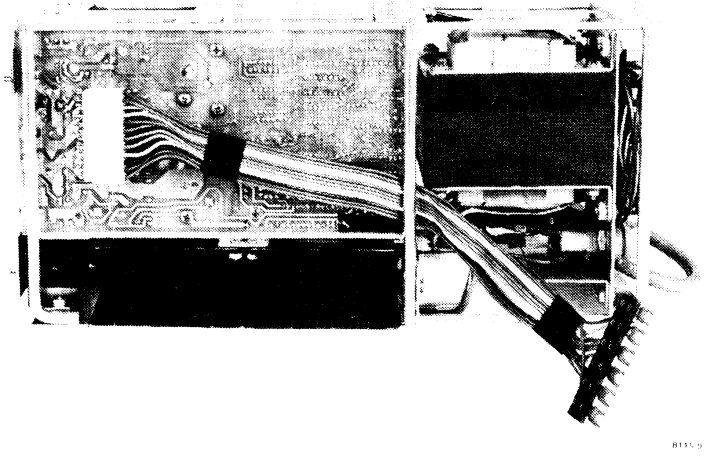
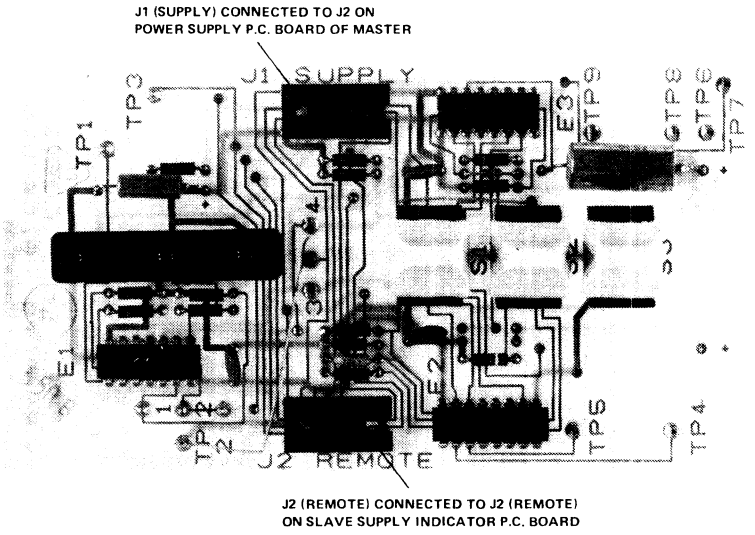
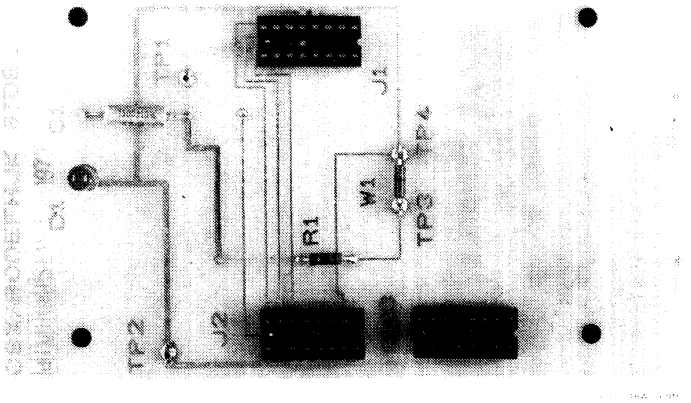


Figure 4-54 H780 DC Output Connector (J4) with Mating DC Output Cable (70-11584-0-0)



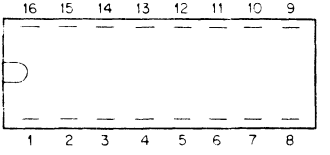
a. H780-H and -J (Master)

8115-2



b. H780-K and -L (Slave)

Figure 4-55 H780 Master-Slave Connections



J2 (REMOTE)

PIN	SIGNAL	PIN	SIGNAL
1	NO CONNECTION	9	NO CONNECTION
2	DC ON H	10	SPARE 3
3	NO CONNECTION	11	SPARE 4
4	SPARE 2	12	SPARE 5
5	GROUND	13	GROUND
6	CL3 L	14	DC OK H
7	CS3 L	15	SPARE 6
8	SPARE 1	16	NO CONNECTION

CP-2411

Figure 4-56 Pinning for J2 (REMOTE) on Console Printed Circuit Board

4.6.4.6 Console Controls and Indicators – The H780-H or -J master console has three LED indicators and three 2-position toggle switches. One of the LED indicators is a spare indicator. Circuitry to drive this indicator is included on the console printed circuit board for user application. The console on the H780-K and -L slave supplies has only one LED indicator, DC ON. Figure 4-57 shows the H780 console controls and indicators; they are described in Table 4-13. Additionally, the rear panel of the H780 contains an AC ON/OFF toggle switch and an ac line fuse (Figure 4-44).

4.6.4.7 +12 V and +5 V Adjustment Procedure – The H780 power supply is factory-adjusted to produce +12 V and +5 V outputs within the operating tolerance of the system. The adjustment procedures presented allow the user to trim the dc outputs of the H780 to meet his particular needs. One adjustment is provided for the +12 V output, while two adjustments (one for the output voltage and one for the switching regulator frequency) are provided for the +5 V. Figure 4-58 shows the location of the adjustments. A DVM, an oscilloscope, and a small screwdriver are required. Power supply loading is provided by the LSI-11 bus or processor.

Table 4-13 H780 Controls and Indicators

Control/ Indicator	Type	Function
DC ON	LED indicator	Illuminates when the DC ON/OFF toggle switch is set to ON and proper dc output voltages are being produced by the H780. If either the +5 or +12 V output from the H780 is faulty, the DC ON indicator will not illuminate. This is the only indicator on the H780-K and -L slave supplies.
RUN	LED indicator	Illuminates when the processor is in the run state (see ENABLE/HALT).
SPARE	LED indicator	Not used by the H780 or processor. The H780 contains circuitry for driving this indicator for user applications.
DC ON/OFF	Two-position toggle switch	When set to ON, enables the dc outputs of the H780. The DC ON indicator will illuminate if the H780 dc output voltages are of proper values. If a slave supply is connected to a master, the slave DC ON indicator will light if the slave dc output voltages are of proper value. When set to OFF, the dc outputs from the H780 are disabled and the DC ON indicator is extinguished. If a slave supply is connected to a master, the slave DC ON indicator will also extinguish.

Table 4-13 H780 Controls and Indicators (Cont)

Control/ Indicator	Type	Function
ENABLE/HALT	Two-position toggle switch	When set to ENABLE, the B HALT L line from the H780 to the processor is not asserted and the processor is in the Run mode (RUN indicator illuminated). When set to HALT, the B HALT L line is asserted, allowing the processor to execute console ODT microcode (RUN indicaor extinguished).
LTC ON/OFF	Two-position toggle switch	When set to ON, enables the generation of the line-time clock (LTC) BEVNT L signal by the H780. When set to OFF, disables the H780 line time clock.
AC ON/OFF (rear panel)	Two-position toggle switch	When set to ON, applies ac power to the H780. When set to OFF, removes ac power from the H780.
FUSE (rear panel)	5 A or 2.5 A fast-blow	Protects H780 from excessive current. H780-C, -H, and -K use a 5 A fuse, H780-D, -J, and -L use a 2.5 A fuse.

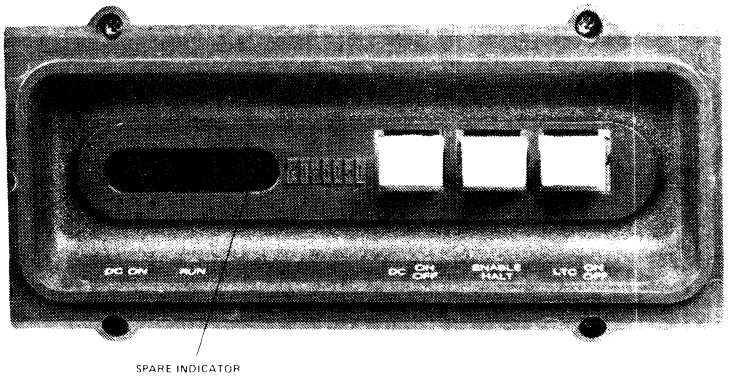


Figure 4-57 Console Controls and Indicators

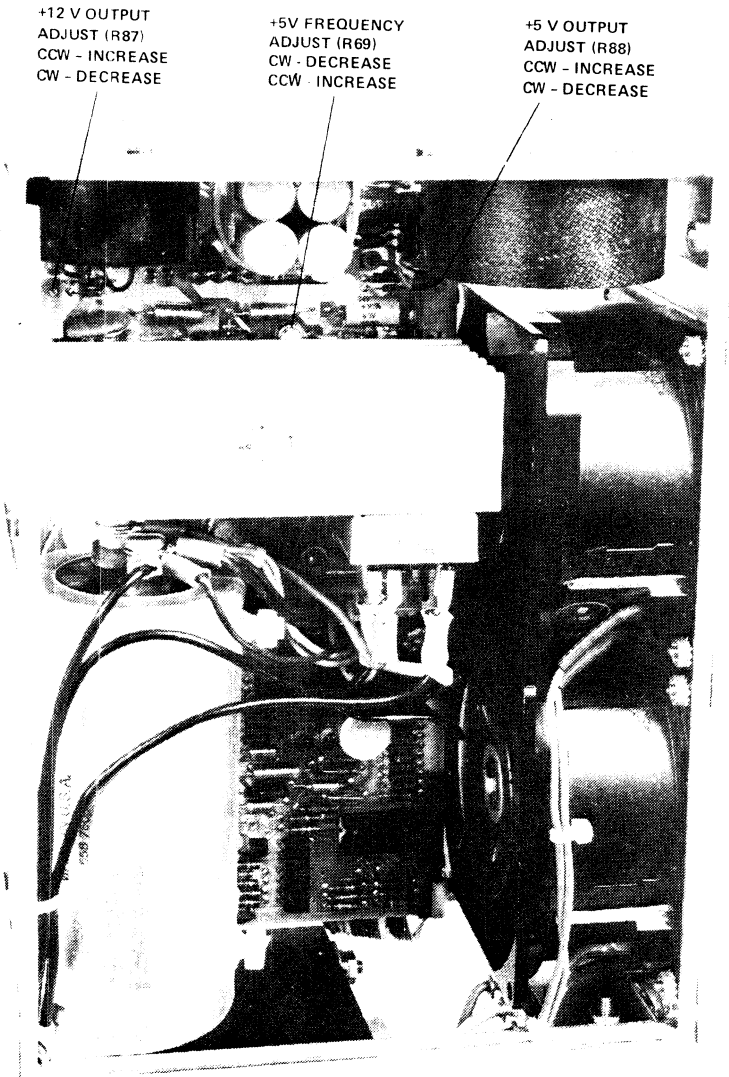


Figure 4-58 Locations of H780 Adjustments

+12 V Adjustment – Perform the following procedure when adjusting the +12 Vdc output.

1. Apply power to the system and allow a 5-minute warmup period.

2. Using a DVM, measure the +12 V output at the system backplane terminal block (Figure 4-51).

3. Using a small screwdriver, adjust R87 (Figure 4-58) until the DVM indicates +12.0 V (+11.64 V to +12.36 V acceptable range). Turning R87 clockwise decreases the +12 V output, while turning counterclockwise increases the output.

NOTE

If R87 is turned too far counterclockwise, the +12 V output will crowbar and drop to approximately 0 V. This will occur between +13.0 V and +16.5 V. Do not allow the supply to crowbar as this may blow the internal fuse (F1) protecting the +12 V regulator.

4. Using an oscilloscope, measure the ripple on the +12 V output at the backplane terminal block. The ripple should not be greater than 350 mV peak-to-peak.

5. Using an oscilloscope, measure the amplitude and frequency of the ripple on the +12 V output at the backplane terminal block. The ripple should not be greater than 350 mV peak-to-peak with a period from 65–140 μs. If the ripple period is not within 80–140 μs, adjust R37 to +12 V.

+5 V Adjustment – Perform the following procedure when adjusting the +5 Vdc output.

1. Apply power to the system and allow a 5-minute warmup period.

2. Using a DVM, measure the +5 V output at the system backplane terminal block (Figure 4-50).

3. Using a small screwdriver, adjust R88 (Figure 4-58) until the DVM indicates +5.0 V (+4.85 V to +5.15 V acceptable range). Turning R88 clockwise decreases the +5 V output, while turning counterclockwise increases the output.

NOTE

If R88 is turned too far counterclockwise, the +5 V output will crowbar and drop to approximately 0 V. This will occur between +5.6 V and +6.8 V. Do not allow the supply to crowbar as this may blow the internal fuse (F2) protecting the +5 V regulator.

4. Using an oscilloscope, measure the amplitude and frequency of the ripple on the +5 V output at the backplane terminal block. The ripple should not be greater than 150 mV peak-to-peak with a period from 80–140 μs. If the ripple period is not within 80–140 μs, adjust R96 (Figure 4-58). Turning R96 clockwise decreases the ripple period, while turning counterclockwise increases the period. After adjusting the ripple period, recheck the +5 V output (steps 2 and 3).

4.7 CABLES AND CONNECTORS

Preassembled cables are available in a variety of lengths and types as listed in Table 4-14. The H854 and H856 connectors are shown in Figure 4-59.

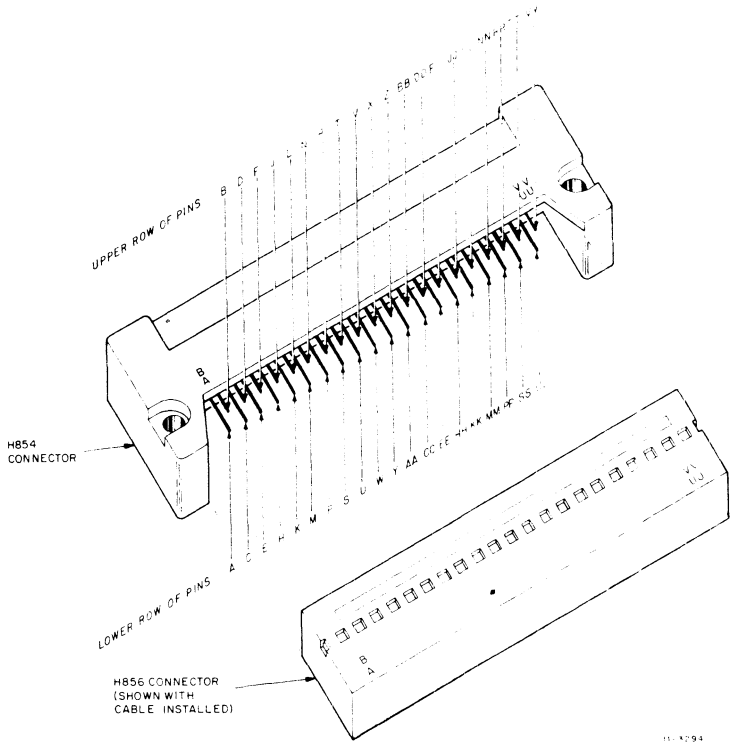


Figure 4-59 J1 or J2 Connector Pin Locations

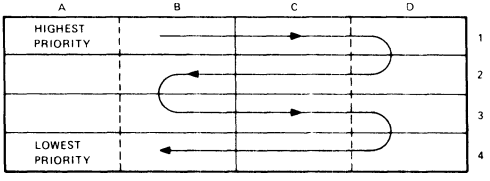
Table 4-14 Preassembled Cables

Part No	Cable Length cm (ft)	Used On	Connector	Cable Material	Connector
BC04Z-10	3.05 m (10 ft)	General purpose	H856	Flat, 40-cond Mylar	Open
BC07D-10	3.05 m (10 ft)	General purpose	H856	Ribbon, 20-conductor	Open
BC07D-15	4.6 m (15 ft)	General purpose	H856	Ribbon, 20-conductor	Open
BC07D-25	7.6 m (25 ft)	General purpose	H856	Ribbon, 20 conductor	Open
BC08R-01	0.3 m (1 ft)	General purpose	H856	Flat, 40-conductor	M856
BC08R-XX	XX	General purpose	H856	Flat 40-cond Mylar	H856
BC05M-02	0.61 m (2 ft)	Multi-use	H856	Round, shielded leads, 2-conductor	12-0934-00
BC05C-25	7.6 m (25 ft)	EIA interface Multi-use	H856	Round, 25-conductor	RS232 (Male)
BC05L-XX*	XX	Backplane expansion	H856	Flat, 40-conductor	H856
BC11V-X	X	Signal	H856	Flat-twisted pair 40-conductor	Open

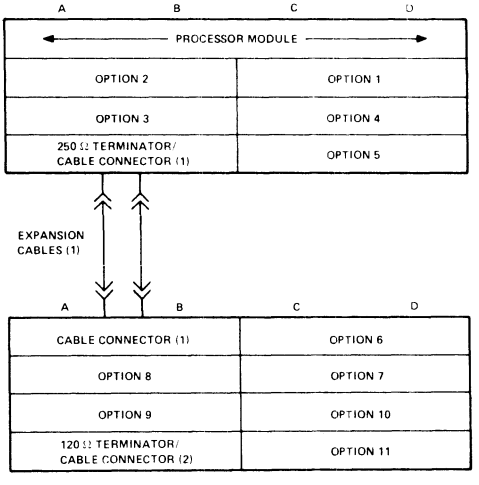
*The BC05L-XX is contained in the BCV1A and BCV1B options.

4.7.1 Using the BCV1B

The BCV1B option includes two BC05L cables, one M9400-YE module, and one M9401 module. This option is always used to connect the first backplane to a second backplane in multiple backplane systems. Refer to Figures 4-60 and 4-61.



Note:
Arrow indicates BDMG and BIAK daisy chain signal routing from highest priority device slot to lowest priority device slot on the backplane.



Notes:
1. Included in BCV1B bus expansion option. (Cables are available in 2, 4, 6, or 12 ft. lengths.)
2. Included in TEV11 bus terminator option.

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Figure 4-60 BCV1B Installation

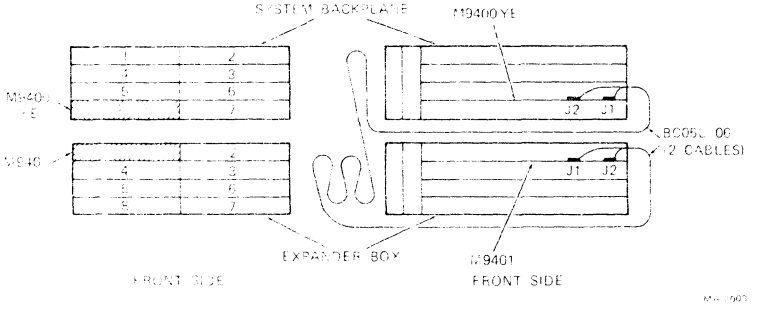
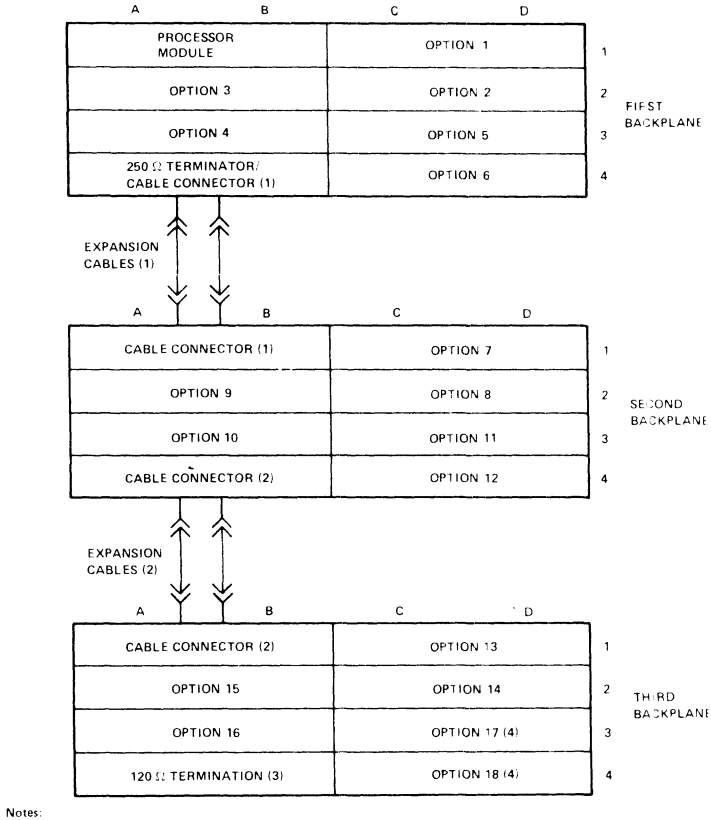


Figure 4-61 BA11-M Expansion Box Interconnections (two-backplane system)

4.7.2 Using the BCV1A

The BCV1A option includes two BC05L cables, one M9400-YD module, and one M9401 module. This option is always used to connect the second backplane to the third backplane in a 3-backplane system as shown in Figure 4-62.



Notes:

1. Included in BCV1B bus expansion option. (Cables are available in 2, 4, 6, or 12 ft. lengths.)
2. Included in BCV1A bus expansion option. (Cables are available in 2, 4, 6, or 12 ft. lengths.)
3. Included in TEV11 bus terminator option.
4. The LSI11 Bus is restricted to 15 options maximum. These option slots would only be used when previous options occupy more than 1 option location.
5. BCV1A and BCV1B expansion cables must differ in length by four feet (minimum).

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Figure 4-62 BCV1A Installation

CHAPTER 5

INTEGRATED CIRCUITS

This chapter contains descriptions, specifications, and circuit diagrams for five integrated circuits available from DIGITAL for use in LSI-11 bus systems. A DMA application design is presented using a combination of these integrated circuits as an illustration of a specific design approach.

5.1 INTEGRATED CIRCUITS

5.1.1 Bus Receivers and Bus Drivers

The equivalent circuits of LSI-11 bus-compatible drivers and receivers are shown in Figure 5-1. To perform the receiver and driver functions, Digital Equipment Corporation uses two monolithic integrated circuits with the characteristics listed in Table 5-1. A typical bus driver circuit is shown in Figure 5-2. Note that 8641 quad transceivers can be used, combining LSI-11 bus receiver and driver functions in a single package. Bus receiver (8640), bus driver (8881), and bus transceivers (8641) are shown in Figures 5-3, 5-4, and 5-5, respectively.

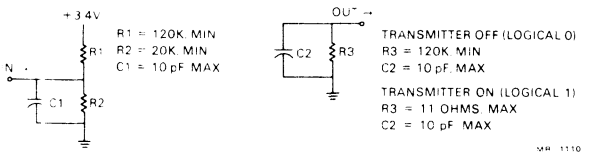


Figure 5-1 Bus Driver and Receiver Equivalent Circuits

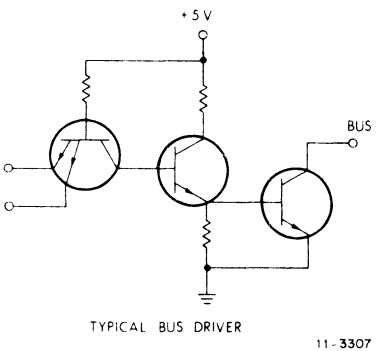


Figure 5-2 Typical Bus Driver Circuit

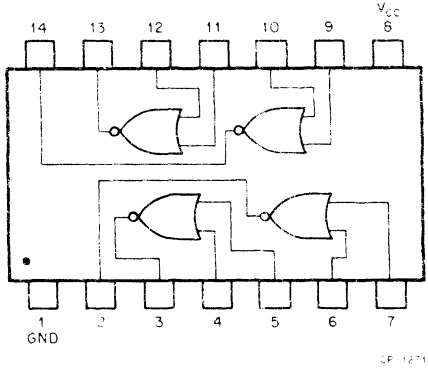


Figure 5-3 8640 Quad 2-Input NOR Gates (Bus Receiver)

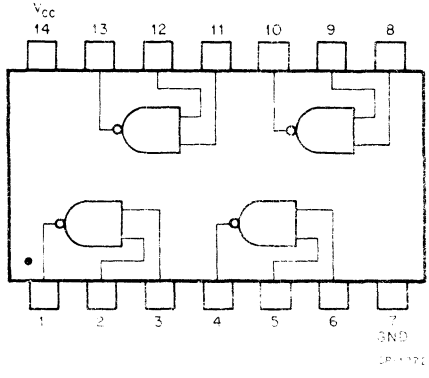


Figure 5-4 8881 Quad 2-Input NAND Gate (Bus Driver)

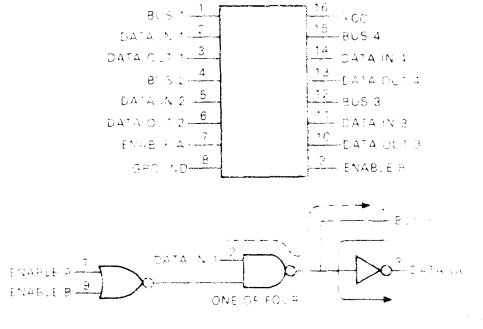


Figure 5-5 8641 Quad Unified Bus Transceiver (Bus Receiver/Driver)

Table 5-1 LSI-11 Bus Driver, Receiver, Transceiver Characteristics

Device	Characteristic	Sym	Specifications	Notes
Receiver	Input high voltage	V_{IH}	1.7 V min	1
(8640)	Input low voltage	V_{IL}	1.3 V max	1
(8641)	Input current at 3.8 V	I_{IH}	80 μA max	1, 3
	Input current at 0 V	I_{IL}	10 μA max	1, 3
	Output high voltage	V_{OH}	2.4 V min	2
	Output high current	V_{OH}	(16 TTL loads)	2, 3
	Output low voltage	V_{OL}	0.4 V max	2
	Output low current	I_{OL}	(16 TTL loads)	2, 3
	Propagation delay to high state	TPDH	10 ns min 35 ns max	4, 5
	Propagation delay to low state	TPDL	10 ns min 35 ns max	1, 5
Driver	Input high voltage	V_{IH}	2.0 V min	
(8881)	Input low voltage	V_{IL}	0.8 V max	
(8641)	Input high current	I_{IH}	60 μA max	6
	Input low current	I_{IL}	–2.0 mA max	6
	Output low voltage 70 mA sink	V_{OL}	0.8 V max	1
	Output high leakage current at 3.5 V	I_{OH}	25 μA max	1, 3
	Propagation delay to low state	TPDL	25 ns max	1, 5
	Propagation delay to high state	TPDH	35 ns max	1, 5

NOTES

1. This is a critical parameter for use on the I/O bus. All other parameters are shown for reference only.
2. This is equivalent to being capable of driving 16 unit loads of standard 7400 series TTL integrated circuits.
3. Current flow is defined as positive if into the terminal.
4. Conditions of load are 390 Ω to +5 V and 1.6 kΩ in parallel with 15 pF to ground for 10 ns min and 50 pF for 35 ns max.
5. Times are measured from 1.5 V level on input to 1.5 V level on output.
6. This is equivalent to 1.25 standard TTL unit loading of input.

Bus receivers and drivers should be well grounded and use V_{CC} to ground bypass capacitors. These gates should be located as close as practical to the module fingers which plug into the backplane and all etch runs to the bus should be kept as short as possible. Attention to these cautions should yield a module design with minimum bus loading (capacitance).

5.1.2 DC003 Interrupt Logic

The interrupt chip is an 18-pin, 0.762 cm center X 2.349 cm long (max) (0.3 in center X 0.925 in long) dual-in-line-package (DIP) device that provides the circuits to perform an interrupt transaction in a computer system that uses a daisy-chain type of arbitration scheme. The device is used in peripheral interfaces to provide two interrupt channels labeled "A" and "B," with the A section at a higher priority than the B section. Bus signals use high-impedance input circuits or high-current open collector outputs, which allow the device to directly attach to the computer system bus. Maximum current required from the V_{CC} supply is 140 mA.

Figure 5-6 is a simplified logic diagram of the DC003 IC. Figure 5-7 shows the timing for the "A" interrupt section, while Figure 5-8 shows the timing for both "A" and "B" interrupt sections. Table 5-2 describes the signals and pins of the DC003 by pin and signal name.

5.1.3 DC004 Protocol Logic

The protocol chip is in a 20-pin, 0.762 cm center X 2.74 cm long (0.3 in center X 1.08 in long) DIP device that functions as a register selector, providing the signals to control data flow into and out of up to four word registers (eight bytes). Bus signals can directly attach to the device because receivers and drivers are provided on the chip. An RC delay circuit is provided to slow the response of the peripheral interface to data transfer requests. The circuit is designed such that if tight tolerance is not required, then only an external 1K ± 20 percent resistor is necessary. External RCs can be added to vary the delay. Maximum current required from the V_{CC} supply is 120 mA.

Figure 5-9 is a simplified logic diagram of the DC004 IC. Signal timing with respect to different loads is shown in Table 5-3 and in Figure 5-10. Figure 5-11 shows the loading for the test conditions in Table 5-3. Signal and pin definitions for the DC004 are presented in Table 5-4.

5.1.4 DC005 Transceiver Logic

The 4-bit transceiver is a 20-pin, 0.762 cm center X 2.74 cm long (0.3 in center X 1.08 in long) DIP, low-power Schottky device; its primary use is in peripheral device interfaces to function as a bidirectional buffer between a data bus and peripheral device logic bus. It also includes a comparison circuit for device address selection and a constant generator for interrupt vector address generation. The bus I/O port provides high-impedance inputs and high-drive (70 mA) open collector outputs to allow direct connection to a computer data bus structure. On the peripheral device side, a bidirectional port is also provided, with standard TTL inputs and 20 mA, tri-state drivers. Data on this port is the logical inversion of the data on the bus side.

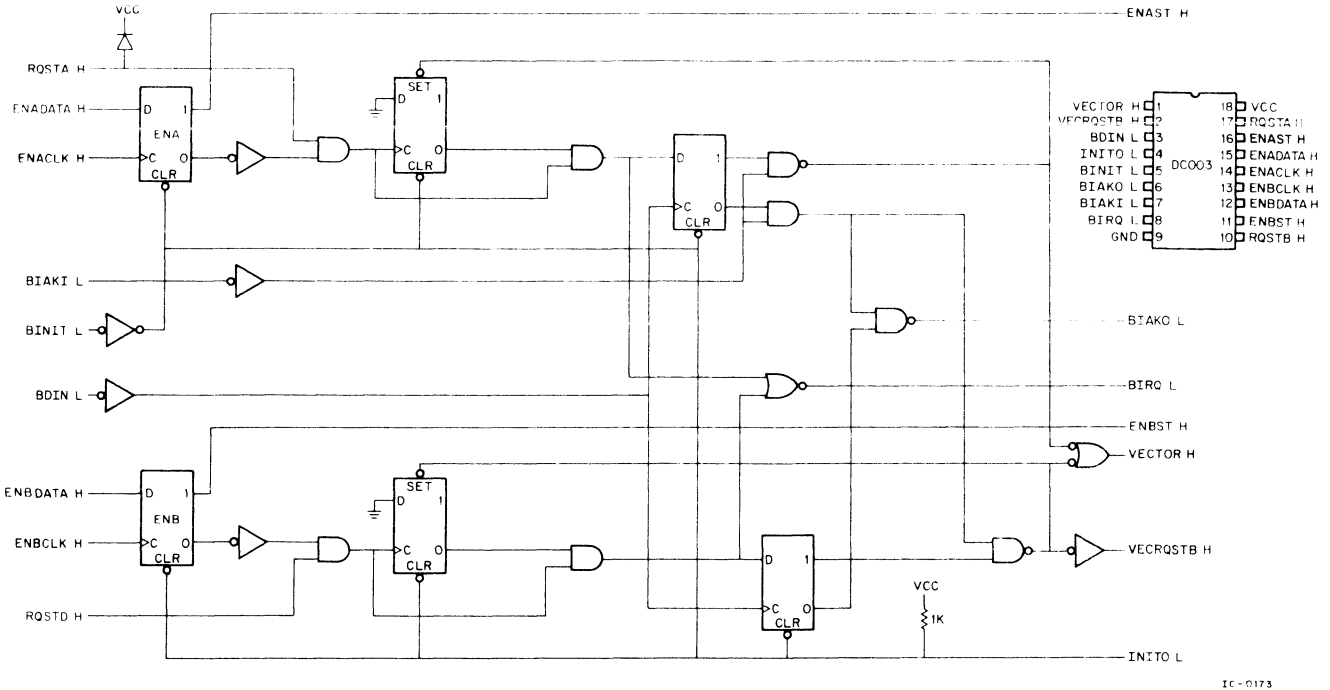


Figure 5-6 DC003 Simplified Logic Diagram

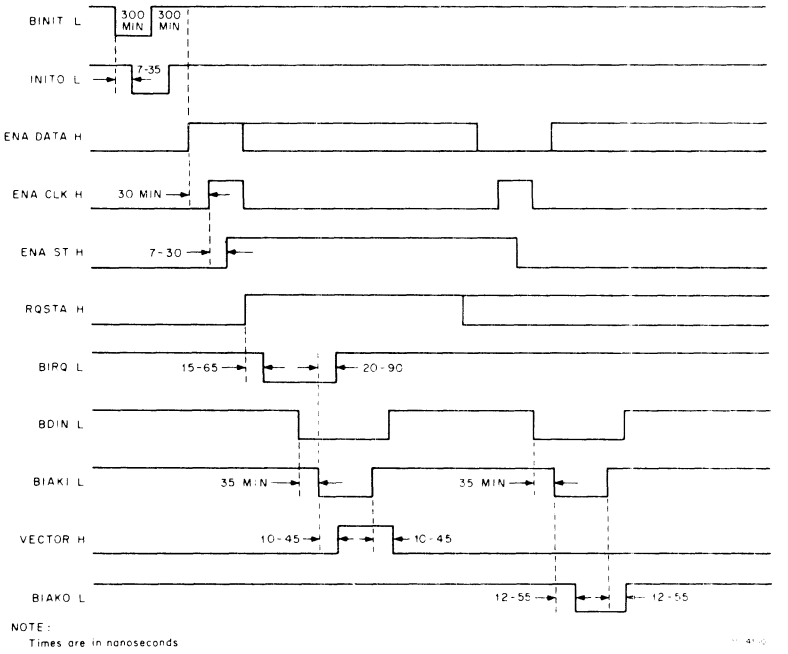


Figure 5-7 DC003 "A" Interrupt Section Timing Diagram

Table 5-2 DC003 Pin/Signal Descriptions

Pin	Signal	Description
1	VECTOR H	Interrupt Vector Gating. This signal should be used to gate the appropriate vector address onto the bus and to form the bus signal called BRPLY L.
2	VEC RQSTB H	Vector Request "B." When asserted, indicates RQST "B" service vector address is required. When unasserted, indicates RQST "A" service vector address is required. VECTOR H is the gating signal for the entire vector address; VEC RQST B H is normally bit 2 of the vector address.
3	BDIN L	Bus Data In. This signal, generated by the processor BDIN, always precedes a BIAK signal.

Table 5-2 DC003 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
4	INITO L	Initialize Out. This is the buffered BINIT L signal used in the device interface for general initialization.
5	BINIT L	Bus Initialize. When asserted, this signal brings all driven lines to their unasserted state (except INITO L).
6	BIAKO L	Bus Interrupt Acknowledge (Out). This signal is the daisy-chained signal that is passed by all devices not requesting interrupt service (see BIAKI L). Once passed by a device, it must remain passed until a new BIAKI L is generated.
7	BIAKI L	Bus Interrupt Acknowledge (In). This signal is the processor's response to BIRQ L true. This signal is daisy-chained such that the first requesting device blocks the signal propagation while non-requesting devices pass the signal on as BIAKO L to the next device in the chain. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device.
8	BIRQ L	Asynchronous Bus Interrupt Request. This signal is from a device needing interrupt service. The request is generated by a false to true transition of the RQST signal along with the associated true interrupt enable signal. The request is removed after the acceptance of the BDIN L signal and on the leading edge of the BIAKI L signal or the removal of the associated interrupt enable or the removal of the associated request signal.
10 17	REQSTB H REQSTA H	Device Interrupt Request. When asserted with the enable "A" flip-flop asserted, will cause the assertion of BIRQ L on the bus. This signal line normally remains asserted until the request is serviced.
11 16	ENB ST H ENA ST H	Interrupt Enable "A" Status. This signal indicates the state of the interrupt enable "A" internal flip-flop which is controlled by the signal line ENA DATA H and the ENA CLK H clock line.

Table 5-2 DC003 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
12 15	ENB DATA H ENA DATA H	Interrupt Enable "A" Data. The level on this line, in conjunction with the ENA CLK H signal, determines the state of the internal interrupt enable "A" flip-flop. The output of this flip-flop is monitored by the ENA ST H signal.
13 14	ENB CLK H ENA CLK H	Interrupt Enable "A" Clock. When asserted (on the positive edge), interrupt enable "A" flip-flop assumes the state of the ENA DATA H signal line.

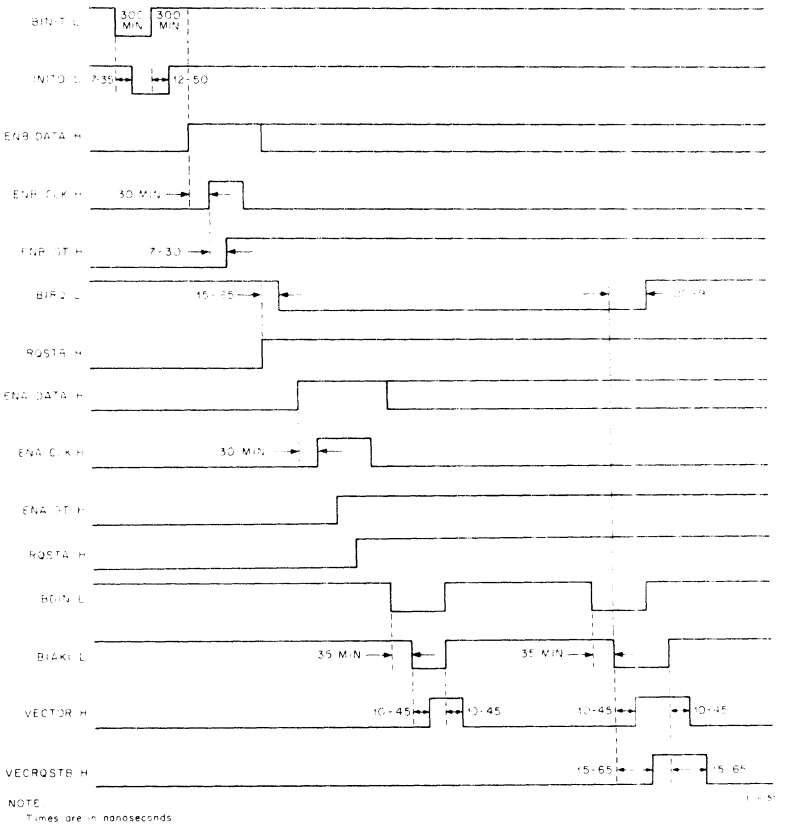


Figure 5-8 DC003 "A" and "B" Interrupt Sections Timing Diagrams

Table 5-3 DC004 Signal Timing vs Output Loading

	Signal	With Respect to	Signal	Output Being Asserted (ns) Min	Max	Output Being Negated (ns) Min	Max	Fig. 5-10 Reference
	SEL (0,2,4,6) L (Load B)		BSYNC L (Load B)	15	40	5	30	T5, T6
	OUTLB L (Load B)		BDOUT L (Load B)	5	30	5	30	T9, T10
	OUTHB L (Load B)		DBOUT L (Load B)	5	30	5	20	T9, T10
	INWD L (Load A)		BDIN L (Load B)	5	30	5	30	T11, T12
Pin 18 Connection RX = 1K ± 5% 330 Ω ± 5% 15 pF ± 5%	BRPLY L (Load A)		OUTLB L (Load B)	20	60	-10	45	T13, T14
	BRPLY L (Load A)		OUTHB L (Load B)	20	60	-10	45	T13, T14
	BRPLY L (Load A)		INWD L (Load B)	20	60	-10	45	T13, T14
	BRPLY L (Load A)		VECTOR H	30	70	0	45	T13, T14

Table 5-3 DC004 Signal Timing vs Output Loading (Cont)

	Signal	With Respect to	Signal	Output Being Asserted (ns) Min	Max	Output Being Negated (ns) Min	Max	Fig. 5-10 Reference
Pin 18 Connection RX = 4.64K ± 1%	BRPLY L (Load A)		OUTLB L (Load B)	300	400	-10	45	T13, T14
	BRPLY L (Load A)		OUTHB L (Load B)	300	400	-10	45	T13, T14
CX = 220 pF ± 1%	BRPLY L (Load A)		INWD L (Load B)	300	400	-10	45	T13, T14
	BRPLY L (Load A)		VECTOR H	330	430	0	45	T13, T14
Pin 18 Connection RX = 330 Ω ± 5% C = 15 pF ± 5%	RXCX H		OUTLB L	10	50	10	50	T15, T16
	RXCX H		OUTHB L	10	50	10	50	T15, T16
	RXCX H		INWD L	10	50	10	50	T15, T16
	RXCX H		VECTOR H	10	50	10	50	T15, T16

Table 5-4 DC004 Pin/Signal Descriptions

Pin	Signal	Description
1	VECTOR H	Vector. This input causes BRPLY L to be generated through the delay circuit. Independent of BSYNC L and ENB H.
2 3 4	BDAL2 L BDAL1 L BDAL0 L	Bus Data Address Lines. These signals are latched at the assert edge of BSYNC L. Lines 2 and 1 are decoded for the select outputs; line 0 is used for byte selection.
5	BWTBT L	Bus Write/Byte. While the BDOUT L input is asserted, this signal indicates a byte or word operation: Asserted = byte, unasserted = word. Decoded with BDOUT L and latched BDAL0 L to form OUTLB L and OUTHB L.
6	BSYNC L	Bus Synchronize. At the assert edge of this signal, address information is trapped in four latches. While unasserted, disables all outputs except the vector term of BRPLY L.
7	BDIN L	Bus Data In. This is a strobing signal to effect a data input transaction. Generates INWD L and BRPLY L through the delay circuit and INWD L.
8	BRPLY L	Bus Reply. This signal is generated through an RC delay by VECTOR H, and strobed by BDIN L or BDOUT L, and BSYNC L and latched ENB H.
9	BDOUT L	Bus Data Out. This is a strobing signal to effect a data output transaction. Decoded with BWTBT L and BDAL0 to form OUTLB L and OUTHB L. Generates BRPLY L through the delay circuit.
11	INWD L	In Word. Used to gate (read) data from a selected register onto the data bus. Enabled by BSYNC L and strobed by BDIN L.
12 13	OUTLB L OUTHB L	Out Low Byte, Out High Byte. Used to load (write) data into the lower, higher, or both bytes of a selected register. Enabled by BSYNC L and decode of BWTBT L and latched BDAL0 L, and strobed by BDOUT L.

Table 5-4 DC004 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
14 15 16 17	SEL0 L SEL2 L SEL4 L SEL6 L	Select Lines. One of these four signals is true as a function of BDAL2 L and BDAL1 L if ENB H is asserted at the assert edge of BSYNC L. They indicate that a word register has been selected for a data transaction. These signals never become asserted except at the assertion of BSYNC L (then only if ENB H is asserted at that time) and once asserted, are not unasserted until BSYNC L becomes unasserted.
18	RXCX	External Resistor Capacitor Node. This node is provided to vary the delay between the BDIN L, BDOUT L, and VECTOR H inputs and BRPLY L output. The external resistor should be tied to V_{CC} and the capacitor to ground. As an output, it is the logical inversion of BRPLY L.
19	ENB H	Enable. This signal is latched at the asserted edge of BSYNC L and is used to enable the select outputs and the address term of BRPLY L.

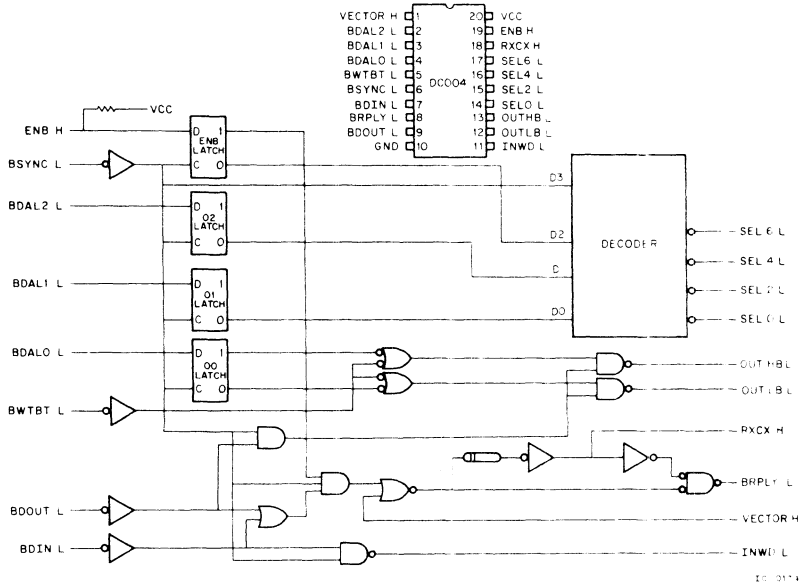


Figure 5-9 DC004 Simplified Logic Diagram

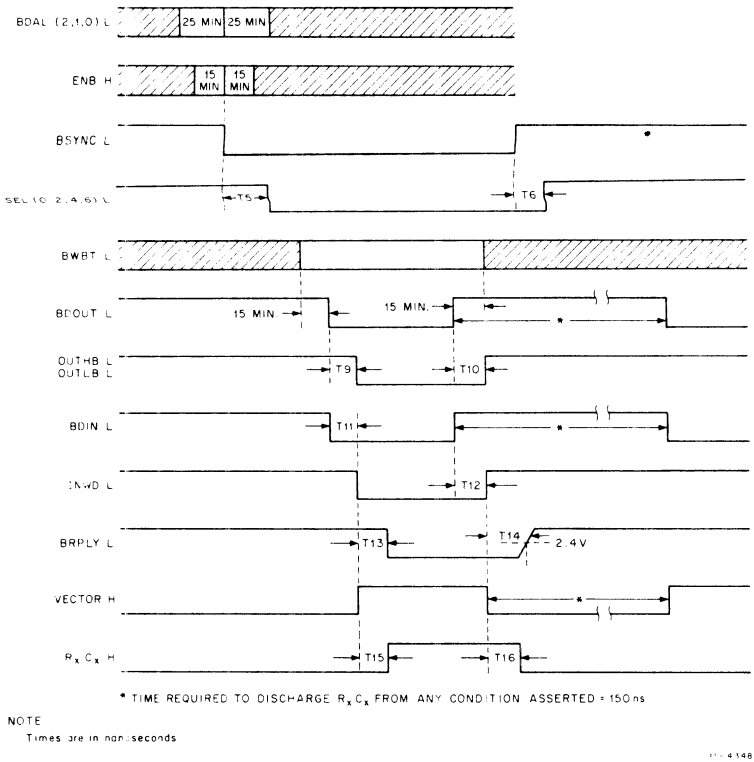


Figure 5-10 DC004 Timing Diagram

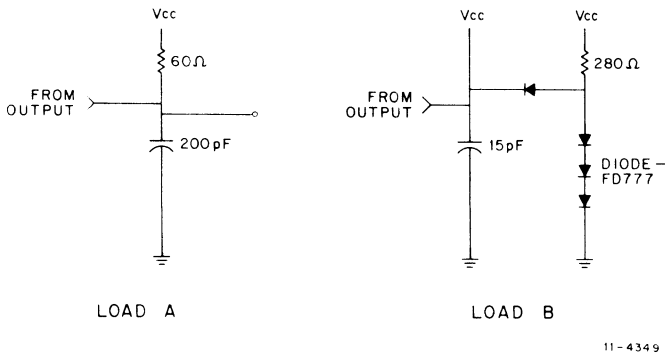


Figure 5-11 DC004 Loading Configurations for Table 5-3

Three address "jumper" inputs are used to compare against three bus inputs to generate the signal MATCH. The MATCH output is open collector, which allows the output of several transceivers to be wire-ANDed to form a composite address match signal. The address jumpers can also be put into a third logical state that disables jumpers for "don't care" address bits. In addition to the three address jumper inputs, a fourth high-impedance input line is used to enable/disable the MATCH output.

Three vector jumper inputs are used to generate a constant that can be passed to the computer bus. The three inputs directly drive three of the bus lines, overriding the action of the control lines.

Two control signals are decoded to give three optional states: receive data, transmit data, and disable.

Maximum current required from the V_{CC} supply is 120 mA.

Figure 5-12 is a simplified logic diagram of the DC005 IC. Timing for the various functions is shown in Figure 5-13. Signal and pin definitions for the DC005 are presented in Table 5-5.

Table 5-5 DC005 Pin/Signal Descriptions

Pin	Signal	Description
	JV(3:1) H	Vector Jumpers. These inputs, with internal pull-down resistors, directly drive BUS (3:1). A low or open on the jumper pin will cause an open condition on the corresponding bus pin if XMIT H is low. A high will cause a one (low) to be transmitted on the bus pin. Note that BUS0 L is not controlled by any jumper input.
14	JV1	
15	JV2	
16	JV3	
13	MENB L	Match Enable. A low on this line will enable the Match output. A high will force Match low, overriding the match circuit.
3	MATCH H	Address Match. When BUS (3:1) match with the state of JA (3:1) and MENB L is low, this output is open; otherwise it is low.

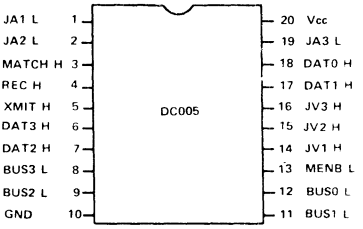
Table 5-5 DC005 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
	JA(3:1) L	Address Jumpers. A strap to ground on these inputs will allow a match to occur with a one (low) on the corresponding BUS line; an open will allow a match with a zero (high); a strap to V_{CC} will disconnect the corresponding address bit from the comparison.
1	JA1 L	
2	JA2 L	
19	JA3 L	
5	XMIT H	Control Inputs. These lines control the operation of the transceiver as follows.
4	REC H	

REC	XMIT	
0	0	DISABLE: BUS, DAT open
0	1	XMIT DATA: DAT → BUS
1	0	RECEIVE: BUS → DAT
1	1	RECEIVE: BUS → DAT

To avoid tri-state signal overlap conditions, an internal circuit delays the change of modes between XMIT DATA and RECEIVE mode and delays tri-state drivers on the DAT lines from enabling. This action is independent of the DISABLE mode.

	BUS(3:0) L	Bus Data. This set of four lines constitutes the bus side of the transceiver. Open collector outputs; high impedance inputs. Low = 1.
12	BUS0	
11	BUS1	
9	BUS2	
8	BUS3	
	DAT(3:0) H	Peripheral Device Data. These four tri-state lines carry the inverted received data from BUS (3:0) when the transceiver is in the receive mode. When in transmit data mode, the data carried on these lines is passed inverted to BUS (3:0). When in the disabled mode, these lines go open (HI-Z). High = 1.
18	DAT0	
17	DAT1	
7	DAT2	
6	DAT3	



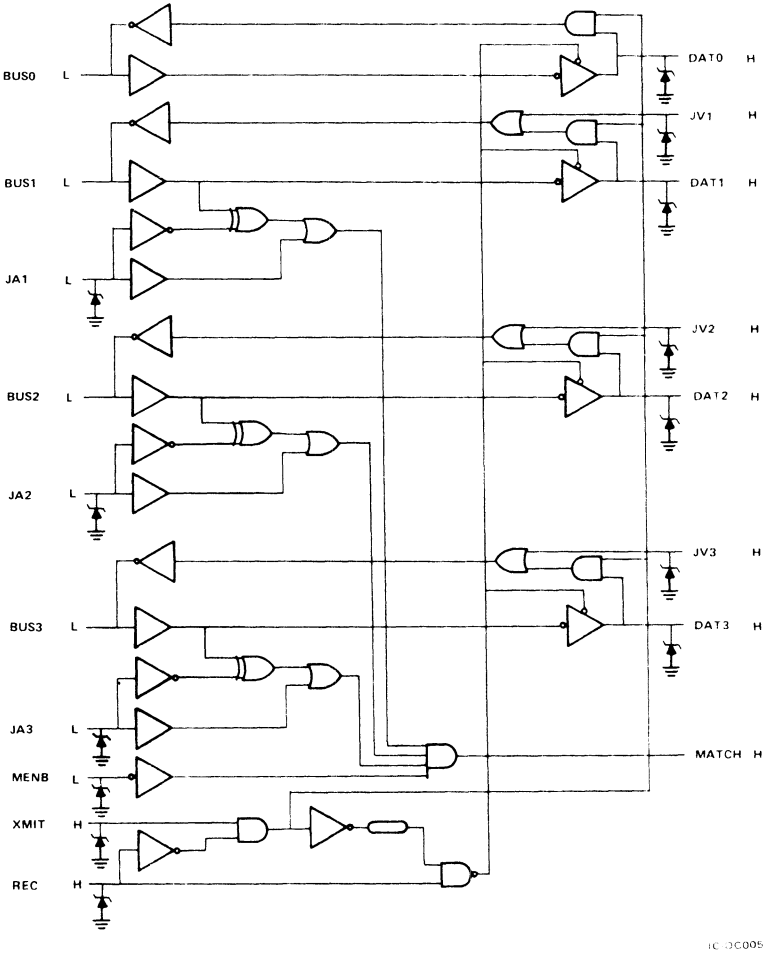


Figure 5-12 DC005 Simplied Logic Diagram

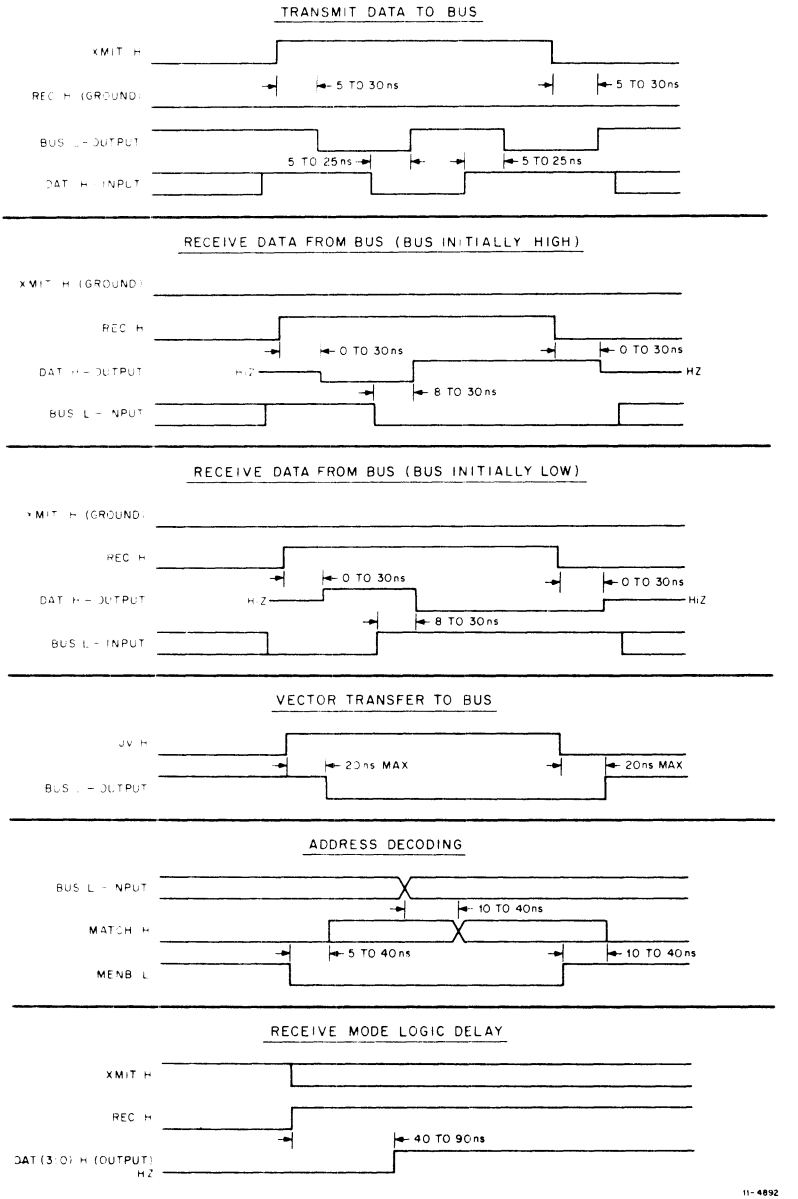


Figure 5-13 DC005 Timing Diagram

5.1.5 DC006 Word Count/Bus Address Logic

The word count/bus address (WC/BA) chip is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in center × 1.08 in long) DIP, low-power Schottky device. Its primary use is in DMA peripheral device interfaces. This IC is designed to connect to the tri-state side of the DC005 transceiver. The DC006 has two 8-bit binary up-counters, one for the word (byte) count and another for bus address. Two DC006 ICs may be cascaded to increase register implementation.

The chip is controlled by the address latch protocol chip (DC004), the DMA chip (DC010), and a minimum of ancillary logic. Both counters may be cleared simultaneously. Each counter is separately loaded by LD and the corresponding select line from the protocol chip. Each counter is incremented separately. The WC counter (word byte count) is always incremented by one; the A counter (bus address) may be incremented by one or two for byte or word addressing, respectively.

Data from the DC006 IC is placed on the tri-state bus via internal tri-state drivers. Each counter is separately read by RD and the corresponding select line.

Figure 5-14 is a block diagram of the DC006 IC while Figure 5-15 illustrates a simplified logic diagram. Figures 5-16 and 5-17 illustrate input and output voltage waveforms. Figure 5-18 shows the timing diagram of the DC006 while the setup time and pulse width switching characteristics are presented in Tables 5-6 and 5-7. The DC006 pin/signal description is presented in Table 5-8.

Table 5-6 Setup Time and Pulse Width Switching Characteristics*

Time	Description	Signal	Min
t_3	Pulse width (min)	S-C to S-A	50 ns
t_5	Setup time	D/F (7:0) to LD	10 ns
t_6	Setup time	S-C to LD	10 ns
t_7	Pulse width (min)	LD	90 ns
t_8	Setup time	S-C to RD	20 ns
t_{11}	Clock pulse width (min)	CLK-C (HI)	40 ns
t_{14}	Setup time	S-C to S-A	20 ns
t_{15}	Setup time	S-A to RD	10 ns
t_{16}	Clock pulse width (min)	CLK-A (HI)	40 ns
t_{18}	Setup time	CNT1A to CLK-A	45 ns
t_{21}	Setup time	RD to RD-A	15 ns
t_{24}	Clock off time (min)	CLK-A, CLK-C	40 ns
t_{25}	Data hold time	LD to DATA IN	20 ns

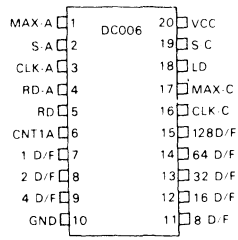
*V_{CC} = 5.0 ± 0.25 V.

TRUTH TABLES

WHERE L = TTL LOW
H = TTL HIGH
X = DON'T CARE
Z = HIGH IMPEDANCE
↓ = HIGH TO LOW TRANSITION

READ CONTROL

INPUTS				OUTPUTS
LD = H		S-A	S-C	D/F<7:0>
RD-A	RD			
L	L	L	L	CLEAR A&C AND READ C
L	L	L	H	A<7:0>
L	L	H	L	C<7:0>
L	L	H	H	Z
L	H	X	X	Z
H	L	L	L	CLEAR A&C AND READ A
H	L	L	H	A<7:0>
H	L	H	L	A<7:0>
H	L	H	H	A<7:0>
H	H	L	L	CLEAR A&C AND READ A
H	H	L	H	A<7:0>
H	H	H	L	A<7:0>
H	H	H	H	A<7:0>



WRITE CONTROL

INPUTS			FUNCTION
RD-A = L, RD = H	S-A	S-C	
LD			
↓	L	L	*ILLEGAL
↓	L	H	LOAD A<7:0>
↓	H	L	LOAD C<7:0>
X	H	H	WC/BA NOT SELECTED
H	L	L	CLEAR BOTH COUNTERS
H	L	H	LOADING DISABLED
H	H	L	LOADING DISABLED

*ILLEGAL CONDITION BECAUSE A LOAD OPERATION AND A CLEAR OPERATION IS ATTEMPTED SIMULTANEOUSLY

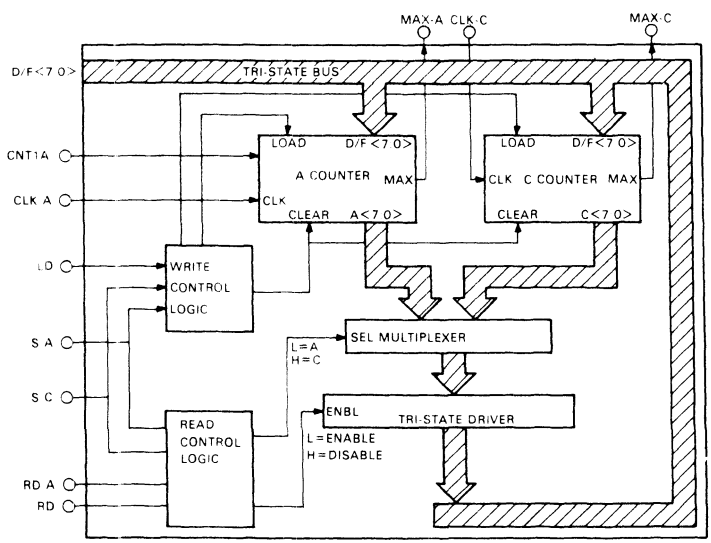


Figure 5-14 DC006 Truth Table, Logic Diagram, and Simplified Block Diagram

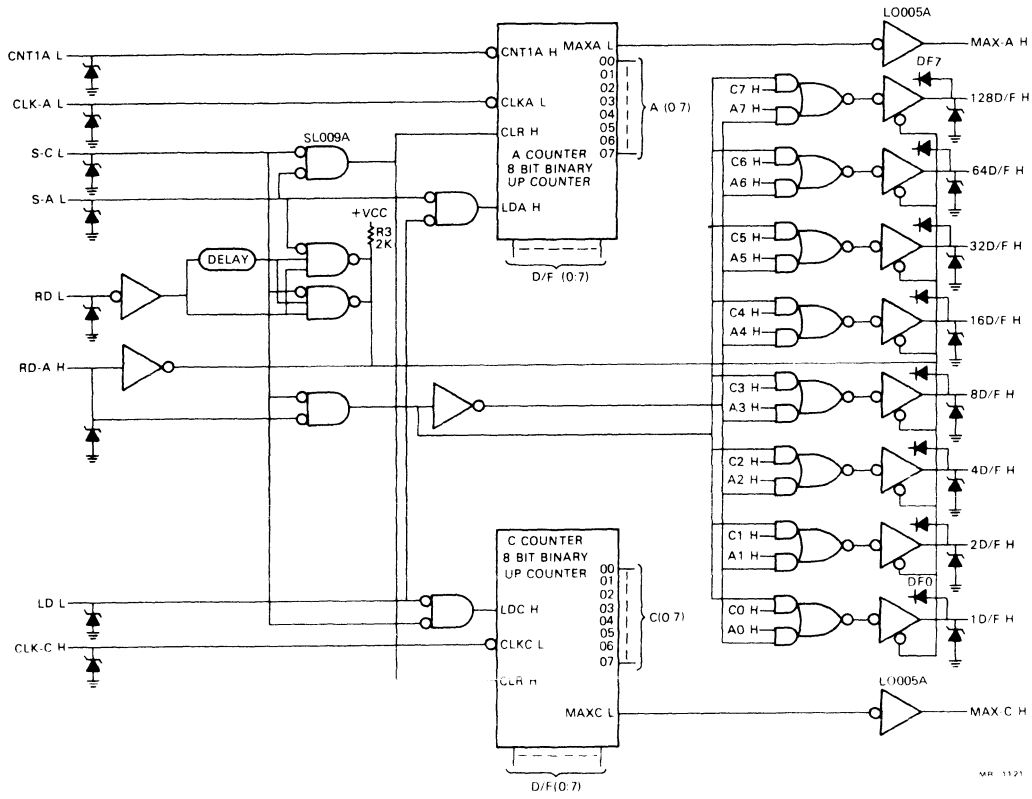


Figure 5-15 DC006 Simplified Logic Diagram

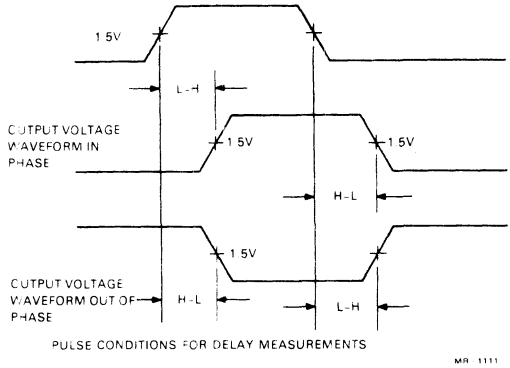
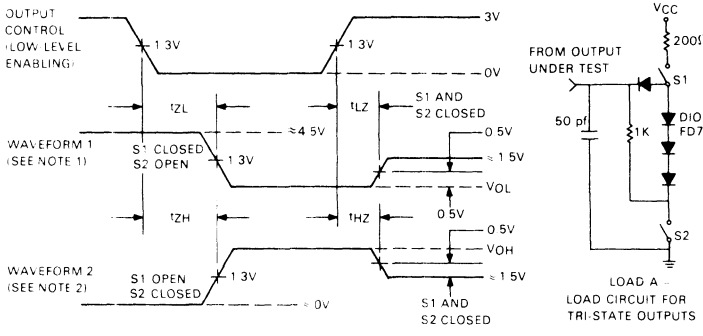


Figure 5-16 Input Voltage Waveform



NOTES

1. WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL

2. WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL

Figure 5-17 Outputs Voltage Waveforms (Tri-State)

Table 5-7 Switching Characteristics*

Time	Input Signal Name	Input Signal Polarity	Output Signal Name	Output Signal Polarity	Test Conditions	Propagation Delay (ns) Min	Propagation Delay (ns) Max
t_1	S-C S-A	H-L H-L	D/F (7:0)	X-L	Load A RD-A=4 V (C Counter)	15	80
t_2	S-C S-A	H-L H-L	D/F (7:0)	X-L	Load A RD-A=4 V (A Counter)	15	80
t_4	RD	L-H	D/F (7:0)	D/F (7:0)-Z	Load A	10	30
t_9	RD	H-L	D/F (7:0)	Z-D/F (7:0)	Load A	34	80
t_{10}	CLK-C	H-L	D/F 1	L-H	Load A	18	55
t_{12}, t_{19}	CLK-C CLK-A	L-H	MAX-C MAX-A	L-H	Load B	10	30

* Loads are presented in Figure 5-10.

Table 5-7 Switching Characteristics* (Cont)

Time	Input Signal Name	Input Signal Polarity	Output Signal Name	Output Signal Polarity	Test Conditions	Propagation Delay (ns) Min	Max
t_{13}	CLK-C	H-L	MAX-C	H-L	Load B	10	30
t_{17}	CLK-A	H-L	D/F 2	L-H	Load A	18	55
t_{20}	CLK-A	H-L	MAX-A	H-L	Load B	10	30
t_{22}	RD-A	L-H	D/F (7:0)	Z-L	Load A	10	30
				Z-H	Load A	10	30
t_{23}	RD-A	H-L	D/F (7:0)	L-Z	Load A	8	25
				H-Z	Load A	8	25

*Loads are presented in Figure 5-10.

Table 5-8 DC006 Pin/Signal Descriptions

Pin	Signal	Description
6	CNT1A	Count A Counter by 1 (TTL Input). This signal controls the least significant bit of the A counter. When CNT1A is low, the A counter increments by one. When high, the LSB is prevented from toggling, hence the counter increments by two. When two counters are cascaded, CNT1A on the high-order counter should be grounded.
3	CLK-A	Clock A Counter (TTL Input). This clock signal increments the A counter on its negative edge. The counter is incremented by one or two, depending on CNT1A. CNT1A and LD must be stable while CLK-A is high.
16	CLK-C	Clock C Counter (TTL Input). This clock signal increments the C counter by one on its negative edge. LD must be stable while CLK-C is high.
2	S-A	Select A Counter (TTL Input). This signal allows the selection of the A counter according to the truth tables (Figure 5-14).
19	S-C	Select C Counter (TTL Input). This signal allows the selection of the C counter according to the truth tables (Figure 5-14).
4	RD-A	Read A Counter (TTL Input). This signal allows the selection of the A counter according to the truth tables (Figure 5-14).
5	RD	Read (TTL Input). This signal allows the read operation to take place according to the truth tables (Figure 5-14).
18	LD	Load (TTL Input). When this signal goes through a high-to-low transition, the load operation is allowed to take place according to the truth tables (Figure 5-14). No data changes permitted while LD is low.

Table 5-8 DC006 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
7–9 11–15	D/F (7:0)	Data Bus (Bidirectional, Tri-State Outputs/TTL Inputs). These eight bidirectional lines are used to carry data in and out of the selected counter.
1	MAX-A	Maximum A Count (TTL Output). This signal is generated by ANDing CLK-A and the maximum count condition of counter A (count 376 when counting by 2 or count 377 when counting by 1).
17	MAX-C	Maximum C Count (TTL Output). This signal is generated by ANDing CLK-C and the maximum count conditions of counter C (count 377).

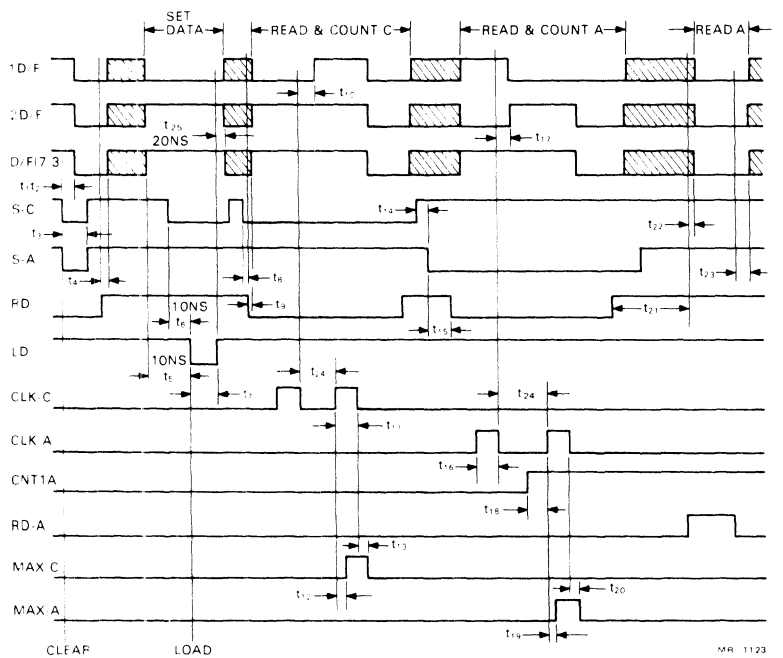


Figure 5-18 DC006 Timing Diagram

5.1.6 DC010 Direct Memory Access Logic

The direct memory access (DMA) chip is a 20-pin, 0.762 cm center × 2.74 cm long (0.3 in center × 1.08 in long) DIP, low-power Schottky device for primary use in DMA peripheral device interfaces using the LSI-11 bus.

This device provides the logic to perform the handshaking operations required to request and to gain control of the system bus. Once bus mastership has been established, the DC010 generates the required signals to perform a DIN, DOUT, or DATIO transfer as specified by control lines to the chip. The DC010 IC has a control line that will allow multiple transfers or only four transfers to take place before giving up bus mastership.

Figure 5-19 is a simplified logic diagram of the DC010 IC. The logic symbols and truth table are presented in Figure 5-20 and the DC010 voltage waveforms are shown in Figure 5-21. Table 5-9 describes the signals and pins of the DC010 by pin and signal name. Figures 5-22 through 5-25 show the timing for the DC010 while the setup time and pulse width specifications are listed in Table 5-10. The switching characteristics are presented in Table 5-11.

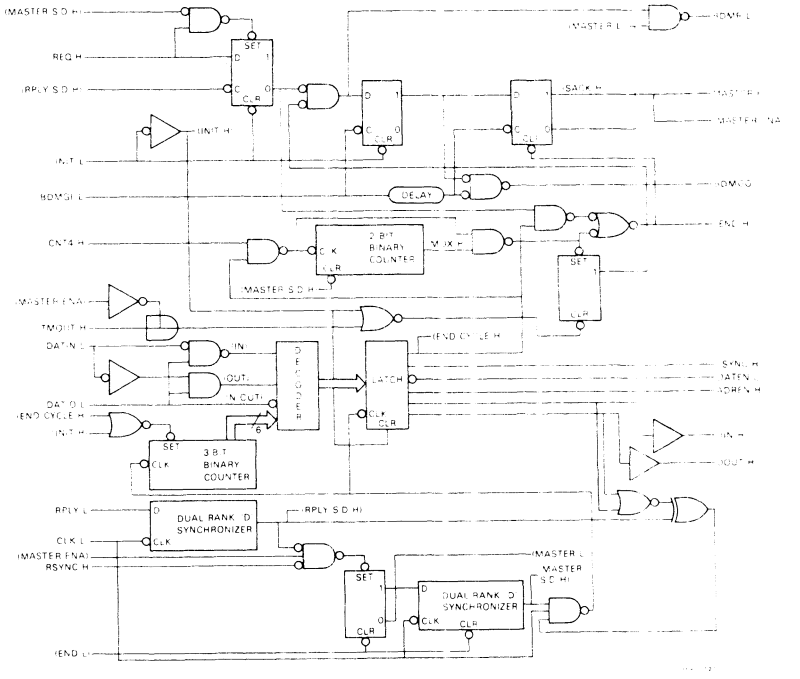


Figure 5-19 DC010 Simplified Logic Diagram

Table 5-9 DC010 Pin/Signal Descriptions

Pin	Signal	Description*
1	REQ H	Request (TTL Input). A high on this signal initiates the bus request transaction. A low allows the termination of bus mastership to take place.
13	BDMGI L	DMA Grant Input (HI-Z Input). A low on this signal allows bus mastership to be established if a bus request was pending (REQ = high); otherwise, this signal is delayed and output as BDMGO.
16	CNT 4 H	Count Four (TTL Output). A high on this signal allows a maximum of four transfers to take place before giving up bus mastership. A low disables this feature and an unlimited transfer will take place as long as REQ is high. If left open, this pin will assume a high state.
14	TMOUT H	Time-Out (TTL Input/Open Collector Output). This I/O pin is low while SACK H is high. It goes into high impedance when SACK H is low. When driven low it prevents the assertion of BDMR; when driven high it allows the assertion of BDMR to take place if BDMR has been negated due to the 4-maximum transfer condition. An RC network may be used on this pin to delay the assertion of BDMR.
3	DATIN L	Data In (TTL Input). This signal allows the selection of the type of transfers to take place according to the truth table (Figure 5-20).
2	DATIO L	Data In/Out (TTL Input). This signal allows the selection of the type of transfer to take place according to the truth table (Figure 5-20). During a DATIO transfer, this signal must be toggled in order to allow the completion of the output portion of the I/O transfer. If left open, this pin will assume a high state.

*Refer to Figures 5-22 through 5-25.

Table 5-9 DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Description*
12	RSYNC H	Receive Synchronize (TTL Input). This signal allows the device to become master according to the following relationship: RSYNC L · RPLY L · SACK H = MASTER
17	CLK L	Clock (TTL Input). This clock signal is used to generate all transfer timing sequences.
15	RPLY H	Reply (TTL Input). This signal is used to enable or disable the free clock signal according to the truth table (Figure 5-20). This signal also allows the device to become master according to the following relationship: RSYNC L · RPLY L · SACK H = MASTER
19	INIT L	Initialize (TTL Input). This signal is used to initialize the chip to the state where REQ is needed to start a bus request transaction. When INIT is low, the following signals are negated: BDMRL, MASTER H, DATENL, ADRENL, SYNCH, DINH, DOUTH.
11	BDMR L	DMA Request (Open Collector Output). A low on this signal indicates that the device is requesting bus mastership. This output may be tied directly to the bus.
9	MASTER H	Master (TTL Output). A high on this signal indicates that the device has bus mastership and a transfer sequence is in progress.
8	BDMGO L	DMA Grant Output (Open Collector Output). This signal is the delayed version of BDMGI if no request is pending; otherwise, it is not asserted. This output may be tied directly to the bus.

*Refer to Figures 5-22 through 5-25.

Table 5-9 DC010 Pin/Signal Descriptions (Cont)

Pin	Signal	Description*
7	TSYNC H	Transmit Synchronize (TTL Output). This signal is asserted by the device to indicate that a transfer is in progress.
18	DATEN L	Data Enable (TTL Output). This signal is asserted to indicate that data may be placed on the bus.
4	ADREN H	Address Enable (TTL Output). This signal is asserted to indicate that an address may be placed on the bus.
6	DIN H	Data In (TTL Output). This signal is asserted to indicate that the bus master device is ready to accept data.
5	DOUT H	Data Out (TTL Output). This signal is asserted to indicate that the bus master device has output valid data.

*Refer to Figures 5-22 through 5-25.

Table 5-10 Setup Time and Pulse Width Switching Characteristics*

Time	Description	Signal	Min	Max
t_1	Pulse width (min)	INIT	35 ns	
t_4	Setup time	INIT to REQ.	25 ns	
t_6	Setup time	BDMR to BDMGI	35 ns	
t_9	Setup time	BDMR to BDMGI	0 ns	
t_{12}	Pulse width (min)	CLK (low)	60 ns	
t_{13}	Pulse width (min)	CLK (high)	60 ns	
t_{14}	Setup time	REQ to CLK	35 ns	
t_{18}	Setup time	DIN to RPLY	0 ns	
t_{22}	Setup time	DATIN, DATIO to CLK	60 ns	
t_{24}	Setup time	RPLY to CLK	30 ns	
t_{28}	Setup time	RPLY to DATIO	35 ns	
t_{29}	Pulse width	DATIO	30 ns	1 clock period
t_{30}	Setup time	DATIO to CLK	65 ns	
t_{32}	Pulse width (min)	REQ	35 ns	

*V_{CC} = 5.0 ± 0.25 V

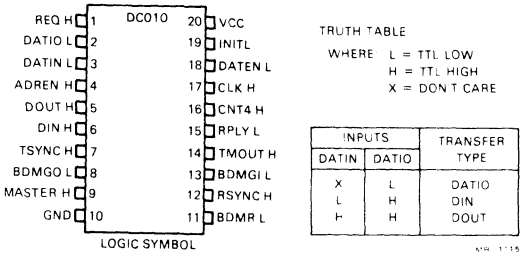


Figure 5-20 DC010 Logic Symbol/Truth Table

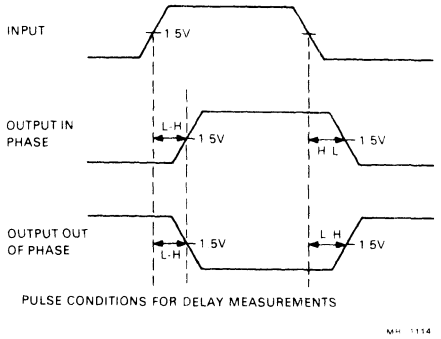


Figure 5-21 DC010 Voltage Waveforms

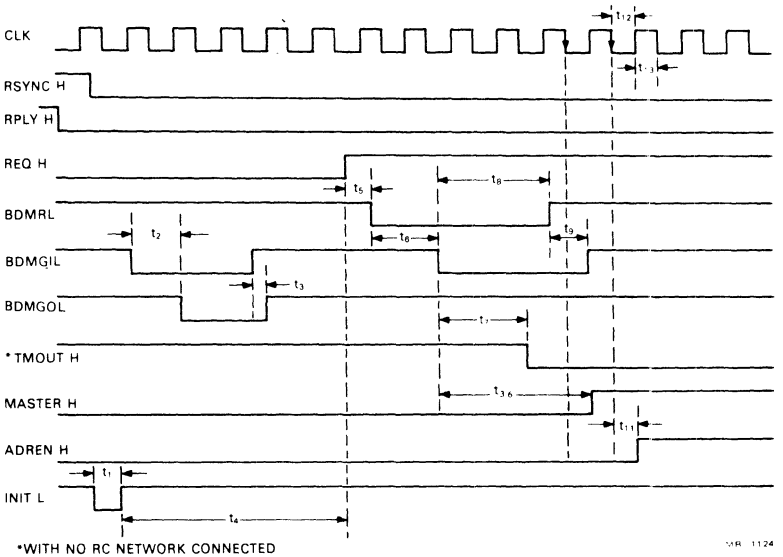


Figure 5-22 DC010 Timing Diagram, DMA Request/Grant

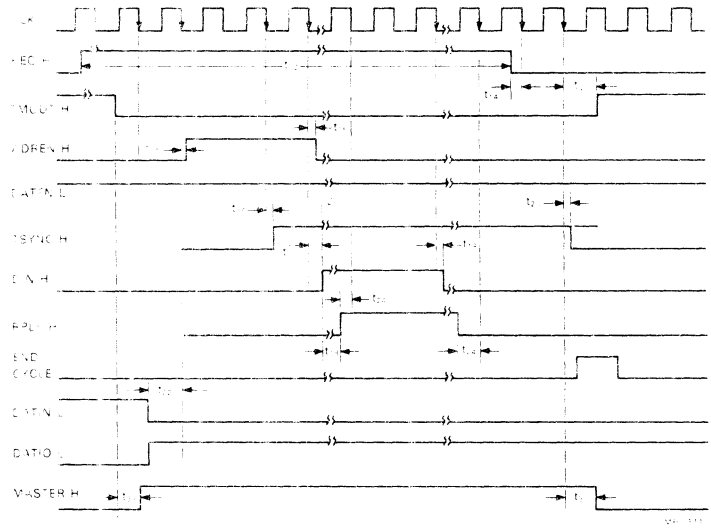


Figure 5-23 DC010 Timing Diagram (Sheet 1 of 2)

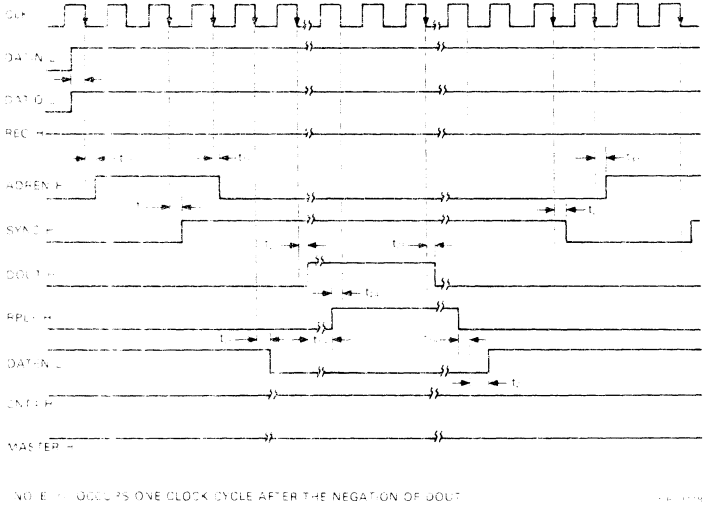


Figure 5-23 DC010 Timing Diagram (Sheet 2 of 2)

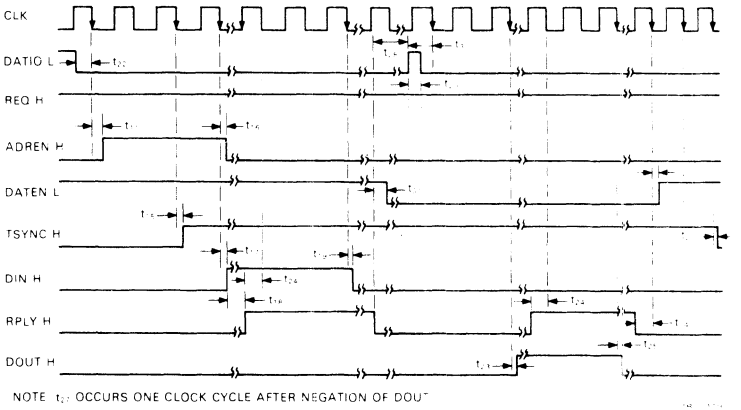


Figure 5-24 DC010 Timing Diagram (DATIO–Multiple Transfer)

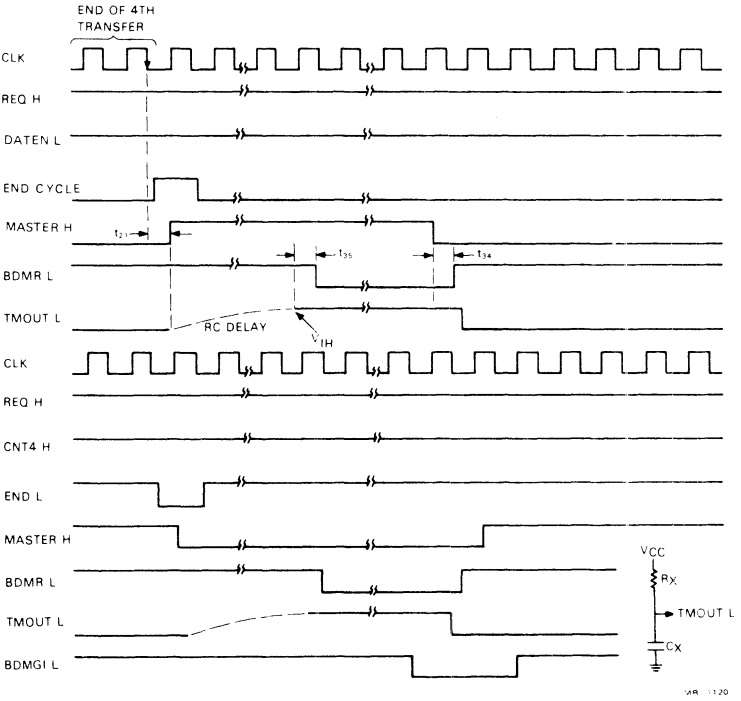


Figure 5-25 DC010 Timing Diagram (Time-Out)

Table 5-11 Switching Characteristics

Time	Input Signal Name	Input Signal Polarity	Output Signal Name	Output Signal Polarity	Test Conditions	Propagation Delay (ns) Min	Propagation Delay (ns) Max
t_2	BDMGI	H-L	BDMGO	H-L	Load A	95	220
t_3	BDMGI	L-H	BDMGO	L-H	Load A	20	60
t_5	REQ	L-H	BDMR	H-L	Load A	25	70
t_7	BDMGI	H-L	TMOUT	H-L	Load A	85	230
t_8	BDMGI	H-L	BDMR	L-H	Load A	117	306
t_{11}*	CLK	H-L	ADREN	L-H	Load B	15	60
t_{15}	CLK	H-L	SYNC	L-H	Load B	18	60†
t_{16}	CLK	H-L	ADREN	H-L	Load B	20	65†
t_{17}	CLK	H-L	DIN	L-H	Load B	18	60†
t_{19}	CLK	H-L	DIN	H-L	Load B	18	60
t_{20}	CLK	H-L	SYNC	H-L	Load B	18	60
t_{21}	CLK	H-L	TMOUT	L-H	Load B	30	90
t_{23}	CLK	H-L	DOUT	L-H	Load B	60	175
t_{25}	CLK	H-L	DOUT	H-L	Load B	20	65†
t_{26}	CLK	H-L	DATEN	H-L	Load B	20	65†

T_{11} represents the first time ADREN is asserted.
t_{33} represents the subsequent times that ADREN is asserted.

†These propagation delays meet the following requirements.

$t_{15}-t_{16} \leqslant 10$ ns
$t_{15}-t_{17} \leqslant 10$ ns
$t_{16}-t_{26} \leqslant 10$ ns
$t_{25}-t_{27} \leqslant 20$ ns
$t_{23}-t_{26} \leqslant 45$ ns
$t_8-t_{36} \geqslant 27$ ns

Table 5-11 Switching Characteristics (Cont)

Time	Input Signal Name	Input Signal Polarity	Output Signal Name	Output Signal Polarity	Test Conditions	Propagation Delay (ns) Min	Propagation Delay (ns) Max
t_{31}	RPLY	H-L	DATEN	H-L	Load B	20	65
t_{27}	CLK	H-L	DATEN	L-H	Load B	20	65†
t_{33}*	CLK	H-L	ADREN	L-H	Load B	18	60
t_{35}	TMOUT	L-H	BDMR	H-L	Load B	20	75
t_{36}	BDMGI	H-L	MASTER	L-H	Load B	90	242
t_{37}	CLK	H-L	MASTER	H-L	Load B	18	66
t_{38}	R SYNC or REPLY	H-L	MASTER	L-H	Load B	10	58

*t_{11} represents the first time ADREN is asserted.
t_{33} represents the subsequent times that ADREN is asserted.

†These propagation delays meet the following requirements.

$t_{15}-t_{19} \leqslant 10$ ns
$t_{15}-t_{17} \leqslant 10$ ns
$t_{16}-t_{24} \leqslant 10$ ns
$t_{25}-t_{27} \leqslant 20$ ns
$t_{23}-t_{26} \leqslant 45$ ns
$t_{8}-t_{35} \geqslant 27$ ns

5.1.7 Specifications

DC003 Electrical Characteristics

DC003 TTL (Non-Bus) Interface
(Specification Group I – TTL Input and Output Pins)
(Pins 1, 2, 4, 11, 12, 13, 14, 15, 16)

Parameter			Requirements		
Name	Symbol	Conditions[1]	Min	Max	Unit
High-level input voltage	V_{IH}		2.0		V
Low-level input voltage	V_{IL}			0.8	V
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = −18 mA		−1.2	V
High-level output voltage	V_{OH}	V_{CC} = 4.75 V I_O = −1 mA	2.7		V
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_O = 20 mA		0.5	V
Input current at maximum input voltage	I_I	V_{CC} = 5.25 V V_I = 5.5 V		1	mA
High-level input current	I_{IH}	V_{CC} = 5.25 V V_I = 2.7 V[2]		50	μA
Low-level input current	I_{IL}	V_{CC} = 5.25 V V_I = 0.5 V[3]		−0.55	mA
Short-circuit output current	I_{OS}	V_{CC} = 5.25 V[4,5]	−40	−100	mA
Supply current	I_{CC}	V_{CC} = 5.25 V		140	mA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

[2]I_{IH} = 100 μA at pins 12 and 15.

[3]I_{IL} = −2.0 mA at pins 12 and 15.

[4]Not more than one output shall be shorted at a time and duration shall not exceed 1 second.

[5]Does not apply to pin 4.

DC003 Bus Driver
(Specification Group II – Open Collector)
(Pins 6 and 8)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
Output reverse current	I_{OR}	V_{CC} = 4.75 V V_{OH} = 3.5 V		25	μA
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_{SINK} = 70 mA I_{SINK} = 16 mA		0.8 0.5	V V

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC003 Bus Receiver
(Specification Group III – High Input Z)
(Pins 3, 5, 7, 10, 17)

Parameters			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}	V_{CC} = 4.75 V V_{CC} = 5.25 V	1.53 1.70		V V
Low-level input voltage	V_{IL}	V_{CC} = 4.75 V V_{CC} = 5.25 V		1.30 1.47	V V
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = −18 mA I_I = +18 mA (pins 10 and 17 only)		−1.2 6.25	V V
High-level input current	I_{IH}	V_I = 3.8 V V_{CC} = 0 V (Do not do for pins 10 and 17) V_{CC} = 5.25 V		40 40	μA μA
Low-level input current	I_{IL}	V_I = 0 V V_{CC} = 0 V (Do not do for pins 10 and 17) V_{CC} = 5.25 V		−10 −10	μA μA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC004 Electrical Characteristics

DC004 TTL (Non-Bus) Interface
(Specification Group I – TTL Input and Output Pins)
(Pins 1, 11, 12, 13, 14, 15, 16, 17, 19)

Parameter			Requirements		
Name	Symbol	Conditions[1]	Min	Max	Unit
High-level input voltage	V_{IH}		2.0		V
Low-level input voltage	V_{IL}			0.8	V
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = −18 mA		−1.2	V
High-level output voltage	V_{OH}	V_{CC} = 4.75 V I_O = −1 mA	2.7		V
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_O = 20 mA		0.5	V
Input current at maximum input voltage	I_I	V_{CC} = 5.25 V V_I = 5.5 V[2]		1	mA
High-level input current	I_{IH}	V_{CC} = 5.25 V V_I = 2.7 V[2]		50	μA
Low-level input current	I_{IL}	V_{CC} = 5.25 V V_I = 0.5 V		−0.70	mA
Short-circuit output current	I_{OS}	V_{CC} = 5.25 V[3]	−40	−100	mA
Supply current	I_{CC}	V_{CC} = 5.25 V		120	mA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.
[2]Limits for pin 19 are:
I_I = 1.40 mA; I_{IH} = −2.25 mA min, −3.85 mA max.
I_{IL} = −4.5 mA min, −800 mA max.
[3]Not more than one output shall be shorted at a time and the duration shall not exceed 1 second.

DC004 Bus Receiver
(Specification Group II – High Input Z)
(Pins 2, 3, 4, 5, 6, 7, 9)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}	V_{CC} = 4.75 V V_{CC} = 5.25 V	1.53 1.70		V V
Low-level input voltage	V_{IL}	V_{CC} = 4.75 V V_{CC} = 5.25 V		1.30 1.47	V V
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = −18 mA		−1.2	V
High-level input current	I_{IH}	V_I = 3.8 V V_{CC} = 0 V V_{CC} = 5.25 V		 40 40	 μA μA
Low-level input current	I_{IL}	V_I = 0 V V_{CC} = 0 V V_{CC} = 5.25 V		 −10 −10	 μA μA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC004 Bus Driver
(Specification Group III – Open Collector)
(Pins 8 and 18)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
Output reverse current	I_{OH}	V_{CC} = 4.75 V V_{OH} = 3.5 V		25[2]	μA
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_{SINK} = 70 mA[3] I_{SINK} = 16 mA[3] I_{SINK} = 15 mA[4]		 0.8 0.5 0.5	 V V V

[1]Ambient operating temperature (T_A) = 0° to 70° C unless otherwise specified.

[2]65 μA for pin 18 (RXCX H).

[3]Pin 8 – Bus Reply only.

[4]Pin 18 – RXCS only.

DC005 Electrical Characteristics

DC005 TTL (Non-Bus) Interface
(Specification Group I – TTL Input and Output Pins)
(Pins 4, 5, 6, 7, 17, 18)

Parameter			Requirements		
Name	Symbol	Conditions[1]	Min	Max	Unit
High-level input voltage	V_{IH}		2		V
Low-level input voltage	V_{IL}			0.8	V
Input clamp voltage	V_I	V_{CC} = 4.75 V I_I = −18 mA		−1.2	V
High-level output voltage	V_{OH}	V_{CC} = 4.75 V I_O = −1 mA	3.65		V
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_O = 20 mA		0.5	V
Input current at maximum input voltage	I_I	V_{CC} = 5.25 V V_I = 5.5 V		1	mA
High-level input current	I_{IH}	V_{CC} = 5.25 V V_I = 2.7 V REC XMIT		 100 50	 μA μA
Low-level input current	I_{IL}	V_{CC} = 5.25 V V_I = 0.5 V REC XMIT		 −2.2 −1.1	 mA mA
Short-circuit output current	I_{OS}	V_{CC} = 5.25 V[2]	−40	−100	mA
Supply current	I_{CC}	V_{CC} = 5.25 V		120	mA
Off state (high-impedance state) output current (DAT pins only)	$I_{O\ (OFF)}$	V_{CC} = 5.25 V V_I = 3.65 V V_I = 0.5 V		 100 −0.36	 μA mA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.
[2]Not more than one output shall be shorted at a time and the duration shall not exceed 1 second.

DC005 Bus Receiver
(Specification Group II – High Input Z)
(Pins 8, 9, 11, 12, 13)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}	V_{CC} = 4.75 V	1.53		V
		V_{CC} = 5.25 V	1.70		V
Low-level input voltage	V_{IL}	V_{CC} = 4.75 V		1.30	V
		V_{CC} = 5.25 V		1.47	V
Input clamp voltage	V_I	I_I = −18 mA, V_{CC} = 4.75 V		−1.2	V
High-level input current (includes open-collector leakage on bus pins)	I_{IH}	V_I = 3.8 V			
MENB		V_{CC} = 0 V		40	μA
		V_{CC} = 5.25 V		40	μA
BUS		V_{CC} = 0 V		65	μA
		V_{CC} = 5.25 V		65	μA
Low-level input current	I_{IL}	V_I = 0.5 V			
		V_{CC} = 0 V		−10	μA
		V_{CC} = 5.25 V		−10	μA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC005 Bus Driver
(Specification Group III – Open Collector
(Pins 3, 8, 9, 11, 12)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level output current (reverse current – match output only[2]	I_{OH}	V_{CC} = 4.75 V, V_{OH} = 5.25 V		25	μA
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V			
		I_{SINK} = 8 mA (Match)		0.5	V
		I_{SINK} = 70 mA (Bus)		0.8	V
		I_{SINK} = 16 mA (Bus)		0.5	V

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.
[2]For bus pins, see I_{IH} under specification group II.

DC005 (Specification Group IV – Ternary State Inputs)
(Pins 1, 2, 19)

Parameter			Requirements		
Name	Symbol	Conditions[1]	Min	Max	Unit
Low-level input voltage	V_{IL}			0.3	V
High-level input voltage	V_{IH}		4.75		V
Open circuit input voltage	V_{OP}	$4.75 < V_{CC} < 5.25$	1	2	V

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC005 (Specification Group V – TTL Input with Pull-Down)
(Pins 14, 15, 16)

Parameter			Requirements		
Name	Symbol	Conditions[1]	Min	Max	Unit
High-level input voltage	V_{IH}		2		V
Low-level input voltage	V_{IL}			0.8	V
Input clamp voltage	V_I	V_{CC} = 4.75 V −18 mA		−1.2	V
High-level input current	I_{IH}	V_{CC} = 5.25 V V_I = 2.4 V		1.2	mA
Low-level input voltage forcing input current	V_{II}	V_{CC} = 4.75 V I_I = 0.1 mA		0.8	V
Input current at low-level	I_{IL}	V_{CC} = 5 V V_I = 0.4 V	50	200	μA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.

DC006 Electrical Characteristics

DC006 TTL (Non-Bus) Interface
(Specification Group I – TTL Input and Output Pins)

Parameter			Requirements		
Name	**Symbol**	**Conditions[1]**	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}		2		V
Low-level input voltage	V_{IL}			0.8	V
Input clamp voltage	V_I	V_{CC} = Open I_I = –18 mA		–1.2	V
High-level output voltage	V_{OH}	V_{CC} = 4.75 V I_O = –1 mA	2.7		V
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_O = 20 mA		0.5	V
Input current at maximum input voltage	I_I	V_{CC} = 5.25 V V_I = 5.5 V		1	mA
High-level input current	I_{IH}	V_{CC} = 5.25 V V_I = 2.7 V			
Except tri-state				50	μA
Tri-state pin				55	μA
Low-level input current	I_{IL}	V_{CC} = 5.25 V V_I = 0.5 V			
CLKA, CLKC				–1.1	mA
CTNTIA				–1.7	mA
D/F(7:0)LD,RD, SC,SA				100	μA
RD-A				200	μA
Off-state high impedance state – output current tri-state only	$I_{O\ (OFF)}$	V_{CC} = 5.25 V V_O = 3.75 V		100	μA
Short-circuit output current	I_{OS}	V_{CC} = 5.25 V[2]	–40	–100	mA
Supply current	I_{CC}	V_{CC} = 5.25 V		150	mA

[1]Ambient operating temperature (T_A) = 0° to +70° C; V_{CC} = 5.0 ± 0.25 unless otherwise specified.
[2]Not more than one output shall be shorted at a time and the duration shall not exceed 1 second.

DC010 Electrical Characteristics

Parameter			Requirements		
Name	**Symbol**	**Conditions**[1]	**Min**	**Max**	**Unit**
High-level input voltage	V_{IH}		2.0		V
		V_{CC} = 4.75 V	1.53		V
		V_{CC} = 5.25 V	1.70		V
Low-level input voltage	V_{IL}			0.8	V
		V_{CC} = 4.75 V		1.30	V
		V_{CC} = 5.25 V		1.47	V
Input clamp voltage	V_I	V_{CC} = open I_I = −18 mA		1.2	V
High-level output voltage	V_{OH}	V_{CC} = 4.75 V I_O = 1 mA	2.7		V
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V			
		I_O = 8 mA		0.5	V
		I_O = 70 mA		0.8	V
Input current at maximum input voltage	I_I	V_{CC} = 5.25 V V_I = 5.5 V		1.0	mA
				1.5	mA
		V_{CC} = 0 to 5.25 V V_I = 3.8 V		40	μA
				65	μA
High-level input current	I_{IH}	V_{CC} = 5.25 V[3]			
		V_I = 2.7 V		50	μA
		V_I = 2.7 V[4]		300	μA
		V_I = 3.8 V		40	μA
		V_I = 3.8 V		65	μA
Low-level input current	I_{IL}	V_I = 0.5 V[3]			
		V_{CC} = 5.25 V		−1.4	mA
		V_{CC} = 5.25 V		−2.0	mA
		V_{CC} = 5.25 V		−10	μA
		V_{CC} = 5.25 V		−10	μA
Output leakage current	I_{OH}	V_{CC} = 4.75 V V_O = 5.25 V		25	μA
Short-circuit output current[2]	I_{OS}	V_{CC} = 5.25 V	15	60	mA
Supply current	I_{CC}	V_{CC} = 5.25 V	130	160	mA

[1]Ambient operating temperature (T_A) = 0° to +70° C unless otherwise specified.
[2]Not more than one output shall be shorted at a time and the duration shall not exceed 1 second.
[3]Except CNT4, DATIO.
[4]CNT4, DATIO.

5.2 TYPICAL APPLICATION

Figures 5-26, 5-29, and 5-30 show a typical application for the DC003, DC004, DC005, DC006, and DC010 integrated circuits. Figure 5-26 shows the LSI-11 bus interface circuits; Figure 5-29 depicts the DMA control, word count/bus address registers, and the output buffers; Figure 5-30 shows miscellaneous logic.

5.2.1 DC003, DC004, DC005 Application

Referring to Figure 5-26, four DC005 transceivers are used to handle the first 16 BDAL lines (BDAL 0–BDAL15) from the LSI-11 bus and to provide the interface to the internal tri-state bus. The transceivers are enabled to receive data from the LSI-11 bus when the REC H line is driven high. Similarly, the transceivers transmit data to the LSI-11 bus when the XMIT H line is driven high. Normally, the DC005s are in the receive state (REC H line asserted) and allow the transceivers to monitor the LSI-11 bus for device addresses.

Device address and vector switch inputs to the transceivers provide convenient address and vector selection.

Switches A3 through A12 are the device address selection switches, and switches V3 through V8 are for vector selection. Switches are ON (closed) for a 1 bit and are OFF (open) for a 0 bit. The switch settings for the device addresses and vector are shown in Figures 5-27 and 5-28 respectively. The addressable registers are:

Register	Bank 7 Octal Address
Bus Address Register	1XXXX0
Word Count Register	1XXXX2
Control/Status Register	1XXXX4
Output Buffers	1XXXX6

The user selects a base address for the bus address register and sets the device address selection switches to decode this address. The remaining register addresses are then properly decoded as sequential addresses beyond the bus address register.

The DC004 is the internal register selector. This integrated circuit monitors BDAL lines 0, 1, and 2 to determine which register address has been placed on the LSI-11 bus. The states of BDOUT and BDIN are also monitored to determine the type of transfer (DATO or DATI). When an address for an internal register is placed on the LSI-11 bus, one of the SEL outputs from the DC004 is driven low. This selects that particular register for the transfer of data. The direction of transfer (in to or out of

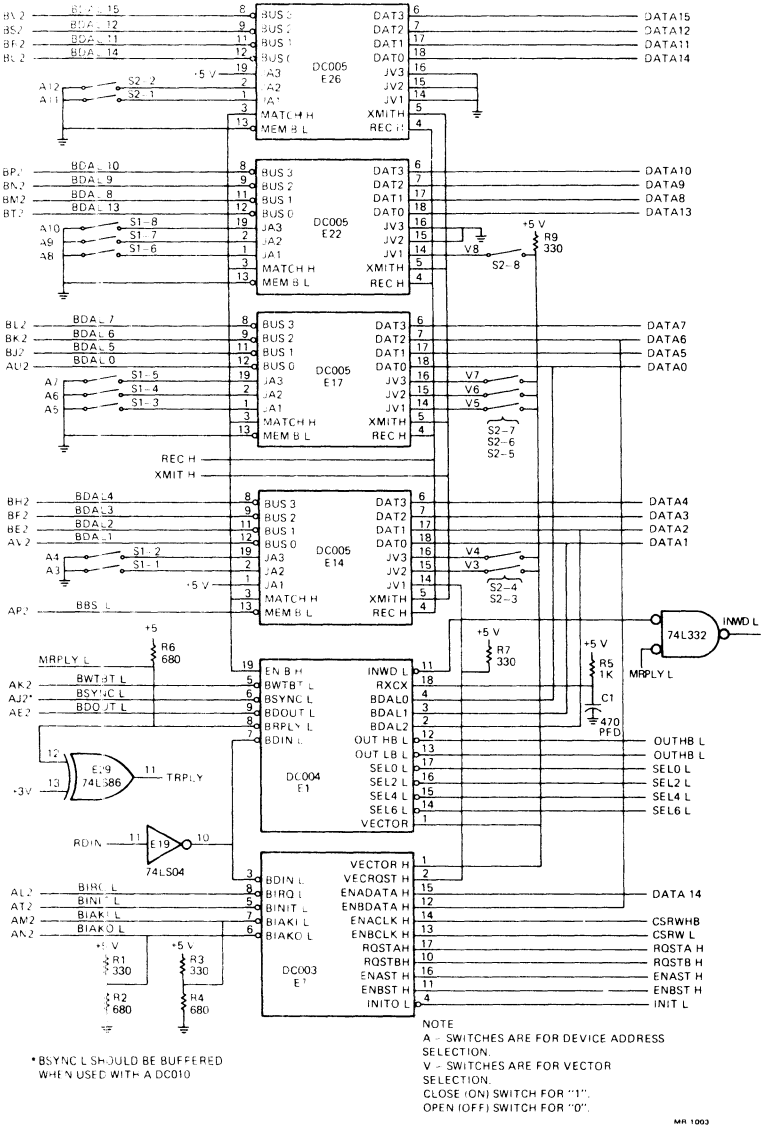


Figure 5-26 Typical Application (DC003, DC004, DC005)

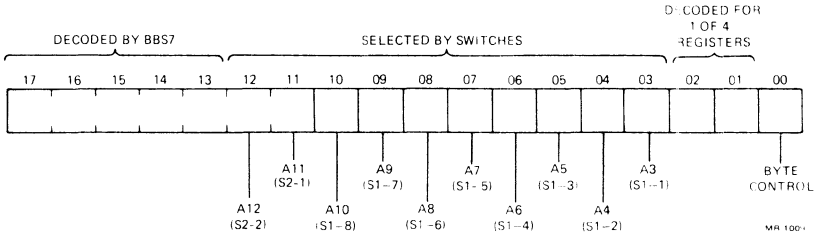


Figure 5-27 Device Address Select Format

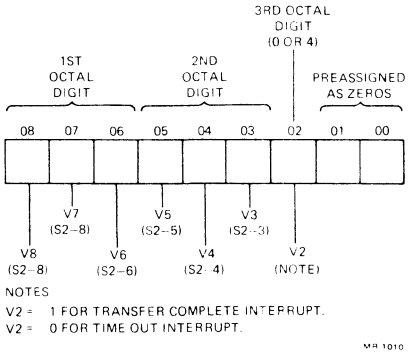


Figure 5-28 Interrupt Vector Select Format

the master device) is determined by the state of the OUTHB L, OUTLB L, or INWD L lines. Internal register selection is summarized as follows:

Control Line	**Select**	**Register**
INWD L (Read)	SEL 0 L	Bus Address Register
INWD L (Read)	SEL 2 L	Word Count Register
OUTHB L (Write High Byte)	SEL 0 L	Bus Address Register
OUTHB L (Write High Byte)	SEL 2 L	Word Count Register
OUTLB L (Write Low Byte)	SEL 0 L	Bus Address Register
OUTLB L (Write Low Byte)	SEL 2 L	Word Count Register
INWD L (Read)	SEL 4 L	Control/Status Register
OUTHB L and MRPLY L (Write CSR High Byte)	SEL 4 L	Control/Status Register
OUTLB L and MRPLY L (Write CSR Low Byte)	SEL 4 L	Control/Status Register
OUTHB L and MRPLY L (Write High Byte)	SEL 6 L	Output Buffer
OUTLB L and RMPLY L (Write Low Byte)	SEL 6 L	Output Buffer

Note that MRPLY L is the BRPLY L output of the DC004 and is used along with OUTHB L and OUTLB L to write either the high or low byte in the control/status register or the output buffers. Write byte selection for the bus address register and the word count register is controlled only by the OUTHB L and OUTLB L lines. Words can be written to the control/status register or the output buffer registers by driving both OUTHB L and OUTLB L to the low state at the same time.

The DC004 integrated circuit is designed to operate directly from the LSI 11 bus. However, since the introduction of the DC005, the DC004 is usually interfaced to the LSI-11 bus through the DC005. Bus signals (BDAL lines) passing through the DC005 are inverted. Therefore, BDAL 0, 1, and 2 signals applied to the DC004 are inverted. Because of this inversion, it is necessary to change the nomenclature on pins 12 through 17 on the DC004. The difference in nomenclature between DC004s operated directly from the LSI-11 bus and through a DC005 are as follows.

From Bus (Non-Inverted BDAL 0, 1, 2)		**From DC005 (Inverted BDAL 0, 1, 2)**	
Pin	**Signal**	**Pin**	**Signal**
12	OUTLB L	12	OUTHB L
13	OUTHB L	13	OUTLB L
14	SEL 0 L	14	SEL 6 L
15	SEL 2 L	15	SEL 4 L
16	SEL 4 L	16	SEL 2 L
17	SEL 6 L	17	SEL 0 L

It is recommended that when a DC005 is used, the DC004 be interfaced to the LSI-11 bus through the DC005 to avoid unnecessary bus loading.

The DC003 IC performs an interrupt transaction that uses the daisy-chain type arbitration scheme to assign priorities to peripheral devices. The DC003 has two channels (A and B) for generating two interrupt requests. Channel A has higher priority than channel B. If a user's device wants control of the LSI-11 bus, the interrupt enable flip-flop within the DC003 must be set. This is accomplished by asserting (logic 1) the ENB DATA line to the DC003 (writing bit 14 or bit 6 to a one) and then clocking the enable flip-flop by asserting (positive transition) the DC003 ENB CLK line. With the interrupt enable flip-flop set, the user's device may then make a bus request by asserting (logic 1) RQST. RQST must be held asserted until the interrupt is serviced. When the RQST is asserted and the interrupt enable flip-flop is set, the DC003 asserts (logic 0) BIRQ L, thus making a bus request. When the request is granted, the processor asserts (logic 0) BDIN L. This causes the DC003 to assert (logic 1) VECTOR H, which is applied to the DC005. VECTOR H at the DC005 causes the device vector to be placed on the BDAL lines to the processor. Interrupts are produced for bus time-outs (CSR bits 15 and 14) and at the completion of a block transfer (CSR bits 7 and 6).

5.2.2 DMA Application

Figure 5-29 shows the DMA control (DC010), the word count/bus address registers (both DC006), the output buffers (both 74LS273s), and the input drivers (74LS367s).

The DC010 performs handshaking operations required to request and gain control of the LSI-11 bus for DMA non-processor request (NPR) data transfers. After becoming bus master, the DC010 produces the signals necessary to perform a DIN, DOUT, or DATIO bus cycle as specified by the control lines. An 8-MHz free-running clock is provided by E8. This clock is used by the DC010 to generate all transfer timing sequences. The actual clock frequency is not critical and can be any frequency up to 8.3 MHz. An RC time constant provided by resistor R14 and capacitor C2 provides a delay for the reassertion of BDMR to the LSI-11 bus. This allows other direct memory access devices to obtain the bus during the time the CNT4 logic releases the bus and re-requests the bus.

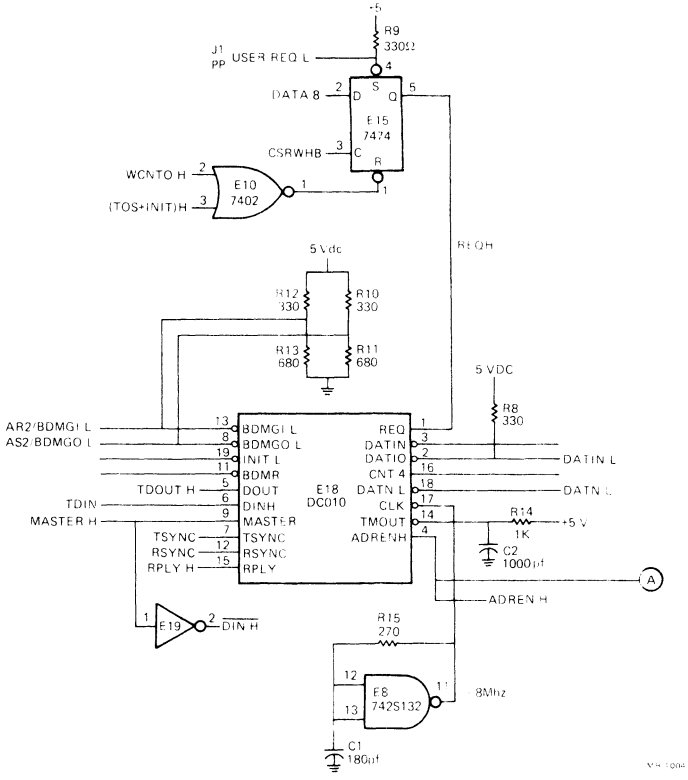


Figure 5-29 Typical Application
(DC006, DC010, Output Delay, and Input Drives)
(Sheet 1 of 2)

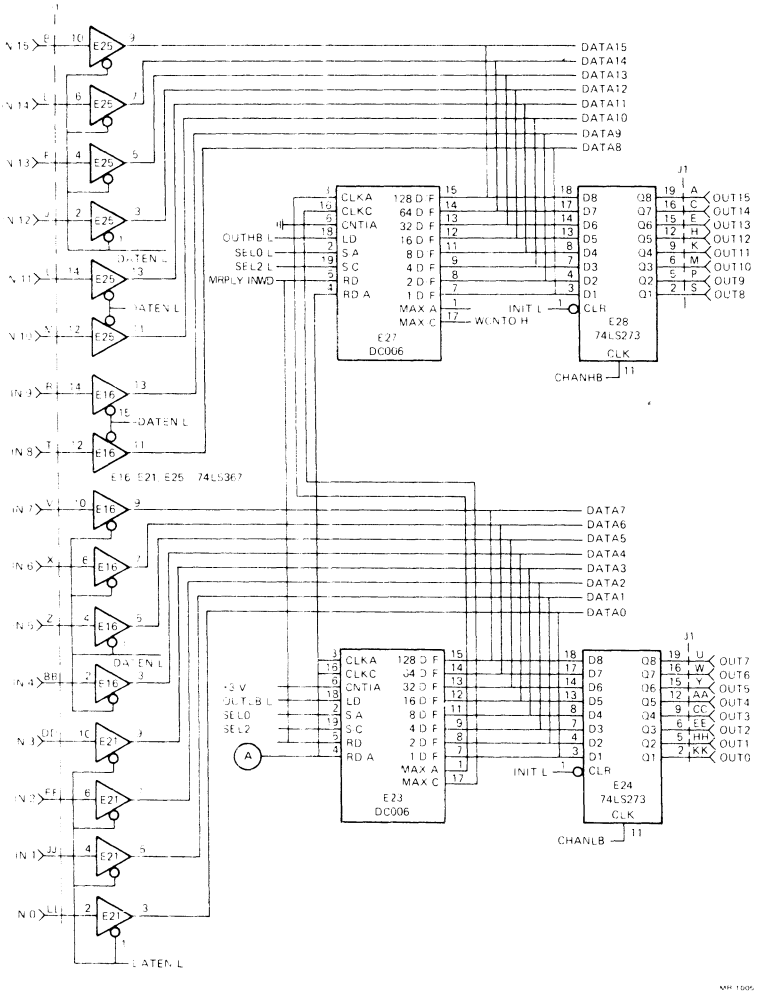


Figure 5-29 Typical Application
(DC006, DC010, Output Delay, and Input Drives)
(Sheet 2 of 2)

User devices initiate bus requests by driving the set input of the request flip-flop (E15) low. This asserts REQ to the DC010 and generates BDMR L to the LSI-11 bus. When the DC010 becomes bus master, it asserts ADREN H to the DC010 bus address registers. ADREN H allows the bus address registers to place the address of the slave (memory) onto the internal bus and, via the DC005 transceivers, onto the LSI-11 bus. The request flip-flop (E15) remains set until the DC006 word count overflows to zero (WCNT0). WCNT0 then resets the request flip-flop.

Two DC006 word count/bus address register ICs are used to provide 16 bits each of word count and bus address. The least significant bits of the word count and bus address are provided by DC006/E23; the most significant bits are provided by DC006/E27. Register A is the bus address register and register C is the word count register. Both registers can be read or written under program control from the LSI-11 bus. Registers are selected by:

• Read bus address register	SEL 0 L INWD L
• Write high byte of bus address register	SEL 0 L OUTHB L
• Write low byte of bus address register	SEL 0 L OUTLB L
• Read word count register	SEL 2 L INWD L
• Write high byte of word count register	SEL 2 L OUTHB L
• Write low byte of word count register	SEL 2 L OUTHB L

The bus address register is incremented by two for word transfers. To accomplish the increment by two, the CNT1A input to the least significant DC006 (E23) must be high, and the CNT1A input to the most significant DC006 (E27) must be grounded. Clocking for DC006 E23 is provided by the transition of the ADREN H line from the DC010. When bus address register DC006 E23 overflows, MAX-A goes high, thus clocking the DC006 E27 bus address register.

The word count register is incremented by one each time a word is transferred. Initially, the word count register is loaded under program control, with the 2's complement of the number of words to be transferred. As words are transferred, the word count register is incremented toward zero. When DC006 E23 overflows, MAX-C goes high. MAX-C clocks the DC006 E27 word count register until DC006 E27 overflows. When E27 overflows, WCNT0 H is generated; WCNT0 H then resets the request flip-flop (E15), thus terminating data transfers.

During DMA data transactions, input data from the DIN bus cycle is placed on the internal tri-state bus via the DC005 transceivers and is

applied to the 74LS273 (E28 and E24) output buffers. These buffers are then clocked by CHANHB and CHANLB, thus placing the data on the 16 OUT lines to the user's device.

For output data transfers (DOUT), the user's device places data on the 16 IN lines to the 74LS367 tri-state drivers. The drivers are enabled by DATEN L, which is asserted during a DOUT cycle. The data passes through the drivers, is applied to the internal tri-state bus and, via the DC005 transceivers, to the LSI-11 bus.

5.2.3 Miscellaneous Logic

Miscellaneous logic is shown in Figure 5-30. This logic includes CSR, output buffer and input driver control, non-existent address time-out, DC005 transceiver receive/transmit control, the control/status register (CSR), additional transceivers (8641s), and the "B" request flip-flop.

The CSR, output buffers, and input driver control receive INWD L, OUTHB L, OUTLB L, SEL 4 L, SEL 6 L, DATN H, and DIN H. These signals are gated to produce enable signals for the CSR, the output buffers, and the input drivers. CSR RD is produced by INWD L and SEL 4 L to enable the CSR data (DATA 5 through DATA 14) (Figure 5-29, sheet 2) to pass through the 74LS367 tri-state drivers and onto the LSI-11 bus via the DC005 transceivers. OUTHB L, OUTLB L, SEL 4 L, and MRPLY L produce either CSRWHB L or CRSWLB L for writing bit 8 of the CSR (7474 E15 on Figure 5-29, sheet 1), or for clocking the "B" request flip-flop. DATEN L is generated either by DATN H or by INWDL and SEL 6 L. DATEN L enables the 74LS367 tri-state input drivers (Figure 5-29, sheet 1) during an IN cycle. The CHANHB and CHANLB signals clock the 74LS273 output buffers during an OUT cycle. When bytes are transferred, OUTHB L, MRPLY L and SEL 6 L enable the high byte (CHANHB L asserted), while OUTLB L, MRPLY and SEL 6 L enable the low byte (CHANLB L). Both bytes are simultaneously transferred (word transfer) when DIN H is negated.

The non-existent address time-out provides a 10 μs time-out in the event that a non-existent address is requested on the LSI-11 bus during a DMA operation. This prevents hanging-up the LSI-11 bus for periods longer than 10 μs. When the DC010 becomes bus master, ADREN H is asserted and clocks the 10 μs one-shot (E11). Normally, RPLY from the LSI-11 bus goes low and the one-shot is cleared. However, if RPLY is high (no response from slave), the one-shot times out and clocks the 74LS74 flip-flop (E12). The flip-flop is set, generating (TOS + INIT) L; this signal is applied to the DC010 (Figure 5-29, sheet 1) clearing the internal synchronization circuit and releasing the LSI-11 bus. (TOS + INIT) H resets the request flip-flop (E15). The 74LS74 flip-flop (E12) can be set and reset with CSRW HB and DATA 15 (CSR bus time-out). This flip-flop is automatically reset during power-up.

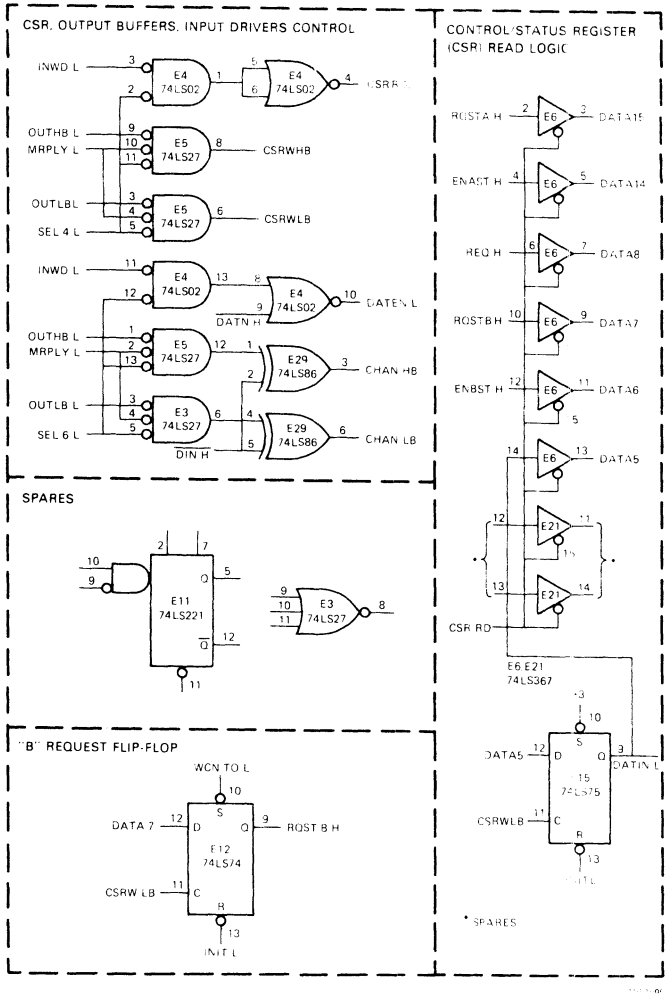


Figure 5-30 Typical Application (Miscellaneous Logic) (Sheet 1 of 3)

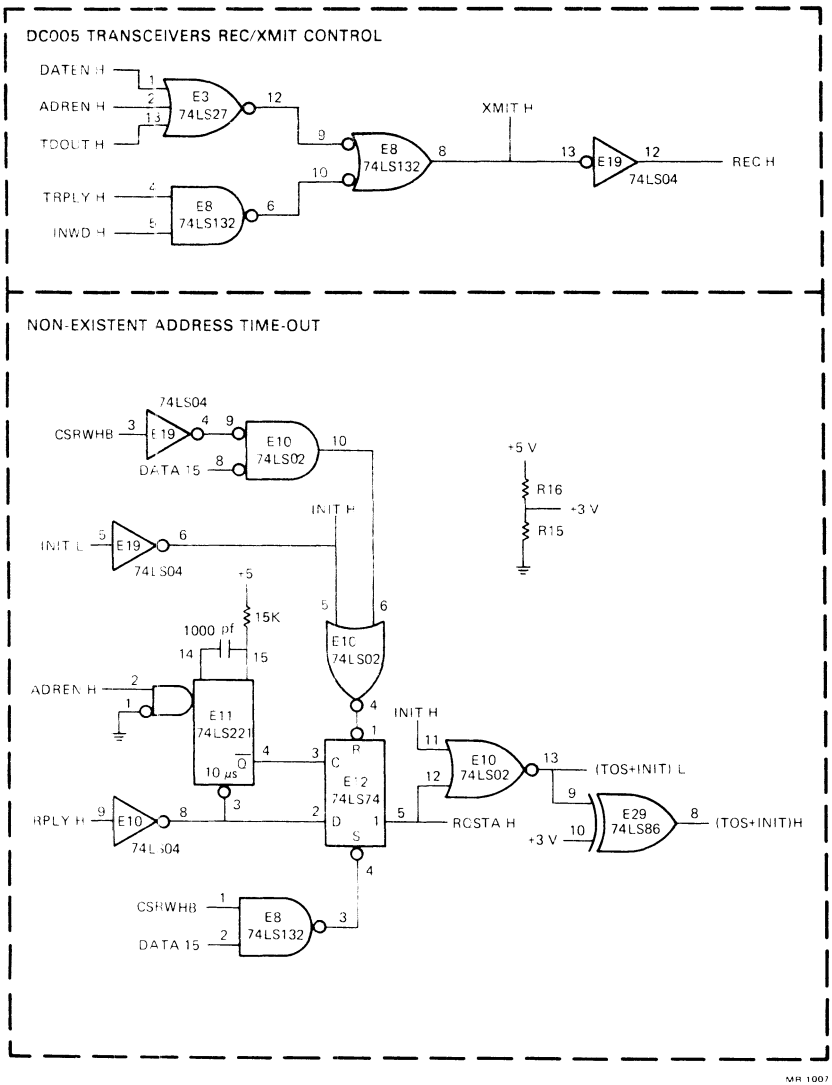


Figure 5-30 Typical Application (Miscellaneous Logic)
(Sheet 2 of 3)

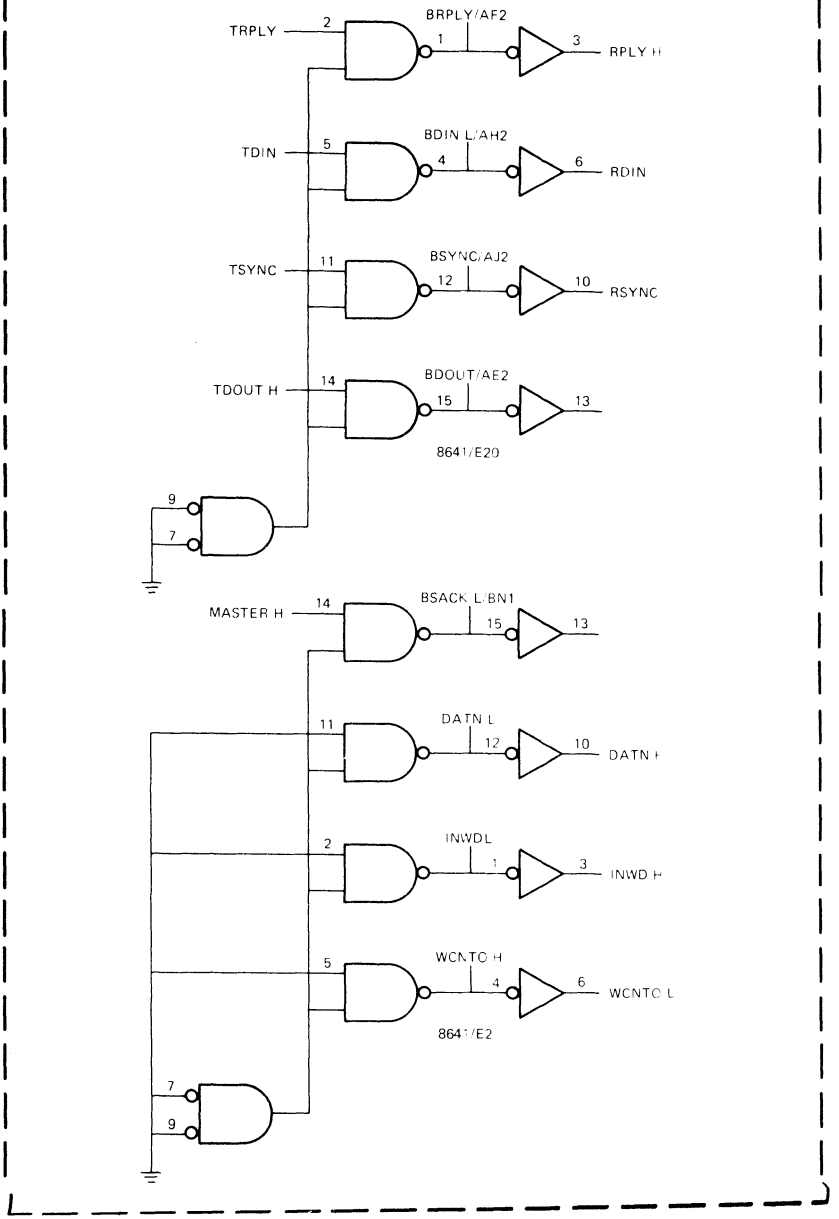


Figure 5-30 Typical Application (Miscellaneous Logic)
(Sheet 3 of 3)

The DC005 transceiver receive/transmit control determines the state of the DC005 transceivers on Figure 5-26. Normally, the transceivers are in the receive state to accept device addresses from the LSI-11 bus. When REC H is asserted (high), XMIT is negated (low). XMIT is asserted (high) when transferring data to the LSI-11 bus (T DOUT, DATEN, and ADREN are high; TRPLY, INWD are low). REC is asserted (high) when receiving data from the LSI-11 bus (TDOUT, DATEN, and ADREN are low; TRPLY, INWD are high).

The control/status register (CSR) (Figure 5-29, sheet 2) has six active bits and is a read/write register comprised of 74LS367 tri-state drivers and flip-flops which are part of other logic circuits shown on Figure 5-29, sheet 1, and Figure 5-30, sheet 3. Figure 5-31 shows the CSR format. The CSR bits are described in Table 5-12.

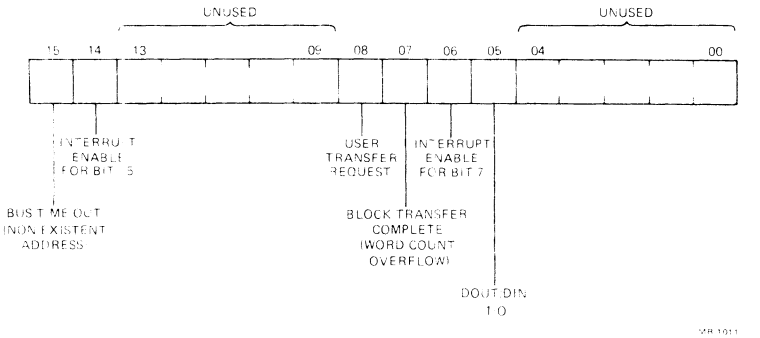


Figure 5-31 Control/Status Register (CSR) Format

The quad transceivers (8641) supplement the DC005 transceivers for interfacing to the LSI-11 bus. In this particular application, the 8641s are permanently enabled by grounding pins 7 and 9.

Table 5-12 CSR Bit Descriptions

Bit	Name	Description
00 01 02 03 04	Unused	
05	DOUT/DIN	When on a 1, indicate a DOUT cycle; when on a 0, indicate a DIN cycle.

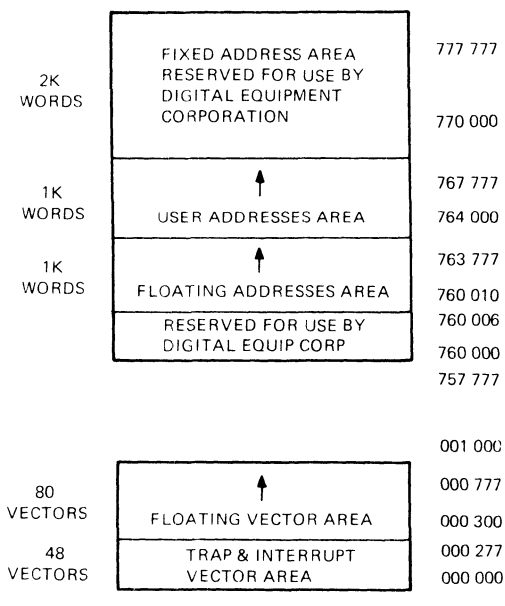
Table 5-12 CSR Bit Descriptions (Cont)

Bit	Name	Description
06	Interrupt enable for bit 7	This bit must be set (1) to enable the word count overflow; interrupt at the end of a block transfer. When on a 0, the interrupt is inhibited.
07	Block transfer complete	This bit sets (1) when the word count register overflows, providing bit 06 is set.
08	User transfer request	The user's device must set (1) this bit to make a bus request and transfer data. User REQ L (J1-PP) must be driven low (0) to set bit 08. This bit is always read as a zero. This is an example for test purposes.
09 10 11 12 13	Unused	
14	Interrupt enable for bit 15	This bit must be set (1) to enable the bus time-out interrupt. When on a 0, the interrupt is inhibited.
15	Bus time-out	This bit sets (1) when a slave on the LSI-11 bus does not respond with BRPLY within 10 μs after being addressed. Bit 14 must be set (1) to enable the bus time-out interrupt.

APPENDIX A

ASSIGNMENT OF ADDRESSES AND VECTORS

A.1 ADDRESS MAP



A.2 FLOATING VECTORS

The conventions for the assignments of floating vectors for modules on the LSI-11 bus will adhere to those established for Unibus devices. Unibus devices are used to explain the priority ranking for floating vectors and are included in the subsequent table of trap and interrupt vectors as a guide to the user.

The floating vector convention used for communications and other devices that interface with the PDP-11 series of products assigns vectors in order starting at 300 and proceeding upward to 777. (Some LSI-11 bus modules, such as the DLV11 and DRV11, have an upper vector limit

of 377.) The following table shows the sequence for assigning vectors to modules. It can be seen that the first vector address, 300, is assigned to the first DLV11 in the system. If another DLV11 is used, it would then be assigned vector address 310, etc. When the vector addresses have been assigned for all the DLV11s (up to a maximum of 32), addresses are then assigned consecutively to each unit of the next highest ranked device (DRV11 or DLV11-E, etc.), then to the other devices in accordance with the ranking.

Ranking for Floating Vectors
(Start at 300 and proceed upward.)

Rank	Unibus	LSI-11 Bus
1	DC11	
2	KL11, DL11-A, -B	DLV11, -F, -J
3	DP11	
4	DM11-A	
5	DN11	
6	DM11-BB	
7	DR11-A	DRV11-B
8	DR11-C	DRV11
9	PA611 Reader	
10	PA611 Punch	
11	DT11	
12	DX11	
13	DL11-C, -D, -E	DLV11-E
14	DJ11	
15	DH11	
16	GT40	
17	LPS11	
18	DQ11	
19	KW11-W	KWV11
20	DU11	DUV11

A.3 INTERRUPT AND TRAP VECTORS

Vector	Unibus	LSI-11 Bus
000	DEC reserved	DEC reserved
004	CPU errors	Bus time-out and illegal instructions (e.g., JMP R0) (odd address and stack overflow traps not implemented on LSI-11)
010	Illegal and reserved instructions	Illegal and reserved instructions
014	BPT, breakpoint trap	BPT instruction and T bit
020	IOT, input/output trap	IOT instruction

Vector	Unibus	LSI-11 Bus
024	Power-fail	Power-fail
030	EMT, emulator trap	EMT instruction
034	TRAP instruction	TRAP instruction
040	System software	
044	System software	
050	System software	
054	System software	
060	Console terminal, keyboard/reader	Console terminal, input
064	Console terminal, printer/punch	Console terminal, output
070	PC11, paper tape reader	
074	PC11, paper tape punch	
100	KW11-L, line clock	External event line interrupt
104	KW11-P, programmable clock	
110		
114	Memory system errors	
120	XY plotter	
124	DR11-B DMA interface; (DA11-B)	DRV11-B
130	AD01, A/D subsystem	
134	AFC11, analog subsystem	
140	AA11, display	
144	AA11, light pen	
150		
154		
160	RL11	RLV11
164		
170	User reserved	
174	User reserved	
200	LP11/LS11, line printer; LA180	LAV11, LPV11
204	RS04/RF11, fixed head disk	
210	RC11, disk	
214	TC11, DECtape	
220	RK11, disk	RKV11
224	TU16/TM11/TS03, magnetic tape	
230	CD11-CM11-CR11, card reader	
234	UDC11, digital control subsystem	
240	PIRQ, program interrupt request (11/45)	
244	Floating-point error	FIS (optional)
250	Memory management	
254	RP04/RP11 disk pack	
260	TA11, cassette	
264	RX11, floppy disk	RXV11

Vector	Unibus	LSI-11 Bus
270	User reserved	
274	User reserved	
300	(Start of floating vectors)	User reserved
.		
.		
374		
400		
404		
410		ADV11-A
414		
420		
424		
430		IBV11-A
434		
440		
444		KW/V11-A
450		
.		
.		User reserved
.		
777	(End of floating vectors)	

A.4 FLOATING ADDRESSES

The conventions for the assignment of floating addresses for modules on the LSI-11 bus will adhere to those established for Unibus devices. Unibus devices are used to explain the ranking sequence and are included in the subsequent table of device addresses as a guide to the user.

The floating address convention used for communications (and other) devices that interface with the PDP-11 series of products assigns addresses in order starting at 760 010 (or 160 010) and proceeds upwards to 763 776 (or 163 776). For compatibility with Unibus convention, addresses are expressed as consisting of 18 bits (7XX XXX) rather than 16 bits (1XX XXX).

Floating addresses are assigned in the following sequence.

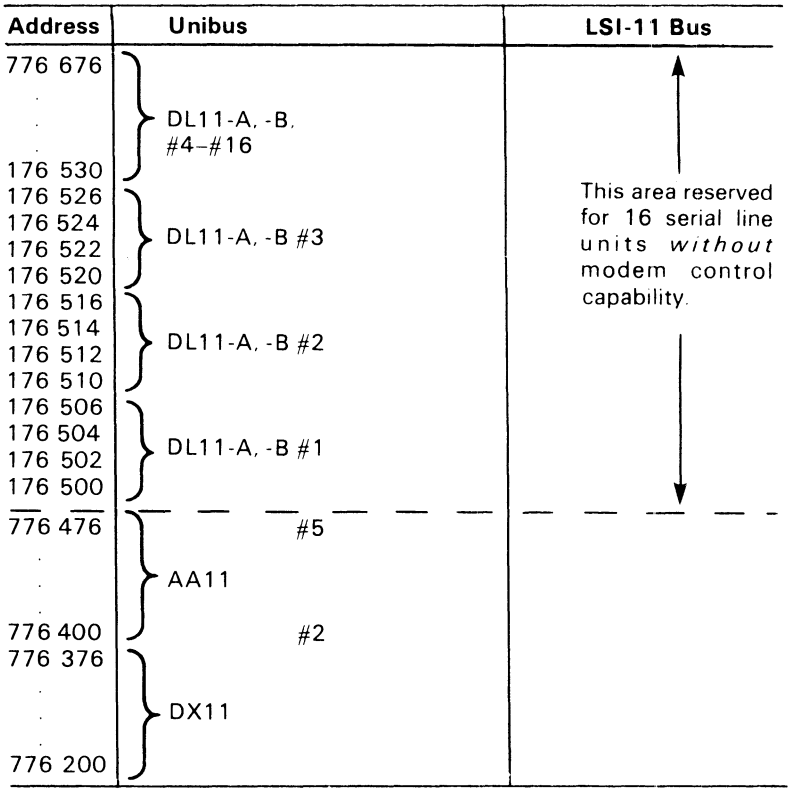
Rank	Unibus Device	LSI-11 Device
1	DJ11	
2	DH11	
3	DQ11	
4	DU11	DUV11
5	DUP11	
6	LK11A	
7	DMC11	
8	DZ11	DZV11
9	KMC11	
10	RL11 (extras)	RLV11 (extras)

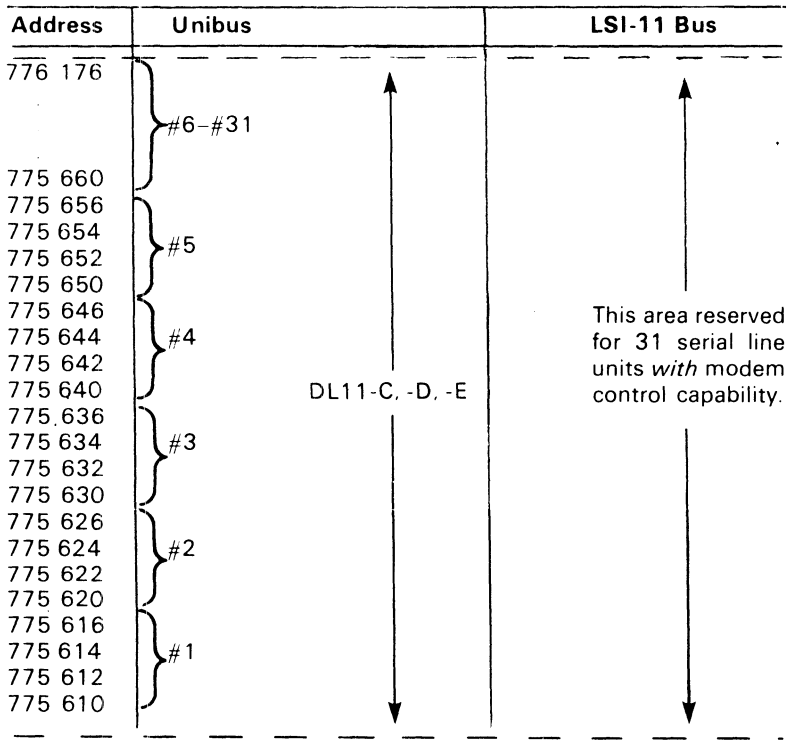
A.5 DEVICE ADDRESSES

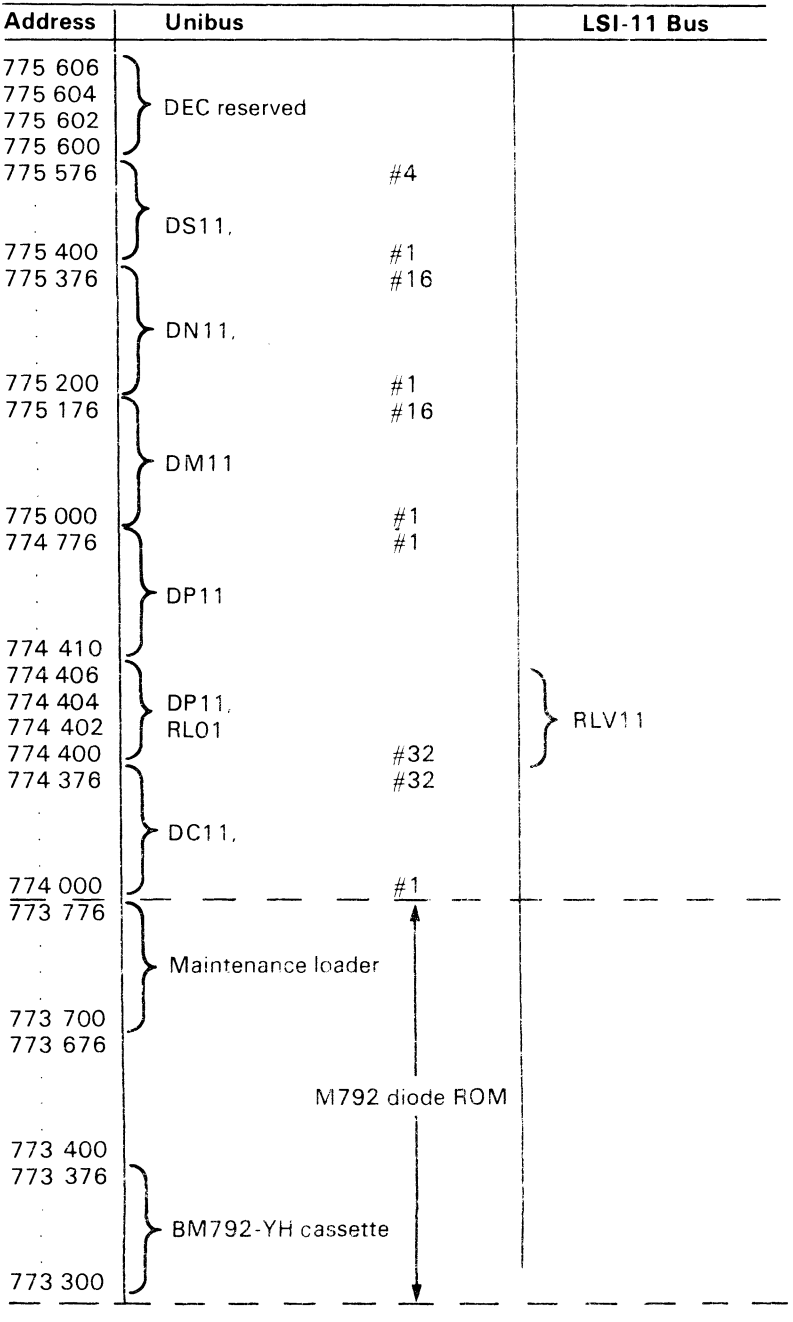
Address	Unibus	LSI-11 Bus
777 776	Processor status word (PS)	
777 774	Stack limit	
777 772	Program interrupt request (PIRQ)	
777 770	DEC reserved	
777 720		
777 716	CPU registers	
777 710		
777 707	R7 (PC)	
777 706	R6 (SP)	
777 705	R5	
777 704	R4 — General Registers	
777 703	R3	
777 702	R2	
777 701	R1	
777 700	R0	
777 676	Memory management	
777 600		
777 576	(SR2)	
777 574	Memory mgt status reg (SR1)	
777 572	(SR0)	
777 570	Console switch and display register	
777 566	(XBUF)	Console Terminal
777 564	(XCSR) — Console Terminal	
777 562	(RBUF)	
777 560	(RCSR)	
777 556	PC11/PR11	
777 554		
777 552		
777 550		
777 546	KW11-L, DL11-W	(LTC) KPV11, BDV11
777 544	XY11	
777 530		
777 526	Unassigned	

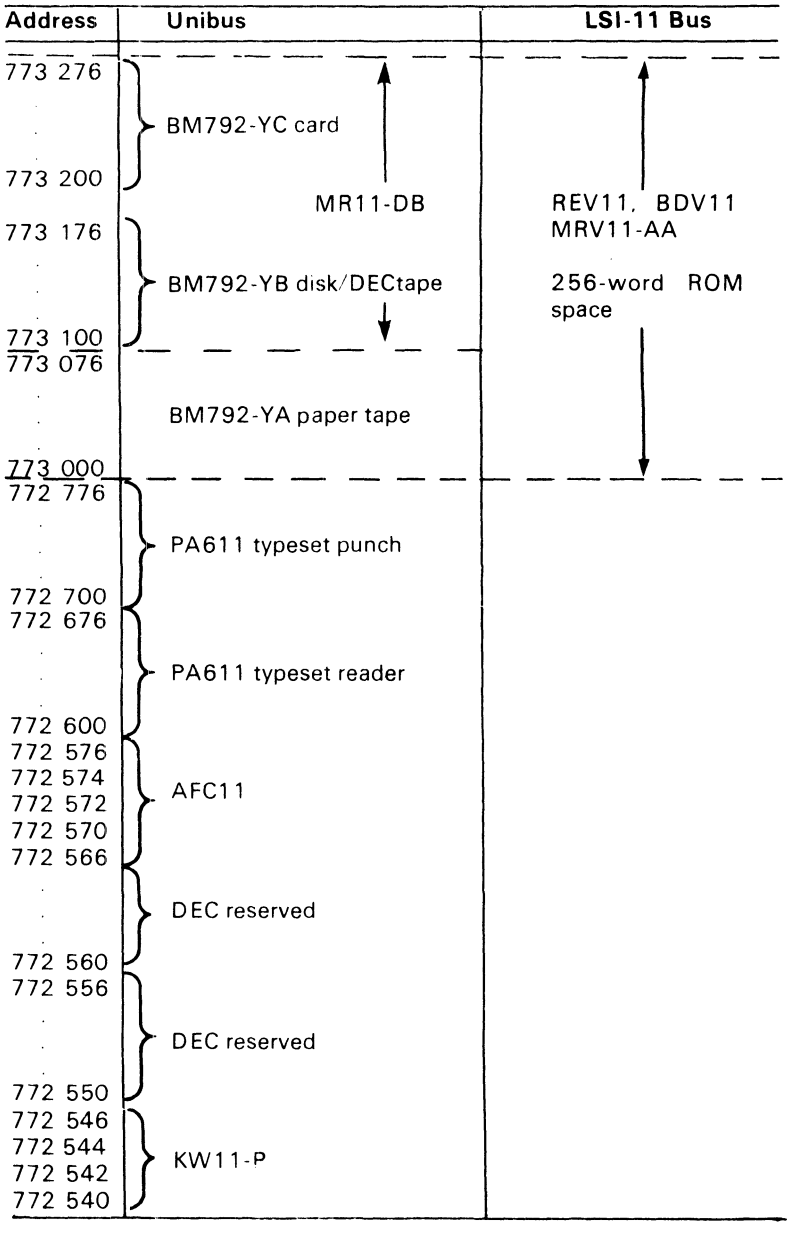
Address	Unibus		LSI-11 Bus
777 524 777 522 777 520	Unassigned		BDV11
777 516 777 514 777 512	LA180, LP11 LS11, LV11		LAV11, LPV11
777 510			
777 506 . . . 777 500	TA11		
777 476 . . . 777 460	RF11		
777 456 . . . 777 440	RC11		
777 436 777 434 777 432 777 430 777 426 777 424 777 422 777 420	DT11, bus switch	#8 #7 #6 #5 #4 #3 #2 #1	
777 416 . . . 777 400	RK11		RKV11
777 376 . . . 777 360	DC14-D		
777 356 . . . 777 340	TC11		
777 336 . . . 777 320	KE11-A, EAE #2		

Address	Unibus		LSI-11 Bus
777 316	KE11-A, EAE #1	arithmetic shift	
777 314		logical shift	
777 312		normalize	
777 310		step count/status register	
777 306		multiply	
777 304		multiplier quotient	
777 302		accumulator	
777 300		divide	
777 276	DEC reserved		
777 200			
777 176	RX11		RXV11
777 174			
777 172			
777 170			
777 166	CR11, CM11, CD11		
777 164			
777 162			
777 160			
777 156	DEC reserved		
777 000			
776 776	AD01		
776 770			
776 766	AA11 #1		
776 750			
776 746	Unassigned		
776 740			
776 736	RP11		
776 700			


Address
Unibus
LSI-11 Bus
776 676
176 530
DL11-A, -B, #4–#16
176 526
176 524
176 522
176 520
DL11-A, -B #3
176 516
176 514
176 512
176 510
DL11-A, -B #2
176 506
176 504
176 502
176 500
DL11-A, -B #1
This area reserved for 16 serial line units without modem control capability.
776 476
#5
AA11
776 400
#2
776 376
DX11
776 200


Address
Unibus
LSI-11 Bus
776 176
#6–#31
775 660
775 656
775 654
775 652
#5
775 650
775 646
775 644
775 642
#4
775 640
775 636
775 634
775 632
#3
775 630
775 626
775 624
775 622
#2
775 620
775 616
775 614
775 612
#1
775 610
DL11-C, -D, -E
This area reserved for 31 serial line units *with* modem control capability.

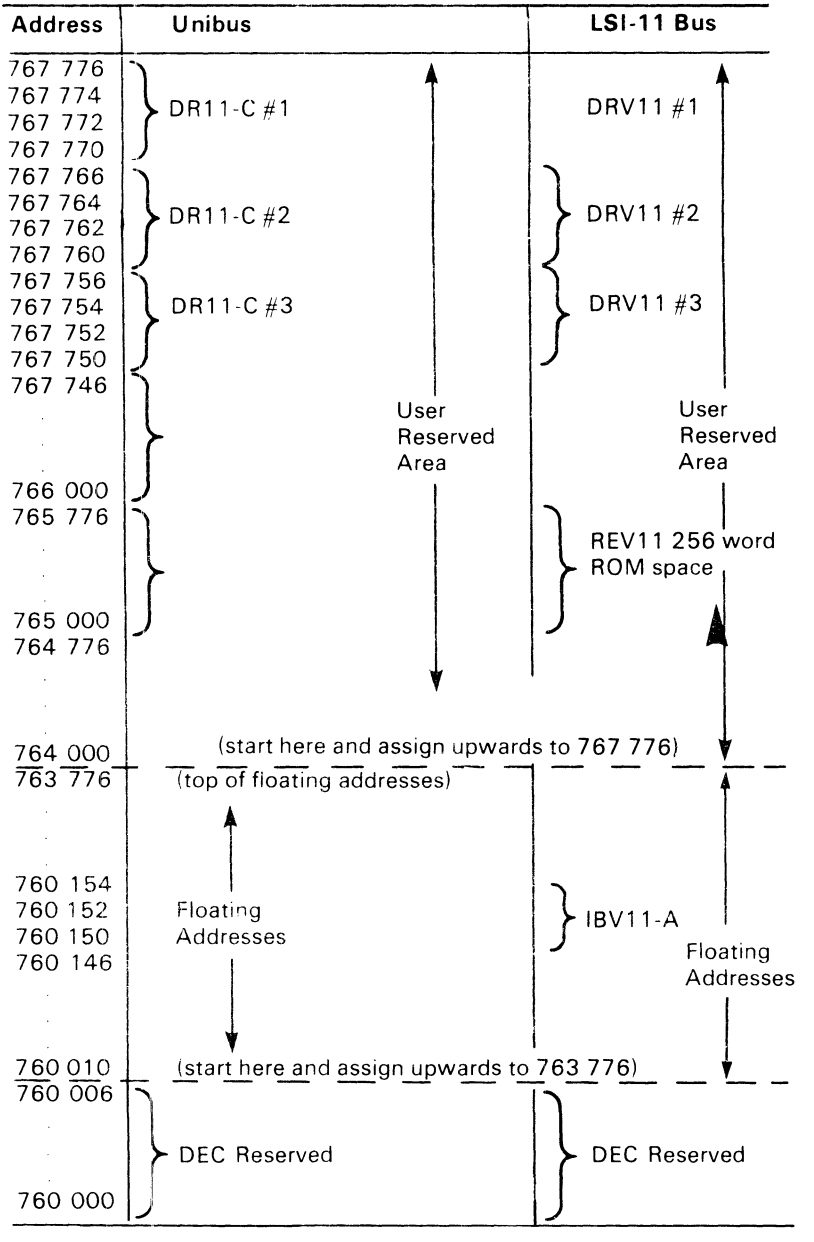

Address
Unibus
LSI-11 Bus
775 606
775 604
775 602
775 600
DEC reserved
775 576
#4
DS11,
775 400
#1
775 376
#16
DN11,
775 200
#1
775 176
#16
DM11
775 000
#1
774 776
#1
DP11
774 410
774 406
774 404
DP11,
RL01
774 402
774 400
#32
RLV11
774 376
#32
DC11,
774 000
#1
773 776
Maintenance loader
773 700
773 676
M792 diode ROM
773 400
773 376
BM792-YH cassette
773 300


Address
Unibus
LSI-11 Bus
773 276
BM792-YC card
773 200
MR11-DB
REV11, BDV11
MRV11-AA
773 176
BM792-YB disk/DECtape
256-word ROM space
773 100
773 076
BM792-YA paper tape
773 000
772 776
PA611 typeset punch
772 700
772 676
PA611 typeset reader
772 600
772 576
772 574
772 572
772 570
772 566
AFC11
DEC reserved
772 560
772 556
DEC reserved
772 550
772 546
772 544
772 542
772 540
KW11-P

Address	Unibus	LSI-11 Bus
772 536 772 534 772 532 772 530 772 526 772 524 772 522 772 520	TM11	
772 516	Memory mgt status reg (SR3)	
772 514 . . . 772 500	OST	
772 456 . . . 772 450	DR11-B #3	
772 446 . . . 772 440	TJU16	
772 436 772 434 772 432 772 430	DR11-B #2	DRV11-B #3
772 426 772 424 772 422 772 420	DEC reserved	DRV11-B #2
772 416 772 414 772 412 772 410	DR11-B, -C #1	DRV11-B #1
772 406 . . . 772 400	KW11-W	
772 376 . . . 772 200	Memory management	

Address	Unibus	LSI-11 Bus
772 176	FP11	
772 160		
772 156	Unassigned	
772 140		
772 136	Memory parity	
772 110		
772 106	Unassigned	
772 102		
772 100	MS11-K, -LP, MM11-LP	
772 076	RL11	
772 070		
772 066	RJS04	
772 040		
772 036	DEC reserved	
772 020		
772 016	GT40, VT48	
772 000		
771 776	UDC functional I/O modules	
771 000		

Address	Unibus		LSI-11 Bus
770 776	KG11	#8	
770 700		#1	
770 676	DM11-BB,	#16	
770 500		#1	
770 476	ADF11		
770 460			
770 456	Unassigned		
770 450			
770 446	LPS11		AAV11-A
770 444			
770 442			
770 440			
770 436			
770 424			KWV11-A
770 422			
770 420			
770 416	AR11, LPS11		
770 404			ADV11-A
770 402			
770 400			
770 376	DEC reserved		
770 000			


Address
Unibus
LSI-11 Bus
767 776
767 774
767 772
767 770
DR11-C #1
DRV11 #1
767 766
767 764
767 762
767 760
DR11-C #2
DRV11 #2
767 756
767 754
767 752
767 750
DR11-C #3
DRV11 #3
767 746
User Reserved Area
User Reserved Area
766 000
765 776
REV11 256 word ROM space
765 000
764 776
764 000
(start here and assign upwards to 767 776)
763 776
(top of floating addresses)
760 154
760 152
760 150
760 146
Floating Addresses
IBV11-A
Floating Addresses
760 010
(start here and assign upwards to 763 776)
760 006
DEC Reserved
DEC Reserved
760 000

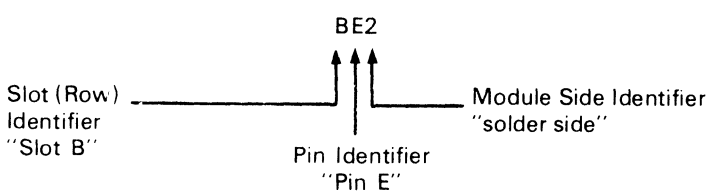
APPENDIX B

LSI-11 BUS SIGNALS

B.1 MODULE CONTACT FINGER IDENTIFICATION

DIGITAL interface modules all use the same contact finger (pin) identification system. The LSI-11 I/O bus is based on the use of double-height modules. These modules plug into a 2-slot bus connector, each containing 36 lines per slot (18 each on component and solder sides of the circuit board). Although the LSI-11 processor module and core memory module are quad-height modules that plug into four connector slots, only two slots (A and B) are used for interface purposes on the processor module. Etched circuit jumpers on the unused portion of the module maintain continuity of grant signals BIAKI L to BIAKO L and BDMGI L to BDMGO L. These daisy-chained signals are described later.

Slots, shown as ROW A and ROW B in Figure B-1, include a numeric identifier for the side of the module. The component side is designated side "1" and the solder side is designated side "2." Letters ranging from A through V (excluding G, I, O, and Q) identify a particular pin on a side of a slot. Hence, a typical pin is designated as:



Note that the positioning notch between the two rows of pins mates with a protrusion on the connector block for correct module positioning.

Quad-height modules are similarly pin numbered. They are identified in Figure B-2.

Individual connector pins, viewed from the underside (wiring side) of a backplane, are identified as shown in Figure B-3. Only the pins for one bus location (two slots) are shown in detail. This pattern of pins is repeated eight times on the H9270 backplane, allowing the user to install one LSI-11 microcomputer module (four slots) and up to six additional 2-slot modules.

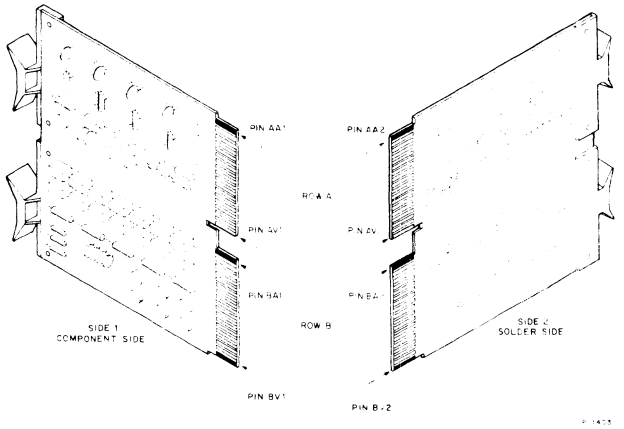


Figure B-1 Dual Module Contact Finger Identification

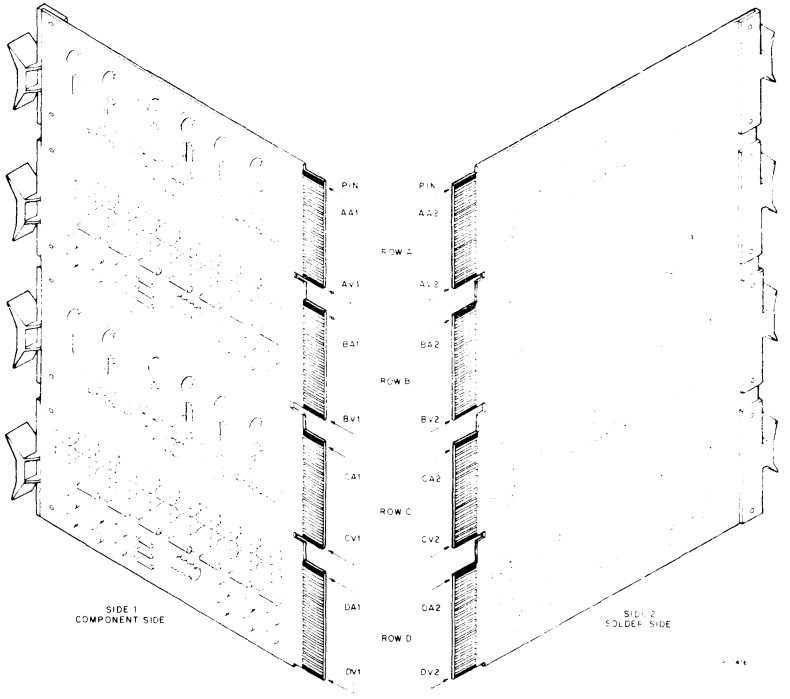


Figure B-2 Quad Module Contact Finger Identification

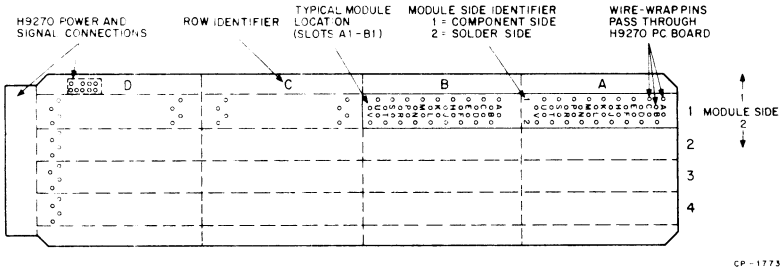


Figure B-3 LSI-11 Backplane Module Pin Identification

B.2 BUS SIGNALS

H9270 backplane pin assignments are listed and described in Table B-1. Only slots A and B are listed. However, they are identical to slots C and D, respectively. Table B-2 alphanumerically lists the LSI-11 bus pin assignments.

Table B-1 Backplane Pin Assignments

Bus Pin	Mnemonic	Description
AA1 AB1	BSPARE1 BSPARE2	Bus Spare (Not assigned, reserved for DIGITAL use.)
AC1 AD1	BDAL16 BDAL17	Extended address bits.
AE1 AF1 AH1	SSPARE1 SSPARE2 SSPARE3	Special Spare (Not assigned, not bused. Available for user interconnections.)
AJ1	GND	Ground – System signal ground and dc return.
AK1 AL1	MSPAREA MSPAREA	Maintenance Spare – Normally connected together on the backplane at each option location (not bused connection).
AM1	GND	Ground – System signal ground and dc return.

Table B-1 Backplane Pin Assignments (Cont)

Bus Pin	Mnemonic	Description
AN1	BDMR L	Direct Memory Access (DMA) Request – A device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master (it has completed a bus cycle and BSYNC L is not being asserted by the processor), it grants bus mastership to the requesting device by asserting BDMGO L. The device responds by negating BDMR L and asserting BSACK L.
AP1	BHALT L	Processor Halt – When BHALT L is asserted, the processor responds by halting normal program execution. External interrupts are ignored but memory refresh interrupts (enabled if W4 on the processor module is removed) and DMA request/grant sequences are enabled. When in the halt state, the processor executes the ODT microcode and the console device operation is invoked.
AR1	BREF L	Memory Refresh – Asserted by a processor microcode-generated refresh interrupt sequence (when enabled) or by an external device. This signal forces all dynamic MOS memory units to be activated for each BSYNC L/BDIN L bus transaction **CAUTION** The user must avoid multiple DMA data transfers (burst or "hog" mode) during a processor-generated refresh operation so that a complete refresh cycle can occur once every 1.6 ms.
AS1	+12B	+12 V Battery Power – Secondary +12 V power connection. Battery power can be used with certain devices.
AT1	GND	Ground – System signal ground and dc return.

Table B-1 Backplane Pin Assignments (Cont)

Bus Pin	Mnemonic	Description
AU1	PSPARE1	Spare (Not assigned. Customer usage not recommended.)
AV1	+5B	+5 V Battery Power – Secondary +5 V power connection. Battery power can be used with certain devices.
BA1	BDCOK H	DC Power OK – Power supply-generated signal that is asserted when there is sufficient dc voltage available to sustain reliable system operation.
BB1	BPOK H	Power OK – Asserted by the power supply when primary power is normal. When negated during processor operation, a power-fail trap sequence is initiated.
BC1 BD1 BE1 BF1 BH1	SSPARE4 SSPARE5 SSPARE6 SSPARE7 SSPARE8	Special Spare (Not assigned, not bused. Available for user interconnections.)
BJ1	GND	Ground – System signal ground and dc return.
BK1 BL1	MSPAREB MSPAREB	Maintenance Spare – Normally connected together on the backplane at each option location (not a bused connection).
BM1	GND	Ground – System signal ground and dc return.
BN1	BSACK L	This signal is asserted by a DMA device in response to the processor's BDMGO L signal, indicating that the DMA device is bus master.
BP1	BSPARE6	Bus Spare (Not assigned. Reserved for DIGITAL use.)

Table B-1 Backplane Pin Assignments (Cont)

Bus Pin	Mnemonic	Description
BR1	BEVNT L	External Event Interrupt Request – When asserted, the processor responds (if PS bit 7 is 0) by entering a service routine via vector address 100<. A typical use of this signal is a line-time clock interrupt.
BS1	PSPARE4	Spare (Not assigned. Customer usage not recommended.)
BT1	GND	Ground – System signal ground and dc return.
BU1	PSPARE2	Spare (Not assigned. Customer usage not recommended.)
BV1	+5	+5 V Power – Normal +5 Vdc system power.
AA2	+5	+5 V Power – Normal +5 Vdc system power.
AB2	–12	–12 V Power – –12 Vdc (optional) power for devices requiring this voltage. **NOTE** LSI-11 modules which require negative voltages contain an inverter circuit (on each module) which generates the required voltage(s); hence, –12 V power is not required with DIGITAL-supplied options.
AC2	GND	Ground – System signal ground and dc return.
AD2	+12	+12 V Power – +12 Vdc system power.
AE2	BDOUT L	Data Output – BDOUT, when asserted, implies that valid data is available on BDAL0–15 L and that an output transfer, with respect to the bus master device, is taking place. BDOUT L is deskewed with respect to data on the bus. The slave device responding to the BDOUT L signal must assert BRPLY L to complete the transfer.

Table B-1 Backplane Pin Assignments (Cont)

Bus Pin	Mnemonic	Description
AF2	BRPLY L	Reply – BRPLY L is asserted in response to BDIN L or BDOUT L and during IAK transaction. It is generated by a slave device to indicate that it has placed its data on the BDAL bus or that it has accepted output data from the bus.
AH2	BDIN L	Data Input – BDIN L is used for two types of bus operation: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master, and requires a response (BRPLY L). BDIN L is asserted when the master device is ready to accept data from a slave device. 2. When asserted without BSYNC L, it indicates that an interrupt operation is occurring. The master device must deskew input data from BRPLY L.
AJ2	BSYNC L	Synchronize – BSYNC L is asserted by the bus master device to indicate that it has placed an address on BDAL0–15 L. The transfer is in process until BSYNC L is negated.
AK2	BWTBT L	Write/Byte – BWTBT L is used in two ways to control a bus cycle: 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence. 2. It is asserted during BDOUT L, in a DATOB bus cycle, for byte addressing.

Table B-1 Backplane Pin Assignments (Cont)

Bus Pin	Mnemonic	Description
AL2	BIRQ L	Interrupt Request – A device asserts this signal when its interrupt enable and interrupt request flip-flops are set. If the processor's PS word bit 7 is 0, the processor responds by acknowledging the request by asserting BDIN L and BIAKO L.
AM2 AN2	BIAKI L BIAKO L	Interrupt Acknowledge Input and Interrupt Acknowledge Output – This is an interrupt acknowledge signal which is generated by the processor in response to an interrupt request (BIRQ L). The processor asserts BIAKO L, which is routed to the BIAKI L pin of the first device on the bus. If it is requesting an interrupt, it will inhibit passing BIAKO L. If it is not asserting BIRQ L, the device will pass BIAKI L to the next (lower priority) device via its BIAKO L pin and the lower priority device's BIAKI L pin.
AP2	BBS7 L	Bank 7 Select – The bus master asserts BBS7 L when an address in the upper 4K bank is placed on the bus. BSYNC L is then asserted and BBS7 L remains active for the duration of the addressing portion of the bus cycle.
AR2 AS2	BDMGI L BDMGO L	DMA Grant Input and DMA Grant Output – This is the processor-generated daisy-chained signal which grants bus mastership to the highest priority DMA device along the bus. The processor generates BDMGO L, which is routed to the BDMGI L pin of the first device on the bus. If it is requesting the bus, it will inhibit passing BDMGO L. If it is not requesting the bus, it will pass the BDMGI L signal to the next (lower priority) device via its BDMGO L pin. The device asserting BDMR L is the device requesting the bus, and it responds to the BDMGI L signal by negating BDMR, asserting BSACK L, assuming bus mastership, and executing the required bus cycle.

Table B-1 Backplane Pin Assignments (Cont)

Bus Pin	Mnemonic	Description
		CAUTION DMA device transfers must be single transfers and must not interfere with the memory refresh cycle.
AT2	BINIT L	Initialize – BINIT is asserted by the processor to initialize or clear all devices connected to the I/O bus. The signal is generated in response to a power-up condition (the negated condition of BDCOK H).
AU2 AV2	BDAL0 L BDAL1 L	Data/Address Lines – These two lines are part of the data/address bus over which address and data information are communicated. Address information is first placed on the bus by the bus master device. The same device then either receives input data from, or outputs data to, the addressed slave device or memory over the same bus lines.
BA2	+5	+5 V Power – Normal +5 Vdc system power.
BB2	–12	–12 V Power – –12 Vdc (optional) power for devices requiring this voltage.
BC2	GND	Ground – System signal ground and dc return.
BD2	+12	+12 V Power – +12 V system power.
BE2	BDAL2 L	
BF2	BDAL3 L	
BH2	BDAL4 L	
BJ2	BDAL5 L	
BK2	BDAL6 L	
BL2	BDAL7 L	
BM2	BDAL8 L	
BN2	BDAL9 L	
BP2	BDAL10 L	Data/Address Lines – These 14 lines are part of the data/address bus previously described.
BR2	BDAL11 L	
BS2	BDAL12 L	
BT2	BDAL13 L	
BU2	BDAL14 L	
BV2	BDAL15 L	

Table B-2 Backplane Pin Assignments (Abbreviated List)

Row A (Same as Row C)		Row B (Same as Row D)	
	Module Side 1 (Component Side)		
AA1	BSPARE1	BA1	BDCOK H
AB1	BSPARE2	BB1	BPOK H
AC1	BDAL16	BC1	SSPARE4
AD1	BDAL17	BD1	SSPARE5
AE1	SSPARE1	BE1	SSPARE6
AF1	SSPARE2	BF1	SSPARE7
AH1	SSPARE3	BH1	SSPARE8
AJ1	GND	BJ1	GND
AK1	MSPAREA	BK1	MSPAREB
AL1	MSPAREA	BL1	MSPAREB
AM1	GND	BM1	GND
AN1	BDMR L	BN1	BSACK L
AP1	BHALT L	BP1	BSPARE6
AR1	BREF L	BR1	BEVNT L
AS1	+12B	BS1	PSPARE4
AT1	GND	BT1	GND
AU1	PSPARE1	BU1	PSPARE2
AV1	+5B	BV1	+5
	Module Side 2 (Solder Side)		
AA2	+5	BA2	+5
AB2	-12	BB2	-12
AC2	GND	BC2	GND
AD2	+12	BD2	+12
AE2	BDOUT L	BE2	BDAL2 L
AF2	BRPLY L	BF2	BDAL3 L
AH2	BDIN L	BH2	BDAL4 L
AJ2	BSYNC L	BJ2	BDAL5 L
AK2	BWTBT L	BK2	BDAL6 L
AL2	BIRQ L	BL2	BDAL7 L
AM2	BIAKI L	BM2	BDAL8 L
AN2	BIAKO L	BN2	BDAL9 L
AP2	BBS7 L	BP2	BDAL10 L
AR2	BDMGI L	BR2	BDAL11 L
AS2	BDMGO L	BS2	BDAL12 L
AT2	BINIT L	BT2	BDAL13 L
AU2	BDAL0 L	BU2	BDAL14 L
AV2	BDAL1 L	BV2	BDAL15 L

APPENDIX C

PERIPHERAL AND OPTION DATA

C.1 MODULE IDENTIFICATION NUMBERS

Module	Option	Description
A012	ADV11-A	16-Channel, 12-Bit A/D Converter
A6001	AAV11-A	4-Channel, 12-Bit D/A Converter
G653	MMV11-A	4K × 16-Bit Core Memory, Mother-board
H223	MMV11-A	4K × 16-Bit Core Memory, Core Stack Board
M7269	RKV11-D	RK05 Disk Drive Bus Interface
M7940	DLV11	Serial Line Unit Interface
M7941	DRV11	Parallel Line Unit Interface
M7942	MRV11-AA	4K × 16-Bit Read-Only Memory (Less PROMs)
M7944	MSV11-B	4K × 16-Bit Read/Write MOS Memory
M7946	RXV11-A	Floppy Disk Drive Bus Interface
M7948	DRV11-P	Foundation Module
M7949	LAV11	LA180 Line Printer Option
M7950	DRV11-B	DMA Interface
M7951	DUV11	Synchronous Serial Line Interface
M7952	KWV11-A	Programmable Real-Time Clock
M7954	IBV11-A	Instrument Bus Interface

M7955-YD	MSV11-CD	16K X 16-Bit Read/Write MOS Memory
M7957	DZV11-A	Asynchronous Line Interface
M8012	BDV11-AA	Bootstrap, Diagnostic, and Terminator
M8013	RLV11	RL01 Disk Drive Disk Control
M8014	RLV11	RL01 Disk Drive Disk Control
M8016	KPV11-A	Power-Fail/Line-Time Clock
M8016-YB	KPV11-B	Power-Fail/Line-Time Clock/120-Ohm Terminator
M8016-YC	KPV11-C	Power-Fail/Line-Time Clock/220-Ohm Terminator
M8017	DLV11-E	Asynchronous Line Interface
M8021	MRV11-BA	UV PROM/RAM (Less PROMs)
M8027	LPV11	LA180/LP05 Printer Option
M8028	DLV11-F	Asynchronous Line Interface
M8043	DLV11-J	Four Asynchronous Line Interfaces
M8044	MSV11-D	4K, 8K, 16K, 32K MOS Memory
M8045	MSV11-E	4K, 8K, 16K, 32K MOS Memory with Parity
M9400-YA	REV11-A	DMA Refresh/Bootstrap ROM/120-Ohm Terminator
M9400-YB	TEV11	120-Ohm Terminator
M9400-YC	REV11-C	DMA Refresh/Bootstrap ROM
M9400-YD	BCV1A	Expansion Module
M9400-YE	BCV1B	Expansion Module
M9400-YH	REV11-H	Remote-11 Boot
M9401	BCV1A,B	Expansion Module

C.2 MODULE SPECIFICATIONS

Option Desig.	Module No(s).	Description	Power Requirements +5 V ± 5%	Power Requirements +12 V ± 3 %	Bus Loads* AC (Max)	Bus Loads* DC	Size
AAV11-A	A6001	4-channel, 12-bit D/A converter	1.5 A	0.4 A	1.9	1	Quad
ADV11-A	A012	16-channel, 12-bit A/D converter	2.0 A	0.45 A	3.25	1	Quad
BDV11-AA	M8012	Boot, term, diagnostic	1.6 A	0.07 A	2.0	1	Quad
DLV11	M7940	Asynchronous serial line interface	1.0 A	0.18A	2.5	1	Double
DLV11-E	M8017	Asynchronous line interface	1.0 A	0.18 A	1.6	1	Double
DLV11-F	M8028	Asynchronous line interface	1.0 A	0.18 A	2.2	1	Double
DLV11-J	M8043	4 Asynchronous serial interface	1.5 A	0.5 A	1	1	Double

*These ac loads figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/AC load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Option Desig.	Module No(s).	Description	Power Requirements +5 V ± 5%	Power Requirements +12 V ± 3 %	Bus Loads* AC (Max)	Bus Loads* DC	Size
DRV11	M7941	Parallel line unit interface	0.9 A	–	1.4	1	Double
DRV11-B	M7950	DMA interface	1.9A	–	3.3	1	Quad
DRV11-P	M7948	Foundation module	1.0A + user logic	–	2.1	1	Quad
DUV11	M7951	Synchronous serial line interface	0.86 A	0.32 A	1.00	1	Quad
DZV11-A	M7957	Asynchronous line interface	1.15 A	0.39 A	4.0	1	Quad
IBV11-A	M7954	Instrument bus interface	0.8 A	–	1.8	1	Double
KPV11-A	M8016	Power-fail/line-time clock	0.56 A	–	1.6	1	Double
KPV11-B	M8016 YB	Power-fail/line-time clock/120 Ω bus terminator	0.56 A		1.6	1	Double

*These ac loads figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/AC load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Option Desig.	Module No(s).	Description	Power Requirements +5 V ± 5%	+12 V ± 3 %	Bus Loads* AC (Max)	DC	Size
KPV11-C	M8016-YC	Power-fail/line-time clock/220 Ω bus terminator	0.56 A	–	1.6	1	Double
KWV11-A	M7952	Programmable real-time clock	1.75 A	0.01 A	3.4	1	Quad
LAV11	M7949	LA180 line printer interface	0.8 A	–	1.8	1	Double
LPV11	M8027	LA180/LP05 printer interface	0.8 A	–	1.4	1	Double
MMV11-A	H223 G653	4K × 16 core memory			1.9	1	2 quads
		(standby current)	3.0 A	0.2 A			
		(operating current)	7.0 A	0.6A			
MRV11-AA	M7942	4K × 16 read-only memory (less PROM integrated circuits)	0.4 A	–	1.8	1	Double

*These ac loads figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/AC load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Option Desig.	Module No(s).	Description	Power Requirements +5 V ± 5%	Power Requirements +12 V ± 3 %	Bus Loads* AC (Max)	Bus Loads* DC	Size
MRV11-AA (Cont)	M7948	(with 32 512 × 4 PROM integrated circuits) (MRV11-AC)	2.8 A				
MRV11-BA	M8021	UV PROM-RAM (less PROM integrated circuits)	0.58 A	0.34 A	2.8	1	Double
		(with 8 1K × 8 PROM integrated circuits) (MRV11-BC)	0.62 A	0.5 A			
MSV11-B	M7944	4K × 16 read/write MOS memory	0.6 A	0.54 A	1.9	1	Double
MSV11-CD	M7955-YD	16K × 16 read/write MOS memory	1.1 A	0.54 A	2.3	1	Quad

*These ac loads figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/AC load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

Option Desig.	Module No(s).	Description	Power Requirements +5 V ± 5%	Power Requirements +12 V ± 3 %	Bus Loads* AC (Max)	Bus Loads* DC	Size
MSV11-D	M8044	4K/16K/32K MOS memory	1.7 A	0.34 A	2.0	1	Double
MSV11-E	M8045	4K/16K/32K MOS memory	2.0 A	0.41 A	2.0	1	Double
REV11-A	M9400-YA	120 Ω terminator, DMA refresh, bootstrap ROM	1.6 A	--	2.2	1	Double
REV11-C	M9400-YC	DMA refresh, bootstrap ROM	1.6 A	–	2.2	1	Double
RKV11-D	M7269	LSI-11 bus control for RKV11-D	1.8 A	–	1.9	1	Double
RLV11	M8013 M8014	RL01 disk drive	5 A	1.0 A	3.2	1	2 quads
RXV11-A	M7946	RX01 interface	1.5 A	–	1.8	1	Double
TEV11	M9400-YB	120 Ω terminator	0.5 A	–	0	0	Double

*These ac loads figures were measured using standard TDR (time domain reflectometry) techniques. The conversion factor is 9.35 pF/AC load. These numbers are nominal values which will tend to vary from module to module due to normal tolerances of components used in the manufacturing of the product.

C.3 BACKPLANE SPECIFICATIONS

Option	Description	Bus Loads AC	DC
H9270	4 X 4 Backplane	5.1	0
H9281A	2 X 4 Backplane	1.3	0
H9281B	2 X 8 Backplane	2.4	0
H9281C	2 X 12 Backplane	3.6	0

APPENDIX D

NOMENCLATURE FOR CIRCUIT SCHEMATICS

D.1 BASIC SIGNAL NAMES

Signal names on DIGITAL print sets are in the following form:

SOURCE (ASSERTION) SIGNAL NAME (STATE) POLARITY

SOURCE indicates the drawing number of the print from which the signal originates. The drawing number of a print is located in the lower right corner of the print title block (D1, D2, D3, etc.)

ASSERTION is either blank or a NOT sign (~). A blank indicates that reference is being made to the asserted state (the true state) of the signal; a NOT sign indicates reference to the negated state (the false state) of the signal. Signals originating from flip-flops do not use the NOT sign to indicate *assertion;* instead, they use a 1 or 0 in parentheses following the signal name for assertion indication.

SIGNAL NAME is the proper name of the signal. The names used on the print are also used in this manual for correlation between the two.

STATE is present when the signal source is a flip-flop; it is either (0) or (1).

POLARITY is either H or L to indicate the voltage level of the signal: H means +3 V; L means ground.

For example, the signal

D5 TX DONE H

originates on sheet 5 of the drawings and is read "when TX DONE is true, this signal is at +3 V."

LSI-11 bus signal lines carry a dual source indicator. These signal names represent a bidirectional wire-ORed bus; as a result multiple sources for a particular bus signal exist.

D.2 FLIP-FLOP SIGNAL NAMES

Flip-flop signal names add an extra dimension. Although flip-flops have only two outputs, four signal names are possible (Figure D-1). The two real outputs are RX DONE (1) H on pin 5 and RX DONE (0) H on pin 6. The two additional outputs are simply the two real outputs reidentified. RX DONE (1) L is electrically the same as RX DONE (0) H and RX DONE (0) L is electrically the same as RX DONE (1) H. For example, the signal RX DONE (0) L is read "when the RX DONE flip-flop is clear (holding a zero), this signal is at ground."

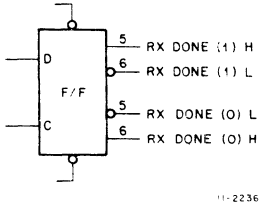


Figure D-1 Flip-Flop Signal Names

APPENDIX E

ASYNCHRONOUS SERIAL LINE UNIT (SLU) COMPARISONS

The characteristics listed in Tables E-1, E-2, and E-3 compare the different members of the DLV11 (LSI-11 bus) and DL11 (Unibus) families of asynchronous serial line products. All modules of the DLV11 series are dual-height modules. The DLV11-E, -F, and -J modules detect overrun conditions which are reported in the receiver CSR. These modules will not generate phantom interrupts on overrun.

DLV11-J
Each of the four serial ports on this module are separate and independent from the others. This is *not* a multiplexed module. Each port has its own CSRs, data buffers, interrupt vectors, baud rates, UARTs, etc. The net effect of this module is to achieve a 4:1 compression ratio over the DLV11. The main functional difference between the ports of the DLV11-J and the DLV11 is that the DLV11-J provides an RS-232C-compatible interface (using RS-422 and RS-423) only and requires the DLV11-KA module (one per port) to accommodate the 110 baud, 20 mA current loop interface.

DLV11-E
This module is functionally equivalent to the DL11-E except that it has programmable baud rates. This module provides one serial port that has full modem control.

DLV11-F
This module is functionally equivalent to the DL11-F except that it has programmable baud rates. This module will eventually replace the DLV11.

DZV11-B
The DZV11-B is a multiplexer interface between four asynchronous serial data communication channels and the LSI-11 bus. The DZV11-B provides EIA level conversion and full modem control suitable for support of Bell series 103, 202, or equivalent modems. Program compatibility is maintained with the Unibus option, DZ11-A. The only compatibility exception is the number of serial channels supported. As a product enhancement feature, additional modem control leads are supported to allow half-duplex operation on switched network type lines.

Table E-1 Comparison of Hardware Features

	Unibus					LSI-11 Bus					
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KB	DZV11-B
No. of ports per module	1	1	1	1	1	1	1	1	4	1	4
EIA RS-232C											
Full modem control					X		X				X
Limited modem interface		X		X		X		X	X		
EIA RS-423, RS-422											
Data leads only									X		
20 mA current loop											
RCVR active or passive						X		X	*	X	
XMIT active or passive						X		X	*	X	
XMIT active only	X	X	X	X							

*The external 20 mA option (DLV11-KB)is required to implement this function.

†Optional feature

‡Applies only to the port assigned to the console device.

§The loop-back cable is required to implement this function.

‖110 baud only.

Table E-1 Comparison of Hardware Features (Cont)

	Unibus					LSI-11 Bus					
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KB	DZV11-B
CCITT		X		X	X						X
Halt on framing error†						X		X	‡		
Boot on framing error†							X	X	‡		
Baud rates (Table E-3)											
Programmable							X	X			X
On-board clocks for split speed	X	X	X	X	X		X	X			X
Reader run control	X		X			X		X	*		
Error flags	X	X	X	X	X		X	X			X

*The external 20 mA option (DLV11-KB)is required to implement this function.

†Optional feature.

‡Applies only to the port assigned to the console device.

§The loop-back cable is required to implement this function.

‖110 baud only.

Table E-1 Comparison of Hardware Features (Cont)

	Unibus					LSI-11 Bus					
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KB	DZV11-B
Break generation bit	X	X	X	X	X	X	X	X	X		X
Receiver active bit	X	X	X	X	X		X	X			
Maintenance bit	X	X	X	X	X	§	X	X	§		X
UART cleared by INIT	X	X	X	X	X		X	X			
UART cleared by DCOK						X			X		
No trap on write to input buffer	X	X	X	X	X		X	X			

*The external 20 mA option (DLV11-KB)is required to implement this function.

†Optional feature.

‡Applies only to the port assigned to the console device

§The loop-back cable is required to implement this function.

‖110 baud only.

Table E-1 Comparison of Hardware Features (Cont)

	Unibus					LSI-11 Bus					
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KB	DZV11-B
Easy configuration using wire-wrap jumpers							X	X	X		
Stop bits											
1			X	X	X	X	X	X	X		X
1.5			X	X	X				X		X
2	X	X	X	X	X	X	‖	‖	X		X

*The external 20 mA option (DLV11-KB)is required to implement this function.

†Optional feature.

‡Applies only to the port assigned to the console device.

§The loop-back cable is required to implement this function.

‖110 baud only.

Table E-2 Baud Rates

Baud Rate	Unibus					LSI-11 Bus					
	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J	DLV11-KB	DZV11-B
50	X	X	X	X	X	X	X	X			X
75	X	X	X	X	X	X	X	X			X
110	X	X	X	X	X	X	X	X	*	X	X
134.5			X	X	X	X	X	X			X
150	X	X	X	X	X	X	X	X	X		X
200			X	X	X	X					
300	X	X	X	X	X	X	X	X	X		X
600	X	X	X	X	X	X	X	X	X		X
1200	X	X	X	X	X	X	X	X	X		X
1800	X	X	X	X	X	X	X	X			X
2000							X	X			X
2400	X	X	X	X	X	X	X	X	X		X
3600							X	X			X
4800			X	X	X	X	X	X	X		X
7200			X	X	X		X	X			X
9600			X	X	X	X	X	X	X		X
19200							X	X	X		

*The external 20 mA option (DLV11-KB) is required to implement this function.

Table E-3 Comparison of Software Features

			Unibus					LSI-11			
Register	**Bit**	**Name**	**DL11-A**	**DL11-B**	**DL11-C**	**DL11-D**	**DL11-E**	**DLV11**	**DLV11-E**	**DLV11-F**	**DLV11-J**
RCSR	15	Data set status/ interrupt					X				
14		Ring				X		X			
	13	CTS					X		X		
	12	CD					X		X		
	11	Receiver active	X	X	X	X	X		X	X	
	10	2d receive					X		X		
	9,8,4	Unused	X	X	X	X	X	X	X	X	X
	7	Receive done	X	X	X	X	X	X	X	X	X
	6	Receive int. enbl.	X	X	X	X	X	X	X	X	X
	5	Data set int. enbl.					X		X		
	3	2d XMT					X		X		
	2	RTS					X		X		
	1	PTR					X		X		
	0	Rdr enable	X		X			X		X	*

* The external 20 mA option (DLV11-KB) is required to implement this function.

Table E-3 Comparison of Software Features (Cont)

			Unibus					LSI-11			
Register	Bit	Name	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	DLV11	DLV11-E	DLV11-F	DLV11-J
RBUF	15	Error			X	X	X		X	X	X
	14	OE			X	X	X		X	X	X
	13	FE			X	X	X		X	X	X
	12	PE			X	X	X		X	X	X
	11–8	Unused	X	X	X	X	X	X	X	X	X
	7–0	Receive data	X	X	X	X	X	X	X	X	X
XCSR	15–8	Unused	X	X	X	X	X	X	X	X	X
	7	XMT ready	X	X	X	X	X	X	X	X	X
	6	XMT int. enbl.	X	X	X	X	X	X	X	X	X
	5–3,1	Unused	X	X	X	X	X	X	X	X	X
	2	Maintenance	X	X	X	X	X	*	X	X	*
	0	XMT break			X	X	X	X	X	X	X
XBUF	15–8	Unused	X	X	X	X	X	X	X	X	X
	7–0	XMT BUF	X	X	X	X	X	X	X	X	X

*The loop-back cable is required to implement this function.

APPENDIX F

COMPARISON OF DATA TRANSMISSION TECHNIQUES

Frequently, the application arises where a data transmission path has to be established between two devices. Usually the distance between the devices is known, and also the rate of data transmission is known. The problem is deciding which is the best communication technique to use to interconnect the devices.

Figure F-1 is a graph of data rate versus distance for the various standard transmission techniques. Parallel data transmission techniques (PLUs and DMA) give the highest data rate; however, they are only good for relatively short distances. The serial techniques (RS-232C, RS-422 and current loops) are good for longer distances but at limited data rates.

While analyzing Figure F-1, remember that the axes are logarithmic and that the data rate is in words per second rather than baud rate. The limits established for distance and data rate are a function of both the inherent limitations of the transmision technique and of the DIGITAL device used to do the interconnection. As an example, look at the 422 section of the graph. Maximum distance is 4000 feet as established by EIA standard RS-422, but the maximum data rate of 1920 words per second is based on the maximum baud rate of the DLV11-J which is 38.4K baud.

Table F-1 is a summary of the LSI-11 bus and Unibus devices which can be used with each communication technique. Currently, there is no Unibus device for EIA RS-422.

NOTES AND ASSUMPTIONS FOR FIGURE F-1

1. Data Rate Definition

   a. One word equals 16 bits.

   b. For serial techniques, one word equals two characters formatted with one start bit, eight data bits, and one stop bit. Asynchronous serial transmission is assumed.

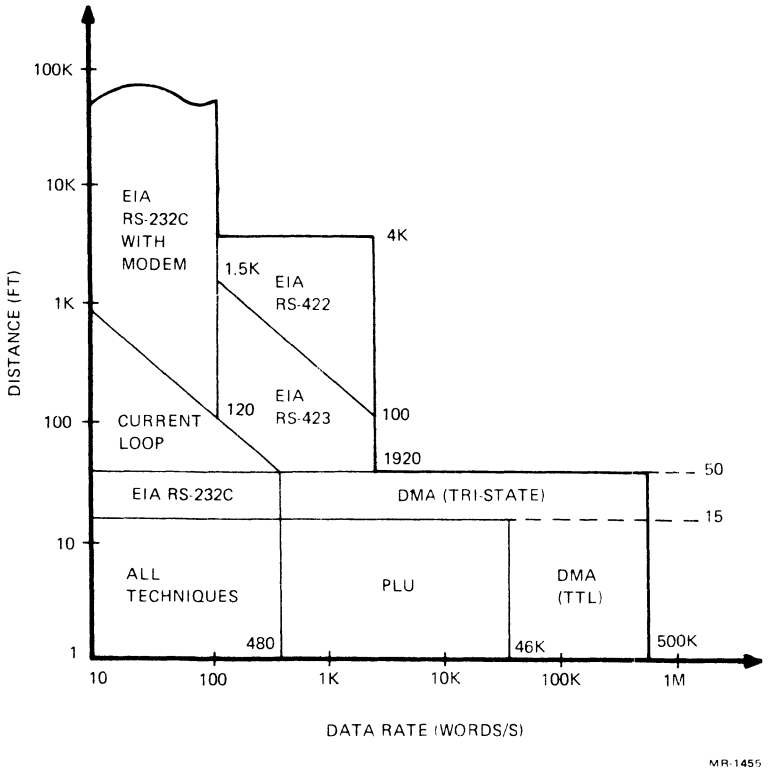


Figure F-1 Data Rate vs Distance with DIGITAL Devices

Table F-1 Communication Techniques

	LSI-11	Unibus
Loop	DLV11	DL11-C
EIA (RS-232C)	DLV11	DL11-D
EIA with Modem	DLV11-E	DL11-E
RS422, RS423	DLV11-J	—
PLU	DRV11	DR11-C
DMA	DRV11-B	DR11-B

2. Serial Line Maximum Data Rate

   a. Modems were limited to 120 words/s (2400 baud) because modems with higher rates cost more than LSI-11 systems usually warrant. Higher data rate modems are generally synchronous rather than asynchronous.

   b. 480 words/s is equal to 9600 baud, the limit of the DLV11 SLU.

   c. 1920 words/s is equal to 38.4 baud, the limit of DLV11-J SLU.

3. PLU (Parallel Line Unit) Limits

   a. The TTL inputs/outputs of the DRV11 limit the distance to 15 feet.

   b. 46K words/s assumes non-interrupt-driven program servicing with bit testing (TSTB, BMI, MOV and SOB). 97K words/s is maximum rate with program servicing without bit testing (MOV and BR). With interrupt-driven servicing, the maximum limit is 20K words/s assuming 50 μs for interrupt latency and software servicing of interrupt.

4. DMA (Direct Memory Access) Limits

   a. The DRV11-B can be used up to 50 feet because it has tri-state drivers and receivers. The distance is limited to 15 feet with TTL devices like the DR11-B.

   b. DMA transfers with the DRV11-B and the DR11-B are limited to 500K words/s in burst mode operation; 250K words/s is the limit for single-cycle mode operation with either device. These limits are device dependent; they are not LSI-11 bus limits (which is 833K words/s). Remember that burst mode can disrupt memory refreshing if bus refreshing (DMA or microcode) is used. Self-refreshing memories (MSV11-CD or MSV11-D) eliminate this problem.

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