MODEL NS 11-04/34Q
ADD-IN MEMORY SYSTEM
SERVICE MANUAL

National Semiconductor
Memory Systems

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PREFACE

This service manual provides information required to install and maintain the National Semiconductor Corporation (NSC) Model NS 11-04/34Q Add-in Memory System.

The information provided in this manual is comprised of the following.

- System Overview
- Theory of Operation
- Installation
- Maintenance
- Troubleshooting
- Reference Drawings

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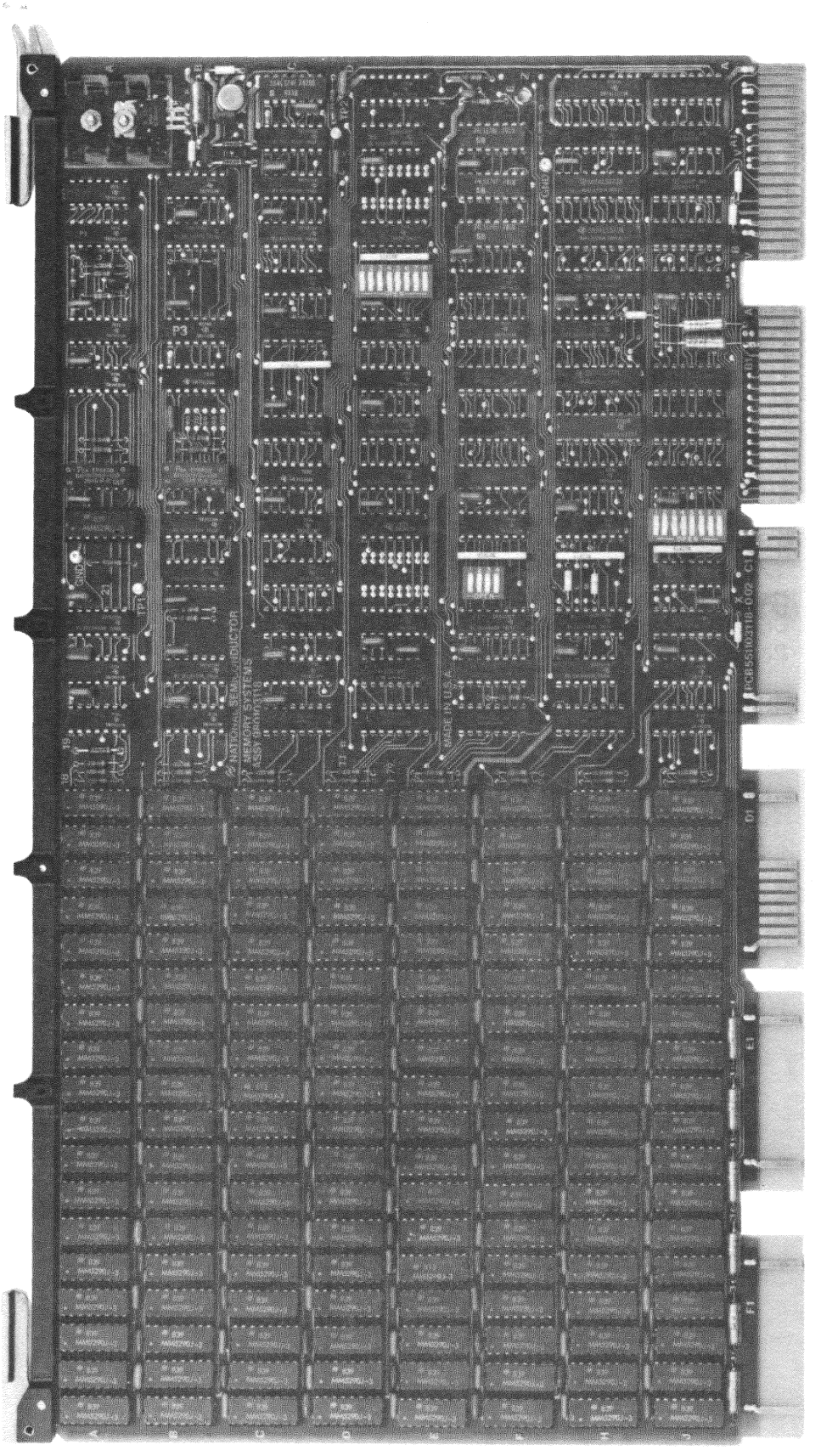


NS 11-04/34Q Add-In Memory System

SECTION 1

SYSTEM OVERVIEW

This section describes the functional capabilities of the NS 11-04/34Q memory, including configurations, mechanical description, power requirements, environmental requirements, features and options, and other documentation.

1.1 GENERAL DESCRIPTION

The NS 11-04/34Q memory contains a random access semiconductor memory array and appropriate drivers and receivers to permit data storage and retrieval. It is designed to operate in DEC's (Digital Equipment Corp.) PDP-11 series computers and is completely compatible with all standard DEC peripheral devices. The NS 11-04/34Q memory can replace or work in conjunction with the DEC model MS 11-FP or the MS 11-JP memories.

Logic levels at the connector input to the NS 11-04/34Q memory are interpreted by the NS 11-04/34Q as follows:

Logic 1 = +0.8V or less
Logic 0 = +2.0V or greater

1.2 CONFIGURATIONS

The NS 11-04/34Q has a maximum storage capacity of 131,072 words of 18 bits each. It is also available in a 96k or 64k by 18-bit configuration and in a 96k/64k by 16-bit configuration.

1.3 MECHANICAL DESCRIPTION

The NS 11-04/34Q memory is completely contained on one multi-layer printed circuit using internal voltage and ground planes. The memory requires only the application of the proper DC power

and I/O connections to become fully operational.

1.3.1 PHYSICAL DIMENSIONS

The NS 11-04/34Q memory is designed to mount on a minimum center-to-center board spacing of 0.50 inch. Two card ejectors permit easy removal of the card. The NS 11-04/34Q memory's dimensions are:

Thickness	0.480 in.
Height	8.680 in.
Length	15.687 in.

1.3.2 I/O CONNECTORS

The NS 11-04/34Q memory is designed to fit mechanically into the following PDP-11 backplanes:

DD 11-DK, slots 2 - 8
DD 11-PK, slots 3 - 8
DD 11-CK, slots 2 - 3

1.4 POWER REQUIREMENTS

The three DC voltages and the current requirements required to operate the NS 11-04/34Q memory are listed in this section.

Table 1-1 compares typical power consumption with the worst-case power requirements of the NS 11-04/34Q memory using the following parameters:

- Standby: Quiescent mode with one refresh cycle every 15 us.
- Operating: 450-ns cycle - continuous read/write memory operation, including refresh.
- Typical: Nominal supply voltages ($\pm$2%)
- Max: Worst case supply voltages ($\pm$5%)

Table 1-1. Standard Power Consumption

Voltage/Mode	Typical	Maximum
+15/20 Standby	0.11A	0.14A
operating	0.65A	0.75A
+5V Standby	2.2A	2.7A
operating	2.4A	3.0A
-15V Standby	0.04A	0.05A
operating	0.06A	0.1A

1.5 ENVIRONMENTAL REQUIREMENTS

The NS 11-04/34Q memory is designed to operate in the following environmental conditions:

- temperature - ambient temperature ranging from $0^{o}C$ to $+50^{o}C$
- thermal shock - relative humidity of 95% maximum without condensation
- altitude - ranging from - 1,000 feet msl to +10,000 feet msl
- cooling - suggested minimum airflow is 25 cfm

1.6 FEATURES AND OPTIONS

This section describes the NS 11-04/34Q memory's features and options.

1.6.1 FEATURES

1.6.1.1 Modes of Operation

The NS 11-04/34Q memory has three basic modes of operation -- read (DATI, DATIP) and write (DATO, DATOB), which are concerned with data retrieval and storage, and refresh, which is transparent to the PDP-11 central processor. Refresh circuitry is entirely contained on the memory and no explicit signal is made

available to the Unibus to indicate that a refresh cycle is in progress.

1.6.1.2 Byte Mode

The NS 11-04/34Q memory can be written on both a byte DATOB (8 bits) or word DATO (16 bits) basis.

1.6.1.3 Access and Cycle Time

The NS 11-04/34Q memory's access and cycle times are listed in Table 1-2.

Table 1-2. Access and Cycle Times

Read	
Cycle Time	450 ns (Min)
Access Time	300 ns (Max)
Parity (CSR Option) Access	340 ns (Max)
Write	
Cycle Time	450 ns (Min)
Access Time (Add/Data latch)	100 ns (Max)
Refresh	
Cycle Time	450 ns (Max)

Note: Cycle requests made during a refresh will extend the cycle and access times an additional 450 ns max.

1.6.1.4 Parity and CSR Description

The NS 11-04/34Q memory is capable of performing on-board parity checking and generation. Memory control logic generates odd parity for each byte during normal memory write cycle, and data is checked for correct parity during read cycle.

The NS 11-04/34Q has an on-board control status register available (CSR). Parity status communication between the CPU and the main memory on the Unibus takes place through control status registers. The CSR's function is to record the memory location where a parity error has occurred and assert the contents of the CSR onto the Unibus when read by the master device. The NS 11-04/34Q memory with on-board CSR is the functional equivalent of DEC's parity controller module M7850.

1.6.2 OPTIONS

1.6.2.1 I/O Space

The NS 11-04/34Q will not respond to addresses within the range of 124 to 128k. See below for optional I/O space. Combinations of D28-6 and D28-5 allow the user to have access of up to 3k of the 4k I/O space.

I/O Space	Switch (D28)	
	6	5
4K	off	off
2k	off	on
1k	on	on

1.6.2.2 Battery Back-up

When DC LO is asserted, the NS 11-04/34Q switches to refresh cycles only. The contents of memory will be retained provided there are battery back-up voltages on +5 BAT (BD1), +15 BAT (AR1) and -15 BAT (AS1). For non-battery back-up, the jumper at location E should be installed with no jumper at location D. With battery back-up, a jumper will be installed at location D and removed at location E.

1.6.2.3 Pre-Tested Memory Replacement

One pre-tested memory device is plugged into an on-board socket for spare requirements. This spare memory device can be used to replace any failing memory devices in the field. The spare memory is at location A23.

1.6.2.4 External Refresh

For certain OEM applications where external refresh control is used, jumpers should be installed at locations F and Z. (External control is at AB2). A 50-ns low going pulse every 15 us will provide the required timing for proper refresh operation.

SECTION 2

THEORY OF OPERATION

This section provides a detailed discussion of the operation of the NS 11-04/34Q add-on memory board. Beginning with an interface description, the discussion proceeds with a functional overview of the board using a block diagram approach. Individual functional blocks, data paths, and timing considerations are then covered with reference to the schematic diagrams in Appendix A.

2.1 INTERFACE DESCRIPTION

Interface between the NS 11-04/34Q add-on memory system and the PDP-11 system is conducted by means of 24 input signals to the NS 11-04/34Q, three output signals to the CPU, and 18 bi-directional data signals. The NS 11-04/34Q, may be used with either a standard or modified Unibus.

The modified Unibus signals and their pin numbers are shown in Table 2-1; standard Unibus signals and pin numbers are shown in Table 2-2. Table 2-3 shows power and grant continuity connectors, and connector locations are shown in Figure 2-1.

2.1.1 INPUT SIGNALS TO MEMORY SYSTEM

The two sets of grouped input signals and four input signals from the PDP-11 CPU to the NS 11-04/34Q are described briefly in this section. The specific function of each signal in the operation of the memory system will become clear as each functional module of the system is described in detail later in the section.

2.1.1.1 A00 - A17

This series contains one control line and 17 address lines used to determine memory location. A00 determines which byte is

Table 2-1. Modified Unibus Signals

Signal (Component Side)	PDP-11 Connector Pin Number		Signal (Solder Side)
INIT L	AA1	AA2	+5V*
INTR L*	AB1	AB2	TP*
D00 L	AC1	AC2	0V
D02 L	AD1	AD2	D01 L
D04 L	AE1	AE2	D03 L
D06 L	AF1	AF2	D05 L
D08 L	AH1	AH2	D07 L
D10 L	AJ1	AJ2	D09 L
D12 L	AK1	AK2	D11 L
D14 L	AL1	AL2	D13 L
PA L*	AM1	AM2	D15 L
PAR P1	AN1	AN2	PB L
PAR P0	AP1	AP2	BBSY L*
+15 BATT	AR1	AR2	SACK L*
-15 BATT	AS1	AS2	NPR L*
0V	AT1	AT2	BR7 L*
+20V*	AU1	AU2	BR6 L*
+20V*	AV1	AV2	+20V*
	A		
RESV*	BA1	BA2	+5V*
RESV*	BB1	BB2	TP*
BR5 L*	BC1	BC2	0V
+5 BATT	BD1	BD2	BR4 L*
SSYN INT L	BE1	BE2	PAR DET L
ACL0 L*	BF1	BF2	DC LO L
A01 L	BH1	BH2	A00 L
A03 L	BJ1	BJ2	A02 L
A05 L	BK1	BK2	A04 L
A07 L	BL1	BL2	A06 L
A09 L	BM1	BM2	A08 L
A11 L	BN1	BN2	A10 L
A13 L	BP1	BP2	A12 L
A15 L	BR1	BR2	A14 L
A17 L	BS1	BS2	A16 L
0V	BT1	BT2	C1 L
SSYN L	BU1	BU2	C0 L
MSYN L	BV1	BV2	-5V*
	B		

*Pins assigned in Unibus connector but not used by memory.

Table 2-2. Standard Unibus Signals

Signal (Component Side)	PDP-11 Connector Pin Number		Signal (Solder Side)
INIT L	AA1	AA2	+5V*
INTR L*	AB1	AB2	0V*
D00 L	AC1	AC2	0V
D02 L	AD1	AD2	D01 L
D04 L	AE1	AE2	D03 L
D06 L	AF1	AF2	D05 L
D08 L	AH1	AH2	D07 L
D10 L	AJ1	AJ2	D09 L
D12 L	AK1	AK2	D11 L
D14 L	AL1	AL2	D13 L
PA INT L	AM1	AM2	D15 L
0V*	AN1	AN2	PB INT L
0V*	AP1	AP2	BBSY L*
0V*	AR1	AR2	SACK L*
0V*	AS1	AS2	NPR L*
0V	AT1	AT2	BR7 L*
NPG H*	AU1	AU2	BR6 L*
DATIP CLR L*	AV1	AV2	0V
	A		
BG6 H*	BA1	BA2	+5V*
BG5 H*	BB1	BB2	0V
BR5 L*	BC1	BC2	0V
0V*	BD1	BD2	BR4 L*
0V*	BE1	BE2	BG4 L*
ACL0 L*	BF1	BF2	DC LO L
A01 L	BH1	BH2	A00 L
A03 L	BJ1	BJ2	A02 L
A05 L	BK1	BK2	A04 L
A07 L	BL1	BL2	A06 L
A09 L	BM1	BM2	A08 L
A11 L	BN1	BN2	A10 L
A13 L	BP1	BP2	A12 L
A15 L	BR1	BR2	A14 L
A17 L	BS1	BS2	A16 L
0V	BT1	BT2	C1 L
SSYN INT L	BU1	BU2	C0 L
MSYN L	BV1	BV2	0V*
	B		

*Pins assigned in Unibus connector but not used by memory.

Table 2-3. Power and Grant Continuity Connections

PDP-11 Connector Pin No.		Signal
CA2,		+5V
		+5V
CU1		+15V
CC2, DC2		0V
EC2, FC2		0V
CT1, DT1		0V
ET1, FT1		0V
DK2	BUS GRANT	1 IN
DL2	BUS GRANT	1 OUT
DM2	BUS GRANT	2 IN
DN2	BUS GRANT	2 OUT
DP2	BUS GRANT	3 IN
DR2	BUS GRANT	3 OUT
DS2	BUS GRANT	4 IN
DT2	BUS GRANT	4 OUT
CA1	NPG	IN
CB1	NPG	OUT

*All other pins not listed above are open circuit.

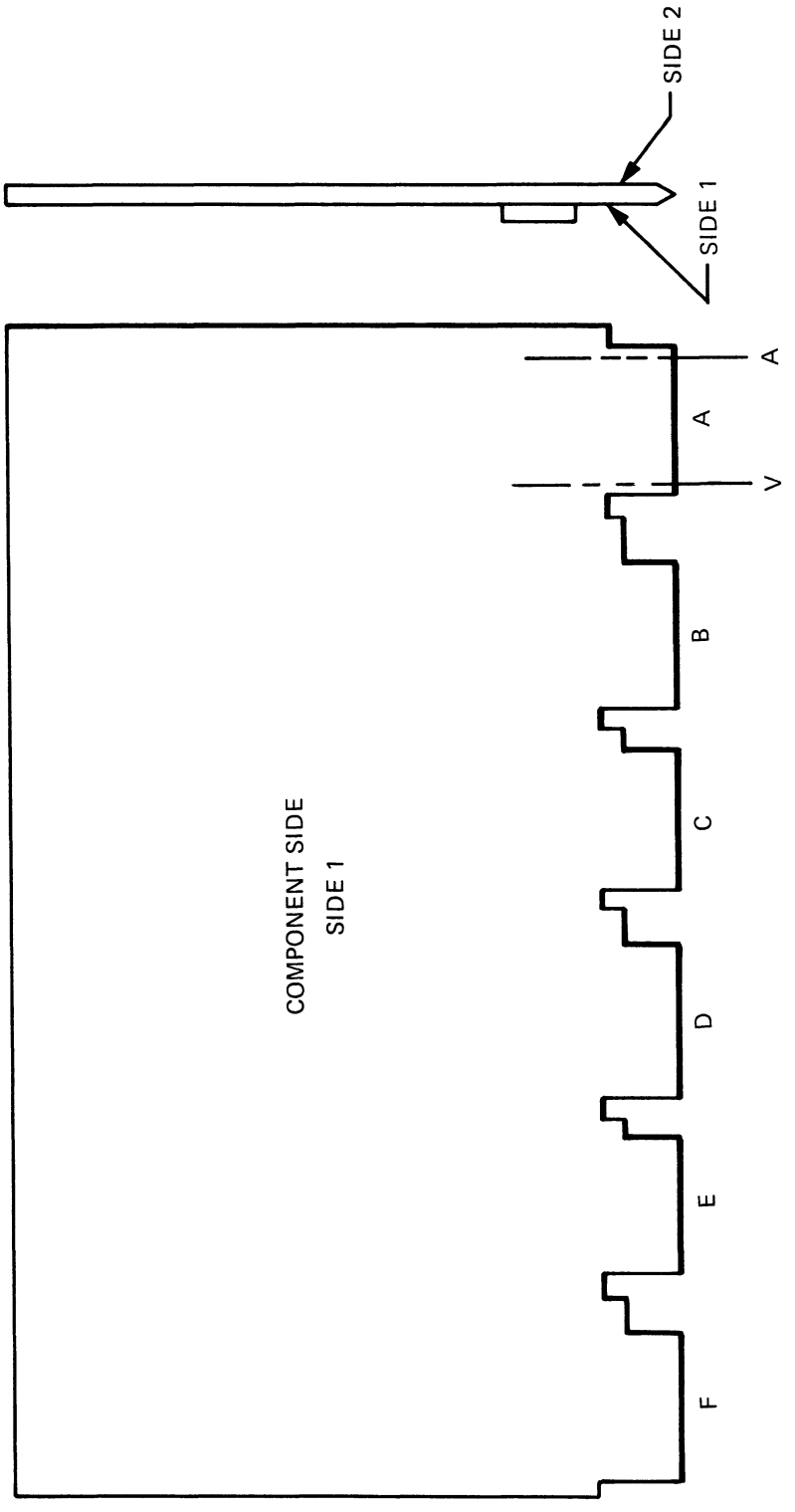


Figure 2-1. Connector Locations

written during a byte write operation.

2.1.1.2 C0, C1

C1 determines whether the cycle will be read or write; C0 determines whether the write function will be byte write or a full write.

2.1.1.3 MSYN

MSYN is the master sync, a bus control signal that initiates a memory cycle when memory is available.

2.1.1.4 INIT

INIT clears the CSR registers.

2.1.1.5 DC LO

DC LO is asserted in the event of power failure to the system. If back-up battery power is provided, the memory will perform refresh only cycles to retain data.

2.1.1.6 PAR DET

PAR DET, the parity detect signal, is held low when the M7650 parity controller is installed.

2.1.2 OUTPUT SIGNALS

Three output signals from the NS 11-04/34Q to the PDP-11 CPU are described briefly in this section. The specific purpose of each signal will become clear as each functional module of the system is described in detail later in the section.

2.1.2.1 SSYN

SSYN is the slave sync signal which, on a read cycle, tells the host system that memory is on-line and data is ready, or, on a write cycle, that the address and the data have been accepted by memory.

2.1.2.2 SSYN INT

SSYN INT is the internal slave sync from memory to the M7850 parity controller.

2.1.2.3 PB

The PB signal indicates that a parity error has been detected.

2.1.3 BI-DIRECTIONAL SIGNALS

The three bi-directional signal functions, as noted below, pertain directly to data being handled by the system.

2.1.3.1 D0 - D15

D0 - D15 are the 16 data lines used to move data information to and from the Unibus.

2.1.3.2 PA, PB

PA and PB are parity data input and output for the standard Unibus. When the CSR option is used, PB is the parity error signal.

2.1.3.3 PAR P1, PAR P0

PAR P1 and PAR P0 are the parity data input and output for the modified Unibus.

2.2 FUNCTIONAL OVERVIEW/BLOCK DIAGRAM

The block diagram of the NS 11-04/34Q is shown in Figure 2-2. Major elements include the address receiver, address register, refresh address counter, and the address multiplexer-driver; the card address field decoder and the timing and control unit; the data transceiver, the control status register, the data in and out registers, the parity generation and checking circuitry, and the memory array itself. This section describes the operation of the NS 11-04/34Q during read and write cycles from a

general standpoint. A detailed discussion of each of these cycles is presented in Section 2.5. The type of memory cycle (read or write) is determined by a combination of A0, C0, C1 as shown below.

A0	C1	C0	Command	Operation
X	0	0	DATI	Read
X	0	1	DATIP	Read
X	1	0	DATO	Write Word
0	1	1	DATOB 0	Write Byte 0
1	1	1	DATOB 1	Write Byte 1

2.2.1 WRITE CYCLE

There are two types of write cycles, byte and full-word. The type of write cycle (as shown previously in Section 2.2) is determined by the state of C1. If only one byte is to be written, signal A00 specifies which byte of the addressed word is to be written. The write cycle is initiated by the master sync (MSYN) signal, indicating to the timing and control circuit that data and address are available on the bus. The address receiver accesses the address and sends it to card address field decoder to determine whether the card contains the addressed location. If so, the address is sent from the address register to the array address multiplex driver. The control logic generates an odd parity bit for each byte, and the timing and control logic clocks the data from the transceiver through the data input register to the array. The slave sync (SSYN) signal is asserted by memory to allow the write cycle to terminate.

2.2.2 READ CYCLE

During the read cycle, MSYNC signals the timing and control circuit when an address is available on the bus. The address is discriminated in the same way as with the write cycle. The data is timed out of the array to the data output register by

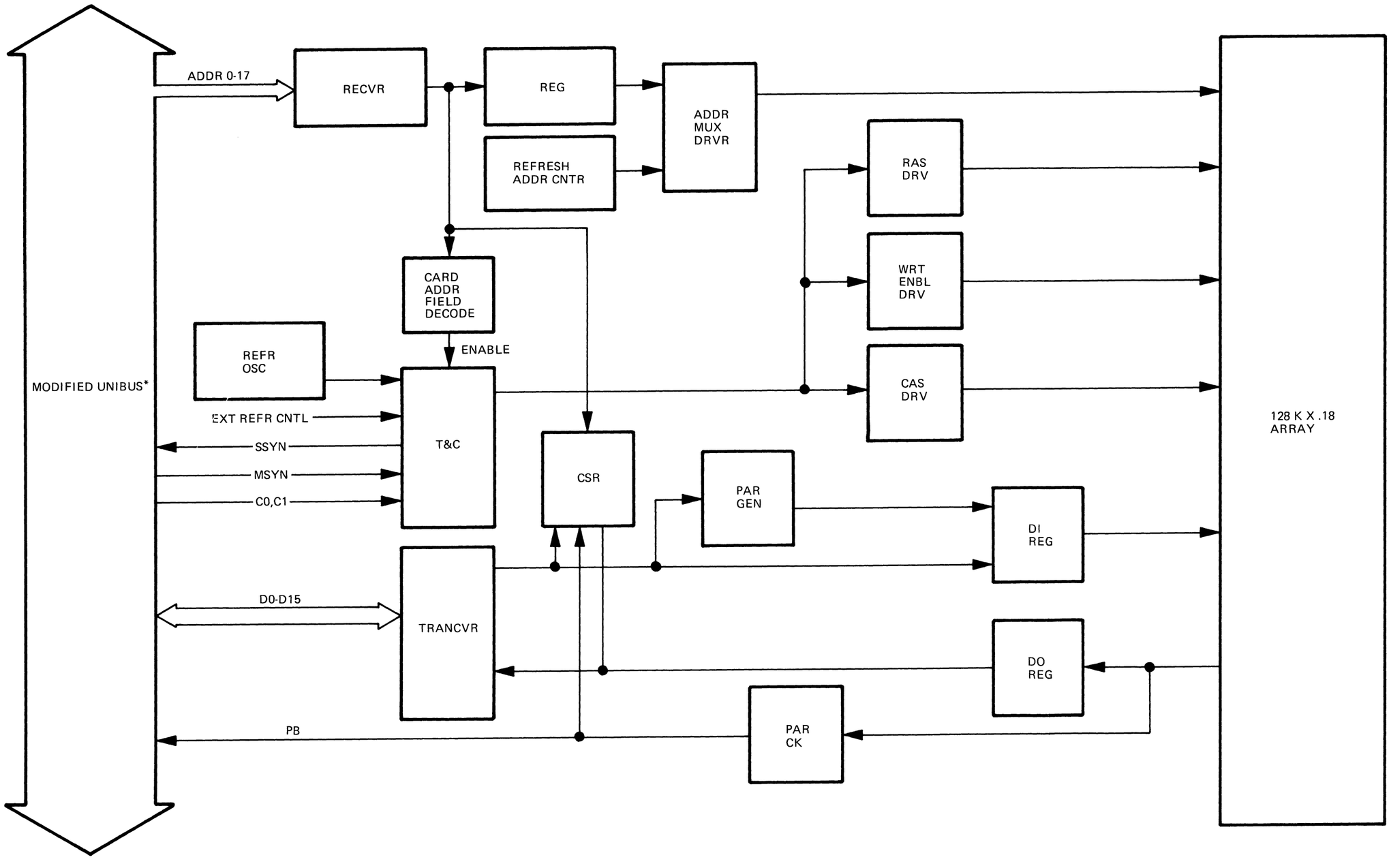


Figure 2-2. NS 11-04/34Q Block Diagram

the timing and control circuit. The transceiver then places the data onto the bus. If a parity error is detected during the read cycle, the address and bit number are placed in the control status register and later sent to the bus (if in CSR option). When the data word is on the bus, the timing and control circuit asserts the SSYN, ending the read cycle.

2.2.3 REFRESH CYCLE

Refresh timing to the timing and control circuit is provided by either the internal refresh oscillator or an external refresh controller. When a memory refresh cycle is initiated, a refresh request signal prevents execution of write and read cycles. After each refresh cycle, the refresh address counter is incremented. If MSYNC is received during a refresh cycle, SSYN will not be asserted until the refresh cycle has terminated and the normal operation cycle has begun.

If the timing and control circuit receives a DC LO signal, cycles in progress are completed and memory will not respond to any new initiates, permitting only refresh cycles to be executed until the signal is no longer asserted.

2.3 POWER CIRCUITRY

The NS 11-04/34Q is powered by three DC voltages provided at the interface. A +15V source is fed in at the interface connector pin CU1 (jumper C closed) if a standard Unibus is used, and either +15V at AR1 (jumper A closed) or +20V at pin AV2 (jumper B closed) for a modified Unibus. There higher DC voltages are run through regulator VR2, where they are regulated at +12V, then used to power the memory array. A -15V source is fed in at pin CB2 and run through voltage regulator VR1, where it is regulated at -5V and sent on to the memory array. A +5V source comes in on pins AA2, BA2, and CA2, and runs directly to the logic circuitry and memory array.

Battery back-up power may be fed in as follows: +15 volts at pin AR1 (jumper A closed), -15 volts at AS1, and +5 volts at BD1 (jumper D closed). When the bus signal DC LO is asserted, battery power is used and the system switches to refresh only cycle to retain data.

2.4 MEMORY ORGANIZATION

The NS 11-04/34Q has a maximum storage capacity of 131,072 words by 18 bits, and is also available in 64k or 96k by 18 bits, and 64k or 96k by 16 bits. The upper 4k of the memory array is reserved for I/O device addressing; the I/O reserve is switch-settable to 2k or 1k. The memory starting address is switch-settable in 4k increments from 0k to 120k (the memory starting address must be less than or equal to 128k minus the size of the memory module).

2.5 DATA PATHS

2.5.1 WRITE CYCLE

To start a write cycle, Bus Master Sync (MSYNC L) is asserted at interface connector pin BV1 and run through receiver (H28) (Appendix A, zone 2D7) to the block start flip-flop (C24) (Appendix A, zone 1C7). If master sync is grounded or held low, the memory will run only one cycle. The block start flip-flop is set by the SSYN timing and is reset by master sync.

Five conditions must be satisfied before any cycle may be initiated: (1) that master sync is not tied low; (2) that no cycle is in progress; (3) that the address requested is within the specified minimum/maximum range for the capacity of the memory; (4) that memory is not in the upper 4k, 2k, or 1k reserved for I/O addressing; and (5) that a refresh request is not present. If these conditions are satisfied at gate (A27) (Appendix A, zone 1C6), then master sync is allowed to start a memory cycle by setting start read/write flip-flop (A29-B30). The start read/

write flip-flop being set sets the read/write flip-flop (C30), which indicates that a read/write cycle is under way.

The signal from the start read/write flip-flop is fed through TP-1 to the delay line (A24) to start the memory cycle. The same signal becomes -START R/W, which is fed to gate A20 (Appendix A, zone 4B7) to provide RAS timing for the memory chips. The output from read/write flip-flop (C30) goes to flip-flop (C32) (Appendix A, zone 1B4), and from flip-flop (C32) through bus driver (H22) (Appendix A, zone 1B2) to interface connector pin BU1, where it becomes the bus slave sync (BUS SSYN L) signal.

This signal tells the processor that the memory has accepted the cycle and that address and data have been latched in.

Data in comes from the bus to transceivers H29 - H32 (Appendix A, zone 3B7), and is latched in at F30 and F32 by -LATCH & ENB (from D23, Appendix A, zone 1B2). These data latches provide data in to the memory chips. The write command to the memory chips (-WRT0-7 and -WRT8-15) comes from gate A20 (Appendix A, zone 1B2). If a full word write is being done, both signals will be active; if a byte write is to be done, command signal C0 will be asserted, and the byte to be written will be determined by A0 (Appendix A, zone 1B7).

When the memory cycle has been completed, -END CYC is generated by gate C31 (Appendix A, zone 1C1). This signal resets the CAS time flip-flop A20-A21 (Appendix A, zone 4B7), the read/write cycle flip-flop C30 (Appendix A, zone 1C4), and a memory cycle is no longer in progress. -RST RAS is applied to B30 pin 5 (Appendix A, zone 1C5), which resets the start read/write flip-flop and enables it to accept the next cycle.

2.5.2 READ CYCLE

The same conditions required of a write cycle must also be satisfied for a read cycle, except that write signals -WRT0-7

and -WRT8-15 are not provided.

When doing a read cycle, pin 12 of the D register C27 (Appendix A, zone 1B3) will be high. Clock for the D register comes from delay A24, and is dependent upon parity generation and checking. When there is no parity, data can appear earlier. The D register C27 is clocked and the output on pin 8 (test point 2), which is the signal -GATE, goes to the data transceivers H29 - H32 (Appendix A, zone 3B7) and enables data out to the bus. Pin 9 of register C27 produces the signal +GATE, which is fed through bus drivers H22 to become the bus slave sync signal BUS SSYN L at H22B pin 5, which tells the processor that data is available. When the memory cycle is complete, -END CYC and -RST RAS reset the read/write cycle flip-flop and the start read/write cycle flip-flop.

The internal timing sequence for the write and read cycles is shown in Figure 2-3.

2.5.3 REFRESH CYCLE

An internal refresh cycle is initiated by the one-shot timer D32 (Appendix A, zone 1C7). When the one-shot times out, D register C32 (Appendix A, zone 1C7) is clocked, producing the refresh request signal +RFSH REQ. +RFSH REQ is also fed to NAND gate B30, and is allowed through provided that there is no regular cycle in process and that the start read/write flip-flop has not been set. This will block out any external cycle request. It is then fed through the delay at A29 (Appendix A, zone 1C5), whre it becomes -SEL RFSH. -SEL RFSH, through multiplexers D19, C19, E19, and F19 (Appendix A, zone 4 B, C and D6), enables the refresh address counter (D20) outputs to the memory array. This counter provides the address to be refreshed, and is advanced at the end of each refresh cycle.

-SEL RFSH, coming from A29 pin 8 (Appendix A, zone 1C5), is fed to B29 pins 12 and 13 through a delay and is used to set the refresh cycle flip-flop C31 and A26 (Appendix A, zone 1C4). The output signal at A29 pin 11 is -START RFSH, which is fed to OR gate A20 (Appendix A, zone 4B7) to become +RAS TIME for a refresh cycle. The refresh cycle flip-flop C31-A26 produces the signal -RFSH CYC, which is also fed to F20 and B20 (UAG). This enables all row RAS drivers. (-WRT0-7, -WRT8-15 and CAS are not present during a refresh cycle). Refresh is done only on a row address strobe (RAS only refresh) basis. The memory does not provide the Bus Slave Sync until the refresh is over. When a refresh cycle has been completed, -END CYC resets the refresh cycle flip-flop and initiates the one-shot timer D32, which begins to time out again.

The internal timing sequence for a refresh cycle is shown in Figure 2-4.

2.6 PARITY GENERATION/CHECKING

For parity checking with an external parity controller, parity switch D28-8 (Appendix A, zone 3D7) must be closed. PAR DET L will be at a low level thus disabling H22B at pin 6, and no bus slave sync (BUS SSYN L) signal will be produced. Instead, internal bus slave sync (INT BUS SSYN L), output at H22A pin 5, is used. For on-board parity generation and checking, switch D28-8 is open, thus disabling INT BUS SSYN L and permitting BUS SSYN L to be present at header pin BU1. Odd parity will be generated for each byte during a normal write cycle; the parity will be checked during a read cycle.

The parity generation and checking circuitry is shown in Appendix A, zone C4 and 5. Parity status communication between a CPU and the main memory on the Unibus takes place through the control status registers (CSRs). The function of the CSR is to record the memory location where the parity error has occurred and insert the contents of the CSR onto the Unibus when read by the

master device. When data bit 0 is set, CSR register E31 pin 12 enables pin 2 of H22A (Appendix A, zone 3D2); when H22A pin 1 goes high, H22 asserts the signal BUS PB to indicate parity error. Gate C23 pin 8 (input to H22 pin 1) can show a parity error only if: (1) there is true parity error, (2) a normal read cycle is being executed, and (3) parity control is on-board.

When a parity error is detected, the current address (address bits 11 - 17) is latched into data bits 5 - 11 of the CSR from the data multiplexer E24-26 (Appendix A, zone 3 A and B 3). Any error location previously stored in the CSR will be destroyed. The enable CSR pulse (-ENB CSR - issued only when a CSR read cycle is in progress and the CSR address selection circuits have been satisfied) is presented at pin 1 of F29 and F31 during a CSR read. When enabled, F29 and F31 provide CSR data to the bus via transceivers H29 - H32.

Data bit 15 is set to a 1 when a parity error is detected. Once set, this bit can be reset only by the bus initialize (BUS INIT L) signal at interface connector pin AA1; BUS INIT L also clears the content of the CSR register. The master device can read or write to the CSR register by setting up the CSR address on the bus and issuing a read or write command (no byte write allowed).

If the CSR is written into and bit 2 is set, the memory will write wrong parity. If bit 2 is set, a high level will be present at C24-2 (Appendix A, zone 3C6). This, in conjunction with a high level from +WRITE (high for normal write cycle), will cause a low level at pin 1 of the parity generators D25 and D31 (Appendix A, zone 3C5) that will force bad (even) parity into memory. This ability to force bad parity is used by the processor as a diagnostic check of proper parity generation and check.

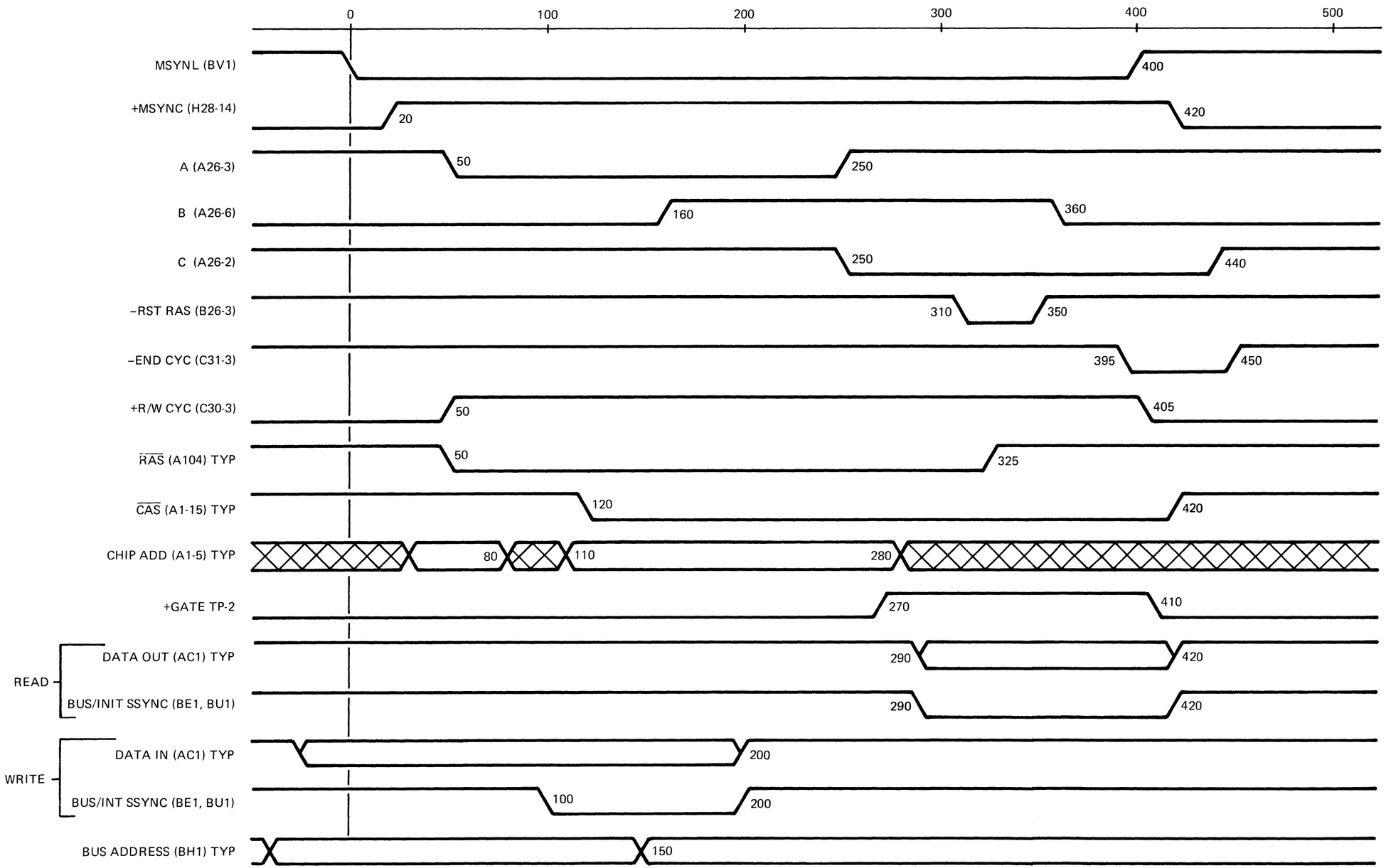


Figure 2-3. Internal Timing Sequence Read and Write Cycles

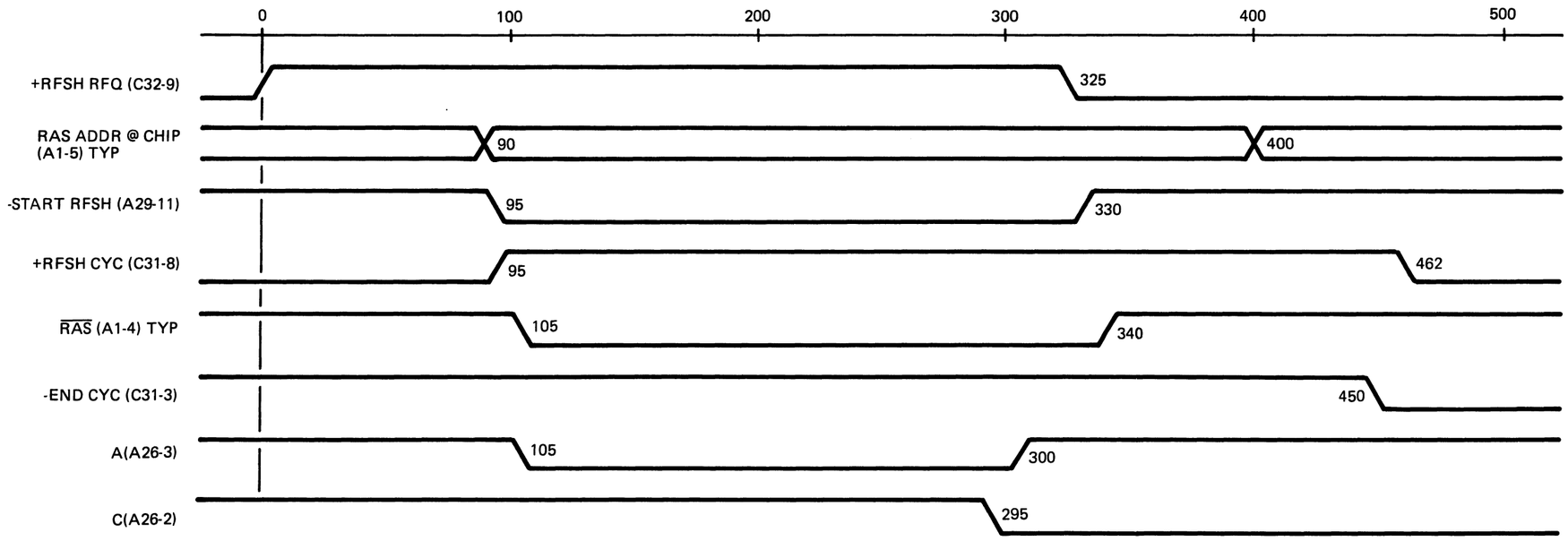


Figure 2-4. Internal Timing Sequence Refresh Cycle

The internal timing sequence for CSR read and write cycles is shown in Figures 2-5 and 2-6.

2.7 ADDRESSING AND DECODING

The address in lines are shown in Appendix A, zone 2C7 and 2D7. The address in signals are buffered by type 8837 receivers H24 - H28 and fed to type LS373 octal latches F25, F26, and F28. The addresses are latched when -LATCH ADDRESS goes low (coming from start read/write flip-flop B30-6, Appendix A, zone 1C5), and are then fed to the row address select and column address select multiplexers E21 and F21 (Appendix A, zone 2D2). Row addresses are provided while the timing signal +CAS ADDR is at a low level (from time delay A24, Appendix A, zone 1D2) at pin 1 of E21 and F21. Column address are provided when +CAS ADDR changes polarity. Outputs from the RAS/CAS address multiplexers are fed to multiplexers D19, C19, E19, and F19 (Appendix A, zone 4 C and D 6), which provide addresses to the memory array when a refresh cycle is not in progress.

Addresses A13 - A20 are fed into the starting address select gates F23 and F24 (Appendix A, zone 2C4). Memory is selectable in 4k increments as determined by the switches at H23 (Appendix A, zone 2B4). Maximum memory address is set at E23 (Appendix A, zone 2C3) by the switches located at E22. If the memory address is above the specified minimum and below the specified maximum and gate D27 (Appendix A, zone 2B4) has been satisfied, then its output, +ADDR SEL, will be high. This signal is fed back to pin 4 of A27 (Appendix A, zone 1C6), and a memory cycle is allowed to run.

The upper order addresses are fed to decoder C20 (Appendix A, zone 2C2), which provides the row select decode that is fed to OR gates F20 and B20 (Appendix A, zone 4A7) to produce the row select for the memory array.

2.8 TIMING

This section briefly discusses bus timing for read and write cycles (see Figure 2-7). Internal timing diagrams for the read, write, and refresh cycles accompany the more detailed circuit descriptions in Section 2.5.

2.8.1 WRITE CYCLE

The address, write request, and write option bits (byte write or full-word write) are placed on the bus at time T-75 ns (min.). The master sync signal, MSYNC L, which indicates that the request has been received and starts the cycle, is issued at time T0. At time T+50 (typ.) the bus slave sync signal SSYNL is issued indicating that memory has accepted the cycle and address and data have been latched in. At approximately time T+100, MSYNC L is disabled; SSYN returns high 25 ns later, and data and address are off the bus at time T+200.

2.8.2 READ CYCLE

As in the write cycle, the address and request are placed on the bus at time T-75 ns, and MSYNC L, beginning the cycle, is issued at time T0. Data is then available on the bus when SSYNL is issued at approximately time T+350 ns.

NOTE

Read and write cycles may be delayed for up to 500 ns in the event of simultaneous refresh and memory requests.

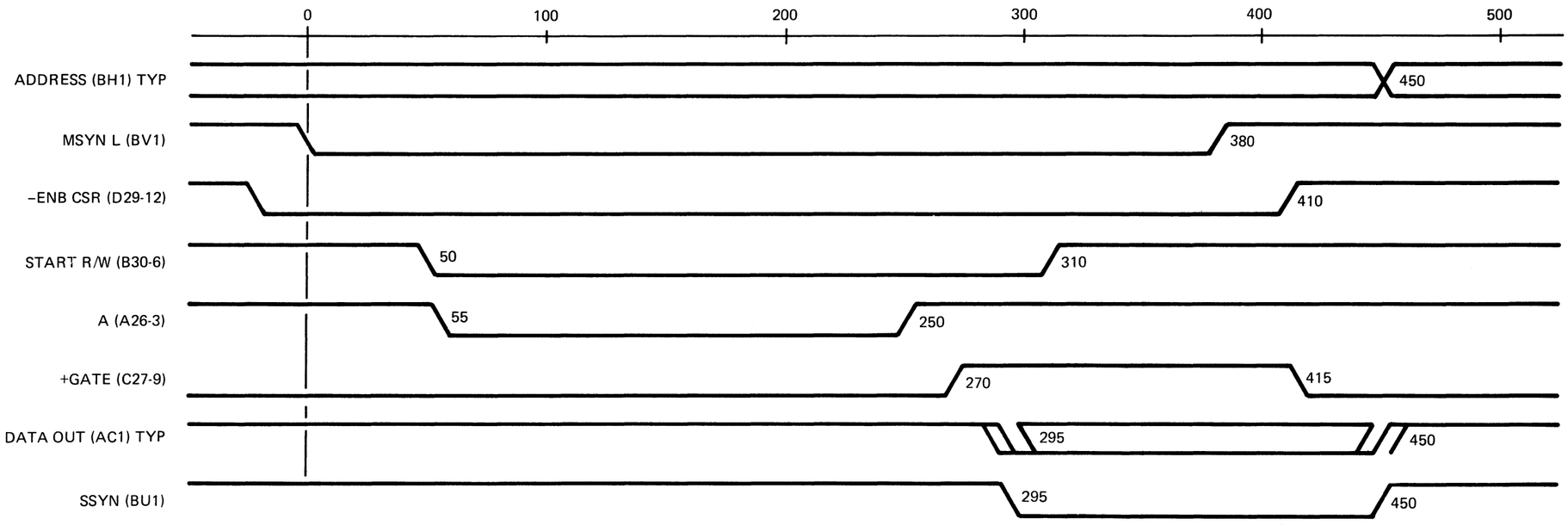


Figure 2-5. CSR Read

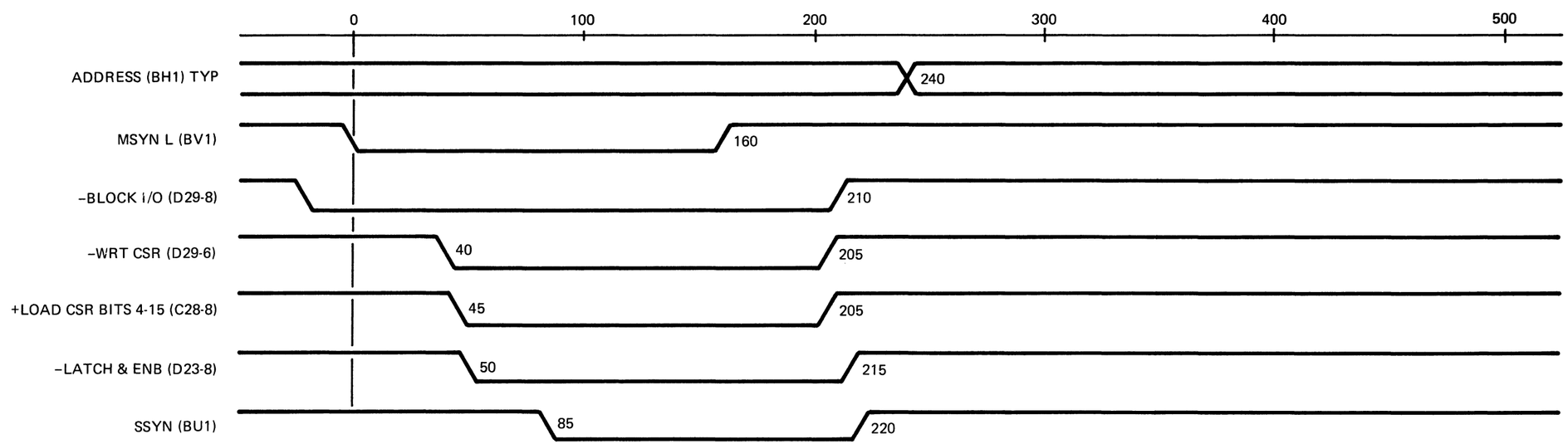
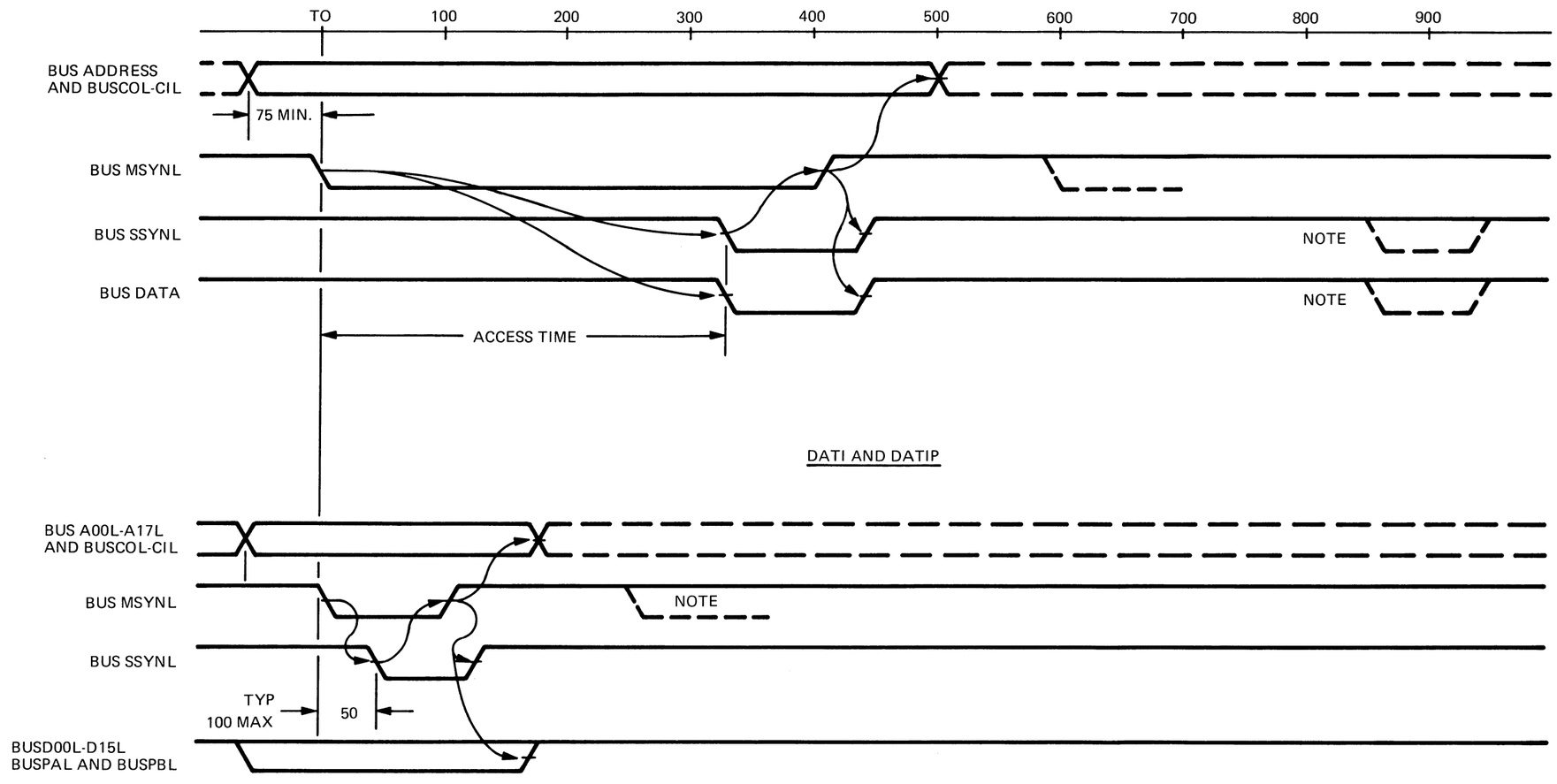


Figure 2-6. CSR Write



NOTE DATA AND SSYNL MAY BE DLEAYED UP TO 500 ns DUE TO SIMULTANEOUS REFRESH AND MEMORY REQUEST.

Figure 2-7. Bus Timing

SECTION 3

INSTALLATION

3.1 OVERVIEW

The National Semiconductor Memory Systems Model NS 11-04/34Q is designed to operate in Digital Equipment Corporations PDP 11/34* Series Computers. The card is directly plug compatible into the following DEC backplanes:

- DD11-DK (slots 2-8)
- DD11-PK (slots 3-8)
- DD11-CK (slots 2,3)

The NS 11-04/34Q is completely compatible with the PDP 11/04/34 computers and all standard DEC peripheral devices. It can be used in both parity (M7850 installed) and non-parity systems. For installation in backplanes not listed above, the subject backplane connector pin assignments must be compatible with the NS-04/34Q pin assignments as listed in Tables 2-1 and 2-2.

The memory is ready for installation upon receipt; however, the memory size and address switches and the option jumpers must be checked before the card is installed.

This section provides detailed information for connecting the proper jumpers and installing the card.

3.2 TOOLS REQUIRED

A list of required tools and equipment is provided in Table 3-1. Test equipment and certain tools, such as electric drills and wire-wrap tools, should always be grounded before being used.

*PDP 11/04 and PDP 11/34 are registered trademarks of Digital Equipment Corp., Maynard, Massachusetts.

Follow instructions in related instruction manuals. Do not defeat the third wire safety ground.

Table 3-1. Field Engineering Tool Kit

1. Chip puller for defective memory replacement
2. Soldering iron, solder
3. Needle-nose pliers
4. Solder remover (Solder-wik, Solda-pullit, etc.)

3.3 SAFETY PRACTICES

The following precautions should be observed during installation.

WARNING

Proper concern for the safety of all personnel is vital when installing equipment. The following safety practices should always be observed.

3.3.1 POWER

a. Remove all power from the system before installation begins, using the related facility and/or system circuit breakers. Remove the AC power plug from the AC receptacle. This is particularly important when cards or components are to be removed.

b. Tag all facility circuit breakers associated with the system with a WARNING tag, so that circuit breakers will not be inadvertently turned on during installation.

c. Although power is off, dangerous voltages may still be present. Therefore, extreme care is necessary when working close to power connectors and power circuits. Always discharge capacitors before working on DC power supplies.

d. When it is necessary to work on a system where power is present, never work alone. Two people must always be present when work is being done within a unit, or on an interconnecting cable, while machine power is applied.

3.3.2 FIRE

a. Good housekeeping is a significant factor in fire and accident prevention. Keep benches and working areas clear of unnecessary articles.

b. Make sure that fire extinguishers of the CO_2 type for electrical fires are readily available.

3.4 UNPACKING AND INSPECTION PROCEDURE

a. Remove all packing materials. Failure to do so could result in damage to the equipment and present a fire hazard. Store the reusable packing materials for future use.

b. Unpack the equipment.

c. Inspect the unit for damage. Identify any damage as to whether it occurred in shipping or while unloading. Check the unit for bent stiffener, damaged gates or cards, broken wires or connectors, dislocated or broken switches or indicators, and any other visual damage. Some damage may not be detected until after applying power and conducting diagnostics.

3.5 INSTALLATION PROCEDURE

a. Verify that the system is performing properly by running the appropriate memory diagnostics before any changes to the CPU configuration are made.

b. Verify that jumper connections and switch settings are correct according to the CPU model, starting address, memory size, CSR address, voltage options, I/O space, and battery back-up as per Section 3.6.

c. Turn off CPU power.

d. Carefully slide the memory into the selected slot. Be sure that the component side faces the correct direction, that the board is aligned in the card guides. Insert and remove slowly so contact is not made with adjacent boards. When the memory has engaged the connectors, press firmly on the card and seat it by exerting equal pressure on the two ejectors.

e. Replace any cables, covers, panels, etc., which were moved during installation. Turn on CPU power.

f. Perform post-installation checks as outlined in Section 3.6.

3.6 OPTION AND CONFIGURATION PROCEDURES

3.6.1 ADDRESSING AND I/O SPACE

A13 through A17 are "strappable" on the memory module. These address lines may be strapped to set the initial address for a memory module. An eight-position switch, located at H23, is provided to set the initial address. Five positions are used for initial address selection in the 0 - 128k address range. The remaining three positions can be used for expansion if a memory mapping scheme is used. Table 3-2 lists the switch configuration for each starting address.

The NS 11-04/34Q will not respond to addresses within the range of 124 to 128k. See Table 3-3 for optional I/O space.

Table 3-2. Address Select (H23) Switch Settings

Unibus Starting Add (Octal)	Memory Starting Address	Switch				
		5	4	3	2	1
000000	0K	off	off	off	off	off
020000	4K	off	off	off	off	on
040000	8K	off	off	off	on	off
060000	12K	off	off	off	on	on
100000	16K	off	off	on	off	off
120000	20K	off	off	on	off	on
140000	24K	off	off	on	on	off
160000	28K	off	off	on	on	on
200000	32K	off	on	off	off	off
220000	36K	off	on	off	off	on
240000	40K	off	on	off	on	off
260000	44K	off	on	off	on	on
300000	48K	off	on	on	off	off
320000	52K	off	on	on	off	on
340000	56K	off	on	on	on	off
360000	60K	off	on	on	on	on
400000	64K	on	off	off	off	off
420000	68K	on	off	off	off	on
440000	72K	on	off	off	on	off
460000	76K	on	off	off	on	on
500000	80K	on	off	on	off	off
520000	84K	on	off	on	off	on
540000	88K	on	off	on	on	off
560000	92K	on	off	on	on	on
600000	96K	on	on	off	off	off
620000	100K	on	on	off	off	on
640000	104K	on	on	off	on	off
660000	108K	on	on	off	on	on
700000	112K	on	on	on	off	off
720000	116K	on	on	on	off	on
740000	120K	on	on	on	on	off

NOTE: The starting address of the NS 11-04/34Q module must be less than or equal to 128K minus the size of the memory module.

Table 3-3. I/O Space Switch Settings

I/O Space	Switch (D28)	
	6	5
4K	Closed (off)	Closed (off)
2K	Closed (off)	Open (on)
1k	Open (on)	Open (on)

3.6.2 MEMORY SIZE

Memory size is determined by the amount of memory installed on memory board. Switch positions should be as per Table 3-4.

Table 3-4. Memory Size Switch (E22) Positions

Switch E22				Memory Size
3	1	2	4	
1	1	1	1	8K
1	1	1	0	16K
1	1	0	1	24K
1	1	0	0	32K
1	0	1	1	40K
1	0	1	0	48K
1	0	0	1	56K
1	0	0	0	64K
0	1	1	1	72K
0	1	1	0	80K
0	1	0	1	88K
0	1	0	0	96K
0	0	1	1	104K
0	0	1	0	112K
0	0	0	1	120K
0	0	0	0	128K

0 = Closed (Low)
1 = Open (High)

3.6.3 CSR STARTING ADDRESS

The CSR address of each memory board is determined by its starting address set by the DIP switch located at D28. The CSR switch address increments in 8K blocks to 120K. See Table 3-5.

Table 3-5. CSR Address (Switch D28)

Switch 4321	Memory Starting Address
0000	0-8K
0001	8-16K
0010	16-24K
0011	24-32K
0100	32-40K
0101	40-48K
0110	48-56K
0111	56-64K
1000	64-72K
1001	72-80K
1010	80-88K
1011	88-96K
1100	96-104K
1101	104-112K
1110	112-120K
1111	120-128K
1 = Open 0 = Closed	

The NS 11-04/34Q memory with on-board CSR performs the equivalent of DEC's parity controller module M7850's functions for the NS 11-04/34Q memory.

3.6.4 PARITY/CSR/NON-PARITY

The NS 11-04/34Q memory may be installed in both the Standard and Modified Unibus by installing the proper jumper combinations and correct switch positions as shown in Table 3-6.

CAUTION

Improper switch settings and jumper positions are a frequent cause of memory failure.

Table 3-6. Parity/CSR/Non-Parity Switch and Jumper Positions

Unibus	Application	Switch D28-8	Jumpers Installed
Standard	+15V No Parity	Closed	C
Standard	+15V Parity Storage	Closed	C, V, X
Standard	+15V Parity (CSR Option)	Open	C, V, X
Modified	+15V No Parity	Closed	A, W, Y
Modified	+15V Parity Storage	Closed	A, W, Y
Modified	+15V Parity (CSR Option)	Open	A, W, Y
Modified	+20V No Parity	Closed	B, W, Y
Modified	+20V Parity Storage	Closed	B, W, Y
Modified	+20V Parity (CSR Option)	Open	B, W, Y

3.6.5 POWER SUPPLY REQUIREMENTS

The NS 11-04/34Q may be operated from a +15V or a +20V power supply. Standard Unibus operation requires +15V at interface connector CU1 and a jumper at location C. For modified Unibus operation, a jumper will be placed at location A for +15V operation (AR1) or location B for +20V operation (AV2). Caution must be taken that only one jumper is installed in locations A, B or C at any given time. (See Figure 3-1 for jumper locations, see Table 3-6 for detailed jumper placement).

3.6.6 BATTERY BACK-UP

When DC LO is asserted, the NS 11-04/34Q switches to refresh cycles only. The contents of memory will be retained provided there are battery back-up voltages on +5 BAT (BD1), +15 BAT (AR1) and -15 BAT (AS1). For non-battery back-up, the jumper at location E should be installed with no jumper at location D. With battery back-up, a jumper will be installed at location D and removed at location E.

3.7 POST-INSTALLATION CHECKS

Post-installation checks consist primarily of checking operation of the memory unit as an integral part of the data processing system in which it is installed. Since the functional checks depend upon the data processing system configuration and user application, the test routines to be used are left to the discretion of the user. Owing to the all-electronic nature of the memory unit, there are no mechanical checks or inspections to be performed once the unit is installed.

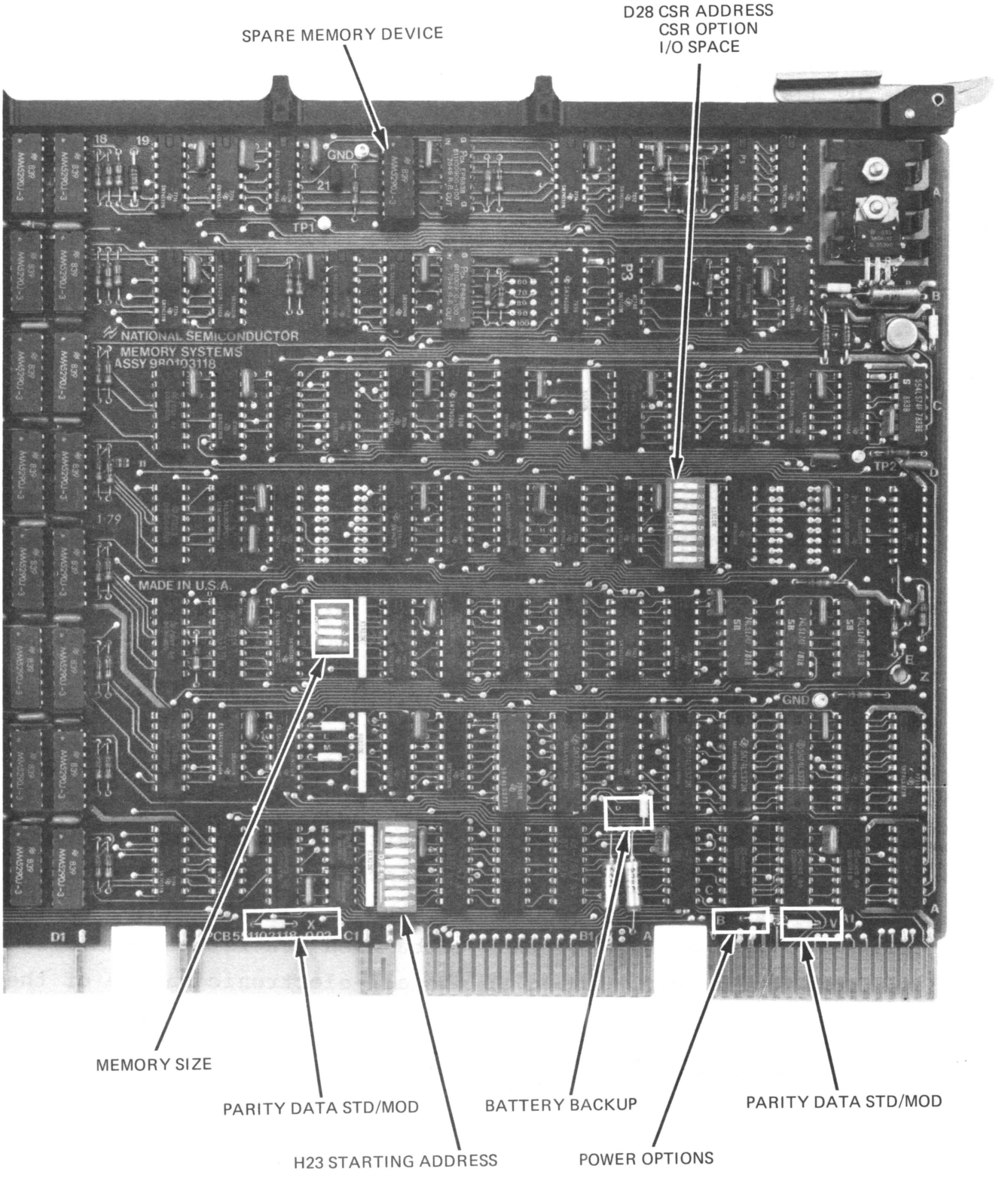


Figure 3-1. Jumper and Switch Locator

NOTE

Any unused modified bus backplane slot must have a bus grant card in location D or CPU will show bus error.

To avoid memory wrap around, memory size must be set for 128K minus the memory starting address (e.g., if starting address is 16K, then memory size is 128K - 16K = 112K). (For memory starting address, see Table 3-2; for memory size, see Table 3-4).

SECTION 4

MAINTENANCE

4.1 OVERVIEW

The maintainability of the NS 11-04/34Q memory is enhanced by the use of fixed timing sequences. Since all timing is controlled by the user, and since only one card type is used, complete interchangeability is accomplished. A spare card can be used in place of a failing unit without the need for any timing adjustments.

The memory devices are all mounted in sockets and the peripheral devices are in common use so that repairs can be affected on-site.

4.2 CORRECTIVE MAINTENANCE

4.2.1 PRELIMINARY CHECKS

If the memory fails, the following preliminary procedure should be followed before component-level troubleshooting.

a. Check the memory installation. It must be installed facing the correct direction. Memory components are facing the same direction as the CPU board components.

b. Remove memory and visually inspect. Wipe edge connector with clean cloth.

c. Recheck the jumper connections and switch settings.

d. Reinstall memory, carefully seating module in the chassis connectors.

e. Using the peripheral equipment, interrogate various address areas of the memory. This will assure the module is fully operational.

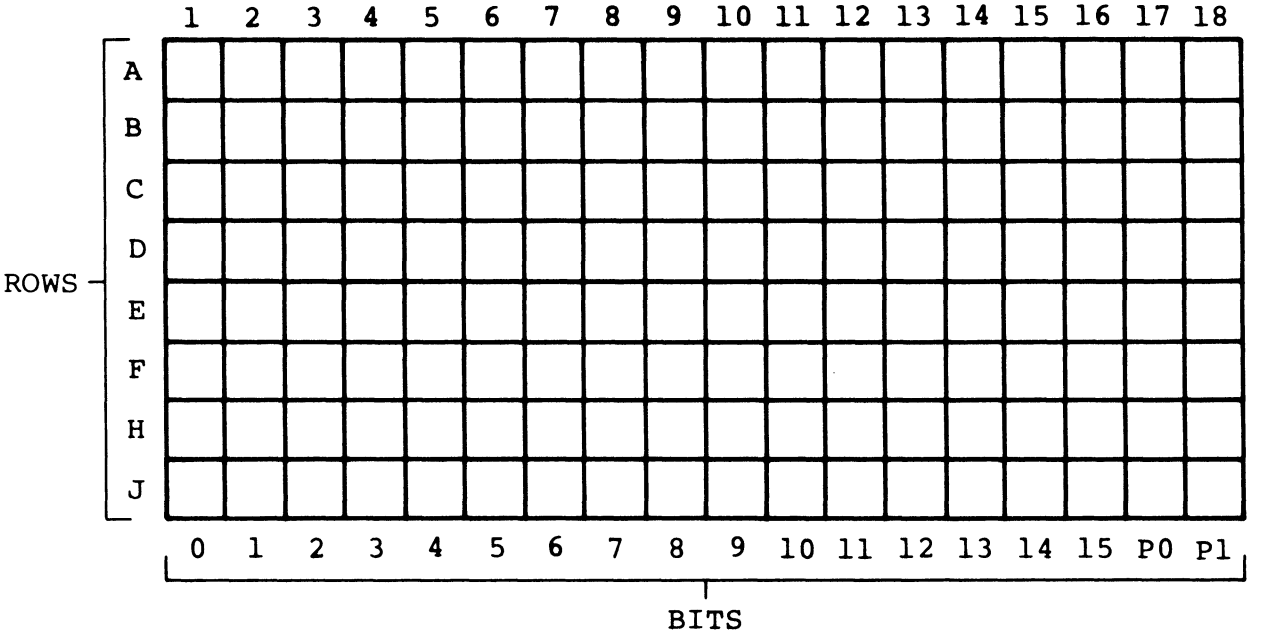
f. When possible, switch with another module known to be operating properly. Use the results to determine whether the problem is in the module or in the processor interface.

4.2.2 PRE-TESTED MEMORY REPLACEMENT

One pre-tested memory device is plugged into an on-board socket for spare requirements. This spare memory device can be used to replace any failing memory devices in the field. The spare memory is at location A23. (See Figure 3-1.)

Table 4-1 may be used for locating defective memory devices. Table 4-2 is provided for decimal to octal conversion when locating faulty devices.

Table 4-1. Memory Component Bit and Row Address Locator



Row	Memory System Address Range
A	0 - 16K $(0 - 077776)_8$
B	16 - 32K $(100000 - 177776)_8$
C	32 - 48K $(200000 - 277776)_8$
D	48 - 64K $(300000 - 377776)_8$
E	64 - 80K $(400000 - 477776)_8$
F	80 - 96K $(500000 - 577776)_8$
H	96 - 112K $(600000 - 677776)_8$
J	112 - 128K $(700000 - 777776)_8$

Table 4-2. Decimal Word to Octal Byte Conversion

Decimal Word	Octal Byte
4096 (4K)	0020000
8192 (8K)	0040000
12288 (12K)	0060000
16384 (16K)	0100000
20480 (20K)	0120000
24576 (24K)	0140000
18672 (28K)	0160000
32768 (32K)	0200000
36864 (36K)	0220000
40960 (40K)	0240000
45056 (44K)	0260000
49152 (48K)	0300000
53248 (52K)	0320000
57344 (56K)	0340000
61440 (60K)	0360000
65536 (64K)	0400000
69632 (68K)	0420000
73728 (72K)	0440000
77824 (76K)	0460000
81920 (80K)	0500000
86016 (84K)	0520000
90112 (88K)	0540000
94208 (92K)	0560000
98304 (96K)	0600000
102400 (100K)	0620000
106496 (104K)	0640000
110592 (108K)	0660000
114688 (112K)	0700000
118784 (116K)	0720000
122880 (120K)	0740000
126976 (124K)	0760000
131072 (128K)	1000000

Appendix A

Reference Drawings

This appendix contains the required reference schematic and assembly drawings for the NS 11-04/34Q memory.

870103118-001	Schematic
980103118-000	Assembly

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	9/18/78	PDD2355	Graney
B	11/12/78	PDD3057	Graney

-ENB CSR (SH-2)
-SET BAD ADDR (SH-3)
-WRT CSR (SH-2)
BUS INIT L (AA1) — H21 1/2 8641 — D24 S04 — B26 S00 +5B
BUS DC LO (BF2)
+WRITE (SH-2)
-I/O BLOCK (SH-2)
BLOCK START — C24 S00 — C23 S11
+READ (SH-2)
+MSYNC (SH-2)
+ADDR SEL (SH-2)
-EXT RFSH (AB2) — EXT RFSH — 3R5 10K — 6R5 10K — 1C5 2200 PF — 1R6 16K — 1/2 LS123 — D32 — C32 — C31 S00 — 4R5 10K — +RFSH REQ
+PARITY (SH-3)
+PARITY (SH-3)
+A0 (SH-2) — B27 — C29 S00
+C0 (SH-2)
PAR DET L (BE2)

-RST RAS
START R/W — 1R9 3.9K — A29 S132 — B30 S10 +5B
-POWER DN
1R10 27R — 47pF 2C6 — A27 S22 +5B
1R8 2.7K
1R7 +5B 3.3K — 1C6 47pF — A27 S22 — A29 S132
2R7 +5B 3.3K — 3C6 47pF — B29 38 — A29 S132
C29 S00 — C30 S00 — C31 S00 — A26 S37 +5B — RSH CYC
R/W CYC — C30 S00 +5B
TP-1
A21 S00 +5B — A26 S37 +5B
S10 — A30 +5B — B26 S00 +5B — -END CYCLE -RST RAS
-RFSH CYC (SH-4)
-CLEAR (SH-3)
+LOAD CSR BITS 4-15 (SH-3)
+RFSH CYC (SH-4)
-LATCH ADDR (SH-2)
-SEL RFSH (SH-4)
-START RFSH (SH-4)
-START R/W (SH-4)
B30 S10 +5B — -CAS SET (SH-4)
B23 S04 +5B — B22 +5B — B26 S00 +5B — +CAS ADDR (SH-2)
DELAY 100SN A24 — 1C2 200Ω — 1C4 360Ω S37 +5B
DELAY B24 100SN — 2C2 200Ω — 2C4 360Ω
10K P.U. C27.1RP1-4
C31 S00 +5B — -END CYC (SH-4)
+GATE (SH-3)
3R1 15Ω — -WRT 8-15 (SH-4)
6R1 15Ω — -WRT 0-7 (SH-4)
D23 27 — -LATCH & ENB (SH-3)
C28 S08 — +WRITE ENB — C27 — +GATE — TP-2
1/2 LS74 — C32 — +MSYNC
+PARITY — B22 S04
1R9 1 10K — +5V
B27 00 — B27 00
C28 S08 — -CTRL (SH-3)
D24 S04
H22A — INT BUS SSYN L (BE1)
75452 H22B — BUS SSYN L (BU1)
-GATE (SH-3)
PAR DET L (SH-3)

+15 (CU1) — VR2 VOLTAGE REGULATOR +12 VOLTS — .47µF 50V C2 (63X) — 6.8µF 35V 1C3 — 1C3-6C3 35V 1C3 THRU 6C3
IN5817 2CR1
-15 (CB2) — VR1 VOLTAGE REGULATOR -5 VOLT — -5 VOLTS — 1CR1 IN5817
3CR1 IN5817
-15B (AS1)
.47µF 50V 1C2 — .47µF 50V 2OC2 — .1µF 50V C1 (32X)
+5 V (AA2 BA2 CA2) — 22µF 10V 2C4 — .1µF 50V C1 (23X) — + 5 VOLTS
+5B (BD1) — 22 µF 10V 1C4 — .1µF 50V C1 (50X) — + 5 B
GND (AC2 AT1 DC2 DT1 / BC2 BT1 EC2 ET1 / CC2 CT1 FC2 FT1)

BUS GRANT SIGNALS
DK2 — DL2
DM2 — DN2
DP2 — DR2
DS2 — DT2
CA1 — CB1

MATERIAL		T.K. 7/26/78	National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, Calif. 95051
FINISH		Graney 9/19/78	NS-11 04/34Q 1/4 MEGABYTE MEMORY
NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED	SIZE D — DR NO 870103118 — 001
			SCALE — SHEET 1 OF 4

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	7/8/78	PDD 2355	
B	11/2/78	PDD 3057	

SH-1 +CAS ADDR

LINE RECEIVERS 8837

BV1 BUS MSYN L
BU2 BUS CO L
BT2 BUS C1 L
BH2 BUS A00
BH1 BUS A01
BJ2 BUS A02
BJ1 BUS A03
BK2 BUS A04
BK1 BUS A05
BL2 BUS A06
BL1 BUS A07
BM2 BUS A08
BM1 BUS A09
BN2 BUS A10
BN1 BUS A11
BP2 BUS A12
BP1 BUS A13
BR2 BUS A14
BR1 BUS A15
BS2 BUS A16
BS1 BUS A17
A18
A19
A20

H28 H26 H25 H24

4RP1 10K P.U. +5

SH-1 -LATCH ADDR

SH-3 +PARITY

ADDRESS LATCHES LS373

F28 F26 F25

LTH OC

+MSYNC SH-1
+CO SH-1
+WRITE SH-1, SH-3
+AO SH-1

A1 A5 A9 A13 A17

+WRITE +MSYNC D27 S11 D24 S04

RAS/CAS MUX S158

E21 F21 S158

-ADD 0 SH-4
-ADD 1 SH-4
-ADD 2 SH-4
-ADD 3 SH-4
-ADD 4 SH-4
-ADD 5 SH-4
-ADD 6 SH-4

8K SEL 3RP1 10K +5

STARTING ADDRESS SELECT S283

F23 F24

E22 3RP1 10K +5

MAX ADDRESS

E23 S283

5RS 10K +5B 8K

E20 LS157

ROW SELECT

C20 S138

-ENB A SH-4
-ENB B SH-4
-ENB C SH-4
-ENB D SH-4
-ENB E SH-4
-ENB F SH-4
-ENB H SH-4
-ENB J SH-4

+ADDR > MIN D23 D24 S04

+> MAX ADD

A30 S10 D27 S11

+ADDR SEL SH-

4RP1 10K +5

5RP1 10K +5

1RP1 10K +5

H23 D26 S11

+READ SH-1, SH-3
-I/O BLOCK SH-1
-WRT CSR SH-1, SH-3
-ENB CSR SH-1, SH-3

D29 S10

D28 2K/1K I/O 2RP1 10K +5

CSR ADDRESS D28 10K 2RP1 +5

P.U. 10K +5 7R5

E28 A=B IN A=B A>B A<B 7485

F27 S04 E27 S133

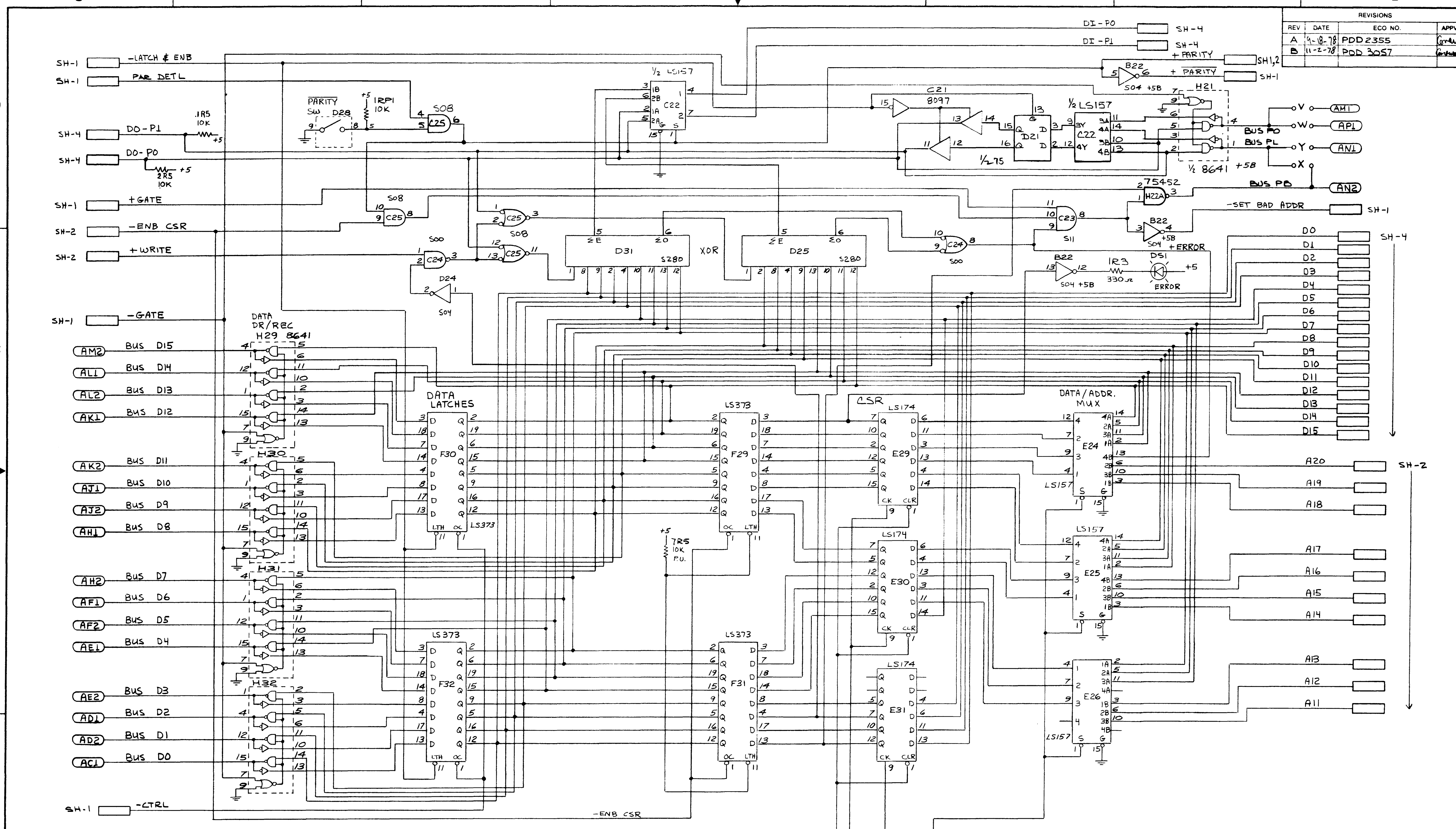
A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 SH-3

MATERIAL		DR BY	
FINISH		CHK BY T.K. 7/26/78	
		M.E.	
		E.E.	
		P.E. Conway 5/18/78	
UNLESS OTHER SPECIFIED			
TOLERANCE ANG. 2 PL 3 PL		DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX	
NEXT ASSY	USED ON		

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

NS-11 04/34Q
1/4 MEGABYTE MEMORY

SIZE D DR NO 870103118 001
SCALE SHEET 2 OF 4



REVISIONS

REV	DATE	ECO NO.	APPVD
A	4-18-78	PDD 2355	
B	11-2-78	PDD 3057	

MATERIAL

FINISH

DR. T.K. 7/26/78

7/18/78

UNLESS OTHER SPECIFIED

TOLERANCE

NEXT ASSY — USED ON

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

NS-11 04/34Q
1/4 MEGABYTE MEMORY

SIZE D — DR NO 870103118 — 001

SHEET 3 OF 4

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	7-18-78	PDD 2355	
B	11-2-78	PDD 3057	

SH-1 −WRT 0-7

SH-1 −WRT 8-15

SH-1 +RFSH CYC

+5B

LS393 D20 (CLR1, CLR2; QC QB QA 2A QD QC QB QA; 5 4 3 1 8 9 10 11)

+5B 3648 D19 (1A 3A 2A 4A 1B 3B 2B 4B; 2 11 5 14 3 10 6 13; 1 3 2 4 12 7 4 15)

C19 (14 5 2 11 13 6 3 10; 4 2 1 3 12 7 4 15)

E19 (2 11 5 14 3 10 6 13; 4 2 1 3 12 7 4 15)

F19 (14 5 2 11 13 6 3 10; 4 2 1 3 12 7 4 15)

SH-2 −ADD 0

SH-2 −ADD 1

SH-2 −ADD 2

SH-2 −ADD 3

SH-2 −ADD 4

SH-2 −ADD 5

SH-2 −ADD 6

SH-1 −SEL RFSH

PIN-13 7A6 5A5 10A4 11A3 12A2 6A1 7A0 5
ADDRESS DRIVE 72 RAMS

PIN-13 7A6 5A5 10A4 11A3 12A2 6A1 7A0 5
ADDRESS DRIVE 72 RAMS

16K RAM (TYP 144 X)

(−5v) VBB 1 — 16 VSS (GND)
DIN 2 — 15 CAS
WRT 3 — 14 DOUT
RAS 4 — 13 A6
A0 5 — 12 A3
A2 6 — 11 A4
A1 7 — 10 A5
(+12v) VDD 8 — 9 VCC (+5B)

SPARE RAM IN A23

WRT	J1	H1	F1	E1	D1	C1	B1	A1	DI DO 2 14	D0 — SH-3
WRT	J2							A2	DI DO 2 14	D1 — SH-3
WRT	J3							A3	DI DO 2 14	D2 — SH-3
WRT	J4							A4	DI DO 2 14	D3 — SH-3
WRT	J5							A5	DI DO 2 14	D4 — SH-3
WRT	J6							A6	DI DO 2 14	D5 — SH-3
WRT	J7							A7	DI DO 2 14	D6 — SH-3
WRT	J8							A8	DI DO 2 14	D7 — SH-3
WRT	J9							A9	DI DO 2 14	D8 — SH-3
WRT	J10							A10	DI DO 2 14	D9 — SH-3
WRT	J11							A11	DI DO 2 14	D10 — SH-3
WRT	J12							A12	DI DO 2 14	D11 — SH-3
WRT	J13							A13	DI DO 2 14	D12 — SH-3
WRT	J14							A14	DI DO 2 14	D13 — SH-3
WRT	J15							A15	DI DO 2 14	D14 — SH-3
WRT	J16							A16	DI DO 2 14	D15 — SH-3
DI WRT	J17							A17	DO 14	DO-P0 — SH-3
DI RAS	J18	H18	F18	E18	D18	C18	B18	A18	DO RAS CAS 14 4 15	DO-P1 — SH-3

SH-3 DI-P0

SH-3 DI-P1

SH-1 −START R/W

SH-1 −START RFSH

SH-1 −CAS SBT

SH-1 −END CYC

SH-1 −RFSH CYC

+5B S37 A20 (4 5 6)

A21 (1 2 3)

A20 (1 2 3)

S00 +5B

+RAS TIME

+CAS TIME

S00

SH-2 −ENB J

SH-2 −ENB H

SH-2 −ENB F

SH-2 −ENB E

SH-2 −ENB D

SH-2 −ENB C

SH-2 −ENB B

SH-2 −ENB A

F20 (10 9 8; 5 4 6; 2 1 3; 13 12 11)

B20 (2 1 3; 13 12 11; 5 4 6; 10 9 8)

S00 +5B

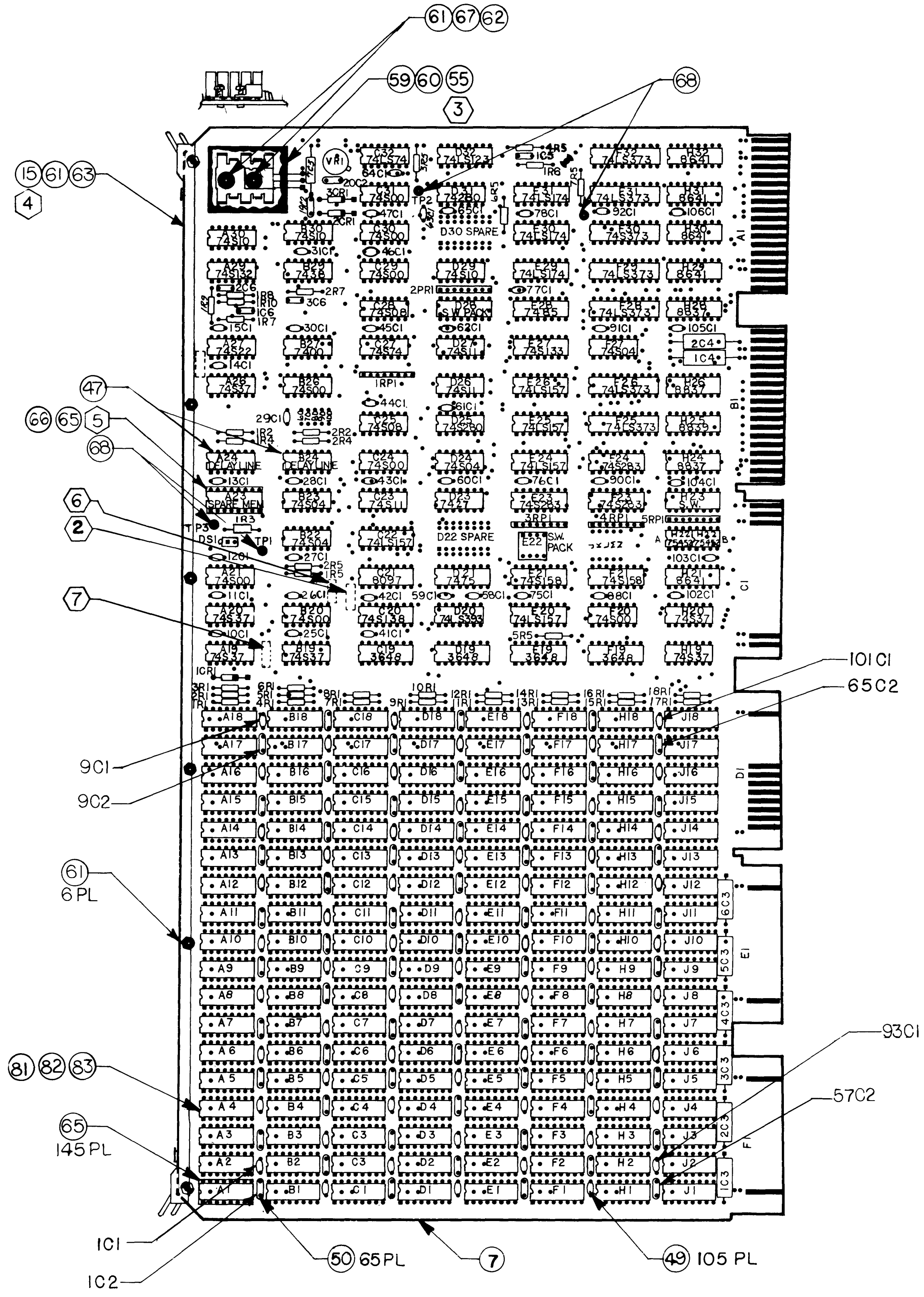
18R1 17R1 16R1 15R1 14R1 13R1 12R1 11R1 10R1 9R1 8R1 7R1 6R1 5R1 4R1 3R1 2R1 1R1 — 15Ω

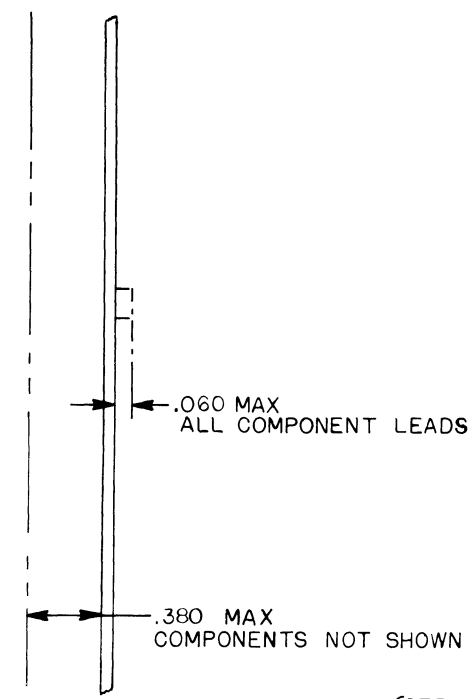
H19 H19 H19 H19 H20 H20 H20 H20 B19 B19 B19 B19 A19 A19 A19 A19 (8 6 11 3 8 6 11 3 12 13 2 1 9 10 5 4)

S37 +5B

MATERIAL	DR BY	National Semiconductor Corporation	
	DES BY T.K. 7/26/78	2900 Semiconductor Drive, Santa Clara, Calif. 95051	
FINISH	ME	NS-11 04/34Q	
	EE	1/4 MEGABYTE MEMORY	
	TEST Graves 9-18-78		
UNLESS OTHER SPECIFIED		SIZE D DR NO 870103/18	001
TOLERANCE	DIMENSIONING ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED NICKEL PLATED FINISHES	SCALE	SHEET 4 OF 4
NEXT ASSY USED ON	REMOVE BURRS AND SHARP EDGES BREAK SHARP CORNERS .015 MAX		

REVISIONS			
REV	DATE	ECO NO	APPVD
A	11-2-78	PDD 3057	





1. ASSEMBLE AND SOLDER PER NSC SPEC. 429101895.
2. MARK ASSY. DASH NO. WITH .12-.18 HIGH CHARACTERS APPROX. WHERE SHOWN.
3. APPLY ITEM 60 (THERMAL COMPOUND) TO MATING SURFACES OF ITEMS 7, 55 AND 59.
4. APPLY ITEM 15 (LOCTITE) TO TAPPED HOLES IN ITEM 63 (STIFFENER) PRIOR TO INSERTING ITEM 61 (SCREWS).
5. INSTALL ITEM 66 AFTER PRE-TESTING PER TEST SPEC. 425103118.
6. MARK ASSY. WITH REV. LEVEL WITH .12-.18 HIGH CHARACTERS WHERE SHOWN.
7. MARK ASSY. S/N WITH .12-.18 HIGH CHARACTERS WHERE SHOWN.
8. INSTALL MEMORY I.C.'s ACCORDING TO THE TABULATED DATA CHART. THE MEMORY ELEMENT P/N IS ASSIGNED IN THE MEMORY ELEMENT PART NO. CHART.
9. VERSION NUMBERS ARE ESTABLISHED TO THE FOLLOWING CODE: –XYZ

X = MEM CHIP TYPE
(SEE MEMORY ELEMENT P/N CHART)

X = 0 16K
X = 1 8 K PARTIAL RH
X = 2 8 K PARTIAL LH

Y = NO. OF BITS

Y = 0 18 BITS
Y = 1 16 BITS

Z = MEMORY ROW POPULATION

Z = 1 ROWS A-J
Z = 2 ROWS A-H
Z = 3 ROWS A-F
Z = 4 ROWS A-E
Z = 5 ROWS A-D
Z = 6 ROWS A-C
Z = 7 ROWS A-B
Z = 8 ROW A

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

P.C.B. ASSEMBLY
NS 1104/34 Q 256 K BYTE MEMORY

MATERIAL
FINISH
TOLERANCE
NEXT ASSY | USED ON

10/13/78 · 11/1/78 · 11-2-78 · 11-2-78

UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX

SIZE D | DR NO 980103118 | 000
SCALE 1:1 | SHEET 1 OF 8

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	11-2-78	PDD 3057	Conaway

NOTES

(10) INSTALL JUMPERS ACCORDING TO THE FACTORY INSTALLED JUMPER TABLE.

(11) AFTER FINAL TEST, INSTALL/REMOVE JUMPERS AS DEFINED BY THE MARKETING CONFIGURATION CODE TABLE.

(8) TABULATED DATA CHART

VERSION (9)	QTY	POPULATED MEMORY ELEMENT LOCATIONS (ROW)	(COLUMN)	CAPACITY 16K RAM	8K RAM	BITS
-X01	144	A,B,C,D,E,F,H,J	(1-18)	128K	64K	18
-X02	126	A,B,C,D,E,F,H	(1-18)	112K	56K	18
-X03	108	A,B,C,D,E,F	(1-18)	96K	48K	18
-X04	90	A,B,C,D,E	(1-18)	80K	40K	18
-X05	72	A,B,C,D	(1-18)	64K	32K	18
-X06	54	A,B,C	(1-18)	48K	24K	18
-X07	36	A,B	(1-18)	32K	16K	18
-X08	18	A	(1-18)	16K	8K	18
-X09	128	A,B,C,D,E,F,H,J	(1-16)	128K	64K	16
-X10	112	A,B,C,D,E,F,H	(1-16)	112K	56K	16
-X11	96	A,B,C,D,E,F	(1-16)	96K	48K	16
-X12	80	A,B,C,D,E	(1-16)	80K	40K	16
-X13	64	A,B,C,D	(1-16)	64K	32K	16
-X14	48	A,B,C	(1-16)	48K	24K	16
-X15	32	A,B	(1-16)	32K	16K	16
-X16	16	A	(1-16)	16K	8K	16

(8) MEMORY ELEMENT PART NO. CHART

X (9)	PART NUMBER	DESCRIPTION
0	482102598-012	16K x 1 DYNAMIC RAM, 200 NS
1	482102989-112	8K x 1 DYN. RAM, PARTIAL RH, 200 NS
2	482103060-112	8K x 1 DYN. RAM, PARTIAL LH, 200 NS

(10) FACTORY INSTALLED JUMPER TABLE

VERSION (9)	JUMPERS INSTALLED	REMARKS
ALL	A,E,S,T,W,Y	MODIFIED UNIBUS,+15V INPUT
-001 THROUGH-016	K,N	16K RAMS
-101 THROUGH-116	J,L,U	8K PARTIAL, LEFT HALF
-201 THROUGH-216	L,U	8K PARTIAL, RIGHT HALF

(11) MARKETING CONFIGURATION CODE TABLE
USER SELECTABLE OPTION JUMPERS

MKTG. CONFIG. CODE	JUMPERS INSTALLED	JUMPERS REMOVED	REMARKS
NONE	—	—	NO OPTIONS
01	B	A	MODIFIED UNIBUS, +20V INPUT
02	D	E	MODIFIED UNIBUS, BATTERY BACKUP
03	C	A	STANDARD UNIBUS, NO PARITY OR ONBOARD PAR CONTROLLER
04	C, V, X	A, W, Y	STANDARD UNIBUS, 18 BIT STORAGE (PARITY)

MATERIAL

FINISH

TOLERANCE ANG. 2 PL ± 3 PL

UNLESS OTHER SPECIFIED

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

REMOVE BURRS AND SHARP EDGES BREAK SHARP CORNERS .015 MAX

NEXT ASSY | USED ON

DR BY Joe Jacoba 11-1-78

CHK BY

M E

PE Conaway 11-2-78

PM Conaway 11-2-78

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

PCB ASSEMBLY
NS 1104/34Q 256K BYTE MEMORY

SIZE D | DR. NO. 980103118 | 000

SCALE _____ | SHEET 2 OF 8